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Minds in Motion

Power Play: Architecture level Optimization for Low Power Video Processing

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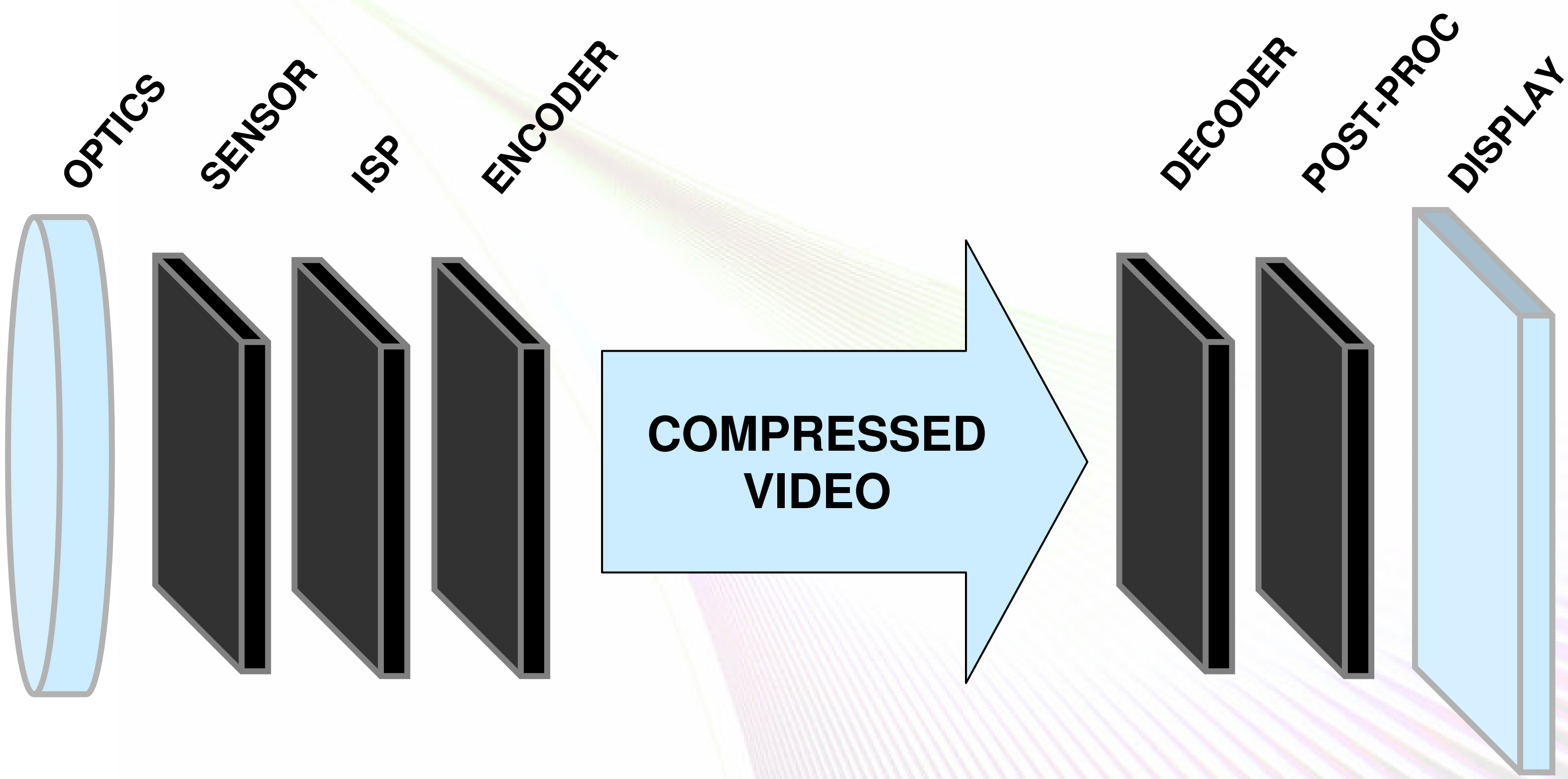
Agenda

- Introduction
  - Portable video applications
  - Video processing requirements
- DV engine architecture
- Factors impacting power dissipation
- System/Architecture level power optimization
- Summary

Portable Video Applications

- Mobile Video Phone
- Portable Media Player
- Portable Video Recorder
- Portable TV (DVB-T, DVB-H)
- Digital Camcorder
- Web terminal

Video Processing Chain



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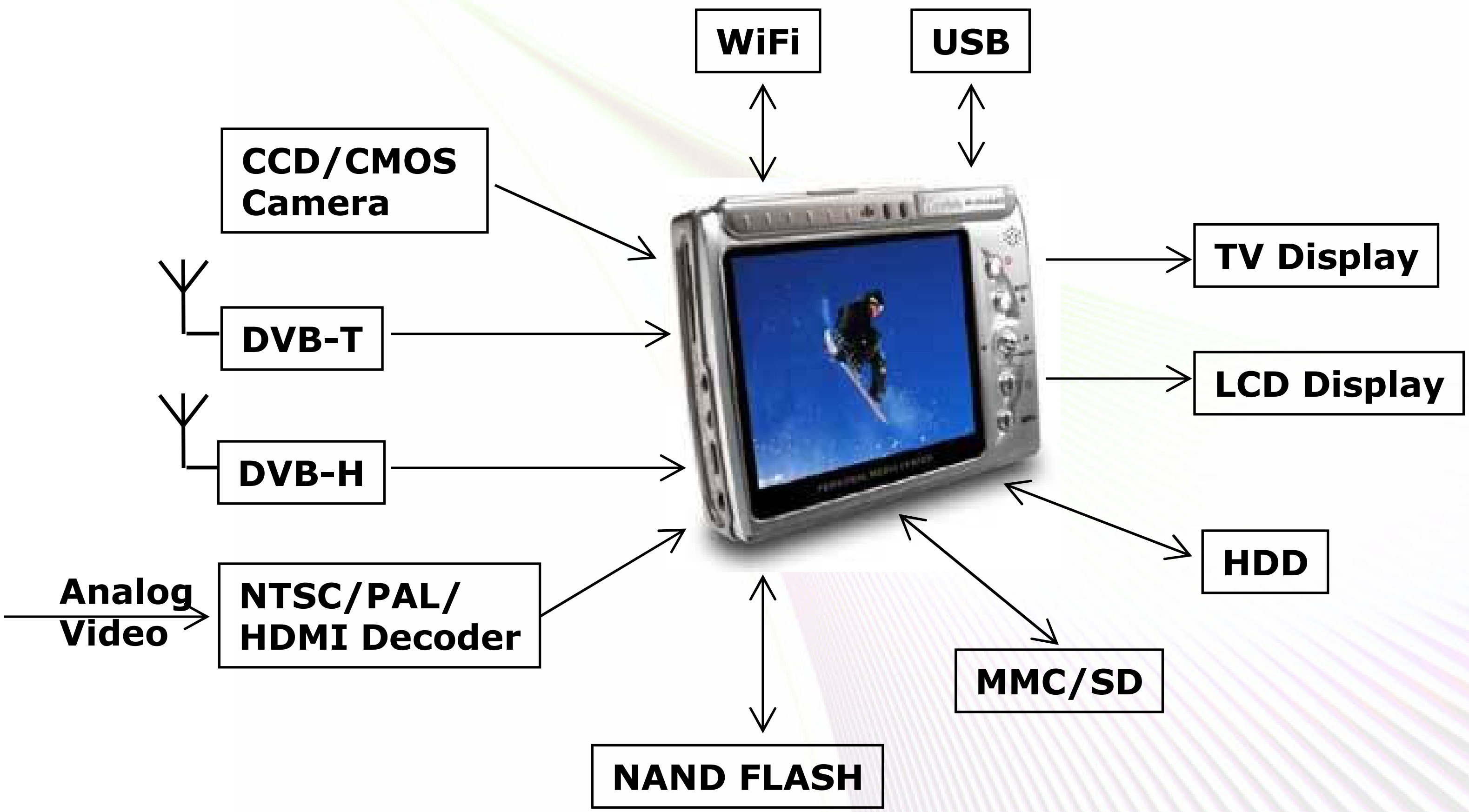
Portable Media Player – video interfaces



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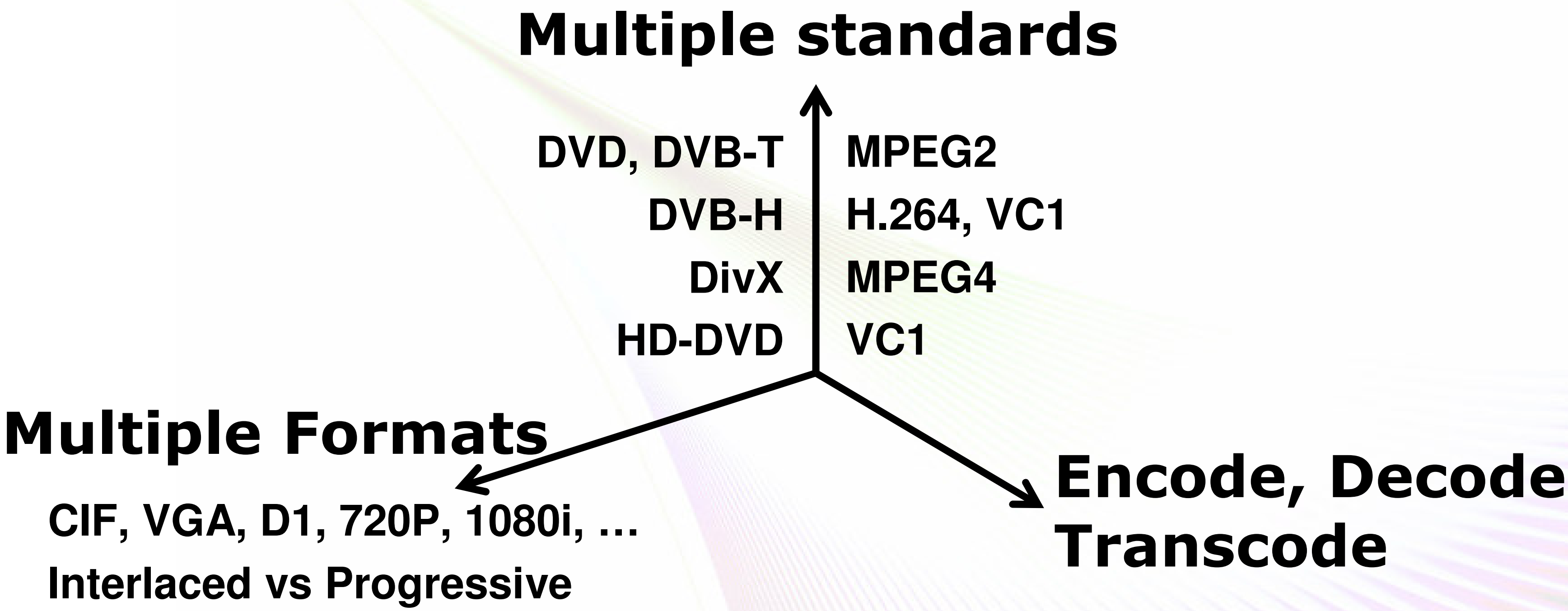
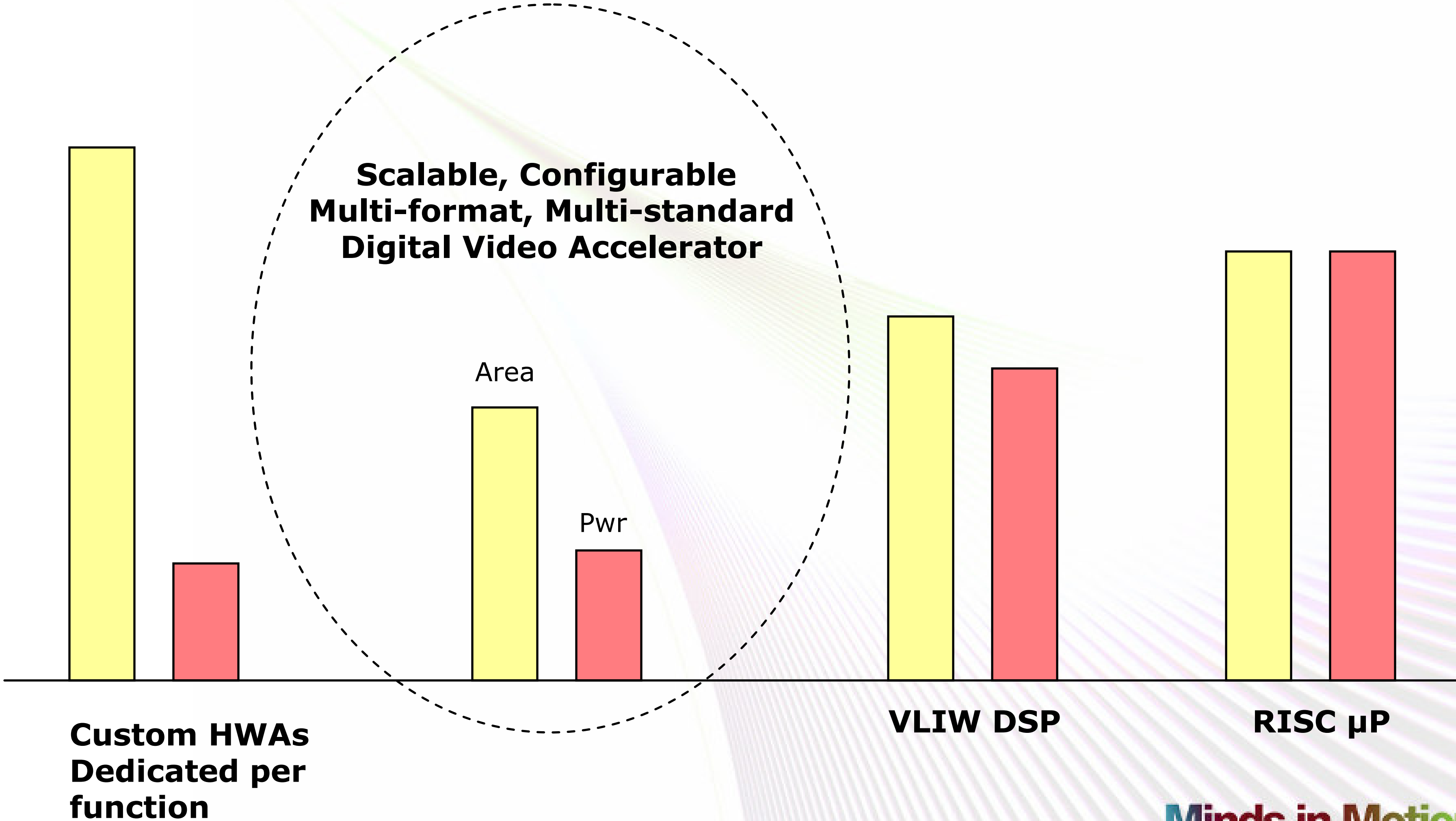
Key Requirements

- Multi-standard, multi-format video processing



- Power/Energy
- Cost

DV Engine Solution Space



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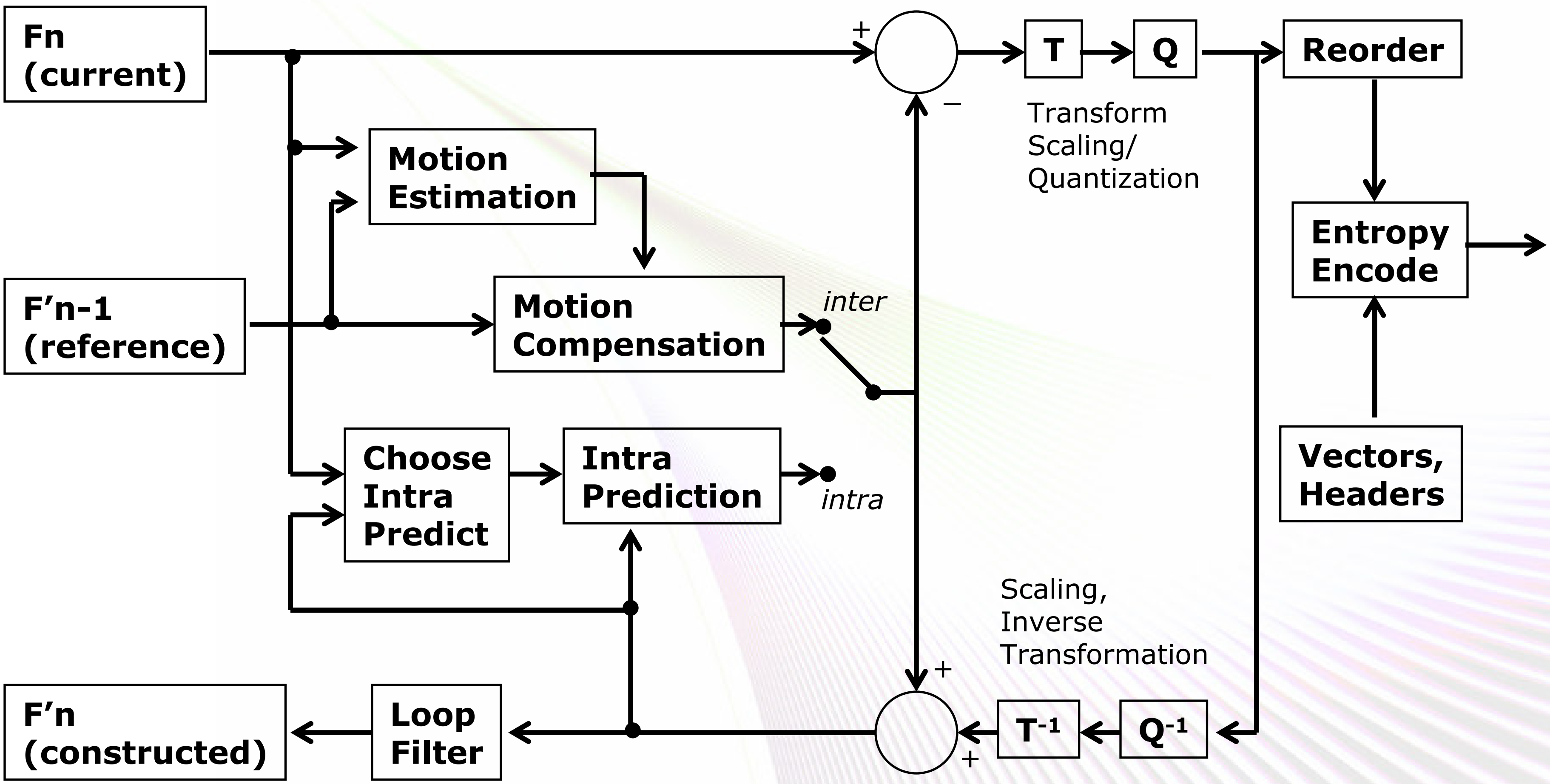
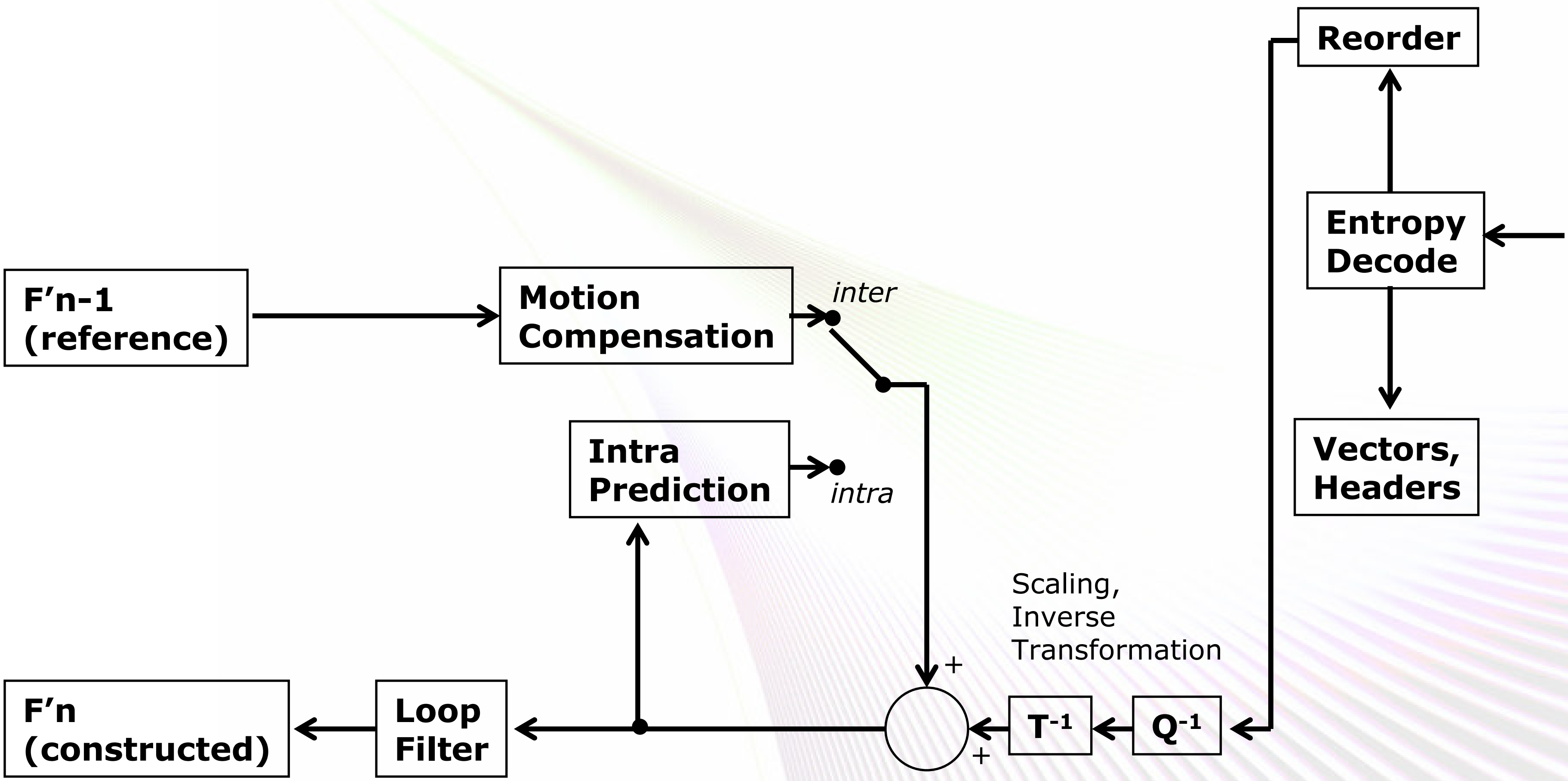
H.264 Encoder



H.264 Decoder



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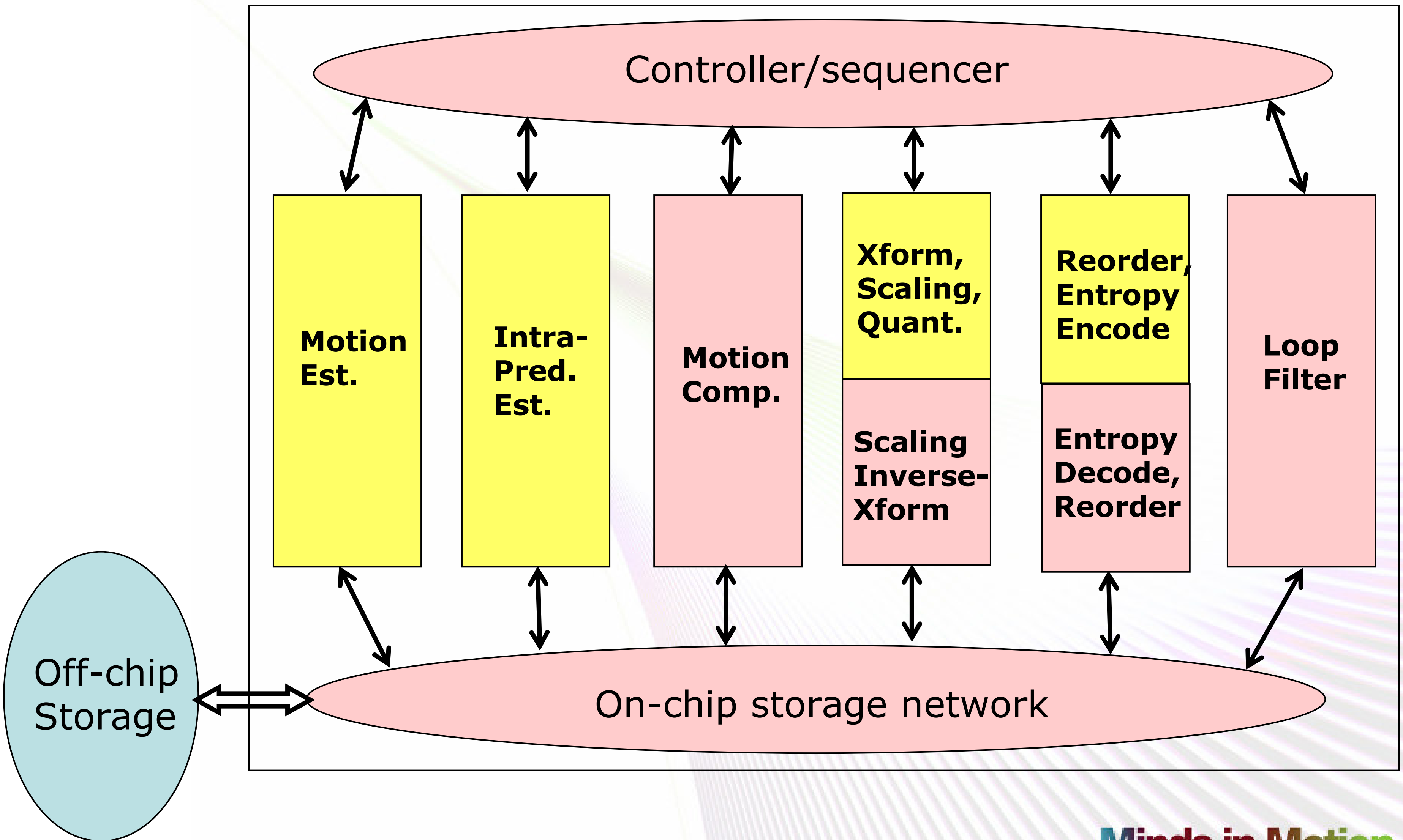
DV Engine



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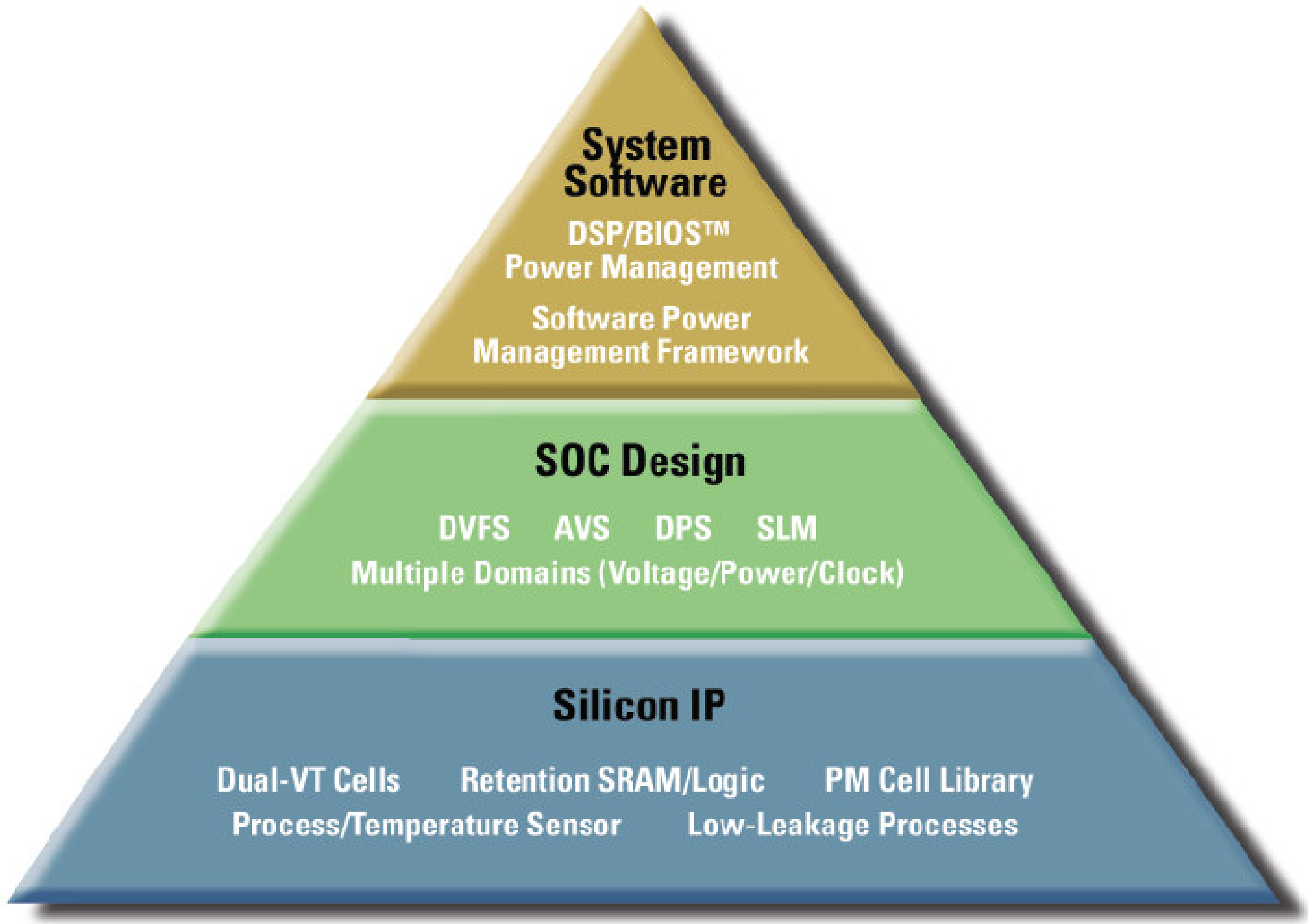
Power Dissipation

Two components of power dissipation

- Dynamic Switching Power
  $= \alpha \, C \, V^2 \, f$

- Static Leakage Power
  f (area, V^3, Temp, Process Tech & corner)

Low Power Design – across all levels



SoC level Power Management Strategies

SOC architectural and design technologies

Technology	Description
Adaptive Voltage Scaling (AVS)	Maintains high performance while minimizing voltage based on silicon process and temperature.
Dynamic Power Switching (DPS)	Dynamically switches between power modes based on system activity to reduce leakage power.
Dynamic Voltage and Frequency Scaling (DVFS)	Dynamically adjusts voltage and frequency to adapt to the performance required.
Multiple Domains (Voltage/Power/Clock)	Enables distinct physical domains for granular power/performance management by software.
Static Leakage Management (SLM)	Maintains lowest static power mode compatible with required system responsiveness to reduce leakage power.

Architecting for low power

- Achieve performance at as lower voltage and as lower frequency as possible:
  - Hardware acceleration vs general purpose programmable processor
  - Use pipelining and parallel processing

- Shut off (clock gating) unused logic (MB/frame level)

- Switch off (power down) unused logic (apps level)

- Leverage variability - scale the operating conditions (voltage and frequency) to match the needs

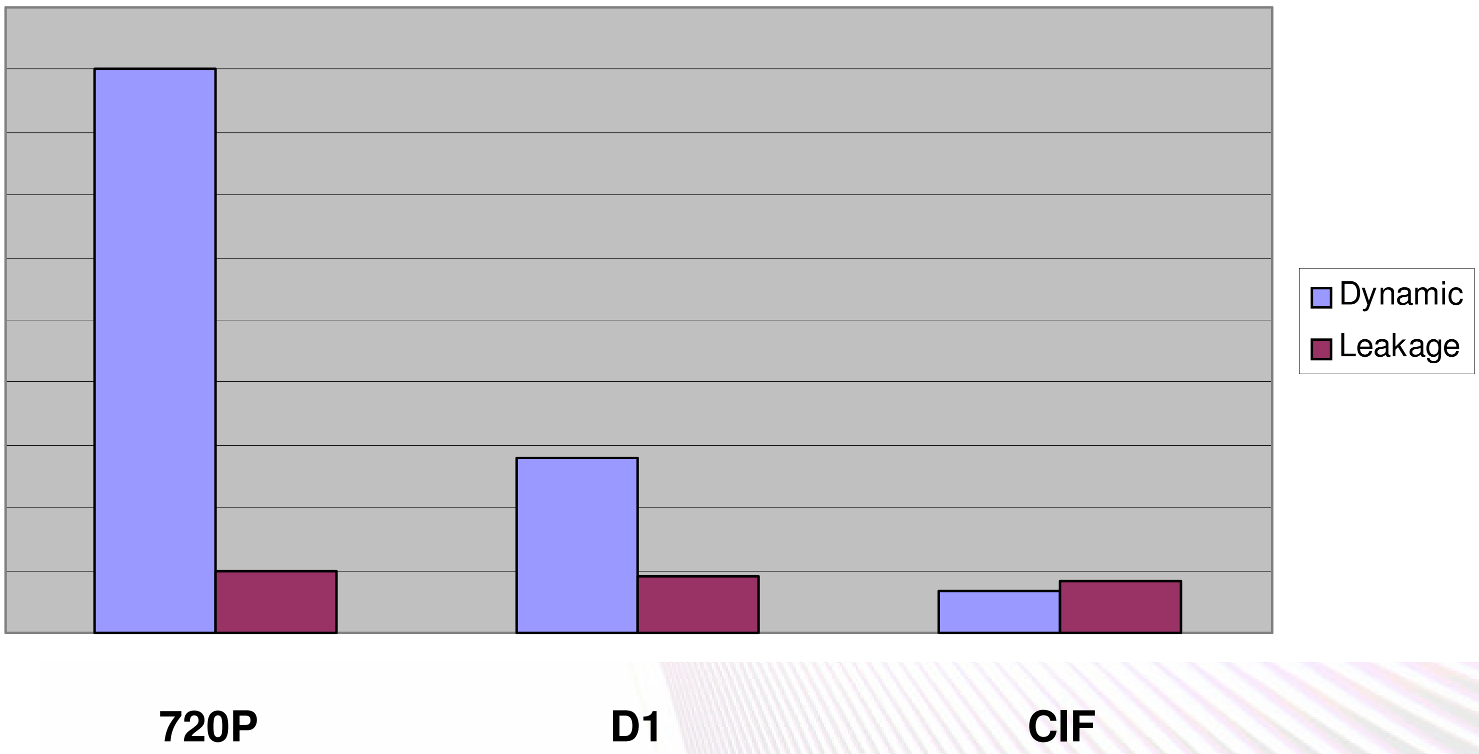
Variability

- Across processing (encode vs decode)
- Across formats (D1 vs 1080i)
- Across standards (MPEG4 vs H.264)
- Data driven variability

Data driven variability in Decoding

Fetch input bit stream	Entropy decoder and reorder	Inverse quantiza-tion, IDCT / Fetch reference frame data for MC	Motion compensa-tion and add residues	Deblocking Filtering
Data rate, System traffic	*Data per frame*	*#MVs, I/B/P frames, System traffic*	*#MV, MV resolution, I/B/P frames*	*Boundary Strength*

Dynamic vs Leakage Power Scaling with Resolution



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Power Reduction for CIF

- Compute requirements significantly lower, voltage scaling is limited by Vcc-min.
- Running the engine at lower frequency without lowering the voltage – does not help save energy
- Multiple approaches:
  1. Significant cycle overhead in completely switching off the engine and switching it back on – does not help at macro-block level, marginal gain at frame level, but done over a group of frames can give power reduction

  2. Power down the engine but save the state using retention flops and putting memories in the retention mode – area overhead

  3. Design the engine as a “bit slice” and switch off one half while processing CIF – has software implications.

DVFS – applicability at SoC level?

- Audio does not scale with resolution
- Any system function which demands real-time response in a narrow time window
- Modules in the video output processing chain which are tied to the resolution of the display device as against resolution of the video being processed
- Addressed using multiple voltage domains

Managing data bandwidth

- Increasing resolution – implies scaling the IO bandwidth accordingly – but may not be feasible, practical – DDR speed limitations, SDRAM limitation, power, area impact etc.

- Need architecture level solution to address this bottleneck
  - On-chip buffers
  - On the fly computation
  - Improving efficiency of 2D transfers
  - SDRAM data organization
  - Compression

- At lower resolution, can minimize SDRAM power by powering down unused banks

Summary

- HD Video is going portable
- Applications require multi-format, multi-standard encode/decode engine
- Need architecture level innovations to achieve low power
- Optimizing just the DV engine not adequate, need to take a system-level view
- TI offers (and will continue to offer) leadership solutions for low power HD video processing

THANK YOU

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