Designing Modular EVMs for Data Acquisition Products

Data Acquisition Products

ABSTRACT

This document defines a common set of design guidelines for modular evaluation modules from the Data Acquisition Products group. Adherence to these recommendations ensures the highest degree of compatibility across system development platforms. This document will help users of the 5-6K interface board (SLAU104) and the HPA449 Demonstration Board (www.softbaugh.com) develop a customizable, reconfigurable, cross-platform software/hardware prototyping system.

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Modular EVM Basics

The modular EVM design provides customers with maximum flexibility for the evaluation of data-acquisition products from Texas Instruments. Several interface boards are available to provide compatibility with the TMS320C5000™ and TMS320C6000™ series of DSP Starter Kits (DSK's), as well as third party development kits such as the TMS320C2000 eZdsp™ series of development boards from Spectrum Digital Incorporated (www.SpectrumDigital.com), and the HPA449 Development Board from SoftBaugh, Incorporated (www.SoftBaugh.com).

Following the guidelines in the *TMS320 Cross-Platform Daughtercard Specification* (SPRA711), signal names and references to the multichannel buffered serial port (McBSP) found throughout this document are common to those found in the SPRA711 document.

The PWB footprints referenced in later sections of this document plug into platform-specific DSK, FPGA or microcontroller-specific interface boards. The platform-specific interface board routes various control and data lines to the modular EVM mating connectors. This allows the same modular EVM design to be used across a variety of host processors.

There are two basic modular EVM types, serial and parallel. Regardless of the interface type, all modular EVMs have a standard analog interface and standard power connector.

Universal Analog I/O

The analog I/O connector provides up to eight single-ended or four differential channels to/from the data converter. External reference voltages may also be applied to the converter through the analog I/O connector. Since the reference requirements vary by converter type, no restrictions are placed on the voltage levels. Single or dual-channel data converters also follow this convention, leaving unused channels open.

Table 1 shows the universal analog connector pinout:

Table 1. Universal Analog I/O Connections

Signal	Pin Number		Signal
A0(-)	**1**	**2**	A0(+)
A1(-)	**3**	**4**	A1(+)
A2(-)	**5**	**6**	A2(+)
A3(-)	**7**	**8**	A3(+)
AGND	**9**	**10**	A4
AGND	**11**	**12**	A5
AGND	**13**	**14**	A6
VCOM	**15**	**16**	A7
AGND	**17**	**18**	REF-
AGND	**19**	**20**	REF+

Applying Differential Signals

There are two possible methods for interfacing differential ADCs or DACs to the common analog I/O connectors. Up to four differential signals may be applied across pins 1-2, 2-3, 3-4 and 4-5 as indicated in Table 1. This is an appropriate method to interface to true differential ADCs and DACs.

In cases where the signal applied to a data converter can be either differential or single ended, differential signals are typically applied between adjacent pairs of connections with pins 2, 6, 10, and 14 designated as (-) and pins 4, 8, 12, and 16 as (+) as shown in Table 2.

Table 2. Alternate Analog I/O Connections

Signal	Pin Number		Signal
AGND	**1**	**2**	A0(-)
AGND	**3**	**4**	A0(+)
AGND	**5**	**6**	A1(-)
AGND	**7**	**8**	A1(+)
AGND	**9**	**10**	A2(-)
AGND	**11**	**12**	A2(+)
AGND	**13**	**14**	A3(-)
VCOM	**15**	**16**	A3(+)
AGND	**17**	**18**	REF-
AGND	**19**	**20**	REF+

Data converters requiring additional analog inputs can use test points to provide access to the additional channels, or the board size can be increased to accommodate a second analog I/O connector. Please see the modular EVM footprint section for details.

Standard Power Connector

The power-connector definition accommodates both the serial and parallel versions of the modular EVM. The primary power connector used on the modular EVM is a ten-pin female connector. The preferred connector is Samtec P/N SSW-105-F-D-VS-K. The power-connector pinout is defined in Table 3.

Table 3. Standard Power Connections

Signal	Pin Number		Signal
+VA (+12V typ.)	**1**	**2**	(-12V typ.) -VA
+5VA	**3**	**4**	-5VA
DGND	**5**	**6**	AGND
+1.8VD	**7**	**8**	VD1
+3.3VD	**9**	**10**	+5VD

Voltage requirements other than those shown in Table 3 may require that the EVM designer regulate the appropriate voltage according to the power requirements of the particular device. The EVM designer must ensure the voltage rating of any component requiring +/- VA connections is a minimum 16-Vdc. Components not rated to 16-Vdc minimum must be protected against over-voltage by appropriate circuitry located within the confines of the EVM.

An appropriate mating connector (Samtec P/N TSM-105-01-T-DV) can be placed on the top side of the EVM to accommodate pass-through applications, such as parallel, daisy-chain or I^2C-controlled devices.

Serial Data/Control Interface

The standard serial interface uses the signals defined in the *TMS320 Cross-Platform Daughtercard Specification* (SPRA711) for DSP-centric data converters. These signals are based on the multichannel buffered serial port (McBSP) interface found on most Texas Instruments DSP's. To accommodate microcontroller/microprocessor-centric data converters, the serial interface also includes an I^2C bus and several GPIO lines.

Careful planning is required when using GPIO as a primary source of control for critical data converter functions. Many digital signal processor starter kits (DSKs) do not provide access to general purpose I/O signals. In order to maintain flexibility and to facilitate multi-platform operation, include jumpers to force the signal to a desired state on critical signal paths controlled by GPIO.

The serial data/control connector used on the modular EVM is a 20-pin female connector located on the bottom side of the PWB with a corresponding a 20-pin male connector located on the top. The preferred connectors are Samtec P/N SSW-110-F-D-VS-K (bottom), and TSM-110-01-T-DV (top). This socket/pin combination allows for board stacking (when appropriate) as well as easy access to the data and control pins for test and debugging purposes.

Table 4 shows the standard serial connector pinout.

Table 4. Standard Serial Control Connections

Signal	Pin Number		Signal
CS (/SS)	**1**	**2**	GPIO0
CLKX (SCLK)	**3**	**4**	DGND
CLKR (clock return)	**5**	**6**	GPIO1
FSX (frame sync transmit)	**7**	**8**	GPIO2
FSR (frame sync return)	**9**	**10**	DGND
DX (MOSI)	**11**	**12**	GPIO3
DR (MISO)	**13**	**14**	GPIO4
*INT (interrupt source to host)	**15**	**16**	SCL
TOUT (clock or timer input)	**17**	**18**	DGND
GPIO5	**19**	**20**	SDA

Designers familiar with the McBSP architecture will recognize the signal names on the odd-numbered pins shown in Table 4. The signals shown in parentheses beside CS, CLKX, DX and DR are the general equivalents to the standard serial-peripheral interface found on many microcontrollers such as the MSP430™, or DSPs such as the TMS430F2407™.

GPIO Accomodation

For cross-platform compatibility, the following sections briefly describe the GPIO functions shown in Table 4. In all cases, GPIO2 thru GPIO5 may be considered as I^2C master-controlled when an I^2C master device is incorporated in the design.

5-6K Interface Board

The C5000 and C6000 series DSKs have limited GPIO capabilities on the expansion and peripheral connectors. The signals from the McBSP port however, can be used to drive GPIO functions under certain conditions. When the transmitter portion of the McBSP is not needed, the design can use the CLKX and FSX pins for GPIO, and the DX pin as GPout. Certain data converters do not require the receiver portion of the McBSP and can use the CLKR and FSR pins as GPIO, while the DR pin can function as a GPin.

The connections shown as GPIO1 thru GPIO5 above are routed to test points on the 5-6K interface board. These test points allow the user to hand-wire any available GPIO to the serial control connector. The signals shown as SCL and SDA form the basis of an I^2C bus and also route to test points for user defined control.

HPA449 Development Board

The HPA449 Development Board provides GPIO2 thru GPIO5 as an expansion from the I^2C bus through a PCF8574 - *Remote 8-Bit I/O Expander*. The GPIO functions can be controlled through an I^2C EPROM located on the modular EVM, or through a virtual I^2C bus developed within the MSP430F449 located on the development board. Since there is no McBSP functionality in the MSP430F449, signals FSX, FSR, and CLKR can be treated as GPIO.

Serial EVM Stacking

Serial EVMs can be stacked, provided that the board designer carefully considers the analog input/output and serial control requirements of the data converter. When designing stackable EVM's, the female connector (located on the bottom side of the board) may be considered as an input to the stack, with the male connector (top side) considered as an output to the next board in line.

An EVM containing an I^2C master device for instance, could use a GPIO expander such as the PCF8574 to develop a unique address for up to eight boards that share a common bus. Daisy chain converters can use a similar approach by receiving data through the lower connector and transmitting the delayed data through the upper connector. Jumpers or analog switches can be incorporated to select individual analog input or output pins.

Parallel Interface

The standard parallel interface also uses the signals defined in the *TMS320 Cross-Platform Daughtercard Specification* (SPRA711). The standard parallel interface consists of two connectors, parallel control and parallel data as described in the following sections.

Parallel Control

The parallel-control connector is a 20-pin female connector located on the bottom side of the PWB and a 20-pin male connector located on the top. The preferred connectors are Samtec P/N SSW-110-F-D-VS-K, and TSM-110-01-T-DV.

Table 5. Parallel Control Connections

Signal	Pin Number		Signal
*CS	1	2	DGND
*WR / R/*W	3	4	DGND
*RD	5	6	DGND
EVM A0 (GP in)	7	8	DGND
EVM A1 (GP in)	9	10	DGND
EVM A2 (GP in)	11	12	DGND
EVM A3 (GP in)	13	14	DGND
EVM A4 (GP in)	15	16	DGND
TOUT	17	18	DGND
*INT	19	20	DGND

The parallel control lines connect to the DSP interface on the interface card. A minor glue logic design accommodates the differences between the read and write strobes of the C5000- and C6000-series DSPs. This logic is incorporated on the 5-6K interface board.

The 5-6K interface board and the C2000 interface board have several jumper options to provide nearly identical pin functions, regardless of the attached DSP. Please see the related user's guides for additional details and specific interface-related issues. The HPA449 demonstration board uses GPIO lines to control the addressing, read, and write functions.

Parallel EVM Stacking

To facilitate stacking, use the signals denoted EVM_A0 through EVM_A3 as address lines, connected through buffers to the DSP address bus. These EVM address lines are selectable as DC_A[2..5] or DC_A[14..17] for the C6xxx DSK, or DC_A[0..3] or DC_A[12..15] for the C5xxx DSKs. Address decoding functions incorporated on the EVM allow stacking of parallel ADC and DAC boards.

The previously-mentioned interface boards each have two analog signal-conditioning sites. To provide a flexible data-acquisition system using both ADC and DAC boards, use analog site 1 as an input to parallel ADC boards, and analog site 2 as an output from DAC boards. For further information, please refer to the various interface board users guides.

Parallel Data Bus

The standard parallel data connector used on the modular EVM is a 32-pin female connector located on the bottom side of the PWB and a 32-pin male connector located on the top. The preferred connectors are Samtec P/N SSW-116-F-D-VS-K and TSM-116-01-T-DV. The parallel data bus is a minimum of 16 bits wide and can be expanded to a maximum of 24 bits in 4-bit increments. Data is aligned LSB to LSB for cross platform compatibility. The following table shows the parallel-data connector options:

Table 6. Parallel Data Connections

Signal	Pin Number		Signal
Use Samtec P/N SSW-116-F-D-VS-K, and TSM-116-01-T-DV for 16-bit data bus			
D0	**1**	**2**	DGND
D1	**3**	**4**	DGND
D2	**5**	**6**	DGND
D3	**7**	**8**	DGND
D4	**9**	**10**	DGND
D5	**11**	**12**	DGND
D6	**13**	**14**	DGND
D7	**15**	**16**	DGND
D8	**17**	**18**	DGND
D9	**19**	**20**	DGND
D10	**21**	**22**	DGND
D11	**23**	**24**	DGND
D12	**25**	**26**	DGND
D13	**27**	**28**	DGND
D14	**29**	**30**	DGND
D15	**31**	**32**	DGND
Use Samtec P/N SSW-120-F-D-VS-K, and TSM-120-01-T-DV for 20-bit data bus			
D16	33	34	DGND
D17	35	36	DGND
D18	37	38	DGND
D19	39	40	DGND
Use Samtec P/N SSW-124-F-D-VS-K, and TSM-124-01-T-DV for 24-bit data bus			
D20	41	42	DGND
D21	43	44	DGND
D22	45	46	DGND
D23	47	48	DGND

Standard EVM Footprints

There are three basic modular EVM footprints: single serial, double serial, and parallel. The following section gives details on the physical size and standard connector placement:

Single Serial

A single-wide serial PWB is 3.200 x 1.700 inches. Using the lower left corner as the origin, the analog I/O connector is placed at 0.250 inches X and 0.850 inches Y. The power connector is located 1.6 inches X and .250 inches Y. The digital I/O connector is placed at 2.950 inches X and 0.850 inches Y. Connector placement is based on the centroid of the component. In all cases, the female connector is located on the bottom side of the PWB while the male is located on top. Pin-1 locations are denoted by the small square.

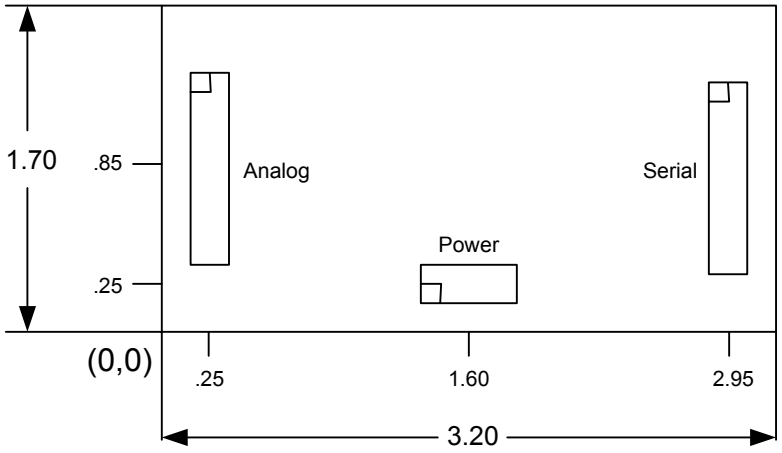


Figure 1. Single Serial

Dual Serial

A dual wide serial PWB is 3.200 x 3.700 inches. Using the lower left corner as the origin, the primary analog I/O connector is placed at 0.250 inches X and 2.850 inches Y. The power connector is located 1.6 inches X and .250 inches Y. The primary digital I/O connector is placed at 2.950 inches X and 2.850 inches Y. Secondary analog I/O and Digital I/O connectors may be placed at 0.250 inches X and 0.850 inches Y and 2.950 inches X and 0.850 inches Y respectively. Connector placement is based on the centroid of the component. In all cases, the female connector is located on the bottom side of the PWB while the male is located on top.

The secondary digital I/O connector may use the secondary McBSP signals as additional GPIO or with devices having multiple serial inputs/outputs.

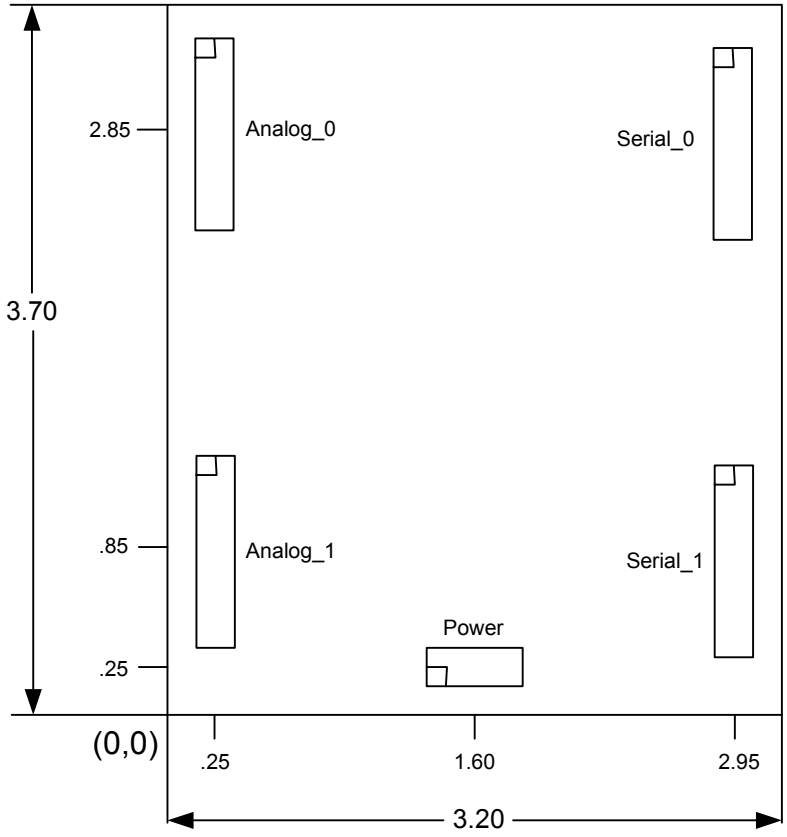


Figure 2. Dual Serial

Parallel Interface

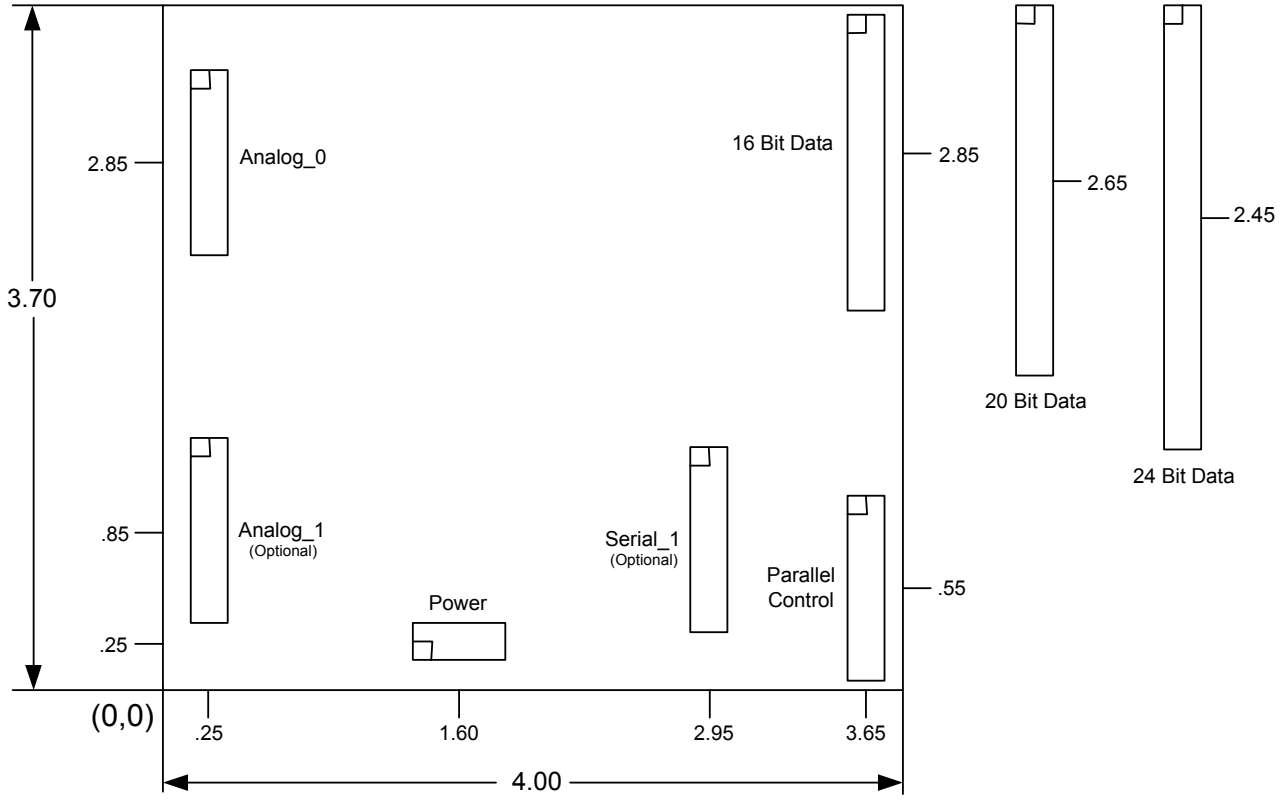
A parallel interface PWB is 4.000 x 3.700 inches. Using the lower left corner as the origin, the primary analog I/O connector is placed at 0.250 inches X and 2.850 inches Y. The Power connector is located 1.6 inches X and .250 inches Y. The parallel control connector is located 3.650 inches X and 0.550 inches Y. Parallel data connector placement is based on size of the connector. In all cases, the parallel data connector is located at 3.650 inches X. Aligning on pin 1, 16, 20 and 24-bit wide connectors are placed at 2.850, 2.650 and 2.350 inches Y.

Connector placement is based on the centroid of the component. In all cases, the female connector is located on the bottom side of the PWB while the male is located on top. Pin 1 is denoted by a small square.

To provide the greatest flexibility in developing a system of data converters, use Analog_0 as the input to the board for ADCs, and Analog_1 as the output for DACs.

For additional GPIO functions or combined serial/parallel devices, a serial control connector can be placed at 2.950 inches X and 0.850 inches Y.

Figure 3. Parallel Interface



Signal Conditioning/Sensor Cards

The interface boards that accommodate the modular EVM provide signal-conditioning sites to allow a variety of amplifiers and/or sensors to be used in conjunction with the ADC and DAC modules. The signal-conditioning board is 1.70 x 3.375 inches. Using the lower left corner as the origin, the primary analog input connector is placed at 0.250 inches X and 2.850 inches Y. The power connector is located 2.45 inches X and .18 inches Y. The analog output connector is located 2.45 inches X and 0.18 inches Y.

Figure 4. Optional Amplifier Card

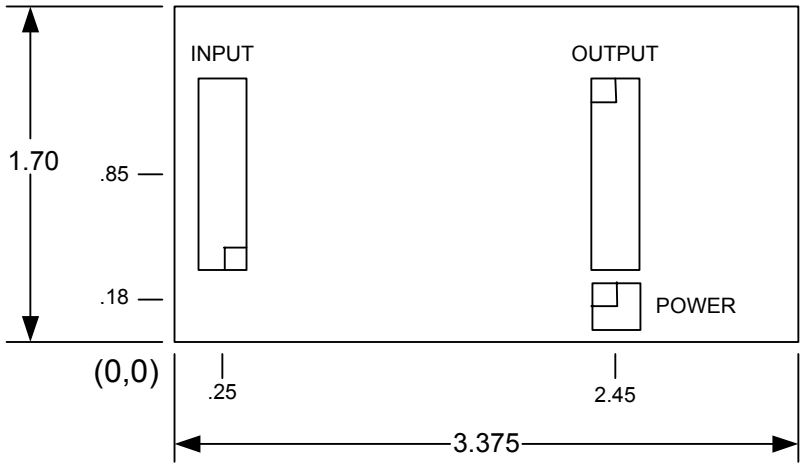


Table 7 provides the pinout for the analog input/output connectors and power connector.

Table 7. Signal Conditioning Connections

Signal	Pin Number		Signal		Signal	Pin Number		Signal
As Input to an ADC					As Output from a DAC			
A0(-)	1	2	A0(+)		A0(-)	1	2	A0(+)
A1(-)	3	4	A1(+)		A1(-)	3	4	A1(+)
A2(-)	5	6	A2(+)		A2(-)	5	6	A2(+)
A3(-)	7	8	A3(+)		A3(-)	7	8	A3(+)
AGND	9	10	A4		AGND	9	10	A4
AGND	11	12	A5		AGND	11	12	A5
AGND	13	14	A6		AGND	13	14	A6
VCOM	15	16	A7		VCOM	15	16	A7
AGND	17	18	SPARE		AGND	17	18	REF-
AGND	19	20	SPARE		AGND	19	20	REF+

Table 8. Amplifier Card Power Connections

Signal	Pin Number		Signal
+VA (+12V typ.)	1	2	(-12V typ.) -VA
+5VA	3	4	-5VA
AGND	5	6	AGND

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265