

# Three-Phase Electronic Watt-Hour Meter Design Using MSP430

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MSP430 Applications

## ABSTRACT

This application report describes the implementation of a three-phase electronic electricity meter using MSP430 4xx family of microcontrollers. The implemented functions are RMS voltage for each phase, RMS current for each phase, frequency, power, and a real-time clock (RTC).

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## 1 Introduction

This application report describes a hardware reference design and software routines for implementing an electronic electricity meter using the MSP430F449 device. An ultra-low-power software real-time clock (RTC) with temperature compensation saves additional cost. Figure 1 shows a block diagram of the design.

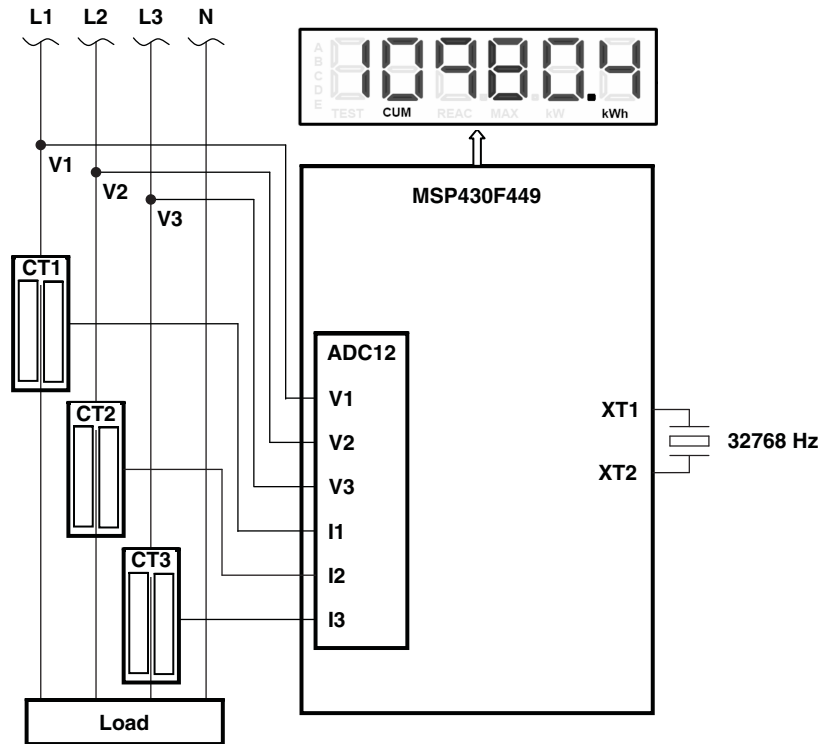


Figure 1. Block Diagram

## 2 Hardware Implementation

The following sections described the design of the hardware for the electronic watt-hour meter.

### 2.1 Capacitor Power Supply

Figure 2 shows a capacitor power supply for a single output voltage of  $V_{CC} = 3\text{ V}$ . If the output current is not sufficient, an NPN output buffer may be used. The design equations for the power supplies are given in *MSP430 Family Mixed-Signal Microcontroller Application Reports (SLAA024)*, Section 3.8.3.2, *Capacitor Power Supplies*. This section also describes other kinds of power supplies and their design equations.

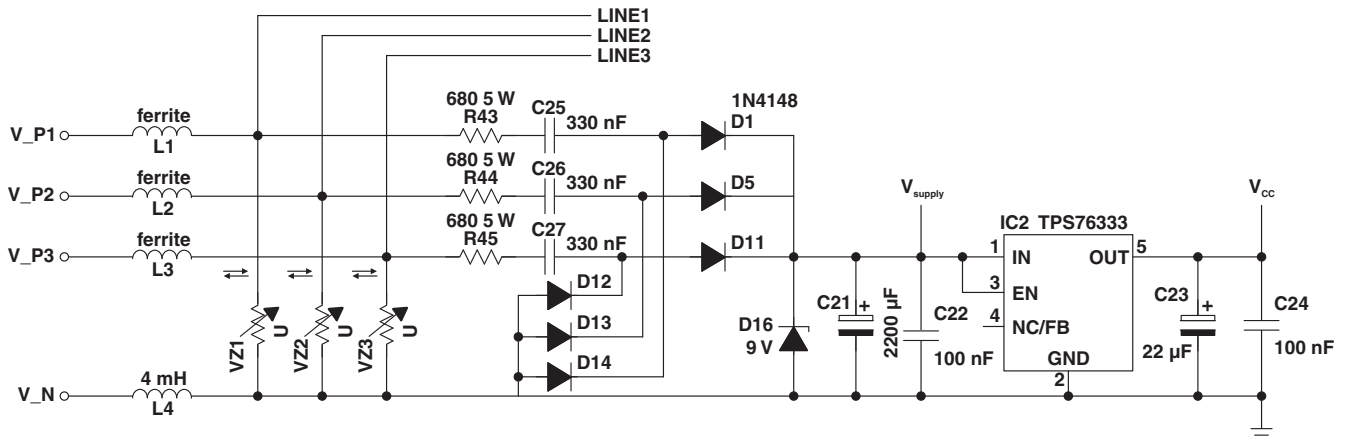


Figure 2. Capacitor Supply

### 2.2 Voltage Inputs

Figure 3 shows the voltage input section. Resistors R46, R47, and R48 reduce the mains voltage to a level that is within the analog-to-digital converter (ADC) input range. Because the ADC inputs are single ended, resistors R42 and R20 pull the input signal above the ground level. An RC filter of  $R = 15\text{ k}\Omega$ ,  $C = 100\text{ nF}$  and  $1\text{ }\mu\text{F}$  is used as the antialiasing filter.

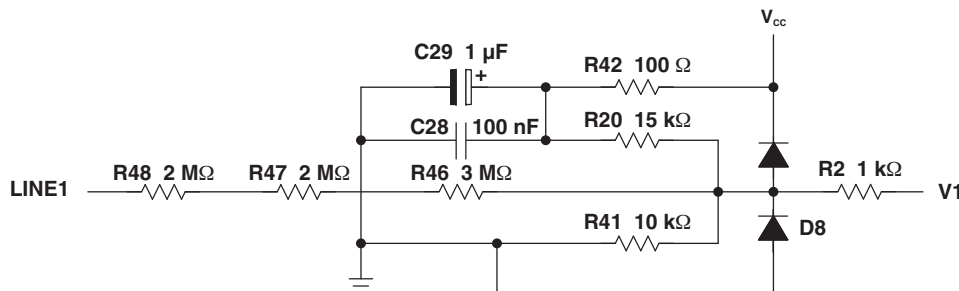


Figure 3. Voltage Inputs

### 2.3 Current Inputs - Current Transformer (CT)

Figure 4 shows the current input section for one CT. R21 is the burden resistor for the CT. The value of the burden resistor is selected based on the CT specification. Also, a bias voltage is added to the CT output to keep the signal level above ground level, as the ADC is single ended.

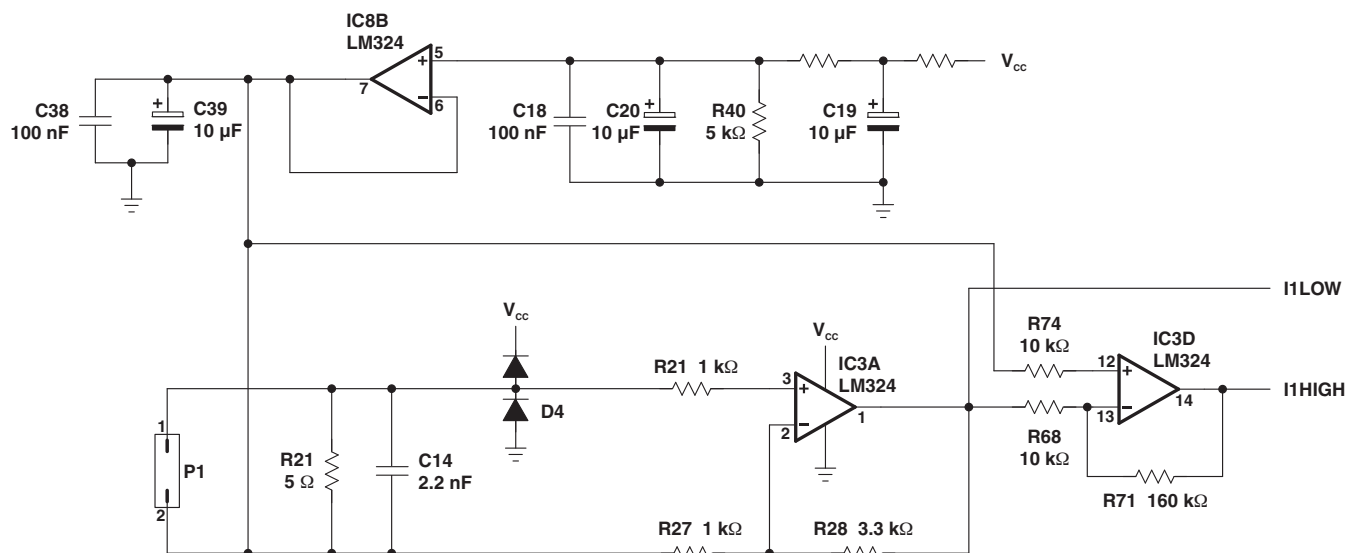


Figure 4. Current Inputs

### 2.4 CT Signal Preamplification

The CT signal is amplified by the operational amplifier using two gain settings. The first gain setting provides a full-scale input to the ADC at maximum current. The second gain setting further amplifies the signal 16 times. These two signals are connected to two ADC12 input pins.

## 3 Software Implementation

Software is implemented into two major areas, the foreground process and the background process. The background functions use a timer interrupt to trigger the ADC and to collect the voltage and current samples of each phase. These samples are further processed and accumulated into buffers. The background function deals mainly with the timing-critical elements of the software.

Once sufficient samples have been accumulated, the foreground functions are used to calculate the final values of  $V_{rms}$ ,  $I_{rms}$ , frequency, and power.

A separate library, `emeter-toolkit-449.lib`, contains most of the commonly used mathematical routines. Also, a setup file contains the initialization routine for the device. Other files include the RTC software implementation, other mathematical functions, and the display functions.

After system reset, the MSP430 hardware is first set up (see Section 3.1). The program then enters the main foreground process loop and waits for the timer interrupt routine to gather data.

### 3.1 Setup

The following sections describe the setup of the device modules and peripherals.

#### 3.1.1 LCD

The LCD is set for 4-mux mode with the internal charge pump on. The refresh rate is set to ACLK/128.

#### 3.1.2 Clock

A 32-kHz watch crystal is connected to the XT1/XT2 pins of MSP430, which sets the ACLK to 32 kHz. The FLL is set to multiply the ACLK of 32 kHz by 256, which gives a CPU clock (MCLK) of approx 8 MHz.

#### 3.1.3 Timer\_A and ADC12

The MSP430 ADC12 sampling and conversion process is triggered by a hardware timing signal coming from Timer\_A. This feature is very important for signal processing, as software-triggered ADC sampling adds timing jitter, which creates additional noise in the signal samples.

The ADC12 also can add a programmable amount of sample-and-hold time so that the sampling time matches with the source impedance of the signals. In the application described in this report, multiple signals are sampled. The ADC is set up such that the trigger from Timer\_A starts a single sequence of samples.

Timer\_A is configured to count in up mode (count to TACCR0) from the timer clock source of 32-kHz ACLK. TACCR0 is set to 9, giving a sampling rate of 3276.8. Compare register CCR1 is programmed to trigger the ADC12. CCR1 is set such that it triggers the ADC conversion in hardware 1/32768 second after the Timer\_A0 interrupt service routine has rearmed the ADC12 sampling sequence.

The ADC12 sequence is defined as:

- I1 low gain = ADC12MEM0
- I1 high gain = ADC12MEM1
- V1 = ADC12MEM2
- I2 low gain = ADC12MEM3
- I2 high gain = ADC12MEM4
- V2 = ADC12MEM5
- I3 low gain = ADC12MEM6
- I3 high gain = ADC12MEM7
- V3 = ADC12MEM8
- Temperature Sensor = ADC12MEM9

The MSC bit of the ADC12 is turned on, so that the ADC12 can complete the sequence as fast as possible. Each sample/conversion requires SampleTimer + 13 ADC clock cycles.

At the end of the sequence, all 11 samples are ready for the interrupt service routine (ISR). Using four ADC channels as an example, [Figure 5](#) shows how this process works:

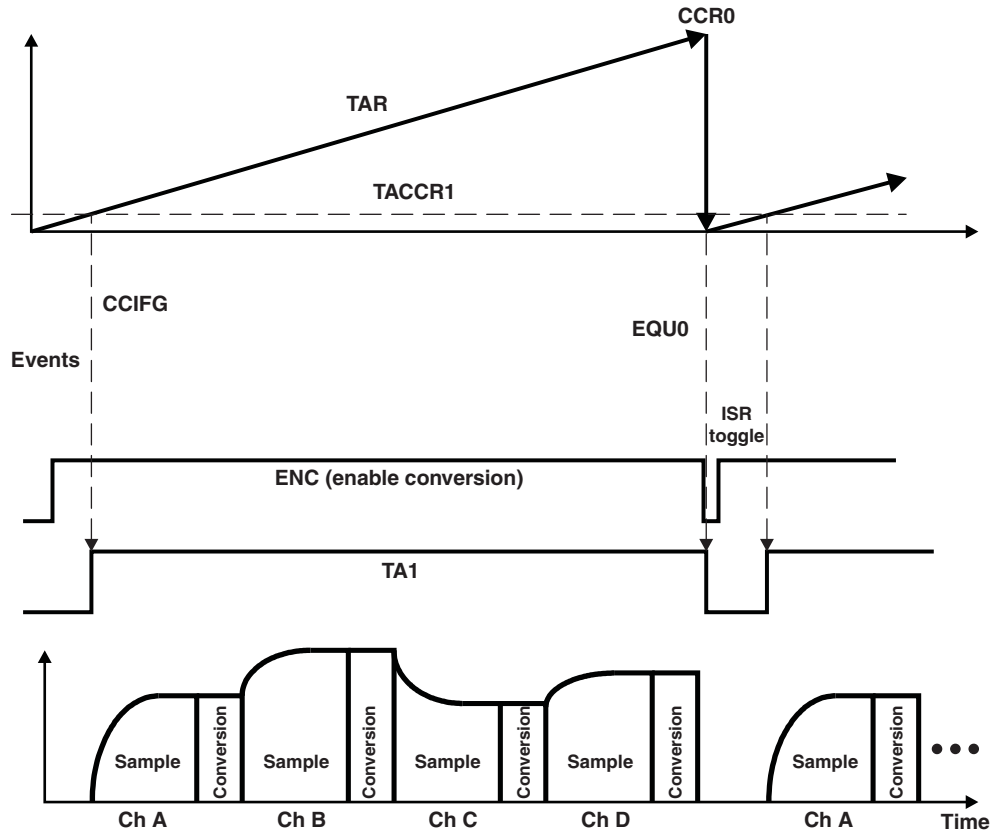


Figure 5. Sample-and-Conversion Process

### 3.1.4 Extending the Resolution of ADC12

To maintain accuracy across the entire current range, the 12-bit ADC resolution must be extended to approximately 15 bits. This is done by providing an additional gain of 16 on each current signal input to the ADC and using software to select which gain setting is the most suitable.

For each current signal, there are two sets of samples available to the ADC, one with low gain and one with high gain. The software chooses the largest nonsaturated signal available on a sample-by-sample basis. This signal is then gain adjusted and phase compensated according to the input it is taken from.

Figure 6 shows this process:

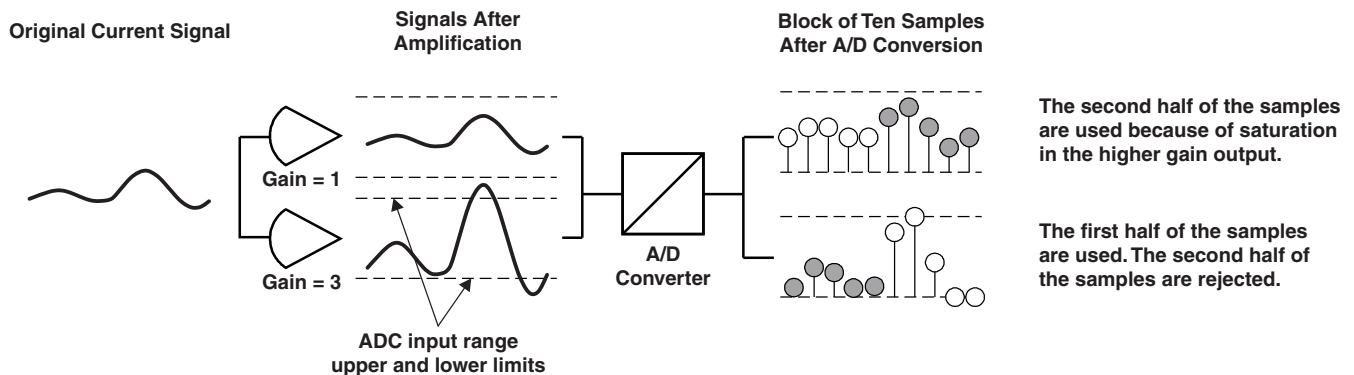


Figure 6. Extending ADC12 Resolution

### 3.1.5 Basic Timer

The basic timer is configured to give a one-second timer interrupt, based on the 32-kHz ACLK, for the real-time clock (RTC) function.

### 3.1.6 Watchdog Timer

The watchdog is enabled. The basic timer interrupt must reset it periodically; otherwise, the watchdog generates a system reset.

### 3.1.7 Voltage Supervisor and System Voltage Monitoring

The built-in hardware Supply Voltage Supervisor (SVS) circuit is turned on to ensure that the MCU is in a known state all the time. At reset, the SVS is first turned on to check whether or not the  $AV_{CC}$  level is high enough for the MCU clock of 8 MHz. Once this is confirmed, the SVS is fully enabled to generate a system reset when the voltage dips below the minimum allowed level for that operating speed.

The  $V_{supply}$  voltage (see [Figure 2](#)) is divided down and connected to the input of the comparator. When a mains blackout occurs,  $V_{supply}$  starts to drop. The comparator can, therefore, warn the system to prepare to go into the ultra-lower power RTC mode.

### 3.2 Background Process

Figure 7 shows the background process that runs in the meter application. The background process deals with the timing-critical elements of electricity measurement.

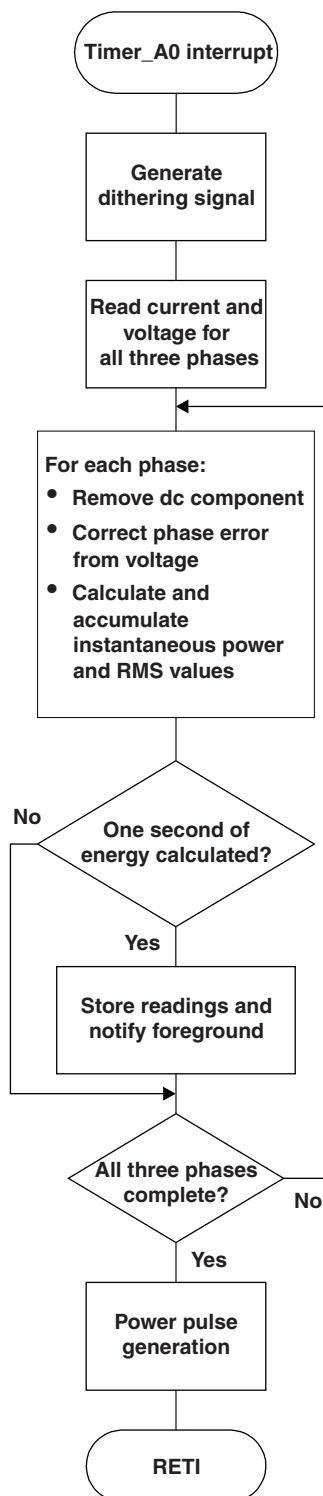


Figure 7. Background Process

### 3.2.1 Timer Interrupt

The ADC is triggered using the precise PWM pulse coming out of Timer\_A1. The sampling frequency is set to  $(32768/10) = 3.2768$  ksp/s.

The ADC12 control registers are set such that each PWM pulse triggers a series of voltage and current conversion cycles, one after another. The PWM pulse width is calculated such that the timer interrupt happens when the conversion results are ready.

Each sample interval, therefore, returns the three pairs of current and voltage samples, the neutral sample, and the CT offset voltage samples.

Figure 8 shows the signal flow for one phase.

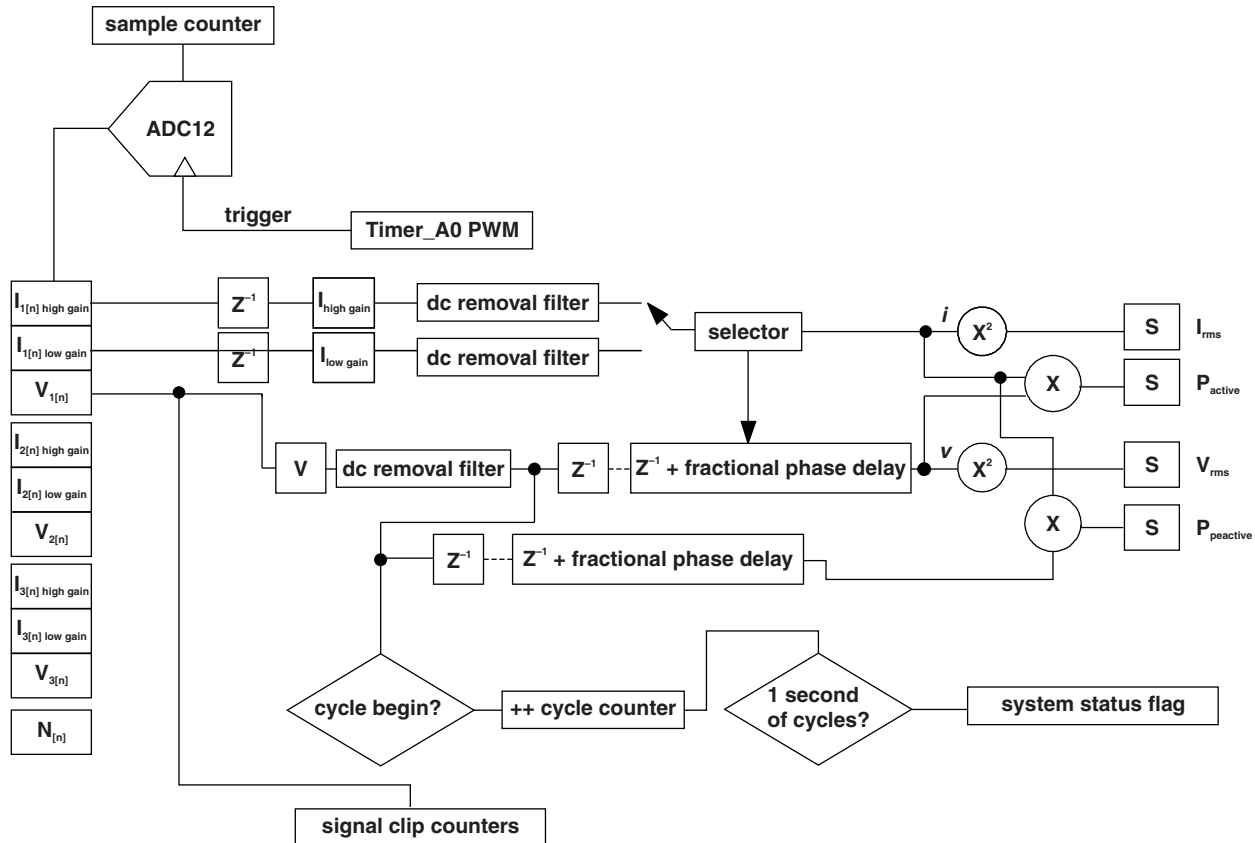


Figure 8. Signal Flow for One Phase

### 3.2.2 Voltage

The voltage signal has both a dc offset and ac component. In electricity measurement, the dc offset is filtered out, and the ac signal is extracted.

There is a phase difference between the current sample and the voltage sample. This is mainly caused by the current transformer, the analog front end circuit, and the sequential sampling process. A simple finite impulse response (FIR) filter is used to remove this phase difference by adding a fractional delay on the voltage signal. Because the current sample is delayed by one sample, by adding the right amount of delay, the phase compensation can be both positive and negative.

The voltage signal is selected for this fractional phase adjustment function, because it is normally a large-amplitude signal and has little harmonics content. These features make it easy to design a single-tap delay filter.

The instantaneous  $v$  samples are used to produce the following information:

- Accumulated squared voltage values
- Accumulated active energy values
- Accumulated reaction energy values (derived by adding a  $90^\circ$  phase shift)

These accumulated values are processed by the foreground process (see [Section 3.3](#)).

### 3.2.3 Current

The dc content also must be removed from the current samples. The offset voltage supplied to the CT is also sampled. Subtracting this offset sample from the current sample creates a pseudodifferential effect, which improves crosstalk and noise disturbances and provides a first-stage dc removal effect. An additional dc removal filter completes this process.

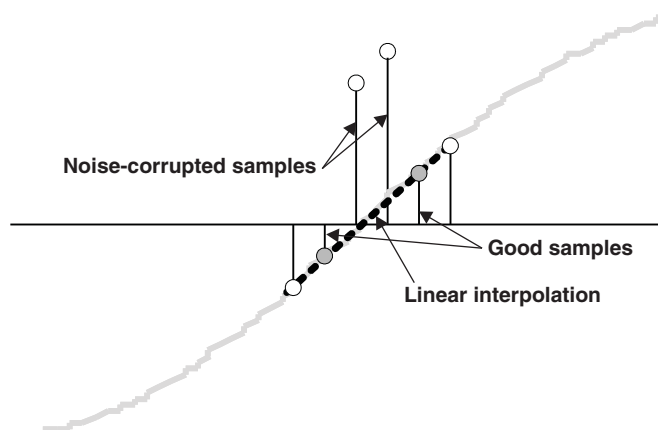
The instantaneous  $i$  samples are used to produce the accumulated squared values and the two energy values.

### 3.2.4 Frequency Measurement and Cycle Tracking

The main task of the background process is to measure and process the instantaneous current and voltage signals for each phase. These are then accumulated in 48-bit registers.

A cycle tracking counter and sample counter keep track of how many samples have been accumulated. When approximately one second's worth of samples have been accumulated in the 48-bit registers by the background process, the foreground process is notified that it can produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process, because this gives very stable results.

For frequency measurements, a straight line interpolation between the zero crossing voltage samples is used. [Figure 9](#) depicts the samples near the zero-crossing point.



**Figure 9. Zero-Crossing Samples**

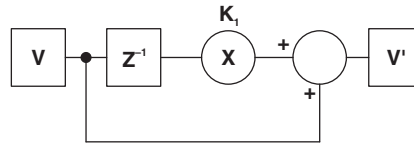
Because noise spikes can cause errors, a rate-of-change check is used to filter out the possible erroneous signals and to ensure that the two points that are being used for the interpolation are genuine zero-crossing points. For example, when two successive samples are negative, a noise spike can make one of them positive and, therefore, make the negative and positive pair look as if there is a zero crossing).

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out cycle-to-cycle variations. The result is a stable and accurate frequency measurement result that is tolerant of noise.

### 3.2.5 Phase Compensation

The CT introduces an additional phase change between the current and voltage signal, which must be compensated. This compensation is performed by delaying the voltage samples by the same time that the CT delays the current samples. The phase compensation that is needed is measured during calibration.

A simple sample-by-sample delay provides a delay in single-sample steps. The fractional delay is implemented through a single-tap FIR filter to provide a delay from minus to plus 0.5 samples (see Figure 10).



**Figure 10. Single-Tap FIR Filter**

The FIR filter does not have unity gain. Its gain would vary depending on the amount of fractional delay. The foreground process compensates for the nonunity gain when the whole block of power samples is calculated.

### 3.2.6 LED Pulse Generation

In electricity meters, the energy consumed is normally measured in fraction of kilowatt-hour pulses. The meter must accurately generate and record the number of these pulses.

It is a general requirement that these pulses are generated with relatively little jitter. Although the time jitters are not an indication of bad accuracy; as long as the jitters average out, it gives a negative impression on the overall accuracy of the meter.

This application uses the average power to generate the energy pulses. The average power (calculated by the foreground process) is accumulated every Timer\_A0 interrupt. This is equivalent to converting the measurement to energy and, once the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept, and the new energy amount is added in the next interrupt cycle.

Because the average power tends to be a stable value, this method of generating the pulses produces energy pulses that are very steady and free of jitter. The threshold determines the energy "tick" specified by the power company and is a constant. For example, this can be in kilowatt-hour. The Timer\_A hardware circuit generates the pulse, which makes it accurate within 1/3276.8 second.

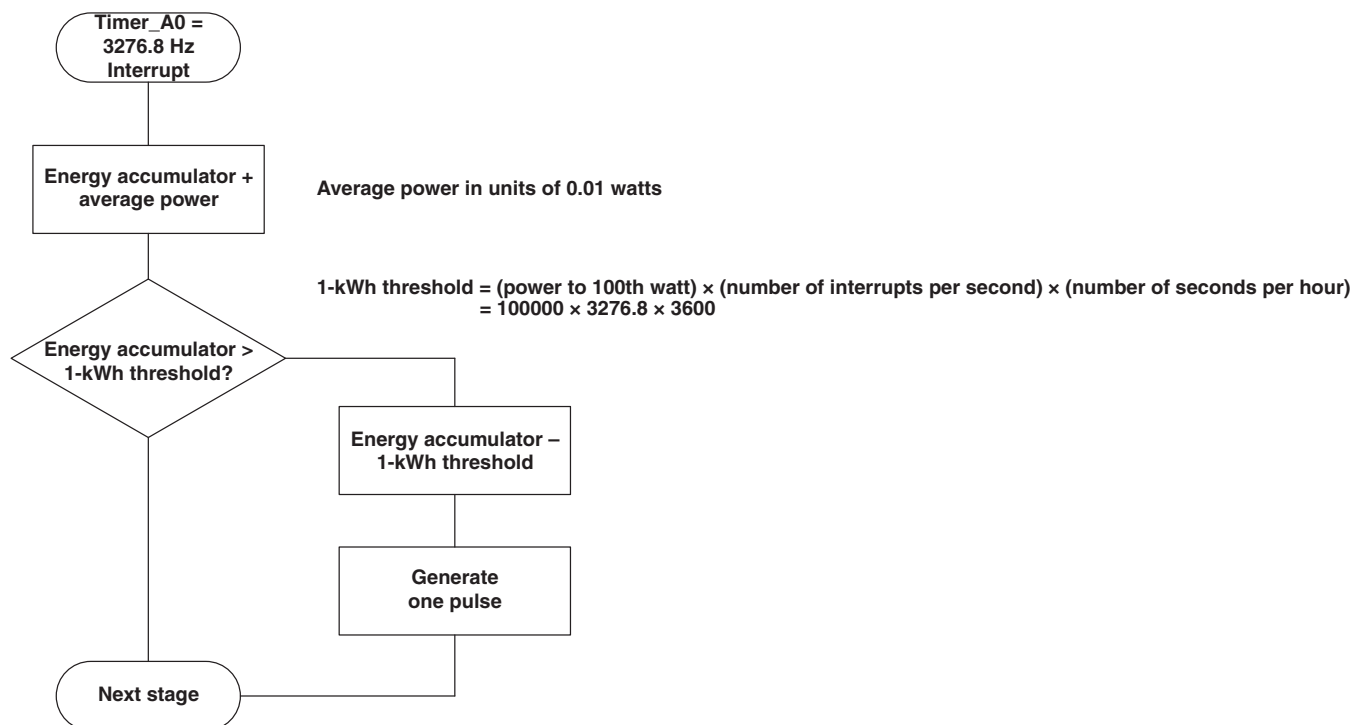


Figure 11. LED Pulse Generation

### 3.3 Foreground Process

The background process notifies the foreground process through a status flag every time a frame of data is available for processing. The data frame consists of the accumulation of 50 or 60 cycles worth of data samples and is synchronized to the incoming voltage signal. At a sampling rate of roughly 65 samples per cycle, this results in approximately 3276 samples.

The data samples consist of processed current, voltage, active energy, and reactive energy information. These values are accumulated in separate 48-bit registers. In addition, a sample counter keeps track of how many samples have been accumulated over the frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The foreground process (see [Figure 12](#)) uses these stored values to calculate the root mean values and the mean values.

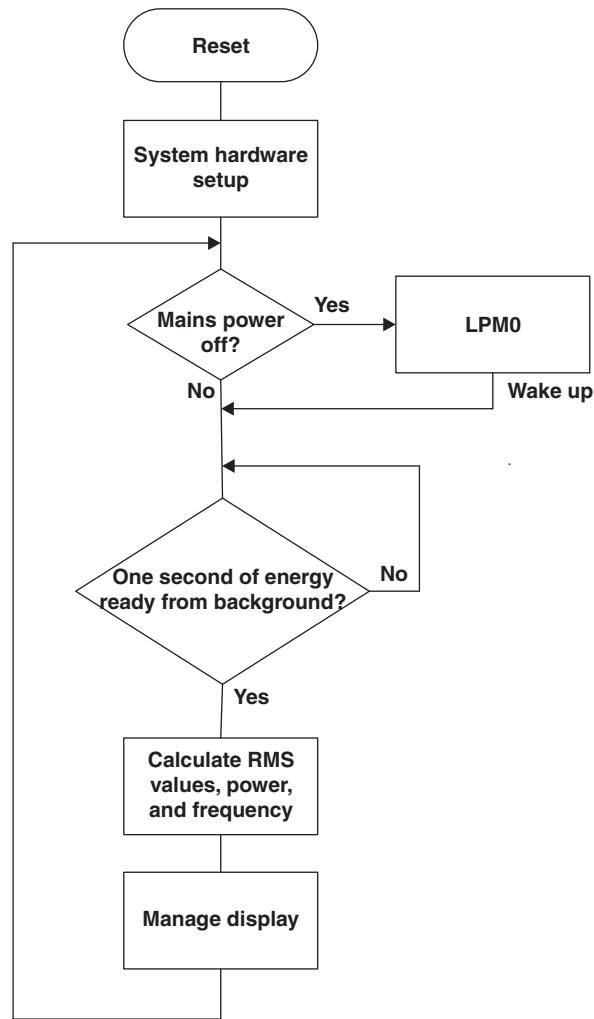


Figure 12. Foreground Process

### 3.3.1 Voltage and Current

The squared voltage and current samples accumulated during one frame are passed to the foreground process, which uses those samples to calculate the root mean square values (see Figure 13).

$$V_{ph,rms} = \text{Scaling factor} \times \sqrt{\frac{\sum_{n=1}^{\text{samplecount}} v_{ph}^2[n]}{\text{samplecount}}}$$

$$I_{ph,rms} = \text{Scaling factor} \times \sqrt{\frac{\sum_{n=1}^{\text{samplecount}} i_{ph}^2[n]}{\text{samplecount}}}$$

ph = 1, 2, or 3

Figure 13. Voltage and Current Calculation

### 3.3.2 Power and Energy

The active and reactive energy samples (phase corrected) accumulated during one frame are passed to the foreground process, which uses those samples to calculate the power values (see [Figure 14](#)). The consumed energy is calculated based on the active power values using a method similar to the method that the background process uses to generate the energy pulses, except that:

$$\text{energy consumed} = P_{\text{active}} \times \text{number of samples in the frame}$$

This value is then stored in EEPROM.

For reactive energy, the 90° phase-shift approach is used for two reasons.

- The reactive power can be measured accurately down to very small currents.
- This approach conforms to internationally specified measurement methods.

Because the frequency of the mains varies, it is important first to measure the mains frequency accurately and then to phase shift the voltage samples accordingly (see [Section 3.2.4](#)). The phase shift consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a fractional delay filter (see [Section 3.2.5](#)).

$$P_{\text{active,total}} = \sum_{\text{ph}=1}^3 \left( \text{Scaling factor} \times \frac{\sum_{n=1}^{\text{samplecount}} v_{\text{ph}}[n] \times i_{\text{ph}}[n]}{\text{samplecount}} \right)$$

$$P_{\text{reactive,total}} = \sum_{\text{ph}=1}^3 \left( \text{Scaling factor} \times \frac{\sum_{n=1}^{\text{samplecount}} v_{\text{ph}}(90)[n] \times i_{\text{ph}}[n]}{\text{samplecount}} \right)$$

ph = 1, 2, or 3

**Figure 14. Power and Energy Calculation**

### 3.3.3 Display

An additional display routine is called from the foreground process. This scrolls through in 2-second delays, displaying a number of values, such as  $V_{\text{rms}}$ ,  $I_{\text{rms}}$ , power, frequency, temperature, real-time clock, etc.

## 4 References

1. IEC 62053 Electricity Meter Specification
2. GB/T 17883-1999 Electricity Meter Specification
3. *Current-Transformer Phase-Shift Compensation and Calibration* ([SLAA122](#))
4. *MSP430 Family Mixed-Signal Microcontroller Application Reports* ([SLAA024](#))

## Appendix A Design Testing

This appendix describes laboratory testing of the meter design that is described in this application report.

### A.1 Test Results Summary

<b>Test Type</b>	3-phase, 4-wire, basic error, and parametric influence tests
<b>Test Setup</b>	Electrical energy meter test bench using the 3-phase, 4-wire electrical energy meter
<b>Test Conditions</b>	Meter class: 0.5S Meter constant: 1600 ipm/kWh Nominal voltage: $3 \times 220$ V Nominal frequency: 50 Hz Current range: $3 \times 5$ (30) A

**Table A-1. Test Results Summary**

Test Number	Type of Test	Test Result
1	Basic error test	Passed
2	Voltage influence	Passed
	Error over the range 0.9Un to 1.1Un	Passed
	Error variation over the range 0.9Un to 1.1Un	Passed
3	Frequency influence	Passed
4	Phase reversal	Passed
5	Harmonic influence	Passed

## A.2 Individual Test Records

The following sections describe the individual tests that are summarized in [Section A.1](#).

### A.2.1 Basic Error Test

<b>Specification</b>	GB/T 17883-1999 section 4.6.1
<b>Test Method</b>	Electrical energy meter test bench
<b>Test Conditions</b>	Voltage $U = U_n$

**Table A-2. Basic Error Test Results, Balanced Load**

Load Current	Power Factor	Error Limit (%)	Test Result
0.01 In	1	1	0.2363
0.02 In	0.5L	1	0.1393
0.02 In	0.8C	1	0.261
0.05 In	1	0.5	0.0627
0.05 In	0.5L	1	0.0117
0.1 In	1	1	0.0143
0.1 In	0.5L	0.6	-0.1077
0.1 In	0.8C	0.6	0.062
0.2 In	1	0.5	0.0233
0.5 In	1	0.5	0.1063
0.5 In	0.5L	0.6	0.0997
0.5 In	0.8C	0.6	0.1127
In	1	0.5	0.0693
In	0.5L	0.6	-0.098
In	0.8C	0.6	0.121
Imax	1	0.5	-0.1077
Imax	0.5L	0.6	-0.2327
Imax	0.8C	0.6	0.204

**Table A-3. Basic Error Test Results, Balanced Load, Per Phase**

Load Current	Power Factor	Error Limit (%)	Test Result		
			Phase A	Phase B	Phase C
0.05 In	1	0.6	0.2803	0.2017	0.2227
0.1 In	1	0.6	0.1553	0.0823	0.124
	0.5L	1	0.374	-0.1603	-0.0157
0.5 In	1	0.6	0.2033	0.2673	0.239
	0.5L	1	0.0747	-0.117	0.5687
In	1	0.6	0.157	0.228	0.1817
	0.5L	1	0.0177	-0.131	0.153
Imax	1	0.6	0.16	0.2273	0.2273
	0.5L	1	-0.0347	-0.1613	-0.2673

**Conclusion: Passed**

**A.2.2 Voltage Influence Test**

<b>Specification</b>	GB/T 17883-1999 section 4.6.2
<b>Test Method</b>	Electrical energy meter test bench
<b>Test Criteria</b>	The meters should function normally for any voltage in the range 0.5Un to 1.5Un. Between 0.9Un and 1.1Un, the error should be within specification. Between 0.9Un and 1.1Un, the error variation should be within specification.
<b>Test Conditions</b>	Over the range 0.9Un to 1.1Un

**Table A-4. Voltage Influence Test Error**

Power Factor	Error Limit (%)	Current	Voltage	Error (%)
1	0.5	I <sub>max</sub>	0.9Un	0.0177
			Un	0.1783
			1.1Un	0.2943
0.5L	0.5	I <sub>max</sub>	0.9Un	-0.2437
			Un	-0.1243
			1.1Un	0.027
1	0.5	I <sub>n</sub>	0.9Un	-0.011
			Un	0.1517
			1.1Un	0.2717
0.5L	0.5	I <sub>n</sub>	0.9Un	-0.1313
			Un	0.0193
			1.1Un	0.1173
0.5L	0.5	0.1I <sub>n</sub>	0.9Un	-0.2117
			Un	-0.0923
			1.1Un	0.0037
1	0.5	0.05I <sub>n</sub>	0.9Un	0.042
			Un	0.1773
			1.1Un	0.2797

**Table A-5. Voltage Influence Test Error Variation**

Power Factor	Error Limit (%)	Current	Voltage	Error (%)
1	0.2	I <sub>max</sub>	0.9Un	0.16
			1.1Un	0.12
0.5L	0.4	I <sub>max</sub>	0.9Un	0.12
			1.1Un	0.15
1	0.2	I <sub>n</sub>	0.9Un	0.16
			1.1Un	0.12
0.5L	0.4	I <sub>n</sub>	0.9Un	0.15
			1.1Un	0.1
0.5L	0.4	0.1I <sub>n</sub>	0.9Un	0.1
			1.1Un	0.1
1	0.2	0.05I <sub>n</sub>	0.9Un	0.14
			1.1Un	0.1

**Conclusion: Passed**

**A.2.3 Mains Frequency Influence Test**

<b>Specification</b>	GB/T17883-1999 section 4.6.2
<b>Test Method</b>	Electrical energy meter test bench
<b>Test Criteria</b>	Error variation (%) $\leq 0.2\%$
<b>Test Conditions</b>	Over the range 47.5 Hz to 52.5 Hz, Voltage $U = U_n$

**Table A-6. Mains Frequency Influence Test Error**

Power Factor		1			0.5L		
		0.05In	In	I <sub>max</sub>	0.1In	In	I <sub>max</sub>
<b>Error (%)</b>							
Frequency	47.5 Hz	0.1567	0.1443	0.1693	-0.0737	0.0167	-0.0757
	50.0 Hz	0.1617	0.146	0.1693	-0.0973	0.0107	-0.049
	52.5 Hz	0.1603	0.1473	0.1693	-0.0897	-0.0217	-0.0757

**Table A-7. Mains Frequency Influence Test Error Variation**

Power Factor		1			0.5L		
		0.05In	In	I <sub>max</sub>	0.1In	In	I <sub>max</sub>
<b>Error (%)</b>							
Frequency	47.5 Hz	0.01	0.00	0.00	0.02	0.01	0.03
	52.5 Hz	0.00	0.00	0.00	0.01	0.01	0.03

**Conclusion: Passed**
**A.2.4 Phase Reversal Test**

<b>Specification</b>	GB/T 17883-1999 section 4.6.2
<b>Test Method</b>	Electrical energy meter test bench
<b>Test Criteria</b>	Error variation $\leq 0.1\%$
<b>Test Conditions</b>	Voltage $U = U_n$ , Current $I = 0.1I_n$ , Power Factor $\cos\phi = 1$

**Table A-8. Phase Reversal Test Results**

	<b>Error (%)</b>
<b>Normal Direction</b>	+0.0540
<b>Reverse Direction</b>	+0.0383
<b>Error Change (%)</b>	0.02

**Conclusion: Passed**

**A.2.5 Harmonic Influence Test**

<b>Specification</b>	GB/T 17883-1999 section 4.6.2
<b>Test Method</b>	Electrical energy meter test bench
<b>Test Criteria</b>	Error variation $\leq 0.1\%$
<b>Test Conditions</b>	Voltage $U = U_n$ , Power Factor $\cos\phi = 1$

**Table A-9. Harmonic Influence Test Results**

Error Limit (%)	Current	Fundamental to Harmonic Phase	Error Change (%)
0.1	0.05I <sub>n</sub>	0°	0.01
		180°	0.01
	I <sub>n</sub>	0°	0.01
		180°	0.02
	I <sub>max</sub>	0°	0.01
		180°	0.01

**Conclusion: Passed**

## IMPORTANT NOTICE

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