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POWERING A 35W DC METAL HALIDE HIGH INTENSITY DISCHARGE (HID) LAMP USING THE UCC3305 HID LAMP CONTROLLER

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POWERING A 35W DC METAL HALIDE HIGH INTENSITY DISCHARGE (HID) LAMP USING THE UCC3305 HID LAMP CONTROLLER

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ABSTRACT

High Intensity Discharge (HID) metal halide lamps are being used in more and more applications where lamp color, long life and efficiency are important. From automotive and industrial lighting to theatrical and stage lighting, HID promises to be the light of the future. HID lamps offer many advantages over many other types of discharge lamps because of their luminous efficiency (their ability to convert electrical power to visible light) and the color of the light output is closer to an ideal source (the sun) then other types of discharge lamps i.e.; low pressure sodium, high pressure sodium etc.

The purpose of this application note is to demonstrate the use of the UCC3305 HID lamp controller IC. Information is presented on a design example to help the user better understand all of the controllers many features.

INTRODUCTION

The following section specifies typical design requirements necessary of an HID ballast which would be powering a DC headlamp in an automotive application. The headlamp used in this application is a 35W DC metal halide lamp manufactured by OSRAM/SYLVANIA.

Input Voltage Requirements - 9 to 16VDC

Startup Requirements - Must run/startup down to 6VDC

Protection/Fault Monitor- Protection against input overvoltage, output open circuit and output short circuit.

Power Regulation - Regulate power to the lamp within +10% over a lamp voltage variation of 60 to 100VDC.

Lamp Ignition Voltage - Provide an open circuit voltage of greater then 500VDC at start-up in order to ignite the lamp.

Efficiency - greater than 85%.

Cold Start - The light output on initial start-up must be within a window as specified by SAE J2009.

Hot Restrike - The ballast must be able to properly light the lamp when hot without a cool down period.

The load presented to the ballast by the lamp is non-linear. Before ignition occurs, the lamp draws very little current from the ballast. The ballast sees essentially an open circuit on its output at start-up. The open circuit voltage feeds an ignitor circuit (internal to the lamp) which steps-up the voltage in order to provide the approximately 20kV ignition voltage necessary for the lamp. Upon ignition, metals and gases inside the lamp are ionized causing the lamp voltage to collapse. During ionization, the lamp will require significant current from the ballast to properly establish and maintain the arc discharge. During this time, the current into the lamp must also be controlled to protect the lamp electrodes [1].

The initial start-up power into the lamp is higher then its steady state value. This is necessary in order to get the light output up to 75% of its steady-state value within 2 seconds, which is a requirement for an automotive application as specified under SAE J2009. The lamp voltage right after the glow to arc transition varies from lamp to lamp but is usually between 20 and 40VDC. As the lamp warms up and the internal pressure inside the arc tube increases, the voltage begins to rise and will gradually reach a steady-state value of between 60 and 110VDC after 150 seconds. This depends on the age of the lamp. A typical steady-state voltage of this type of lamp is between 75 and 90VDC.
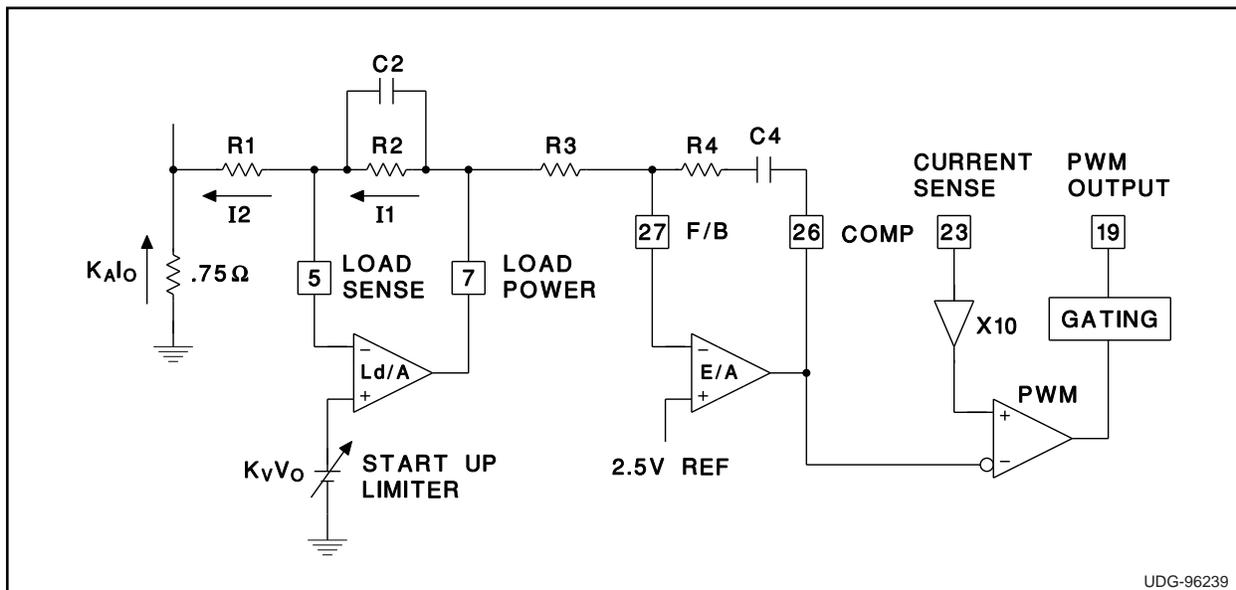
Figure 1. Power Regulation Loop

Optimal converter topology

The optimal converter topology for this application would meet the following requirements;

1) Output voltage that is capable of being higher then input voltage.
2) Low input current ripple for reduced input filter requirements
3) High efficiency
4) Minimal number of magnetic components
5) Minimal number of power semiconductors

There are a few candidate topologies which meet some of the above requirements. The best choice for this particular application is the SEPIC converter which meets all of the above requirements for a 35W lamp. The schematic of this circuit is shown in Figure 2 [2].

The UCC3305 HID controller

The features of the UCC3305 HID controller are outlined below:

- OV input protection
- Output fault protection/timing
- Power regulation vs. lamp voltage
- Lamp start-up/cool down simulation
- Current-mode control
- Fixed frequency operation
- DC or AC lamp drive capability
- High current drive capability
- On board charge pump to provide gate drive down to 6VDC
- Adjustable start-up to steady-state current ratio

Below is a summation of the different functional blocks of the UCC3305 and their major electrical characteristics;

VCC/OV Protection/VREF/VBOOST Block

VCC Maximum Voltage - 8 Volts
Must bypass with 0.1μF to 1.0μF Ceramic Monolithic Capacitor as close to the IC as possible

OV Threshold - Internal Comparator with reference voltage tied to internal 5V. OV threshold adjustable with external resistor divider

VREF:
5.0V Trimmed Bandgap Reference
Must bypass with 0.1μF Low ESR Capacitor as close to the IC as possible

VBOOST Max Voltage - 12 Volts
Supplies drive for output drive stage
Must bypass with 0.1μF to 1μF Ceramic Monolithic Capacitor as close to IC as possible

Output Drive Stage:

PWMOUT:
1.0A Peak current drive capability

Q and Q not outputs
Outputs to drive external bridge via external MOSFET drivers Output frequency is fs/512
At lamp start, outputs are disabled via RC from NOT-ON and DIV. PAUSE

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Oscillator:

OSC:
Sawtooth Oscillator with Programmable
Frequency D_{MAX} from 0% to 100% possible
With R_{SET} = 150k, Fs ~ 22xe-6/C_{OSC}
Maximum operating frequency is 300kHz

Load Power and Main Error Amplifiers:

LOADSENSE, LPOWER, COMP AND FB

The LOADSENSE amplifier, the main error amplifier and its external associated resistors and capacitors will determine where the peak of the power curve occurs as well as the shape of the frequency response of the ballast. Below is an analysis of this operational block based on the 35W DC lamp in an attempt to show how the power curve of the ballast is determined for this particular application.

From the simplified schematic of this loop shown in Figure 2 below, the power curve equation is determined as follows;

Power curve equation

From the simplified schematic of the power regulation loop, shown in Figure1, the currents I_1 and I_2 can be found as follows;

$$I_1 = \frac{V_{REF} - K_V \bullet V_O}{R2}$$

$$I_2 = \frac{K_V \bullet V_O + K_I \bullet I_O}{R1}$$

where K_V and K_I are the proportionality constants for voltage and current respectively; since

$$I_1 = I_2$$

$$\frac{V_{REF} - K_V \bullet V_O}{R2} = \frac{K_V \bullet V_O + K_I \bullet I_O}{R1}$$

rearranging the above equation and solving for I_O,

$$K_I \bullet I_O = (V_{REF} - K_V \bullet V_O) \bullet \frac{R1}{R2} - K_V \bullet V_O$$

$$I_O = \left[(V_{REF} - K_V \bullet V_O) \bullet \frac{R1}{R2} - KV \bullet V_O\right] \bullet \frac{1}{K_I}$$

since

$$P_O = V_O \bullet I_O$$

substituting the expression found for I_O into the power equation,
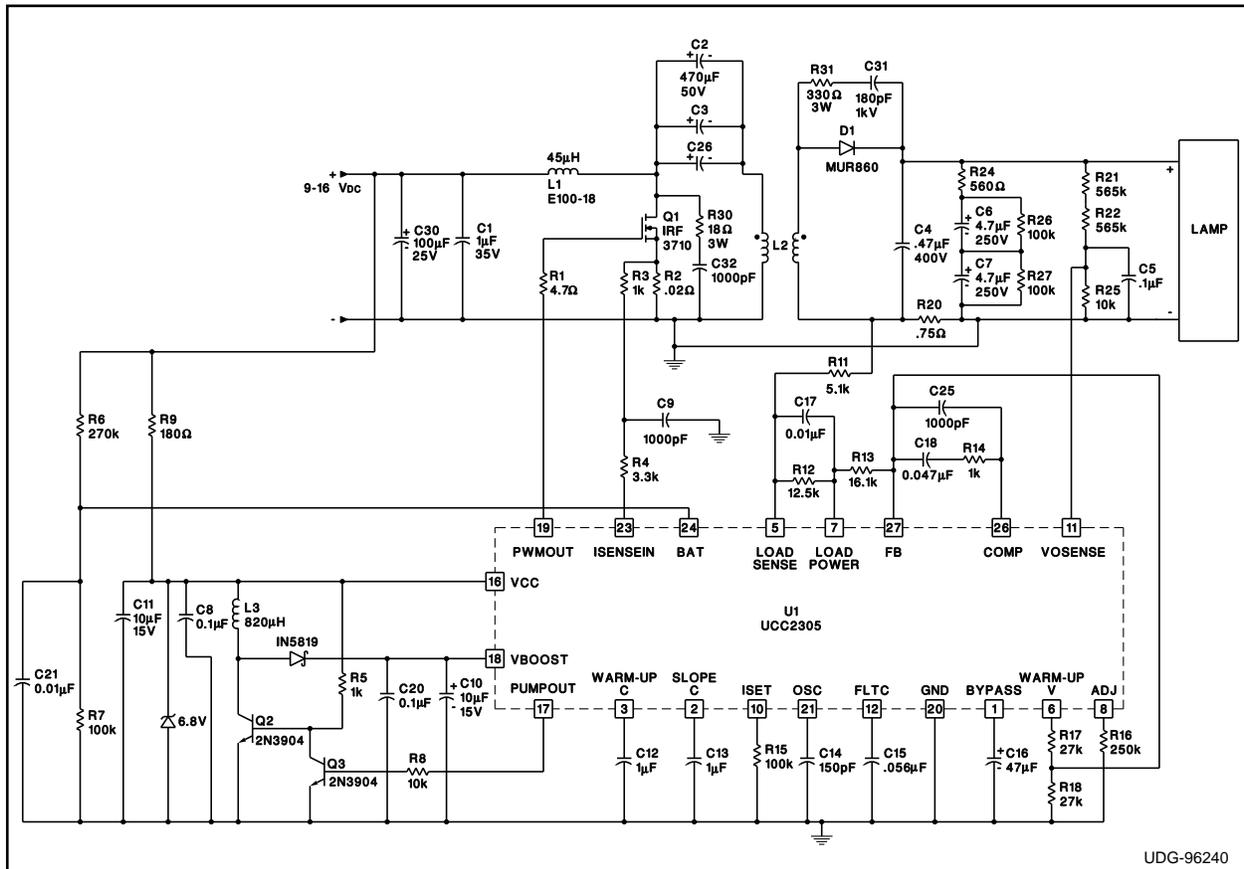
Figure 2. 35W DC HID Ballast Schematic

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The expression for P_{O1} is valid for lamp voltages from 60 to 105V. The expression for P_{O2} is valid for lamp voltages above 105V (This is due to the limiter block inside the UCC3305). Above approximately 105V, the lamp will be driven in a constant current mode which results in the straight line for power vs. lamp voltage as shown. The output power can be regulated with a variation of less than ±10% from a nominal of 34.5W with a lamp voltage variation from 60 to 110V.

As the lamp ages, the voltage will normally increase due to the lamp electrode material erosion over time. Therefore it is beneficial to limit the current available to the lamp above a certain voltage.
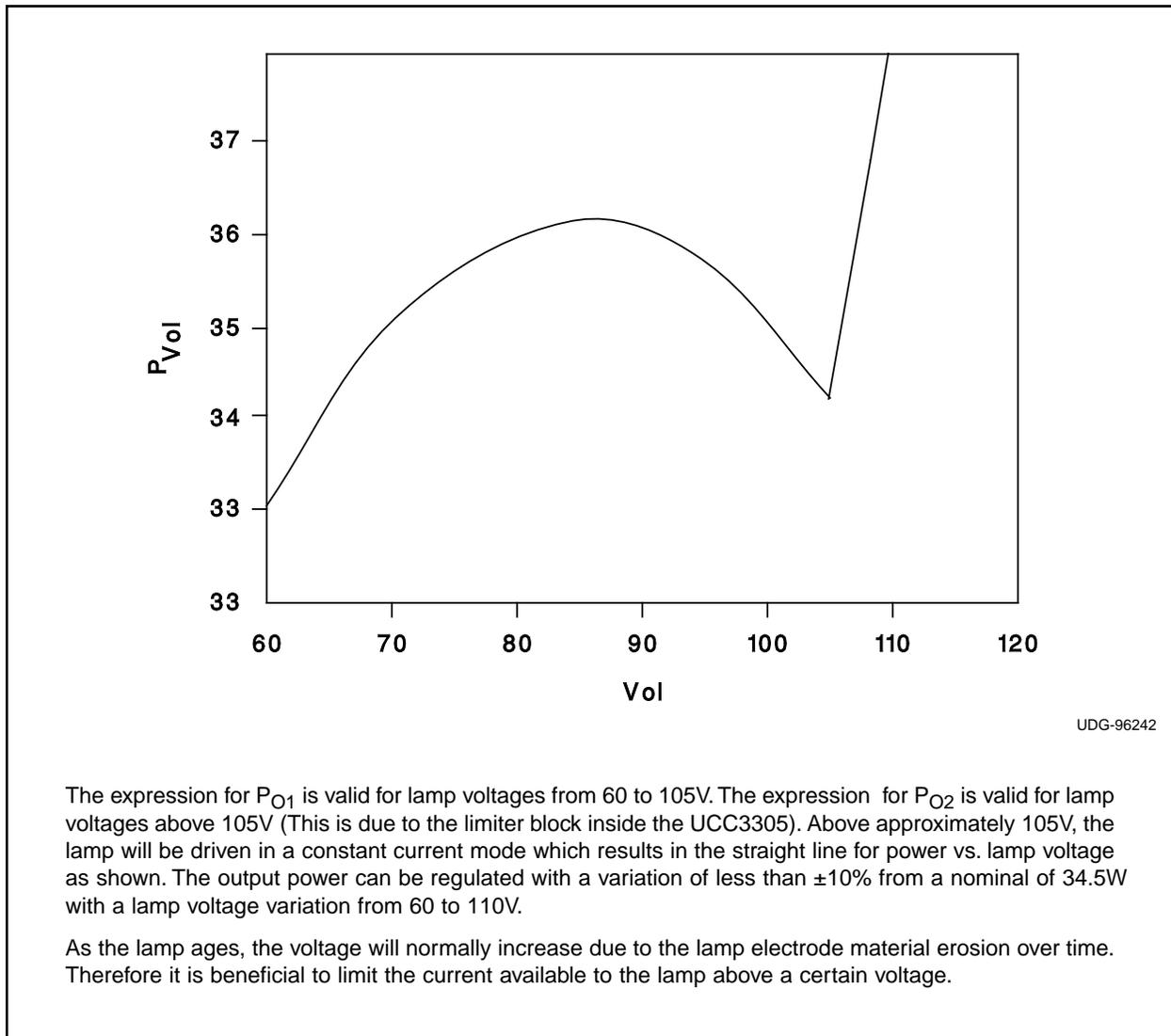
Figure 3. Calculated Power Curve vs. Lamp Voltage of UCC3305 Controlled 35W Ballast Powering DC Metal Halide Osram/Sylvania Lamp

$$P_O = \frac{V_O}{K_I} \bullet \left[V_{REF} \bullet \frac{R1}{R2} - K_V \bullet V_O \bullet \left(1 + \frac{R1}{R2} \right) \right]$$

where

$$R_{EQ} = \frac{R_A \bullet R_B}{R_A + R_B}$$

from block diagram of UCC3305, where 1/120 is the voltage divider attenuation ratio. R_{EQ} is the parallel combination of the 100k and the 5.35k internal resistors.

$$K_V \approx \frac{1}{120} \bullet \frac{R_{EQ}}{R_{EQ} + 7.85k}$$

$$R_A = 100k$$

$$R_B = 5.35k$$

$$R_{EQ} = 5.078 \bullet K$$

$$K_V \approx 0.0032$$

$$K_I = 0.75$$

K_I is equal to the current sense resistor value

Substituting the values found for the constants K_V and K_I and the actual resistor values used in the circuit into the power equation, the power curve can be plotted for a range of lamp voltages as shown in the figure below.

$$K_V \approx 0.0032$$

$$R_1 = 4.7k$$

$K_I = 0.75$

$R2 = 16k$

$V_{O1} = 60, 65..110$

$V_{REF} = 2.5$

$V_{O2} = 110, 115..120$

$$P_{Vo(1)} = \frac{V_{O1}}{K_I} \bullet \left[\left(\frac{R1}{R2}\right) \bullet V_{REF} - K_V \bullet V_O1 \right.$$
$$\left. \bullet \left(\frac{R1}{R2} + 1\right) \right],$$

$$P_{Vo(2)} = \frac{V_{O2}}{K_I} \bullet \left[\left(\frac{R1}{R2}\right) \bullet V_{REF} - 0.322 \right.$$
$$\left. \bullet \left(\frac{R1}{R2} + 1\right) \right]$$

Current sense comparators/amplifiers

The INPUT ISENSE comparitor/amplifier inside the UCC3305 provides cycle by cycle current control as in a typical peak current-mode controller. An added feature allows the user to program the start-up to steady-state current ratio of this current. This allows the ballast to provide increased power to the lamp at start-up in order to get the lamp light output up to its steady-state level as quick as possible. The simplified schematic of this section is shown in Figure 4 below.

By the addition of an external resistor from the ADJ. pin to ground, this ratio can be programmed. At the instant of start-up, the output of the limiter is at zero volts since the WARMUPC capacitor has not charged. Because of this, the inverting input to amplifier A1 is at ground with $20\mu A \bullet R_{ADJ}$ volts on its non-inverting input. As an example, if $R_{ADJ} = 150k$, then the voltage at the non-inverting input is 3V.

$$V_{O(-)} = -\left(\frac{V_{(-)}}{83k}\right) \bullet 10k$$

$$V_{O(-)} = -\left(\frac{V_{(-)}}{83k}\right) \bullet 10k + V_{(+)}$$

where

$V_{O(+)}$ = the contribution of the non-inverting input to V_O of A1

$V_{O(-)}$ = the contribution of the inverting input to V_O of A1

$V_{(+)}$ = the voltage at the non-inverting input of A1

$$V_O = V_{(+)} \bullet \left(\frac{10k}{83k} + 1\right) - V_{(-)} \bullet \left(\frac{10k}{83k}\right)$$

on start-up,

$$V_{(-)} = 0$$

so;

$$V_O = 3.36 \text{ Volts}$$

Figure 4. Current Sense / Limit Block

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The current sense threshold is then;

$$V_S = \frac{3.36}{10}$$

$$V_S = 0.336 \text{ Volts}$$

This translates to a peak switch current at start-up of;

$$I_P = \frac{3.36}{0.02}$$

$$I_P = 16.8 \text{ Amps}$$

This current threshold will gradually decrease as the WARMUPC capacitor charges up to 10V.

The limiter limits the inverting input of A1 at steady-state to 5V. The current limit at this point is then;

$$V_O = 3.36 - 0.6$$

$$V_O = 2.76 \text{ Volts}$$

$$I_P = \frac{0.276}{0.02}$$

$$I_P = 13.8 \text{ Amps}$$

The switch current in the SEPIC converter is a combination of the input inductor current plus the reflected load current. At steady-state, 9 V_{IN}, the peak-to-peak current thru the output rectifier is approximately 1A. This reflects back to the primary as 6A into the switch plus 3.1 Amps from the inductor. The total current thru Q1 is then 9.1 Amps.

Output current limit on start-up

From Figure 2 the start-up current limit into the lamp can be determined. On start-up, the WARMUPV pin, which is a buffered version of WARMUPC, is at ground. Therefore, the two 27k resistors are in parallel resulting in an equivalent resistance of 13.5k. The current that flows from FB to ground is then;

$$I = \frac{2.5}{13.5k}$$

$$I_1 = 185\mu A$$

The voltage at the output of the load sense amplifier is then;

$$V_{LS} = 185\mu A \bullet 16k + 2.5V$$

$$V_{LS} = 5.46V$$

The current which flows thru the feedback resistor of the load sense amplifier is;

$$I_{LS} = \frac{5.46 - 0.30}{12k}$$

$$I_{LS} = 430\mu A$$

Assuming that the current which flows thru the feedback resistor also flows thru the inverting input resistor, the voltage across the output current sense resistor is;

$$V_{CS} = 0.30 - (430\mu A \bullet 5.1k)$$

$$V_{CS} = 1.89V$$

(the negative sign of the voltage is ignored since this is defined as positive current)

$$I_L = \frac{1.89}{0.83}$$

$$I_L = 2.3 \text{ Amps}$$

This defines the maximum startup current which flows into the lamp at ignition. The current into the lamp will decay exponentially due to the voltage charging characteristic of the WARMUPC and SLOPEC capacitors. The current will decay to a steady-state value of approximately 450mA after a period of time given by the time constant of the internal 50 Meg resistor and the capacitor placed from the SLOPEC pin to ground. In this example, the time to steady-state is 150 seconds from:

$$t = 50 \exp(6) \bullet C_{SLOPEC}$$

The capacitors used for the SLOPEC and WARMUPC functions must have low leakage characteristics since they are charged from nanoamp current sources internal to the IC. Any significant amount of leakage current caused by these components will have an effect on the output power regulation characteristic of the ballast.

Slope compensation resistor

Slope compensation in the UCC3305 is provided by the addition of an external resistor in series with the INPUT ISENSE pin. This resistor adds a portion of the oscillator ramp into the current sense signal to provide the necessary slope compensation for duty cycles exceeding 50%. The amount of slope compensation that is needed is dependent on the topology used as well as the inductor values chosen. In the SEPIC converter, both input and output inductors need to be considered when determining how much slope compensation is necessary.

The current sense comparator compares the current sense signal to the output of the error amplifier to determine the duty cycle of the power switch [3]. V_I, the voltage at the current sense resistor can be determined as follows

$$V_I = R_I \bullet \left(\frac{N_S}{N_P} \right) \bullet \left(I_{OAV} + M2 \bullet t \right)$$

$$+ R_I \left(I_{IN} + \frac{M_1}{2} \bullet t_{OFF} \right)$$

where;

N_S = number of turns of secondary winding of L2

N_P = number of turns of primary windings of L2

R_I = current sense resistor

L_{OAV} = secondary average output current

M_2 = down slope of secondary current thru L2

M_1 = down slope of primary current thru L1

I_{IN} = average input current

t_{OFF} = off time of switch

The above equation can be rewritten as follows;

$$V_I = R_I \bullet \left(\frac{N_S}{N_P} \right) \bullet \left(L_{OAV} + M2 \bullet (T - t_{ON}) \right)$$

$$+ R_I \left[I_{IN} + \frac{M_1}{2} \bullet (T - t_{ON}) \right]$$

The first term is the contribution of the output current thru L2 (output inductor) to the current sense resistor. The second term is the contribution of the input current thru L1 (input inductor) to the current sense resistor

This signal is set equal to the voltage at the output of the error amplifier. This results in the following equation after rearranging terms;

$$R_I \left(\frac{N_S}{N_P} \right) \bullet L_{OAV} = V_{EA} + t_{ON}$$

$$\bullet \left(\frac{M_1}{2} \bullet R_I + R_I \frac{N_s}{N_P} \bullet M_2 - m \right)$$

$$- I_{IN} - \frac{M_1}{2} \bullet T \bullet R_I - M_2 \bullet T$$

In order to eliminate the possibility of subharmonic oscillations, the term which multiplies t_{ON} should be set equal to zero eliminating any dependency on duty cycle.

$$\frac{M_1}{2} \bullet R_I + R_I \bullet \frac{N_S}{N_P} \bullet M_2 = M$$

From the simplified schematic of the current sense circuit;

$$S = \frac{2}{10 \bullet \exp(-6)}$$

where S is defined as the slope of the oscillator ramp. Substituting the following values into the equation for R_P will allow us to determine the value of the slope compensation resistor.

$M_2 = 178571$

$N_S = 60$

$M_1 = 178571$

$N_P = 10$

$R_I = 0.01$

$S = 181818$

$$R_P = \frac{\frac{M_1}{2} \bullet R_I + \frac{N_S}{N_P} \bullet R_I \bullet M_2}{2}$$

$R_P = 0.064$

$R4 = 50k$

R3 is the slope compensation resistor and R4 is the internal 50kΩ resistor;

$$R_P = \frac{R3}{R3 + R4}$$

Solving for R3;

$$R3 = 0.064 \bullet \frac{R4}{1 - 0.064}$$

$R3 = 3.419k$

Therefore, the slope compensation resistor chosen must be greater than 3.42k in order for stable converter operation at duty cycles which exceed 50%.

Frequency response of the power regulation loop

The frequency response of the ballast is determined by analysis of the power regulation loop. Since it is really the output current that is being regulated and not the output voltage (any change in output voltage is attenuated by 1/120), the analysis can be simplified by modeling the power stage as a voltage controlled current source with some transconductance gain G_M. This assumption is valid for a loop cross over frequency below resonance of the power stage which is approximately 10kHz.

The transconductance gain, G_M, can be found as follows;

$$G_M = \frac{\Delta I_O}{\Delta V_E}$$

The output current is converted to a voltage by the output current sense resistor. The gain of the power stage is then;

$$G_P = R_{Is} \frac{\Delta I_O}{\Delta V_E}$$

or;

$$G_P = R_{Is} G_M$$

where; R_{Is} = the load sense resistance (0.75Ω)

ΔI_O = load current change (500mA)

ΔV_E = error amp voltage change (5V)

$G_P = -22.5dB$

The loop response must now be tailored for good power regulation (high DC gain) and adequate phase and gain margin at the loop crossover frequency. The gain of the LOAD SENSE amplifier is restricted due to the fact that gain of this stage effects the power curve characteristic as shown in above analysis of the power curve equation.

The LOADSENSE amplifier should be set up as an integrator so that it can filter out switching frequency noise from the control loop. The pole frequency was chosen to be at 1kHz to give good rejection of the switching frequency noise. This results in a capacitor value of 0.01μF. The low frequency gain of this amplifier is set to 7.5dB. The combination of this gain and the power stage gain results in −15dB of low frequency gain with a pole at 1kHz.

The response can now be tailored with the main error amplifier. A zero must be added in the amplifier response at some mid-band frequency so that the DC gain for the overall loop is as high as possible. The high frequency gain of this amplifier must be well below 0dB to ensure adequate gain and phase margin for the open loop gain. Since the 16kΩ, resistor has been determined from the power curve characteristic desired, only the feedback resistor value can be chosen. If this resistor is chosen so that the high frequency gain is to be less then −20dB for good gain margin, or the feedback resistor value of 1kΩ, the capacitor value can then be determined. If a zero frequency of 3.4kHz this assumed, this will give an adequate low frequency gain boost. From this, the value of the capacitor can now be determined to be 0.047μF. The gain and

phase margin with these component values is greater than 20dB and 60 degrees, respectively.

CIRCUIT EXAMPLE:

A 9 to 16VDC input SEPIC converter powering a 35W OSRAM/SYLVANIA DC lamp was built and tested. Data on efficiency, power curve and various oscillagrams of current and voltages in the power/control circuit were taken and are discussed.

Magnetics Design

L1

The input inductor L1, is designed based on the same criteria as a boost inductor. Energy is stored in L1 during the on time of Q1 and transferred during the off time. L1 is designed to operate in the continuous mode with low current ripple. At 9 V_{IN} with 36W of output power and a converter efficiency of 85%, the average input current is 4.7 Amps. If a total peak-to-peak ripple current of 2 Amps is assumed the inductance of L1 can be found. But before we can calculate the inductance required, the minimum and maximum duty cycle must be found so that the maximum and minimum on time of Q1 can be determined. The SEPIC converter has a DC transfer function of;

$$V_O = V_{IN} \bullet n \frac{D}{1 - D};$$

The turns ratio, n can be found from the maximum acceptable voltage stress on Q1. The stress on Q1 is the sum of the capacitor voltage plus the reflected secondary voltage. The capacitor voltage is essentially equal to V_{IN}, so;

$$V_{DS} = V_{IN} + \frac{V_O}{n} ;$$

The worst case output voltage on startup of the lamp is restricted to 500V, since this voltage will be reflected back to the drain of Q1. The turns ratio must be chosen so that the drain voltage never exceeds its maximum rating. A IRF1310 was chosen for this application in part because of its 45mΩ on resistance and V_{DS} = 100V. Calculating the turns ratio at V_{IN} = 16V; n is then found to be 5.8. A turns ratio of 6 is used.

The maximum duty cycle can now be determined from the DC transfer function. To find the maximum duty cycle, the worst case steady-state lamp voltage is used of 110VDC at V_{IN} = 9V. Lamp voltages between 60 and 110V will be within the power regulation range of the ballast. Lamp voltages outside of this range will be operated in the constant current mode. Therefore;

$D_{MAX} = 0.67$

The minimum duty cycle is determined using the minimum steady-state lamp voltage of 60VDC and $V_{IN} = 16V$.

$D_{MIN} = 0.38$

For a switching frequency of 100kHz, $t_{ON\ MAX} = 6.7\mu S$, $t_{ON\ MIN} = 3.8\mu S$

The inductance based on $t_{ON\ MAX}$ at $V_{IN\ MIN}$ can be calculated;

$$L1 = \frac{9 \bullet 6.7\mu S}{2} = 30\mu H.$$

L1 consists of 30T of 19AWG wound on a Micrometals E100 −18 core.

L2

The voltage across the primary winding of L2 when Q1 is on, is for all practical purposes, equal to the input voltage (neglecting voltage ripple on the capacitor) since the series capacitor is switched across the primary. The inductance of the primary winding is chosen based on the peak current desired (it is desired that the inductor current is continuous). The peak current chosen is based on a tradeoff between the voltage stress on Q1 and minimal number of turns to minimize the leakage inductance which in turn means reducing the number of layers of windings. If the peak current thru L2 is restricted to 3.0A, the primary inductance can then calculated as;

$$L2 = \frac{9 \bullet 6.7\mu S}{3} = 20\mu H.$$

The inductance of L1 and L2 could have been set equal to each other. This would have made both inductors "easy" to integrate on the same core. This was not attempted here because of leakage inductance concerns between the primary and secondary windings of L2.

The number of turns for L2 can now be determined based on the particular core geometry chosen. The area product (AP) required is found from;

$$AP = \frac{L \bullet I_P \bullet I_{RMS}}{K_F \bullet J \bullet B_M} = 0.362\ cm^2$$

This is based on the following parameters;

$B = 0.1T$	$L = 20\mu H$	$I_P = 4.7A$
$J = 450A/cm$	$K = 0.4$	$I_{RMS} = 5.2A$

An RM10PA250-3F3 core was used which has an AP of 0.379. The number of primary turns is then;

$$N_P = \frac{L \bullet I_P}{A_E \bullet B} = \frac{20\mu H \bullet 3A}{89 \bullet e\text{-}6 \bullet 0.1T} = 7T$$

(10T is used since this will easily fit in one layer with the desired core and wire gauge chosen)

This ferrite core must be gapped since it stores energy. It is desired that the total gap be placed in the center leg. The gap is calculated from;

$$L_P = \frac{u_O \bullet u_R \bullet N_P^2 \bullet A_E}{L} = 12.56 \bullet 10^{-7}$$

$$\frac{0.89 \bullet 100}{0.020mH} = 0.56mm = 0.02\ in$$

The secondary turns can be calculated from the turns ratio as 60T. The core used for L2 has a center leg gap of 0.022 in. Multifilar wire is used for both the primary and secondary turns to minimize the copper losses. The winding sequence used was; primary-secondary-primary-secondary-primary.

Performance data

Performance data on the ballast is presented in the following curves showing efficiency and the measured power curve. Oscillograms of Q1 voltage and current are also given as well as startup characteristics of the lamp voltage and current. The maximum efficiency achieved was 86.2% at a lamp voltage of 100V. The efficiency decrease after this point is due to an increase in output power which occurs at lamp voltages above 100 to 105V. The lamp cold start voltage and current waveforms are shown with a time base of 50mS and 1Sec. As can be seen, the ballast output voltage is 600V before lamp ignition. Once the lamp ignites, the voltage collapses and the lamp current increases to 2A. Eventually, the lamp voltage begins to increase and the current decreases. They will arrive to their steady-state values of 80 to 90VDC and 450mA respectively after approximately 150 seconds.
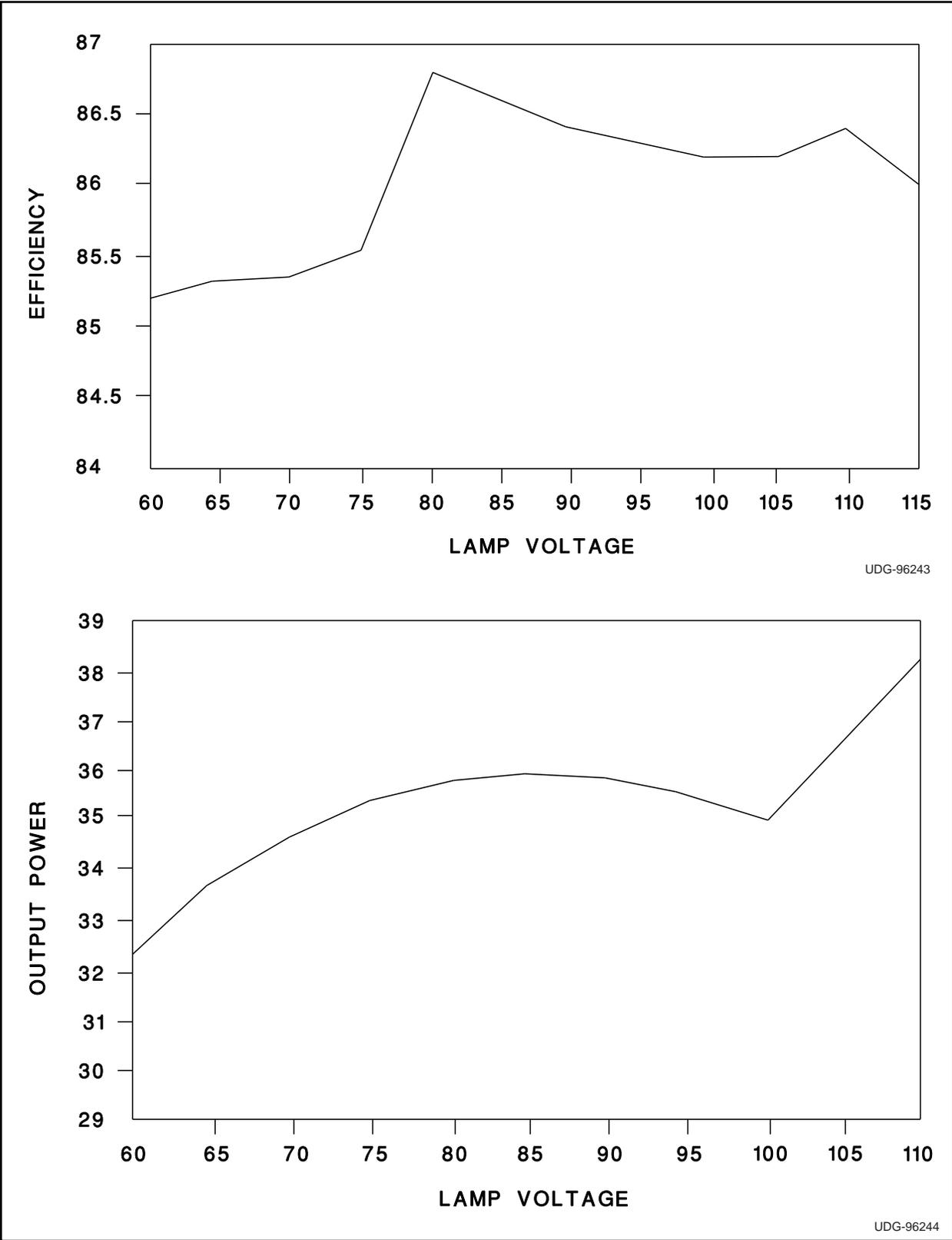
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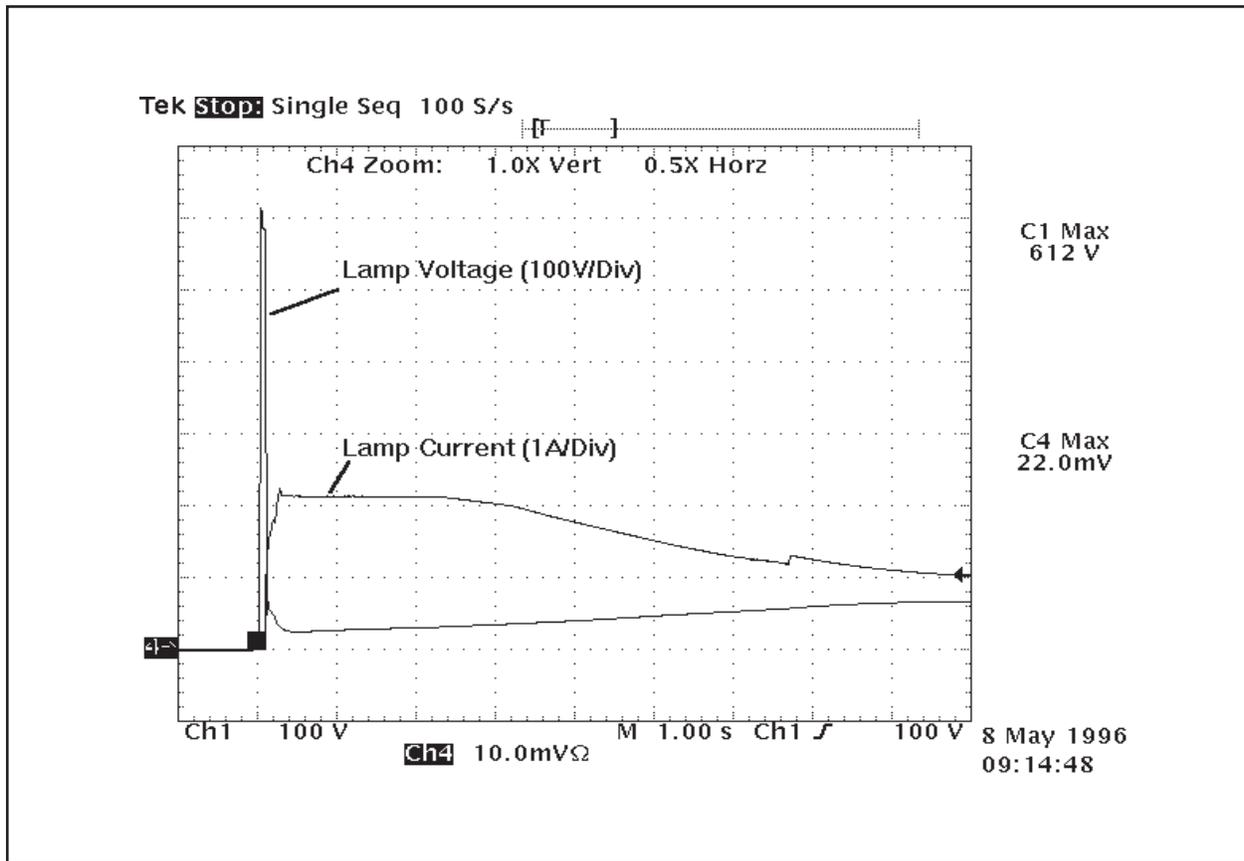**Figure 5.** Efficiency and Power Curve of 35W HID Ballast

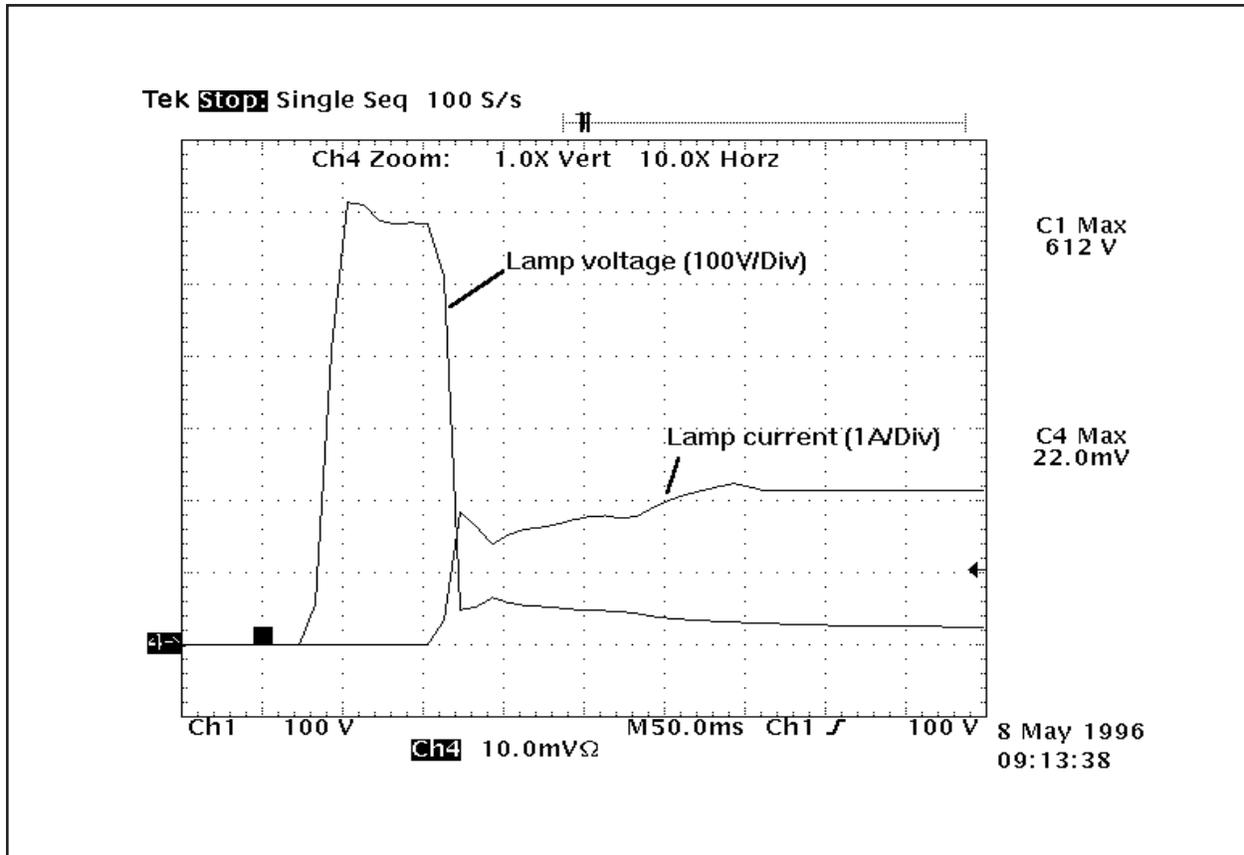**Figure 6.** Ballast Output Voltage and Current

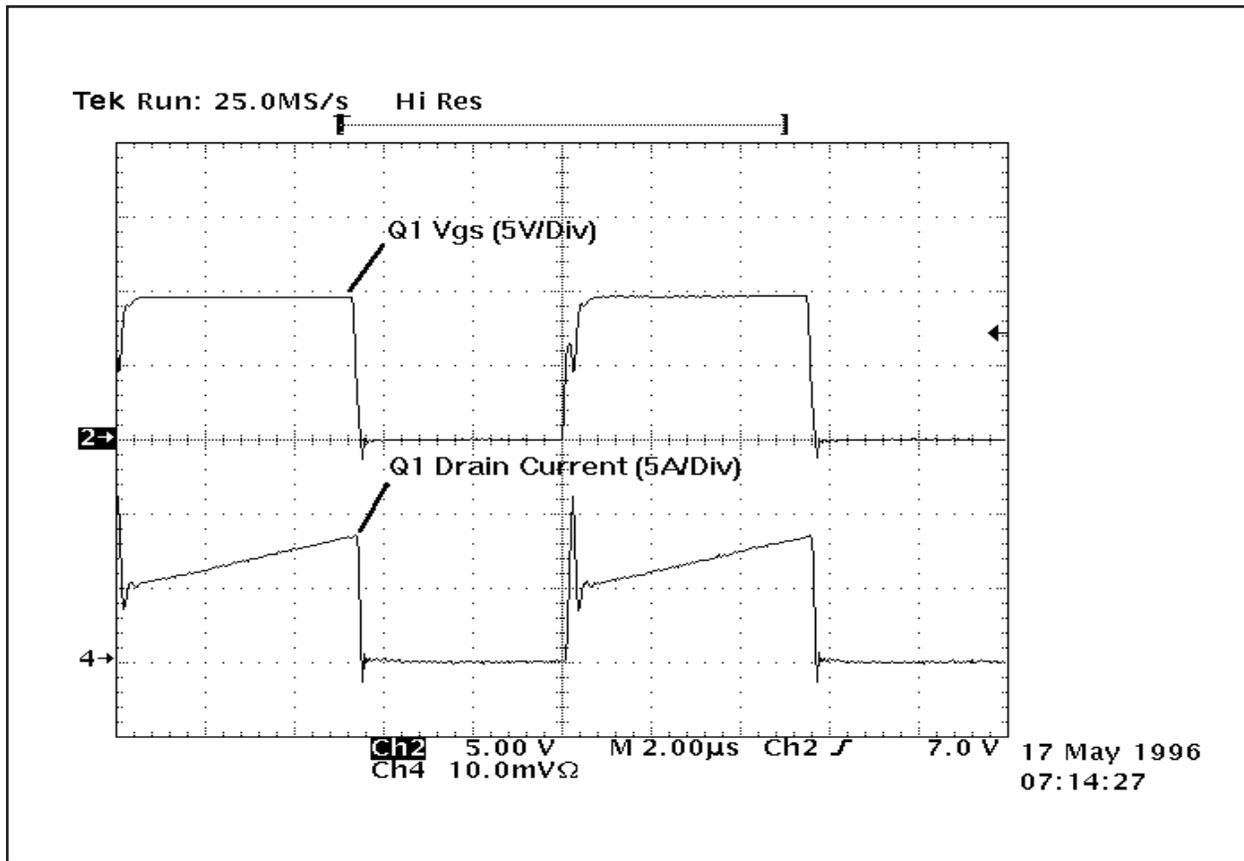**Figure 7.** Ballast Output Voltage and Current

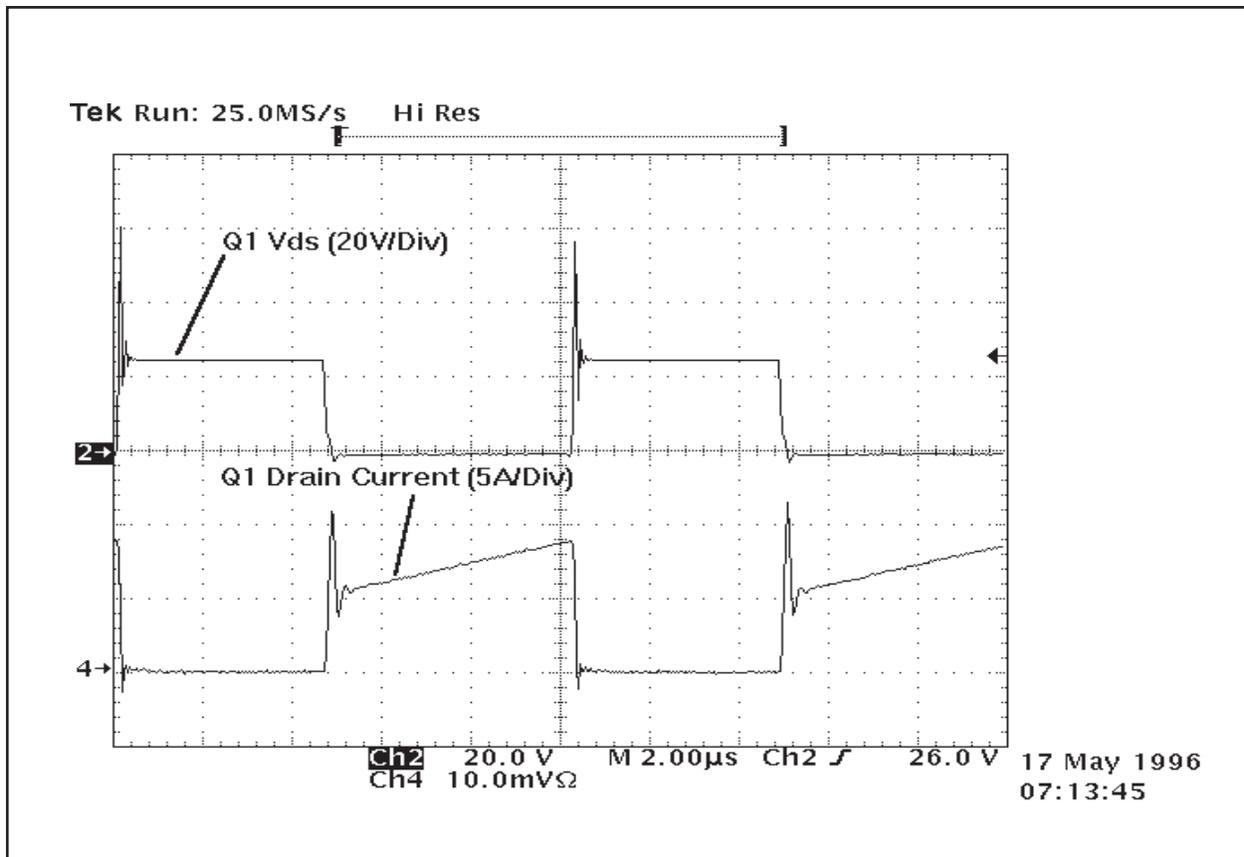**Figure 8.** MOSFET (Q1) Gate and Drain Voltage at Steady State

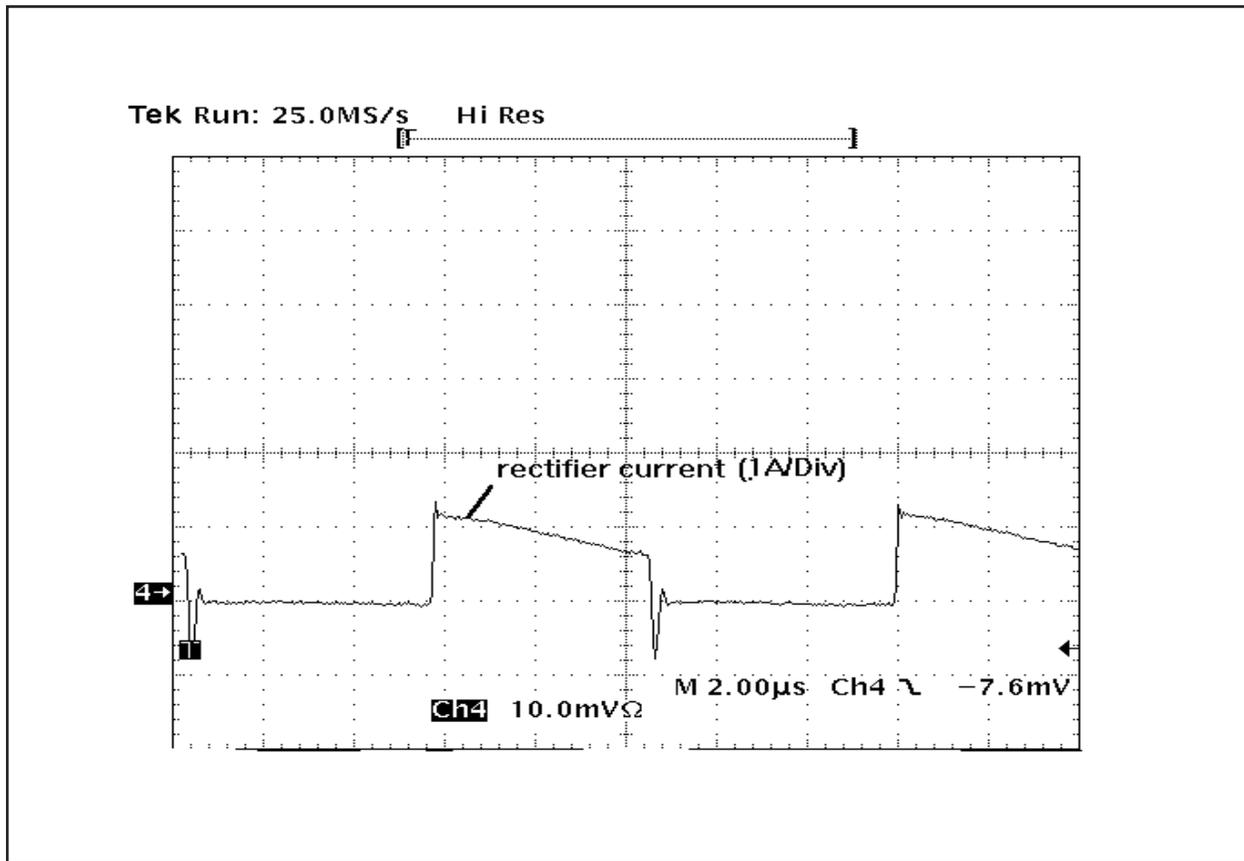**Figure 9.** MOSFET (Q1) Drain Voltage and Current at Steady State
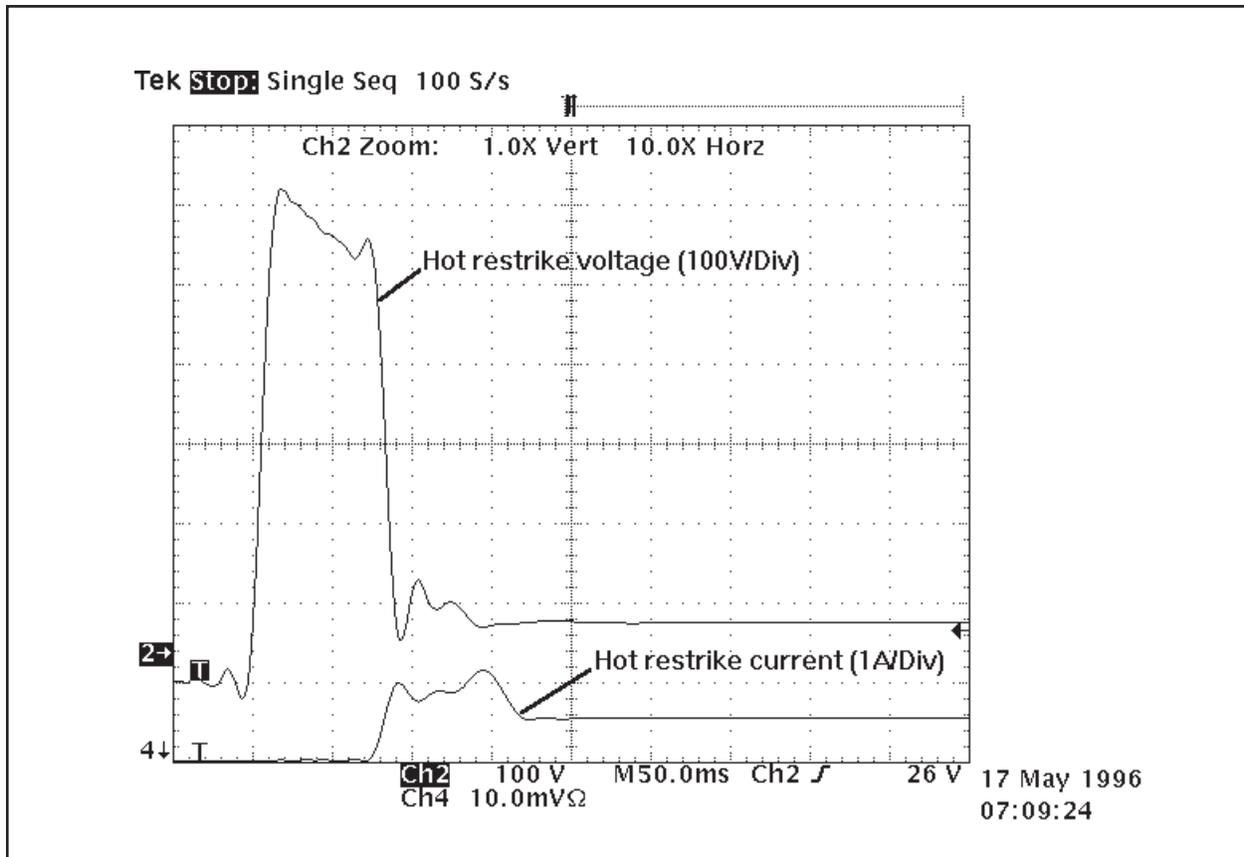
Figure 10. Output Rectifier (D1) Current at Steady State

Figure 11. Ballast Hot Restrike Voltage and Current

35W HID BALLAST PARTS LIST			
REF DES	**PART DESCRIPTION**	**DIGIKEY NUMBER**	**QTYPER**
RI	4.7Ω 1/4 W CC	10QBK-ND	1
R2	0.02Ω 1W		1
R3, R5	1k 1/4W CC	1KQBK-ND	2
R4	3.3k 1/4W CC	4KQBK-ND	1
R6	270k 1/4W CC	270KQBK-ND	1
R7	100k 1/4W CC	100KQBK-ND	1
R9	180Ω 1/2W CC	220HBK-ND	1
R11	5.1k 1/4W CC	5.1KQBK-ND	1
R12	12.5k 1/4W CC	15KQBK-ND	1
R13	16.1k 1/4W CC	16KQBK-ND	1
R14	1k 1/4W CC	1KQBK-ND	1
R15	150k 1/4W CC	150KQBK-ND	1
R16	250k 1/4W CC	250KQBK-ND	1
R17,R18	27k 1/4W CC	27KQBK-ND	2
R19,R25,R32,R8	10k 1/4W CC	10KQBK-ND	4
R20	0.75Ω 3W CC	VC3D.75-ND	1
R21	565k 1/4W CC	562KXBK-ND	1
R22,R23	282k 1/4W CC	280KXBK-ND	2
R24	560Ω 1/2W CC	560HBK-ND	1
R26,R27	100k 1/4W CC	100KQBK-ND	2
R30	18Ω 3W CC	VC3D18-ND	1
R31	330Ω 3W CC	VC3D330-ND	1
C33	10µF/100V POLY FILM	EF1106-ND	1
C1	1µF/50V METALLIZED FILM	P4675-ND	1
C2,C3,C26	470µF/50V ALUM ELEC	P1248-ND	3
C4	0.47µF/630V POLY FILM	EF4225-ND	1
C8,C11	0.47µF/50V CERAMIC	P4671-ND	2
C6,C7	4.7µF/250V ALUM ELEC	P6187-ND	2
C9	470pF/25V CERAMIC	P4808-ND	1
C10	10µF/35V ALUM ELEC	P1227-ND	1
C12,C13	1µF METALIZED FILM, NISSEI #R68105K63B		2
C14	150pF/50V CERAMIC	P4804-ND	1
C15	0.056µF/25V CERAMIC	P1240-ND	1
C16	47µF/25V ALUM ELEC	P1220-ND	1
C17,C18,C19	0.01µF/50V CERAMIC	P4513-ND	3
C5,C24	0.1µF/50V CERAMIC	P4525-ND	2
C25	1000pF/50V CERAMIC	P4812-ND	1
C30	100µF/25V ALUM ELEC	P1221-ND	1
C31	180pF/1kV CERAMIC DISK	P4119-ND	1
C32	1000pF/100V CERAMIC	P4036-ND	1
Z1	1N5235B, 6.8V ZENER	1N5235BCT-ND	1
Q2,Q3	2N3904, 40V, 0.200mA TRANISTOR		2
Q1	IRF1310, 100V, 0.027Ω	NEWARK#IRF1310	1
D1	MUR860, 600V, 8A FST REC	NEWARK#MUR860	1
HS2,3,4,5	THERMALLOY#7128D, HS FOR Q2,Q3,Q4	NEWARK#95F715	4
U1	UCC3305JP		1
HS1	THERMALLOY #6398-P2,HS FOR Q1		1
L1	E100-8 MICROMETALS		1
	CORE-30T #18AWG		
	35µH		
L2	RM10PA250-3F3 PHILIPS		
	10T PRIMARY LITZ(2X10X,1)		
	60T SECONDARY LITZ(1X15X,1)		
	WINDING SEQUENCE		
	(PRIM-10T, SEC-30T, PRIM-10T,SEC-30T, PRIM-10T)		

CONCLUSION

The performance data presented of a typical UCC3305 HID lamp controller application, demonstrated it to be a excellent means of controlling a 35W DC metal halide HID lamp. The power regulation and efficiency achieved using the SEPIC converter topology proved it to be a good alternative to other conventional circuit topologies for an automotive lighting application. The many protection and control features of the UCC3305 simplify the task of the ballast designer considerably, making it an economically feasable choice for AC as well as DC HID lamp applications.

REFERENCES

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[2] Lloyd Dixon, "High Power Factor Preregular Using Sepic Converter", Unitrode Power Supply Seminar SEM1100.

[3] Abraham Pressman: SWITCHING POWER SUPPLY DESIGN, Mc Graw-Hill, Inc.