Introduction to phase-locked loop system modeling

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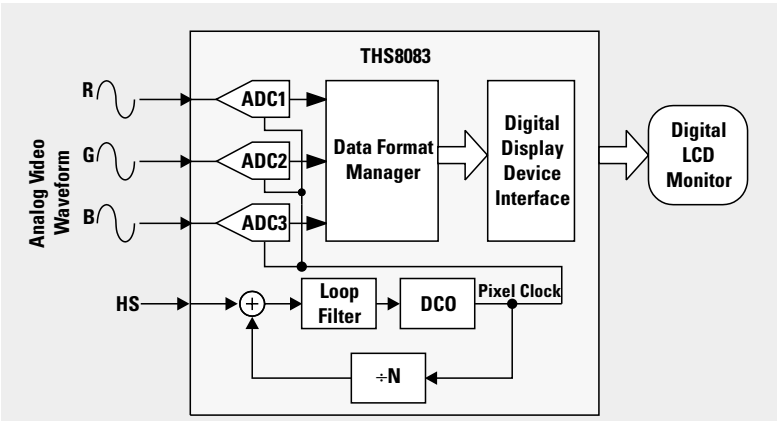
Introduction

Phase-locked loops (PLLs) are one of the basic building blocks in modern electronic systems. They have been widely used in communications, multimedia and many other applications. The theory and mathematical models used to describe PLLs are of two types: linear and nonlinear. Nonlinear theory is often complicated and difficult to deal with in real-world designs. Analog PLLs have been well modeled by linear control theory. Starting from a well-defined model in the continuous-time domain, this article introduces a modeling and design method for a digital PLL based on linear control theory. It has been proved that a linear model is accurate enough for most electronic applications as long as certain conditions are met. Figure 1 shows a block diagram of the Texas Instruments THS8083 device that targets LCD monitor and digital TV applications. The task of the PLLs in these devices is to recover the pixel clock based on input reference HS (horizontal sync). This PLL has been accurately modeled by the method introduced in this article.

Figure 1. A typical PLL application



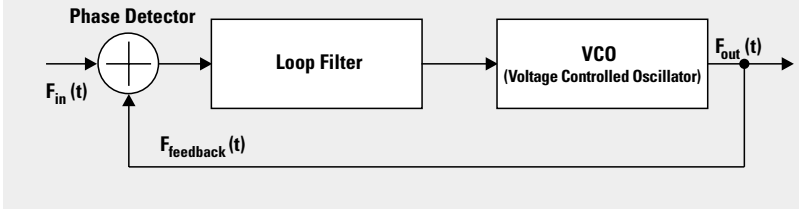
From a PLL system point of view, the DCO has the same function as the VCO, but it is implemented in the digital domain, so the output frequency of the DCO is a function of the input digital value.

A linear PLL model in the continuous-time domain (S-domain)

From Figure 2, the PLL can be easily recognized as a feedback control system. This system consists of the following components.

- Phase detector—detects the phase difference between the input signal $F_{in}(t)$ and the feedback signal $F_{feedback}(t)$
- Loop filter—typically, a filter with low-pass characterization
- VCO—voltage-controlled oscillator whose output frequency is a function of its input voltage

Figure 2. Functional block diagram of a typical PLL

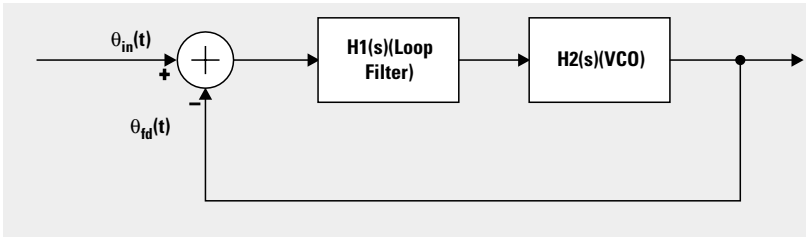


A linear model of the PLL in S-domain

Based on the condition that phase error is small, which can be expressed mathematically as $\sin(\theta) \approx \theta$, a PLL can be accurately described by a linear model. Figure 2 is a block diagram of a linear PLL model.

In Figure 3, $\theta_{in}(t)$ is the phase of the input signal, and $\theta_{fd}(t)$ is the phase of the feedback signal. Since the system is described in the continuous-time

Figure 3. A linear model of the PLL in S-domain



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domain, the transfer functions of each component are given out in Laplace-transform format.

- Transfer function of loop filter:

$$H1(s) = \frac{G_{lp}}{G_{lp} + S} \quad \textbf{(1)}$$

- Transfer function of VCO:

$$H2(s) = \frac{G_{vco}}{S} \quad \textbf{(2)}$$

- Closed-loop transfer function of a PLL:

$$H_{cl}(s) = \frac{G_{lp}G_{vco}}{S^2 + G_{lp}S + G_{lp}G_{vco}} \quad \textbf{(3)}$$

Based on the closed-loop transfer function (Equation 3), one can see that this is a second-order system. In automatic control system theory, the transfer function of the second-order system often can be written as

$$H_s(S) = \frac{{\omega_n}^2}{S^2 + 2\zeta\omega_n S + {\omega_n}^2}, \quad \textbf{(4)}$$

where ω_n is defined as natural undamped frequency, and ζ is defined as damping ratio. This system is called a standard prototype second-order system.

Based on the transfer function of a second-order prototype system, a characteristic equation of the system is defined as

$$\Delta(s) = S^2 + 2\zeta\omega_n S + {\omega_n}^2 \quad \textbf{(5)}$$

By solving the roots of the characteristic equation, two poles of the system, S_0 and S_1, can be derived.

$$S_0 = -\zeta\omega_n + j\omega_n\sqrt{1-\zeta^2} = -\alpha + j\omega, \quad \text{and} \quad \textbf{(6)}$$

$$S_1 = -\zeta\omega_n - j\omega_n\sqrt{1-\zeta^2} = -\alpha - j\omega, \quad \textbf{(7)}$$

where α is defined as damping factor and ω is defined as damped frequency.

Based on Equations 6 and 7, as soon as ζ and ω_n of the system are given, the poles of a second-order prototype system can be determined. Those two parameters are usually used to specify performance requirements of a system. As a matter of fact, most transient-response performances of a system can be determined based on these two parameters. The following is a list of performance parameters defined based on ζ and ω_n. Derivations of these equations can be found in most control theory textbooks.[1]

Damping factor α:

$$\alpha = \zeta\omega_n \quad \textbf{(8)}$$

Damped frequency ω:

$$\omega = \omega_n\sqrt{1-\zeta^2} \quad \textbf{(9)}$$

Settling time:

$$t_s = \frac{4}{\zeta\omega_n} \quad \textbf{(10)}$$

Maximum overshoot time:

$$t_{max} = \frac{\pi}{\omega_n\sqrt{1-\zeta^2}} \quad \textbf{(11)}$$

Maximum overshoot:

$$M = 1 + e^{-\pi\zeta/\sqrt{1-\zeta^2}} \quad \textbf{(12)}$$

Maximum overshoot in percentage:

$$M_{pct} = 100e^{-\pi\zeta/\sqrt{1-\zeta^2}} \quad \textbf{(13)}$$

Until this point, a second-order system has been defined in S-domain, and this system will meet performance requirements specified by ζ and ω_n.

Modeling of digital PLL (DPLL) in the discrete-time domain (Z-domain)

So far, all the modeling shown is in the continuous-time domain. This model can be applied directly to an analog PLL. But the design requirement is for a digital PLL. Normally, the output responses of a discrete-time control system are also functions of continuous-time variable t. Therefore, the goal is to map the system that meets the time-response performance requirements specified by ζ and ω_n to a corresponding second-order model in Z-domain.

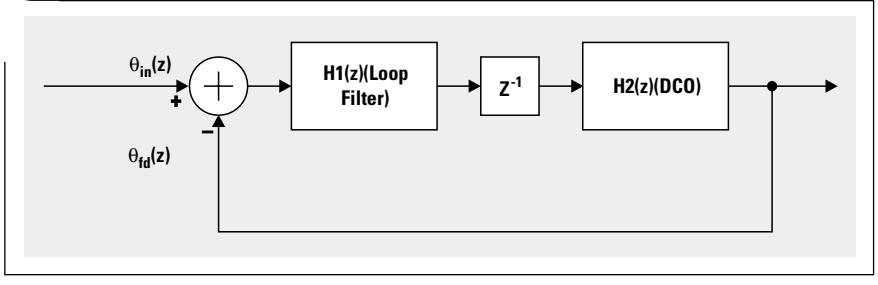
A linear model of PLL in discrete-time domain

A block diagram of the model of a DPLL is shown in Figure 4. Transfer functions of each component in the DPLL are in the Z-transfer format as follows.

- Transfer function of loop filter:

$$H1(Z) = \frac{aZ-1}{Z-1} \quad \textbf{(14)}$$

Figure 4. A DPLL model in the Z-domain



- Transfer function of a digital controlled oscillator (DCO):

$$H2(Z) = \frac{cZ}{Z-1} \quad \textbf{(15)}$$

- Z^{-1} is a delay unit, usually a register or register array.

With the block diagram and the transfer functions of components, a Linear Time Invariant (LTI) model can be developed to represent the PLL. The closed-loop transfer function of the DPLL model is then derived:

$$H(Z) = \frac{acZ - c}{Z^2 + (ac-2)Z + (1-c)} \quad \textbf{(16)}$$

Mapping the poles of a second-order system from S-domain to Z-domain

The transfer function of a second-order PLL in the Z-domain can be written in a general format as

$$H(z) = \frac{N(z)}{(Z-Z_1)(Z-Z_0)}, \quad \textbf{(17)}$$

where Z_0 and Z_1 are two poles of the system in Z-domain. Corresponding to the S-domain analysis, a characteristic equation of a discrete-time system is defined as

$$\Delta(z) = (Z-Z_1)(Z-Z_0) = Z^2 - (Z_1+Z_0)Z + Z_1Z_0 \quad \textbf{(18)}$$

C_1 and C_0 are defined as coefficients of the characteristic equation:

$$\begin{aligned} C_1 &= -(Z_1+Z_0) \\ C_0 &= Z_1Z_0 \end{aligned} \quad \textbf{(19)}$$

Then the characteristic equation can be written in the simplified format

$$\Delta(z) = Z^2 + C_1Z + C_0 \quad \textbf{(20)}$$

By definition of a discrete-time transformation,[2] two poles of this system in the Z-domain can be mapped from the poles in S-domain as

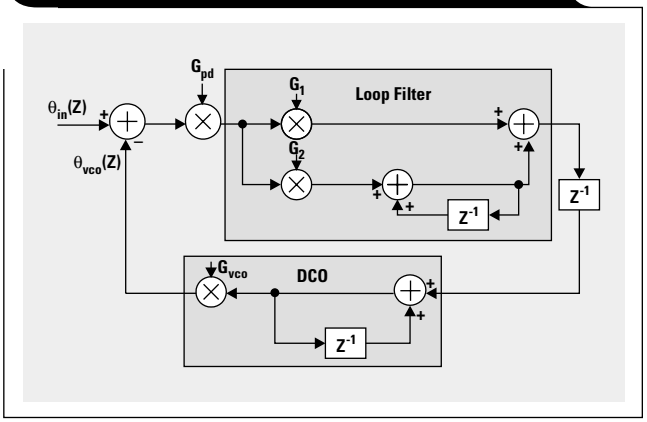
$$\begin{aligned} Z_0 &= e^{S_0T_s} = e^{\left(-\zeta\omega_nT_s + j\omega_nT_s\sqrt{1-\zeta^2}\right)} \text{ and} \\ Z_1 &= e^{S_1T_s} = e^{\left(-\zeta\omega_nT_s - j\omega_nT_s\sqrt{1-\zeta^2}\right)}, \end{aligned} \quad \textbf{(21)}$$

where T_s is the sampling period of the discrete system.

With the poles mapped in the Z-domain and Equation 19, coefficients C_0 and C_1 of the characteristic equation (Equation 20) can be derived in a format that is described by the parameters ζ and ω_n:

$$\begin{aligned} C_0 &= e^{-2\zeta\omega_nT_s} \\ C_1 &= -2e^{-\zeta\omega_nT_s}\cos\left(\omega_nT_s\sqrt{1-\zeta^2}\right) \end{aligned} \quad \textbf{(22)}$$

Figure 5. A completely implemented block diagram of a second-order DPLL system



Then a characteristic equation is derived by mapping the poles in a continuous-time domain system. Since the characteristic function will largely affect system transient responses, Equations 20 and 17 can determine the transfer function of a DPLL. The numerator of Equation 17 can be a constant scaling factor, or zeros can be introduced to tune the performance of the system. For example, if the DPLL adopts the architecture-based Equation 16, its transfer function will be determined as soon as the poles are mapped. The following section presents a completely implemented DPLL.

Implementation of a second-order DPLL

This section presents detailed information for implementing a completed DPLL system based on the previous analysis and model mapping results. An architecture diagram of a second-order DPLL system is presented in Figure 5. Based on this architecture, each basic building block is described.

- Loop filter—an IIR filter has been designed as the loop filter. H1(z) is its transfer function:

$$H1(z) = \frac{G_1 + G_2 - G_1Z^{-1}}{1-Z^{-1}}, \quad \textbf{(23)}$$

where G_1 and G_2 are the gains of the IIR filter.

- A digital-controlled VCO or a discrete-time oscillator (DTO) will have H2(z) as its transfer function:

$$H2(z) = \frac{G_{vco}}{1-Z^{-1}}, \quad \textbf{(24)}$$

where G_{vco} is the gain of the discrete VCO.

With these building blocks of the DPLL system, the closed-loop transfer function can be written as

$$H(z) = \frac{\theta_{vco}(z)}{\theta_{in}(z)} = \frac{H1(z)H2(z)Z^{-1}G_{pd}}{1+H1(z)H2(z)Z^{-1}G_{pd}}, \quad \textbf{(25)}$$

where G_{pd} is the gain of the phase detector.

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The expended format of this transfer function can be written as

$$H(z)=\frac{\theta_{vco}(z)}{\theta_{in}(z)}=\frac{(g1+g2)Z-g1}{Z^2+(g1+g2-2)Z+(1-g1)}, \quad \textbf{(26)}$$

where $g1 = G_{pd}G_{vco}G_1$ and $g2 = G_{pd}G_{vco}G_2$.

By comparing the characteristic equation $\Delta(z)$ of a DPLL (Equation 20), the following equation can be constructed:

$$C_0 = 1-g1$$
$$C_1 = g1+g2-2 \quad \textbf{(27)}$$

The g1 and g2 can be resolved based on Equations 27 and 22:

$$g1 = 1-e^{-2\zeta\omega_n T_s}$$
$$g2 = 1+e^{-2\zeta\omega_n T_s}-2e^{-\zeta\omega_n T_s}\cos\left(\omega_n T_s\sqrt{1-\zeta^2}\right) \quad \textbf{(28)}$$

With Equations 26 and 28, the model of a DPLL is completely derived.

Stability and steady-state error study of the DPLL system

Stability of the DPLL system

One mandatory requirement for designing DPLLs is that the DPLL system must be stable. Basically, the stable condition of a discrete-time system occurs when the roots of the characteristic equation are inside the unit circle $|Z| = 1$ in the Z-plane. Normally, after a system is implemented, numerical coefficients can be substituted into the characteristic equation. By solving the characteristic equation numerically, the positions of the poles can be found to determine if the system is stable; however, this method is technically difficult to use when implementing a DPLL, since numerical coefficients will not be available at the beginning of the process.

One of the most efficient methods for testing the stability of a discrete-time system is Jury's stability criterion.[1] This method can guide designs of a DPLL to converge to an optimized stable system quickly, without a large amount of numerical calculation and simulation. It can be applied directly to the second-order DPLL model to determine the stable condition. According to this criterion, the necessary and sufficient conditions are that the characteristic equation of a second-order system,

$$\Delta(Z) = a_2Z^2 + a_1Z + a_0 = 0, \quad \textbf{(29)}$$

should meet the following conditions in order to have no roots on or outside the unit circle:

$\Delta(1) > 0$,
$\Delta(-1) > 0$, and
$|a_0| < a_2$

Applying these conditions to the denominator of Equation 26, stable condition ranges of this DPLL architecture can be derived:

$$0 < g1 < 2 \quad \textbf{(30)}$$

$$0 < g2 < 4 \quad \textbf{(31)}$$

Steady-state error analysis of the DPLL

A steady-state error analysis of a DPLL is extremely important in PLL design. Now that a stable system has been described, the steady-state error of phase and frequency of the DPLL will be studied. It will be proven that both the phase and frequency error of this DPLL system will be zero when the system reaches its steady state.

Phase error analysis

Assume that the phase of the input signal has a step change. In the time domain, step changing of the phase of the input signal can be described by the step function

$$\Theta in(t) = \Delta\Theta \times u(t) \quad \textbf{(32)}$$

Here, $\Delta\Theta$ is the constant value by which the input signal phase jumped. Applying the Z-transform to Equation 32 yields

$$\Theta in(Z) = \frac{\Delta\Theta \times Z}{Z-1} \quad \textbf{(33)}$$

Based on the linear model, the output-response function of the DPLL for a phase-step input can be written as

$$\Theta fd(z) = H(Z) \times \Theta in(Z)$$
$$= \frac{\Delta\Theta \times Z(acZ-c)}{(Z-1)[Z^2+(ac-2)Z+(1-c)]} \quad \textbf{(34)}$$

Based on Equation 34, a numerical analysis can be carried out by using an existing software tool such as MATLAB. In this way, the steady-state error of an implemented DPLL system can be observed. The focus is on the general analytical results.

Assuming E(Z) is the phase-error function, by definition E(Z) can be written as

$$E(Z) = \Theta in(Z) - \Theta fd(Z) \quad \textbf{(35)}$$

Substituting Equation 34 into Equation 35 produces

$$E(Z) = [1-H(Z)]\Theta in(Z) \quad \textbf{(36)}$$

Substituting Equations 33 and 16 into Equation 36, the phase-error function is written as

$$E(Z) = \frac{\Delta\Theta Z(Z-1)}{Z^2+(ac-2)Z+(1-c)} \quad \textbf{(37)}$$

According to the Final-Value Theorem,

$$\lim_{k\to\infty} e(kT) = \lim_{z\to 1}(1-Z^{-1})E(Z) \quad \textbf{(38)}$$

Based on this theorem, the steady-state error, which is the final value of e(kT) in the time domain, can be derived. The condition for using the Final-Value Theorem is that the function $(1 - Z^{-1})E(Z)$ has no poles on or outside the unit circle $|Z| = 1$ in the Z-plane. The detailed method for meeting this condition has already been established.

Substituting Equation 37 into Equation 38 yields

$$\lim_{k\to\infty} e(kT) = \lim_{z\to 1} \frac{\Delta\Theta Z(Z-1)}{Z^2+(ac-2)Z+(1-c)} = 0 \qquad \textbf{(39)}$$

Conclusion: When the phase of the input signal s makes a step-jump, the phase error of this DPLL eventually will be eliminated by the closed-loop system.

Frequency error analysis

Given an input signal, assuming t = 0, its frequency jumps from $\omega 0$ to $\omega 1$, and let $\Delta\omega = \omega 1 - \omega 0$. The input phase can be written as

$$\Theta in(t) = \Delta\omega \times t \times U(t) \qquad \textbf{(40)}$$

Applying the Z-transform to Equation 40 to transfer it to Z-domain yields

$$\Theta in(Z) = \frac{\Delta\omega TZ}{(Z-1)^2} \qquad \textbf{(41)}$$

Substituting Equations 41 and 16 into Equation 36, the frequency-error function is derived as follows:

$$E(Z) = \frac{\Delta\omega TZ}{Z^2+(ac-2)Z+(1-c)} \qquad \textbf{(42)}$$

The Final-Value Theorem is applied to Equation 42 to get the steady-state error in time domain:

$$\lim_{k\to\infty} e(kT) = \lim_{z\to 1}(1-Z^{-1})E(Z)$$

$$= \lim_{z\to 1} \frac{\Delta\omega T(Z-1)}{Z^2+(ac-2)Z+(1-c)} = 0 \qquad \textbf{(43)}$$

Conclusion: When the frequency of an input signal has a step jump, the phase error of the DPLL eventually will be eliminated by the closed-loop system.

A design example

Following are a real design example and the simulation/ measuring results of the system.

Design requirements:

- Design a digital PLL that can recover the pixel clock of a PC graphics VGA output signal.
- The frequency of horizontal synchronization signal HS of VGA is f_s = 60023 Hz, T_s = 0.00001666s.
- The relationship between a period of the pixel clock T_p and a period of horizontal sync T_s is $T_s = 1312T_p$.
- PLL locking time is < 15 ms.
- One overshoot occurs during the locking process.

Based on these requirements, the following performance parameters can be determined:

$\zeta = 0.707$
$\omega_n = 2\pi 100$ rad/s
f_s = 60023 Hz, T_s = 0.00001666s

Based on these parameters, C_0, C_1, g1, and g2 can be calculated by using Equations 22 and 28:

$C_0 = 0.9853$
$C_1 = -1.9852$
g1 = 0.0147
g2 = 0.0001

The transfer function of the DPLL that meets the performance specification can be constructed:

$$H(z) = \frac{0.0148Z - 0.0147}{Z^2 - 1.9852Z + 0.9853} \qquad \textbf{(44)}$$

Based on this Z-domain model, the DPLL system performance can be simulated at system level. Figures 6 and 7 are simulation results based on this model.

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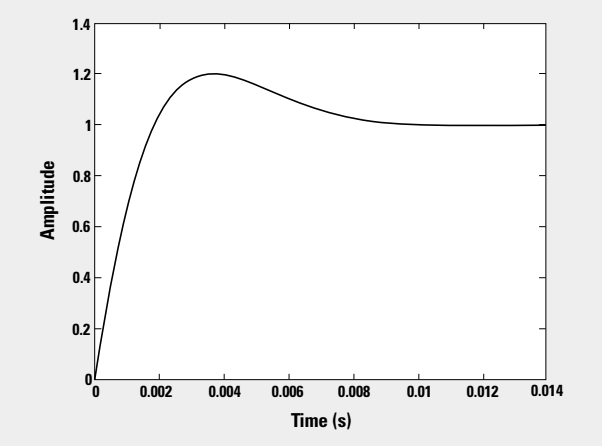
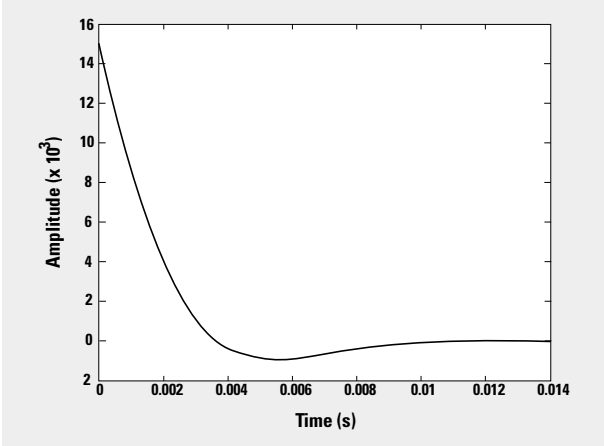
Figure 6. Step response of the DPLL system



1. Step function input response of the model describes the behavior of the system when the input signal phase is a step function. It also proves that the system is stable.

Figure 7. Impulse input response of the DPLL system



2. Impulse function input response of the model describes the behavior of the system when the input signal has a phase impulse error. It proves that the stable error of the system is zero.

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Physically, this DPLL is implemented in the following way:

- Phase detector—a high-speed counter to sample the input signal and calculate the phase error
- Loop filter—a digital IIR filter
- DCO—a DDS (direct-digital-synthesis) oscillator. From a PLL system point of view, the DCO has the same function as the VCO, but it is implemented in digital domain, so the output frequency of the DCO is a function of the input digital value.

References

1. Benjamin C. Kuo, *Automatic Control Systems*.
2. Alan V. Oppenheim and Ronald W. Schafer, *Discrete-Time Signal Processing*.
3. John L. Stensby, *Phase-Locked Loops, Theory and Applications*.

Related Web sites

www.ti.com/sc/docs/products/msp/dataconv/index.htm

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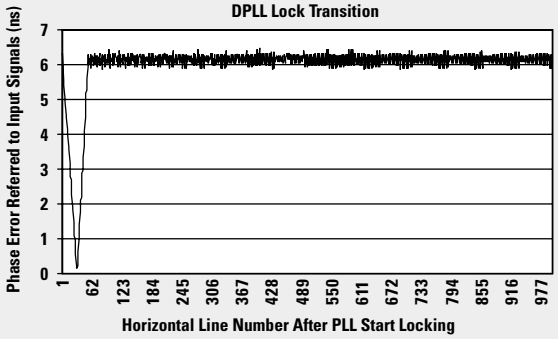
Figure 8. DPLL lock process based on a silicon-implemented DPLL



3. Silicon-implemented DPLL based on the Equation 32 model. It shows gate-level simulation/measuring results for a phase-locking process.

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