

Configuring Stellaris® Tempest- and Firestorm-Class Microcontrollers With Pin Multiplexing

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ABSTRACT

Stellaris Tempest- and Firestorm-class devices provide system designers with a great deal of control over the placement and selection of peripheral module signals that are alternate functions for GPIO signals. This application note provides an overview of the pin muxing implementation, an explanation of how a system designer defines a pin configuration, and examples of the pin configuration process for several Stellaris LM3S devices.

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1 Introduction

Stellaris Tempest- and Firestorm-class microcontrollers provide system designers with a great deal of control over the placement and selection of peripheral module signals that are alternate functions for GPIO signals. These devices have a various number of pins that can be used for peripheral functions or as GPIOs. These pins can be customized to provide the best possible signal combination for each individual system design. The remaining pins on the package are power and ground pins, crystal inputs, and a few other functions (Hibernation module signals, USB and Ethernet I/O signals, and BIAS inputs) that require fixed pin location and function.

This application note provides an overview of the pin muxing implementation, an explanation of how a system designer defines a pin configuration, and examples of the pin configuration process using various Stellaris LM3S microcontrollers.

2 Pin Muxing Overview

Most of the GPIO pins default to GPIO signals at reset, with the following exceptions:

- JTAG/SWD signals needed at power up for the debugger
- UART0 Rx/Tx signals needed to allow the Stellaris Boot Loader to operate from ROM
- SSI0 Clk/Fss/Rx/Tx signals needed to allow the Stellaris Boot Loader to operate from ROM
- I²C SCL/SDA signals needed to allow the Stellaris Boot Loader to operate from ROM

Users can select one from up to 11 possible alternate functions for each pin using the **GPIO Port Control (GPIOCTLx)** registers. The *GPIO Pins and Alternate Functions* table in the **Signal Tables** chapter of a specific device data sheet shows all the possible functions for each GPIO pin.

To configure a GPIO pin to an alternate function, follow these steps:

- Step 1. Enable the clock to the appropriate GPIO port using the `SysCtlPeripheralEnable()` function.
- Step 2. Enable the clock to the peripherals using the `SysCtlPeripheralEnable()` function.
- Step 3. Configure the pins to the appropriate function using the `GPIOPinConfigure()` function.
- Step 4. Configure the signal attributes using the `GPIOPinTypePexxx()` function to configure the pins for the desired specific peripheral function.

3 Pin Allocation

To decide how to distribute the signals on the device, make a list of the signals needed in the system. Three factors to keep in mind when allocating signals are:

- The number of possible pin assignments for each signal. Some signals can only be assigned to one pin, while others can be assigned to up to 10 pins.
- Some signals should be assigned to the same GPIO port so that they can be accessed in a single write, for example, when using both PWM2 and PWM3 for bit banging.
- Some signals with similar functions are fungible. For example, if you need four CCP signals, you can choose any of the CCPx signals; if you need one Fault signal, you can choose any of the Faultx signals.

To begin pin allocation, first assign the signals that have only one available location, then assign the ones that have two, then three, and so on, bearing in mind the factors listed above. Once the pins have been allocated, then write the code to properly configure the GPIOs for the signal selections.

The *Possible Pin Assignments for Alternate Functions* table in the *Signal Tables* chapter of a specific device data sheet shows the possible pin assignments for that device.

4 Examples

Table 1 summarizes the examples in this application report. The code for these examples can be found at <http://www.ti.com/mcu/docs/litabs/multiplefilelist.tsp?sectionId=96&tabId=1502&literatureNumber=spma008b&docCategoryId=1&familyId=2940>. If your application matches (or is a subset of) one of these examples, you can simply use the code for that example, modifying it to remove any unneeded signals. If your application requires additional or different signals that have several possible pin assignments, you may be able to easily modify one of the following examples to meet your requirements. However, if the additional signals that your application requires have few possible pin assignments, it is usually easiest to start from scratch with the pin assignments following those described in the [Pin Allocation](#) section.

The code to create the examples implements Steps 1 and 3 described in the [Pin Muxing Overview](#) section. Steps 2 and 4 are outside the scope of this example and are not included in the code.

Table 1. Example Configurations

Ex. No.	Eth	USB	EPI ⁽¹⁾	HIB	PWM	Fault	QEI	CAN	UART	I ² C	SSI	I ² S	ADC	Ext Ref	Timer	CCP
1	Y	Host	N	Y	NA	NA	NA	1	3	2	2	0	16	Y	4	8
2	Y	OTG	N	Y	NA	NA	NA	1	2	2	2	1	4	Y	4	7
3	Y	OTG	N	Y	NA	NA	NA	0	2 ⁽²⁾	2	2	0	0	N	4	0
4	Y	OTG	HB	Y	NA	NA	NA	2	1	1	1	0	4	Y	4	0
5	Y	OTG	GP	Y	NA	NA	NA	0	1	1	0	1	4	Y	4	0
6	Y	OTG	N	NA	8	4	1	1	1	2	2	0	12	N	4	7
7	Y	N	S	NA	6	1	1	2	2	1	1	0	4	Y	4	2
8	Y	N	HB	NA	0	0	0	0	2	2	1	1	4	N	4	1
9	Y	Host	N	NA	0	0	0	1	3	2	2	1	4	N	4	7
10	Y	N	GP	NA	6	1	0	1	1	1	1	0	4	Y	4	4
11	Y	N	HBF	NA	8	1	1	2	3	2	0	0	4	Y	4	0
12	NA	NA	N	Y	8	4	2	0	2	2	2	0	16	N	4	1
13	NA	NA	S	Y	0	0	0	1	3	1	2	0	4	Y	4	0
14	NA	NA	HBF	Y	8	2	2	2	2	0	0	0	4	Y	4	0
15	NA	NA	S	Y	8	2	2	2	2	0	0	0	4	Y	4	0
16	NA	N	N	NA	0	0	0	1	3 ⁽²⁾	2	2	1	4	N	4	8
17	NA	N	GP	NA	0	0	0	1	2	1	1	1	2	N	4	6
18	NA	OTG	HB	NA	0	0	0	1	1	1	1	1	2	N	4	5
19	NA	OTG	HB	NA	0	0	0	0	2 ⁽²⁾	0	1	0	4	Y	4	6
20	NA	OTG	GP	NA	4	2	1	1	1	1	1	0	4	Y	4	0
21	NA	OTG	GP	NA	8	1	1	1	0	0	0	0	4	Y	4	0

⁽¹⁾ **N** = no EPI interface; **HB** = Host-Bus interface; **GP** = General-Purpose interface; **S** = SDRAM interface; **HBF** = Host-Bus FIFO interface.

⁽²⁾ UART1 uses modem controls.

4.1 Example 1: LM3S9B90

Example 1 uses the LM3S9B90 device with the modules and signals shown in [Table 2](#).

Table 2. Example 1 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB host	USB0PFLT, USB0EPEN	Remaining signals have fixed locations.
Hibernate	—	Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U2Rx, U2Tx	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
ADC	AIN[15:0], VREFA	PB[5:4], PD[7:0], PE[7:2], and PB6 used as analog functions.
Four timers, eight CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5, CCP6, CCP7	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port F: LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with two available pin assignments:

- This configuration does not use any of the pins with two possible pin assignments.

Step 3: Assign signals with three available pin assignments:

- Port H: SSI1Clk (PH4), SSI1Fss (PH5), SSI1Rx (PH6), SSI1Tx (PH7)

Step 4: Assign signals with four available pin assignments:

- Port A: CAN0Rx (PA6), CAN0Tx (PA7)
- Port G: U2Rx (PG0), U2Tx (PG1)
- Port J: I2C1SCL (PJ0), I2C1SDA (PJ1)

Step 5: Assign signals with five available pin assignments:

- Port C: CCP4 (PC4)
- Port H: CCP6 (PH0), CCP7 (PH1), USB0EPEN (PH3)

Step 6: Assign signals with six available pin assignments:

- Port C: U1Rx (PC6), U1Tx (PC7)
- Port G: CCP5 (PG7)

Step 7: Assign signals with seven available pin assignments:

- Port C: CCP1 (PC5)
- Port E: USB0PFLT (PE0)

Step 8: Assign signals with eight available pin assignments:

- Port F: CCP3 (PF1)

Step 9: Assign signals with nine available pin assignments:

- Port E: CCP2 (PE1)
- Port F: CCP0 (PF4)

Table 3 shows the final pin assignments for Example 1. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 3. Final Pin Assignments for Example 1

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	—	TCK/SWCLK	AIN15	USB0PFLT	—	U2Rx	CCP6	I2C1SCL
1	U0Tx	—	TMS/SWDIO	AIN14	CCP2	CCP3	U2Tx	CCP7	I2C1SDA
2	SSI0Clk	I2C0SCL	TDI	AIN13	AIN9	LED1	NA	—	—
3	SSI0Fss	I2C0SDA	TDO/SWO	AIN12	AIN8	LED0	NA	USB0EPEN	NA
4	SSI0Rx	AIN10	CCP4	AIN7	AIN3	CCP0	NA	SSI1Clk	NA
5	SSI0Tx	AIN11	CCP1	AIN6	AIN2	—	NA	SSI1Fss	NA
6	CAN0Rx	VREFA	U1Rx	AIN5	AIN1	NA	NA	SSI1Rx	NA
7	CAN0Tx	NMI	U1Tx	AIN4	AIN0	NA	CCP5	SSI1Tx	NA

4.2 Example 2: LM3S9B90

Example 2 uses the LM3S9B90 device with the modules and signals shown in [Table 4](#).

Table 4. Example 2 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
Hibernate	—	Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
I ² S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers, seven CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5, CCP6	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port D: I2S0RXSCK (PD0), I2S0RXWS (PD1)
- Port F: I2S0TXMCLK (PF1), LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with two available pin assignments:

- Port D: I2S0RXSD (PD4), I2S0RXMCLK (PD5)
- Port F: I2S0TXSD (PF0)

Step 3: Assign signals with three available pin assignments:

- Port D: I2S0TXSCK (PD6), I2S0TXWS (PD7)
- Port E: SSI1C1k (PE0), SSI1Fss (PE1), SSI1Rx (PE2), SSI1Tx (PE3)

Step 4: Assign signals with four available pin assignments:

- Port A: CAN0Rx (PA6), CAN0Tx (PA7)
- Port G: I2C1SCL (PG0), I2C1SDA (PG1)

Step 5: Assign signals with five available pin assignments:

- Port C: USB0EPEN (PC5), CCP4 (PC7)
- Port H: CCP6 (PH0)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB4), U1Tx (PB5)
- Port D: CCP5 (PD2)

Step 7: Assign signals with seven available pin assignments:

- Port C: CCP1 (PC4)
- Port H: USB0PFLT (PH4)

Step 8: Assign signals with eight available pin assignments:

- Port C: CCP3 (PC6)

Step 9: Assign signals with nine available pin assignments:

- Port D: CCP0 (PD3)
- Port F: CCP2 (PF5)

[Table 5](#) shows the final pin assignments for Example 2. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 5. Final Pin Assignments for Example 2

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	I2S0RXSCK	SSI1C1k	I2S0TXSD	I2C1SCL	CCP6	—
1	U0Tx	USB0VBUS	TMS/SWDIO	I2S0RXWS	SSI1C1k	I2S0TXMCLK	I2C1SDA	—	—
2	SSI0C1k	I2C0SCL	TDI	CCP5	SSI1Rx	LED1	NA	—	—
3	SSI0Fss	I2C0SDA	TDO/SWO	CCP0	SSI1Tx	LED0	NA	—	NA
4	SSI0Rx	U1Rx	CCP1	I2S0RXSD	AIN3	—	NA	USB0PFLT	NA
5	SSI0Tx	U1Tx	USB0EPEN	I2S0RXMCLK	AIN2	CCP2	NA	—	NA
6	CAN0Rx	VREFA	CCP3	I2S0TXSCK	AIN1	NA	NA	—	NA
7	CAN0Tx	NMI	CCP4	I2S0TXWS	AIN0	NA	—	—	NA

4.3 Example 3: LM3S9B90

Example 3 uses the LM3S9B90 device with the modules and signals shown in [Table 6](#).

Table 6. Example 3 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
Hibernate	—	Signals have fixed locations.
UART	U0Rx, U0Tx, U1Rx, U1Tx, U1CTS, U1DCD, U1DSR, U1DTR, U1RI, U1RTS	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
Four timers	—	No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port D: U1RI (PD4), **U1DTR** (PD7)
- Port F: U1DSR (PF0), U1RTS (PF1), LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with two available pin assignments:

This configuration does not use any of the pins with two possible pin assignments.

Step 3: Assign signals with three available pin assignments:

- Port A: U1CTS (PA6), U1DCD (PA7)
- Port E: SSI1Clk (PE0), SSI1Fss (PE1), SSI1Rx (PE2), SSI1Tx (PE3)

Step 4: Assign signals with four available pin assignments:

- Port G: I2C1SCL (PG0), I2C1SDA (PG1)

Step 5: Assign signals with five available pin assignments:

- Port C: USB0EPEN (PC5)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB4), U1Tx (PB5)

Step 7: Assign signals with seven available pin assignments:

- Port C: USB0PFLT (PC6)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with nine possible pin assignments.

[Table 7](#) shows the final pin assignments for Example 3. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 7. Final Pin Assignments for Example 3

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	—	SSI1Clk	U1DSR	I2C1SCL	—	—
1	U0Tx	USB0VBUS	TMS/SWDIO	—	SSI1Fss	U1RTS	I2C1SDA	—	—
2	SSI0Clk	I2C0SCL	TDI	—	SSI1Rx	LED1	NA	—	—
3	SSI0Fss	I2C0SDA	TDO/SWO	—	SSI1Tx	LED0	NA	—	NA
4	SSI0Rx	U1Rx	—	U1RI	—	—	NA	—	NA
5	SSI0Tx	U1Tx	USB0EPEN	—	—	—	NA	—	NA
6	U1CTS	—	USB0PFLT	—	—	NA	NA	—	NA
7	U1DTD	NMI	—	U1DTR	—	NA	—	—	NA

4.4 Example 4: LM3S9B90

Example 4 uses the LM3S9B90 device with the modules and signals shown in [Table 8](#).

Table 8. Example 4 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
EPI interface to Host Bus	EPI0S[31:0]	
Hibernate	—	Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx, CAN1Rx, CAN1Tx	
UART	U0Rx, U0Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers	—	No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3), EPI0S19 (PD4), EPI0S28 (PD5), EPI0S29 (PD6), EPI0S30 (PD7)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port F: CAN1Rx (PF0), CAN1Tx (PF1), LED1 (PF2), LED0 (PF3), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

This configuration does not use any of the pins with two possible pin assignments.

Step 3: Assign signals with three available pin assignments:

This configuration does not use any of the pins with three possible pin assignments.

Step 4: Assign signals with four available pin assignments:

- Port D: CAN0Rx (PD0), CAN0Tx (PD1)

Step 5: Assign signals with five available pin assignments:

- Port A: USB0EPEN (PA6)

Step 6: Assign signals with six available pin assignments:

This configuration does not use any of the pins with six possible pin assignments.

Step 7: Assign signals with seven available pin assignments:

- Port A: USB0PFLT (PA7)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with nine possible pin assignments.

Table 9 shows the final pin assignments for Example 4. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 9. Final Pin Assignments for Example 4

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	CAN0Rx	EPI0S8	CAN1Rx	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/SWDIO	CAN0Tx	EPI0S9	CAN1Tx	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	LED1	NA	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	LED0	NA	EPI0S0	NA
4	SSI0Rx	EPI0S23	EPI0S2	EPI0S19	AIN3	EPI0S12	NA	EPI0S10	NA
5	SSI0Tx	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	NA	EPI0S11	NA
6	USB0EPEN	VREFA	EPI0S4	EPI0S29	AIN1	NA	NA	EPI0S26	NA
7	USB0PFLT	NMI	EPI0S5	EPI0S30	AIN0	NA	EPI0S31	EPI0S27	NA

4.5 Example 5: LM3S9B90

Example 5 uses the LM3S9B90 device with the modules and signals shown in [Table 10](#).

Table 10. Example 5 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
EPI interface in general-purpose mode	EPI0S[31:0]	
Hibernate	—	Signals have fixed locations.
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx	
I ² C	I2C0SCL, I2C0SDA	
I ² S	I2S0RXCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	

Table 10. Example 5 Module and Signal List (continued)

Module	Signals	Notes
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: I2S0RXSCK (PD0), I2S0RXWS (PD1), EPI0S20 (PD2), EPI0S21 (PD3), EPI0S19 (PD4), EPI0S28 (PD5), EPI0S29 (PD6), EPI0S30 (PD7)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port F: I2S0TXMCLK (PF1), LED1 (PF2), LED0 (PF3), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port A: I2S0RXSD (PA2), I2S0RXMCLK (PA3)
- Port F: I2S0TXSD (PF0)

Step 3: Assign signals with three available pin assignments:

- Port A: I2S0TXSCK (PA4), I2S0TXWS (PA5)

Step 4: Assign signals with four available pin assignments:

This configuration does not use any of the pins with four possible pin assignments.

Step 5: Assign signals with five available pin assignments:

- Port A: USB0EPEN (PA6)

Step 6: Assign signals with six available pin assignments:

This configuration does not use any of the pins with six possible pin assignments.

Step 7: Assign signals with seven available pin assignments:

- Port A: USB0PFLT (PA7)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with nine possible pin assignments.

Table 11 shows the final pin assignments for Example 5. **NA** appears in a column when a pin is not available on the microcontroller. — appears in a column when a pin is not used for an analog or alternate digital function.

Table 11. Final Pin Assignments for Example 5

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	I2S0RXSCK	EPI0S8	I2S0TXSD	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/SWDIO	I2S0RXWS	EPI0S9	I2S0TXMCLK	EPI0S14	EPI0S7	EPI0S17
2	I2S0RXSD	I2C0SCL	TDI	EPI0S20	EPI0S24	LED1	NA	EPI0S1	EPI0S18
3	I2S0RXMCLK	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	LED0	NA	EPI0S0	NA
4	I2S0TXSCK	EPI0S23	EPI0S2	EPI0S19	AIN3	EPI0S12	NA	EPI0S10	NA
5	I2S0TXWS	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	NA	EPI0S11	NA
6	USB0EPEN	VREFA	EPI0S4	EPI0S29	AIN1	NA	NA	EPI0S26	NA
7	USB0PFLT	NMI	EPI0S5	EPI0S30	AIN0	NA	EPI0S31	EPI0S27	NA

4.6 Example 6: LM3S9B92

Example 6 uses the LM3S9B92 device with the modules and signals shown in Table 12.

Table 12. Example 6 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, Fault0, Fault1, Fault2, Fault3	
QEI	PhA0, PhB0, IDX0	
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
ADC	AIN[11:0]	PB[5:4], PD[7:4] and PE[7:2] used as analog functions.
Four timers, seven CCP inputs	CCP0, CCP1, CCP2, CCP4, CCP5, CCP6, CCP7	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), Fault1 (PB6), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port F: LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with two available pin assignments:

- Port C: PWM6 (PC4), Fault2 (PC5)
- Port H: Fault3 (PH2)

Step 3: Assign signals with three available pin assignments:

- Port C: PWM7 (PC6)
- Port D: PhA0 (PD1)
- Port H: SSI1Clk (PH4), SSI1Fss (PH5), SSI1Rx (PH6), SSI1Tx (PH7)

Step 4: Assign signals with four available pin assignments:

- Port A: CAN0Rx (PA6), CAN0Tx (PA7)
- Port D: PWM2 (PD2), PWM3 (PD3)
- Port J: I2C1SCL (PJ0), I2C1SDA (PJ1)

Step 5: Assign signals with five available pin assignments:

- Port C: PhB0 (PC7)
- Port D: IDX0 (PD0)
- Port F: PWM0 (PF0), PWM1 (PF1)
- Port H: CCP7 (PH1), USB0EPEN (PH3)

Step 6: Assign signals with six available pin assignments:

- Port G: CCP5 (PG7)
- Port H: CCP6 (PH0)
- Port J: CCP4 (PJ4)

Step 7: Assign signals with seven available pin assignments:

- Port E: USB0PFLT (PE0), Fault0 (PE1)

Step 8: Assign signals with eight available pin assignments:

- Port G: PWM4 (PG0), PWM5 (PG1)
- Port J: CCP1 (PJ6)

On the LM3S9B92 microcontroller, no signals have nine possible pin assignments.

Step 9: Assign signals with 10 available pin assignments:

- Port J: CCP0 (PJ2), CCP2 (PJ5)

Table 13 shows the final pin assignments for Example 6. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 13. Final Pin Assignments for Example 6

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	IDX0	USB0PFLT	PWM0	PWM4	CCP6	I2C1SCL
1	U0Tx	USB0VBUS	TMS/SWDIO	PhA0	Fault0	PWM1	PWM5	CCP7	I2C1SDA
2	SSI0Clk	I2C0SCL	TDI	PWM2	AIN9	LED1	NA	Fault3	CCP0
3	SSI0Fss	I2C0SDA	TDO/SWO	PWM3	AIN8	LED0	NA	USB0EPEN	—
4	SSI0Rx	AIN10	PWM6	AIN7	AIN3	—	NA	SSI1Clk	CCP4
5	SSI0Tx	AIN11	Fault2	AIN6	AIN2	—	NA	SSI1Fss	CCP2
6	CAN0Rx	Fault1	PWM7	AIN5	AIN1	NA	NA	SSI1Rx	CCP1
7	CAN0Tx	NMI	PhB0	AIN4	AIN0	NA	CCP5	SSI1Tx	—

4.7 Example 7: LM3S9B92

Example 7 uses the LM3S9B92 device with the modules and signals shown in Table 14.

Table 14. Example 7 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
EPI interface to SDRAM	EPIOS{31:28}, EPIOS[19:0]	
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, Fault0	
QEI	PhA0, PhB0, IDX0	
CAN	CAN0Rx, CAN0Tx, CAN1Rx, CAN1Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers, two CCP inputs	CCP0, CCP1	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPIOS2 (PC4), EPIOS3 (PC5), EPIOS4 (PC6), EPIOS5 (PC7)
- Port E: EPIOS8 (PE0), EPIOS9 (PE1)
- Port F: CAN1Rx (PF0), CAN1Tx (PF1), LED1 (PF2), LED0 (PF3), EPIOS12 (PF4), EPIOS15 (PF5)
- Port G: EPIOS13 (PG0), EPIOS14 (PG1), EPIOS31 (PG7)
- Port H: EPIOS6 (PH0), EPIOS7 (PH1), EPIOS1 (PH2), EPIOS0 (PH3), EPIOS10 (PH4), EPIOS11 (PH5)
- Port J: EPIOS16 (PJ0), EPIOS17 (PJ1), EPIOS18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: EPIOS19 (PD4), EPIOS28 (PD5), EPIOS30 (PD7)
- Port J: EPIOS29 (PJ5)

Step 3: Assign signals with three available pin assignments:

- Port E: PhA0 (PE2)

Step 4: Assign signals with four available pin assignments:

- Port D: CAN0Rx (PD0), CAN0Tx (PD1), PWM2 (PD2), PWM3 (PD3)

Step 5: Assign signals with five available pin assignments:

- Port A: PWM0 (PA6), PWM1 (PA7)
- Port B: IDX0 (PB4)
- Port E: PhB0 (PE3)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)

Step 7: Assign signals with seven available pin assignments:

- Port D: Fault0 (PD6)

Step 8: Assign signals with eight available pin assignments:

- Port H: PWM4 (PH6), PWM5 (PH7)
- Port J: CCP1 (PJ6)

On the LM3S9B92 microcontroller, no signals have nine possible pin assignments.

Step 9: Assign signals with 10 available pin assignments:

- Port B: CCP0 (PB5)

Table 15 shows the final pin assignments for Example 7. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 15. Final Pin Assignments for Example 7

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	CAN0Rx	EPIOS8	CAN1Rx	EPIOS13	EPIOS6	EPIOS16
1	U0Tx	U1Tx	TMS/SWDIO	CAN0Tx	EPIOS9	CAN1Tx	EPIOS14	EPIOS7	EPIOS17
2	SSI0Clk	I2C0SCL	TDI	PWM2	PhA0	LED1	NA	EPIOS1	EPIOS18
3	SSI0Fss	I2C0SDA	TDO/SWO	PWM3	PhB0	LED0	NA	EPIOS0	—
4	SSI0Rx	IDX0	EPIOS2	EPIOS19	AIN3	EPIOS12	NA	EPIOS10	—
5	SSI0Tx	CCP0	EPIOS3	EPIOS28	AIN2	EPIOS15	NA	EPIOS11	EPIOS29
6	PWM0	VREFA	EPIOS4	Fault0	AIN1	NA	NA	PWM4	CCP1
7	PWM1	NMI	EPIOS5	EPIOS30	AIN0	NA	EPIOS31	PWM5	—

4.8 Example 8: LM3S9B92

Example 8 uses the LM3S9B92 device with the modules and signals shown in Table 16.

Table 16. Example 8 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
EPI interface to Host Bus	EPIOS[31:0]	
UART	U0Rx, U0Tx, U1Rx, U1Tx	

Table 16. Example 8 Module and Signal List (continued)

Module	Signals	Notes
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
I ² S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0]	PE[7:4] used as analog functions.
Four timers, one CCP input	CCP0	No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: I2S0RXSCK (PD0), I2S0RXWS (PD1), EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port F: I2S0TXMCLK (PF1), LED1 (PF2), LED0 (PF3), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: I2S0RXSD (PD4), I2S0RXMCLK (PD5), EPI0S29 (PD6)
- Port F: I2S0TXSD (PF0)
- Port J: EPI0S19 (PJ3), EPI0S28 (PJ4), EPI0S30 (PJ6)

Step 3: Assign signals with three available pin assignments:

- Port B: I2S0TXSCK (PB6)
- Port D: I2S0TXWS (PD7)

Step 4: Assign signals with four available pin assignments:

- Port A: I2C1SCL (PA6), I2C1SDA (PA7)

Step 5: Assign signals with five available pin assignments:

- Port A: PWM0 (PA6), PWM1 (PA7)
- Port B: IDX0 (PB4)
- Port E: PhB0 (PE3)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)

Step 7: Assign signals with seven available pin assignments:

This configuration does not use any of the pins with seven possible pin assignments.

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

On the LM3S9B92 microcontroller, no signals have nine possible pin assignments.

Step 9: Assign signals with 10 available pin assignments:

- Port J: CCP0 (PJ7)

Table 17 shows the final pin assignments for Example 8. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 17. Final Pin Assignments for Example 8

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	I2S0RXSCK	EPI0S8	I2S0TXSD	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	U1Tx	TMS/SWDIO	I2S0RXSWS	EPI0S9	I2S0TXMCLK	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	LED1	NA	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	LED0	NA	EPI0S0	EPI0S19
4	SSI0Rx	EPI0S23	EPI0S2	I2S0RXSD	AIN3	EPI0S12	NA	EPI0S10	EPI0S28
5	SSI0Tx	EPI0S22	EPI0S3	I2S0RXMCLK	AIN2	EPI0S15	NA	EPI0S11	—
6	I2C1SCL	I2S0TXSCK	EPI0S4	EPI0S29	AIN1	NA	NA	EPI0S26	EPI0S30
7	I2C1SDA	NMI	EPI0S5	I2S0TXWS	AIN0	NA	EPI0S31	EPI0S27	CCP0

4.9 Example 9: LM3S9B92

Example 9 uses the LM3S9B92 device with the modules and signals shown in Table 18.

Table 18. Example 9 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
USB Host	USB0PFLT, USB0EPEN	
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U2Rx, U2Tx	
I ² C	I2C0SCL, I2C1SDA I2C0SDA, I2C1SCL,	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
I ² S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0]	PE[7:4] used as analog functions.
Four timers, seven CCP inputs	CCP0, CCP1, CCP2, CCP4, CCP5, CCP6, CCP7	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)
- Port D: I2S0RXSCK (PD0), I2S0RXWS (PD1)
- Port F: I2S0TXMCLK (PF1), LED1 (PF2), LED0 (PF3)

Step 2: Assign signals with two available pin assignments:

- Port D: I2S0RXSD (PD4), I2S0RXMCLK (PD5)
- Port F: I2S0TXSD (PF0)

Step 3: Assign signals with three available pin assignments:

- Port B: I2S0TXSCK (PB6)
- Port D: I2S0TXWS (PD7)
- Port E: SSI1Clk (PE0), SSI1Fss (PE1), SSI1Rx (PE2), SSI1Tx (PE3)

Step 4: Assign signals with four available pin assignments:

- Port A: CAN0Rx (PA6), CAN0Tx (PA7)
- Port G: U2Rx (PG0), U2Tx (PG1)
- Port J: I2C1SCL (PJ0), I2C1SDA (PJ1)

Step 5: Assign signals with five available pin assignments:

- Port C: USB0EPEN (PC5)
- Port D: CCP7 (PD3)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB4), U1Tx (PB5)
- Port D: CCP6 (PD2)
- Port G: CCP5 (PG7)
- Port J: CCP4 (PJ4)

Step 7: Assign signals with seven available pin assignments:

- Port C: USB0PFLT (PC6)

Step 8: Assign signals with eight available pin assignments:

- Port J: CCP1 (PJ6)

On the LM3S9B92 microcontroller, no signals have nine possible pin assignments.

Step 9: Assign signals with 10 available pin assignments:

- Port J: CCP2 (PJ5), CCP0 (PJ7)

Table 19 shows the final pin assignments for Example 9. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 19. Final Pin Assignments for Example 9

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	—	TCK/SWCLK	I2S0RXSCK	SSI1Clk	I2S0TXSD	U2Rx	—	I2C1SCL
1	U0Tx	—	TMS/SWDIO	I2S0RXSWS	SSI1Fss	I2S0TXMCLK	U2Tx	—	I2C1SDA
2	SSI0Clk	I2C0SCL	TDI	CCP6	SSI1Rx	LED1	NA	—	—
3	SSI0Fss	I2C0SDA	TDO/SWO	CCP7	SSI1Tx	LED0	NA	—	—
4	SSI0Rx	U1Rx	—	I2S0RXSD	AIN3	—	NA	—	CCP4
5	SSI0Tx	U1Tx	USB0EPEN	I2S0RXMCLK	AIN2	—	NA	—	CCP2
6	CAN0Rx	I2S0TXSCK	USB0PFLT	—	AIN1	NA	NA	—	CCP1
7	CAN0Tx	NMI	—	I2S0TXWS	AIN0	NA	CCP5	—	CCP0

4.10 Example 10: LM3S9B92

Example 10 uses the LM3S9B92 device with the modules and signals shown in Table 20.

Table 20. Example 10 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
EPI interface in general-purpose mode	EPI0S[31:0]	
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, Fault0	
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers, four CCP inputs	CCP0, CCP1, CCP2, CCP3	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port F: LED1 (PF2), LED0 (PF3), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: EPI0S30 (PD7)
- Port J: EPI0S19 (PJ3), EPI0S28 (PJ4), EPI0S29 (PJ5)

Step 3: Assign signals with three available pin assignments:

This configuration does not use any of the pins with three possible pin assignments.

Step 4: Assign signals with four available pin assignments:

- Port B: PWM2 (PB0), PWM3 (PB1)
- Port D: CAN0Rx (PD0), CAN0Tx (PD1)

Step 5: Assign signals with five available pin assignments:

- Port F: PWM0 (PF0), PWM1 (PF1)

Step 6: Assign signals with six available pin assignments:

This configuration does not use any of the pins with six possible pin assignments.

Step 7: Assign signals with seven available pin assignments:

- Port D: Fault0 (PD6)

Step 8: Assign signals with eight available pin assignments:

- Port A: PWM4 (PA6), PWM5 (PA7)
- Port D: CCP3 (PD4)
- Port J: CCP1 (PJ6)

On the LM3S9B92 microcontroller, no signals have nine possible pin assignments.

Step 9: Assign signals with 10 available pin assignments:

- Port D: CCP2 (PD5)
- Port J: CCP0 (PJ7)

Table 21 shows the final pin assignments for Example 10. **NA** appears in a column when a pin is not available on the microcontroller. — appears in a column when a pin is not used for an analog or alternate digital function.

Table 21. Final Pin Assignments for Example 10

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	PWM2	TCK/SWCLK	CAN0Rx	EPI0S8	PWM0	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	PWM3	TMS/SWDIO	CAN0Tx	EPI0S9	PWM1	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	LED1	NA	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	LED0	NA	EPI0S0	EPI0S19
4	SSI0Rx	EPI0S23	EPI0S2	CCP3	AIN3	EPI0S12	NA	EPI0S10	EPI0S28
5	SSI0Tx	EPI0S22	EPI0S3	CCP2	AIN2	EPI0S15	NA	EPI0S11	EPI0S29
6	PWM4	VREFA	EPI0S4	Fault0	AIN1	NA	NA	EPI0S26	CCP1
7	PWM5	NMI	EPI0S5	EPI0S30	AIN0	NA	EPI0S31	EPI0S27	CCP0

4.11 Example 11: LM3S9B92

Example 11 uses the LM3S9B92 device with the modules and signals shown in Table 22.

Table 22. Example 11 Module and Signal List

Module	Signals	Notes
Ethernet	LED0, LED1	Remaining signals have fixed locations.
EPI interface in Host-Bus 8 FIFO mode	EPI0S31, EPI0S[29:26], EPI0S[7:0]	

Table 22. Example 11 Module and Signal List (continued)

Module	Signals	Notes
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, Fault0	
QEI	PhA0, PhB0, IDX0	
CAN	CAN0Rx, CAN0Tx, CAN1Rx, CAN1Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U2Rx, U2Tx	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPIOS2 (PC4), EPIOS3 (PC5), EPIOS4 (PC6), EPIOS5 (PC7)
- Port F: CAN1Rx (PF0), CAN1Tx (PF1), LED1 (PF2), LED0 (PF3)
- Port G: EPIOS31 (PG7)
- Port H: EPIOS6 (PH0), EPIOS7 (PH1), EPIOS1 (PH2), EPIOS0 (PH3), EPIOS26 (PH6), EPIOS27 (PH7)
- Port J: EPIOS16 (PJ0), EPIOS17 (PJ1), EPIOS18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port A: PWM6 (PA4)
- Port D: EPIOS28 (PD5)
- Port J: EPIOS29 (PJ5)

Step 3: Assign signals with three available pin assignments:

- Port A: PWM7 (PA5)
- Port E: PhA0 (PE2)

Step 4: Assign signals with four available pin assignments:

- Port A: I2C1SCL (PA6), I2C1SDA (PA7)
- Port B: CAN0Rx (PB4), CAN0Tx (PB5)
- Port D: U2Rx (PD0), U2Tx (PD1), PWM2 (PD2), PWM3 (PD3)

Step 5: Assign signals with five available pin assignments:

- Port D: IDX0 (PD7)
- Port E: PhB0 (PE3)
- Port G: PWM0 (PG0), PWM1 (PG1)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)

Step 7: Assign signals with seven available pin assignments:

- Port D: Fault0 (PD6)

Step 8: Assign signals with eight available pin assignments:

- Port A: PWM4 (PA2), PWM5 (PA3)

On the LM3S9B92 microcontroller, no signals have nine possible pin assignments.

Step 9: Assign signals with 10 available pin assignments:

This configuration does not use any of the pins with 10 possible pin assignments.

Table 23 shows the final pin assignments for Example 11. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 23. Final Pin Assignments for Example 11

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	U2Rx	—	CAN1Rx	PWM0	EPI0S6	—
1	U0Tx	U1Tx	TMS/SWDIO	U2Tx	—	CAN1Tx	PWM1	EPI0S7	—
2	PWM4	I2C0SCL	TDI	PWM2	PhA0	LED1	NA	EPI0S1	—
3	PWM5	I2C0SDA	TDO/SWO	PWM3	PhB0	LED0	NA	EPI0S0	—
4	PWM6	CAN0Rx	EPI0S2	—	AIN3	—	NA	—	—
5	PWM7	CAN0Tx	EPI0S3	EPI0S28	AIN2	—	NA	—	EPI0S29
6	I2C1SCL	VREFA	EPI0S4	Fault0	AIN1	NA	NA	EPI0S26	—
7	I2C1SDA	NMI	EPI0S5	IDX0	AIN0	NA	EPI0S31	EPI0S27	—

4.12 Example 12: LM3S2B93

Example 12 uses the LM3S2B93 device with the modules and signals shown in [Table 24](#).

Table 24. Example 12 Module and Signal List

Module	Signals	Notes
Hibernate		Signals have fixed locations.
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, Fault0, Fault1, Fault2, Fault3	
QE1	PhA0, PhB0, IDX0, PhA1, PhB1, IDX1	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
ADC	AIN[15:0]	PB[5:4], PD[7:0], PE[7:2], and PB6 used as analog functions.
Four timers, one CCP input	CCP0	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)

Step 2: Assign signals with two available pin assignments:

- Port G: PhA1 (PG6)
- Port H: Fault3 (PH2)

Step 3: Assign signals with three available pin assignments:

- Port C: Fault2 (PC5)
- Port F: SSI1Clk (PF2), SSI1Fss (PF3), SSI1Rx (PF4), SSI1Tx (PF5)
- Port G: IDX1 (PG2), PhB1 (PG7)

Step 4: Assign signals with four available pin assignments:

- Port A: I2C1SCL (PA6), I2C1SDA (PA7)
- Port C: PWM6 (PC4), PWM7 (PC6)
- Port F: PhA0 (PF6)
- Port H: PWM2 (PH0), PWM3 (PH1)

Step 5: Assign signals with five available pin assignments:

- Port B: Fault1 (PB6)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)
- Port C: PhB0 (PC7)
- Port F: PWM0 (PF0), PWM1 (PF1)
- Port G: IDX0 (PG5)

Step 7: Assign signals with seven available pin assignments:

This configuration does not use the pin with seven possible pin assignments.

Step 8: Assign signals with eight available pin assignments:

- Port G: PWM4 (PG0), PWM5 (PG1)

Step 9: Assign signals with nine available pin assignments:

- Port E: Fault0 (PE1)
- Port J: CCP0 (PJ2)

Table 25 shows the final pin assignments for Example 12. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 25. Final Pin Assignments for Example 12

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	AIN15	—	PWM0	PWM4	PWM2	—
1	U0Tx	U1Tx	TMS/SWDIO	AIN14	Fault0	PWM1	PWM5	PWM3	—
2	SSI0Clk	I2C0SCL	TDI	AIN13	AIN9	SSI1Clk	IDX1	Fault3	CCP0
3	SSI0Fss	I2C0SDA	TDO/SWO	AIN12	AIN8	SSI1Fss	—	—	NA
4	SSI0Rx	AIN10	PWM6	AIN7	AIN3	SSI1Rx	—	—	NA
5	SSI0Tx	AIN11	Fault2	AIN6	AIN2	SSI1Tx	IDX0	—	NA
6	I2C1SCL	Fault1	PWM7	AIN5	AIN1	PhA0	PhA1	—	NA
7	I2C1SDA	NMI	PhB0	AIN4	AIN0	Fault1	PhB1	—	NA

4.13 Example 13: LM3S2B93

Example 13 uses the LM3S2B93 device with the modules and signals shown in [Table 26](#).

Table 26. Example 13 Module and Signal List

Module	Signals	Notes
Hibernate		Signals have fixed locations.
EPI interface to SDRAM	EPIOS[31:28], EPIOS[19:0]	
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U2Rx, U2Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPIOS2 (PC4), EPIOS3 (PC5), EPIOS4 (PC6), EPIOS5 (PC7)
- Port D: EPIOS19 (PD4), EPIOS28 (PD5), EPIOS29 (PD6), EPIOS30 (PD7)
- Port E: EPIOS8 (PE0), EPIOS9 (PE1)
- Port G: EPIOS13 (PG0), EPIOS14 (PG1), EPIOS31 (PG7)
- Port H: EPIOS6 (PH0), EPIOS7 (PH1), EPIOS1 (PH2), EPIOS0 (PH3), EPIOS10 (PH4), EPIOS11 (PH5)
- Port J: EPIOS16 (PJ0), EPIOS17 (PJ1), EPIOS18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port F: EPIOS12 (PF7)
- Port G: EPIOS15 (PG4)

Step 3: Assign signals with three available pin assignments:

- Port F: SSI1Clk (PF2), SSI1Fss (PF3), SSI1Rx (PF4), SSI1Tx (PF5)

Step 4: Assign signals with four available pin assignments:

- Port A: CAN0Rx (PA6), CAN0Tx (PA7)
- Port D: U2Rx (PD0), U2Tx (PD1)

Step 5: Assign signals with five available pin assignments:

This configuration does not use any of the pins with five possible pin assignments.

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)

Step 7: Assign signals with seven available pin assignments:

This configuration does not use the pin with seven possible pin assignments.

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with nine available pin assignments:

This configuration does not use any of the pins with nine possible pin assignments.

Table 27 shows the final pin assignments for Example 13. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 27. Final Pin Assignments for Example 13

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	U2Rx	EPI0S8	—	EPI0S15	EPI0S6	EPI0S16
1	U0Tx	U1Tx	TMS/SWDIO	U2Tx	EPI0S9	—	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	—	—	SSI1Clk	—	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	—	—	SSI1Fss	—	EPI0S0	NA
4	SSI0Rx	—	EPI0S2	EPI0S19	AIN3	SSI1Rx	EPI0S15	EPI0S10	NA
5	SSI0Tx	—	EPI0S3	EPI0S28	AIN2	SSI1Tx	—	EPI0S11	NA
6	CAN0Rx	VREFA	EPI0S4	EPI0S29	AIN1	—	—	—	NA
7	CAN0Tx	NMI	EPI0S5	EPI0S30	AIN0	EPI0S12	EPI0S31	—	NA

4.14 Example 14: LM3S2B93

Example 14 uses the LM3S2B93 device with the modules and signals shown in Table 28.

Table 28. Example 14 Module and Signal List

Module	Signals	Notes
Hibernate		Signals have fixed locations.
EPI interface to HosPWMt-Bus 8 FIFO mode	EPI0S31, EPI0S[29:26], EPI0S[7:0]	
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, Fault0, Fault1	
QEI	PhA0, PhB0, IDX0, PhA1, PhB1, IDX1	
CAN	CAN0Rx, CAN0Tx, CAN1Rx, CAN1Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1)
- Port B: NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S28 (PD5), EPI0S29 (PD6)
- Port F: CAN1Rx (PF0), CAN1Tx (PF1)
- Port G: EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port G: PhA1 (PG6)

Step 3: Assign signals with three available pin assignments:

- Port E: PhB1 (PE2)
- Port G: IDX1 (PG2)

Step 4: Assign signals with four available pin assignments:

- Port A: PWM6 (PA4), PWM7 (PA5)
- Port B: CAN0Rx (PB4), CAN0Tx (PB5)
- Port D: PhA0 (PD1), PWM2 (PD2), PWM3 (PD3)

Step 5: Assign signals with five available pin assignments:

- Port F: Fault1 (PF7)

Step 6: Assign signals with six available pin assignments:

- Port A: PWM0 (PA6), PWM1 (PA7)
- Port B: U1Rx (PB0), U1Tx (PB1), IDX0 (PB2)
- Port E: PhB0 (PE3)

Step 7: Assign signals with seven available pin assignments:

This configuration does not use the pin with seven possible pin assignments.

Step 8: Assign signals with eight available pin assignments:

- Port A: PWM4 (PA2), PWM5 (PA3)

Step 9: Assign signals with nine available pin assignments:

- Port B: Fault0 (PB3)

Table 29 shows the final pin assignments for Example 14. **NA** appears in a column when a pin is not available on the microcontroller. — appears in a column when a pin is not used for an analog or alternate digital function.

Table 29. Final Pin Assignments for Example 14

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	—	—	CAN1Rx	—	EPI0S6	—
1	U0Tx	U1Tx	TMS/SWDIO	PhA0	—	CAN1Tx	—	EPI0S7	—
2	PWM4	IDX0	TDI	PWM2	PhB1	—	IDX1	EPI0S1	—
3	PWM5	Fault0	TDO/SWO	PWM3	PhB0	—	—	EPI0S0	NA
4	PWM6	CAN0Rx	EPI0S2	—	AIN3	—	—	—	NA
5	PWM7	CAN0Tx	EPI0S3	EPI0S28	AIN2	—	—	—	NA
6	PWM0	VREFA	EPI0S4	EPI0S29	AIN1	—	PhA1	EPI0S26	NA
7	PWM1	NMI	EPI0S5	—	AIN0	Fault1	EPI0S31	EPI0S27	NA

4.15 Example 15: LM3S2B93

Example 15 uses the LM3S2B93 device with the modules and signals shown in [Table 30](#).

Table 30. Example 15 Module and Signal List

Module	Signals	Notes
Hibernate		Signals have fixed locations.
EPI interface to SDRAM	EPIOS[31:28], EPIOS[19:0]	
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, Fault0, Fault1	
QEI	PhA0, PhB0, IDX0, PhA1, PhB1, IDX1	
CAN	CAN0Rx, CAN0Tx, CAN1Rx, CAN1Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1)
- Port B: NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPIOS2 (PC4), EPIOS3 (PC5), EPIOS4 (PC6), EPIOS5 (PC7)
- Port D: EPIOS19 (PD4), EPIOS28 (PD5), EPIOS29 (PD6), EPIOS30 (PD7)
- Port E: EPIOS8 (PE0), EPIOS9 (PE1)
- Port F: CAN1Rx (PF0), CAN1Tx (PF1)
- Port G: EPIOS13 (PG0), EPIOS14 (PG1), EPIOS31 (PG7)
- Port H: EPIOS6 (PH0), EPIOS7 (PH1), EPIOS1 (PH2), EPIOS0 (PH3), EPIOS10 (PH4), EPIOS11 (PH5)
- Port J: EPIOS16 (PJ0), EPIOS17 (PJ1), EPIOS18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port F: EPI0S12 (PF4), EPI0S15 (PF5)
- Port G: PhA1 (PG6)

Step 3: Assign signals with three available pin assignments:

- Port E: PhB1 (PE2)
- Port G: IDX1 (PG2)

Step 4: Assign signals with four available pin assignments:

- Port A: PWM6 (PA4), PWM7 (PA5)
- Port B: CAN0Rx (PB4), CAN0Tx (PB5)
- Port D: PhA0 (PD1), PWM2 (PD2), PWM3 (PD3)

Step 5: Assign signals with five available pin assignments:

- Port F: Fault1 (PF7)

Step 6: Assign signals with six available pin assignments:

- Port A: PWM0 (PA6), PWM1 (PA7)
- Port B: U1Rx (PB0), U1Tx (PB1), IDX0 (PB2)
- Port E: PhB0 (PE3)

Step 7: Assign signals with seven available pin assignments:

This configuration does not use the pin with seven possible pin assignments.

Step 8: Assign signals with eight available pin assignments:

- Port A: PWM4 (PA2), PWM5 (PA3)

Step 9: Assign signals with nine available pin assignments:

- Port B: Fault0 (PB3)

[Table 31](#) shows the final pin assignments for Example 15. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 31. Final Pin Assignments for Example 15

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	—	EPI0S8	CAN1Rx	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	U1Tx	TMS/SWDIO	PhA0	EPI0S9	CAN1Tx	EPI0S14	EPI0S7	EPI0S17
2	PWM4	IDX0	TDI	PWM2	PhB1	—	IDX1	EPI0S1	EPI0S18
3	PWM5	Fault0	TDO/SWO	PWM3	PhB0	—	—	EPI0S0	NA
4	PWM6	CAN0Rx	EPI0S2	EPI0S19	AIN3	EPI0S12	—	EPI0S10	NA
5	PWM7	CAN0Tx	EPI0S3	EPI0S28	AIN2	EPI0S15	—	EPI0S11	NA
6	PWM0	VREFA	EPI0S4	EPI0S29	AIN1	—	PhA1	—	NA
7	PWM1	NMI	EPI0S5	EPI0S30	AIN0	Fault1	EPI0S31	—	NA

4.16 Example 16: LM3S5B91

Example 16 uses the LM3S5B91 device with the modules and signals shown in [Table 32](#).

Table 32. Example 16 Module and Signal List

Module	Signals	Notes
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U1CTS, U1DCD, U1DSR, U1DTR, U1RI, U1RTS, U2Rx, U2Tx	
I ² C	I2C0SCL, I2C0SDA, I2C1SCL, I2C1SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx, SSI1Clk, SSI1Fss, SSI1Rx, SSI1Tx	
I ² S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0]	PE[7:4] used as analog functions.
Four timers, eight CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5, CCP6, CCP7	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3)

Step 2: Assign signals with two available pin assignments:

- Port D: I2S0RXSCK (PD0)
- Port F: I2S0TXSD (PF0), I2S0TXMCLK (PF6)
- Port G: I2S0RXWS (PG6)
- Port J: U1DSR (PJ5)

Step 3: Assign signals with three available pin assignments:

- Port B: I2S0TXSCK (PB6)
- Port D: U1RI (PD4), I2S0TXWS (PD7)
- Port E: SSI1Clk (PE0), SSI1Fss (PE1), SSI1Rx (PE2), SSI1Tx (PE3)
- Port F: U1RTS (PF1)
- Port G: I2S0RXSD (PG2), I2S0RXMCLK (PG3), U1DTR (PG5)

Step 4: Assign signals with four available pin assignments:

- Port A: U1CTS (PA6), U1DCD (PA7)
- Port B: CAN0Rx (PB4), CAN0Tx (PB5)
- Port D: U2Tx (PD1), U2Rx (PD5)
- Port G: I2C1SCL (PG0), I2C1SDA (PG1)

Step 5: Assign signals with five available pin assignments:

- Port D: CCP7 (PD3)

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)
- Port D: CCP6 (PD2)

Step 7: Assign signals with seven available pin assignments:

- Port C: CCP4 (PC4)
- Port G: CCP5 (PG7)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with nine available pin assignments:

- Port C: CCP1 (PC5), CCP3 (PC6)

Step 10: Assign signals with 10 available pin assignments:

- Port C: CCP0 (PC7)
- Port F: CCP2 (PF5)

Table 33 shows the final pin assignments for Example 16. **NA** appears in a column when a pin is not available on the microcontroller. — appears in a column when a pin is not used for an analog or alternate digital function.

Table 33. Final Pin Assignments for Example 16

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	I2S0RXSCK	SSI1Clk	I2S0TXSD	I2C1SCL	—	—
1	U0Tx	U1Tx	TMS/SWDIO	U2TX	SSI1Fss	U1RTS	I2C1SDA	—	—
2	SSI0Clk	I2C0SCL	TDI	CCP6	SSI1Rx	—	I2S0RXSD	—	—
3	SSI0Fss	I2C0SDA	TDO/SWO	CCP7	SSI1Tx	—	I2S0RXMCLK	—	—
4	SSI0Rx	CAN0Rx	CCP4	U1R1	AIN3	—	—	—	—
5	SSI0Tx	CAN0Tx	CCP1	U2Rx	AIN2	CCP2	U1DTR	—	U1SDR
6	U1CTS	I2S0TXSCK	CCP3	—	AIN1	I2S0TXMCLK	I2S0RXWS	—	—
7	U1DCD	NMI	CCP0	I2S0TXWS	AIN0	—	CCP5	—	—

4.17 Example 17: LM3S5B91

Example 17 uses the LM3S5B91 device with the modules and signals shown in [Table 34](#).

Table 34. Example 17 Module and Signal List

Module	Signals	Notes
EPI interface to general-purpose mode	EPI0S[31:0]	
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx, U1Rx, U1Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
I ² S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[3:0]	PE[7:4] used as analog functions.
Four timers, six CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: I2S0RXSCK (PD0), I2S0RXWS (PD1), EPI0S29 (PD6)
- Port E: I2S0TXSD (PE5)
- Port F: I2S0TXMCLK (PF1), EPI0S12 (PF4), EPI0S15 (PF5)
- Port J: EPI0S19 (PJ3), EPI0S28 (PJ4), EPI0S30 (PJ6)

Step 3: Assign signals with three available pin assignments:

- Port B: I2S0TXSCK (PB6)
- Port D: I2S0RXSD (PD4), I2S0RXMCLK (PD5), I2S0TXWS (PD7)

Step 4: Assign signals with four available pin assignments:

- Port A: CAN0Rx (PA6), CAN0Tx (PA7)

Step 5: Assign signals with five available pin assignments:

This configuration does not use any of the pins with five possible pin assignments.

Step 6: Assign signals with six available pin assignments:

- Port B: U1Rx (PB0), U1Tx (PB1)

Step 7: Assign signals with seven available pin assignments:

- Port F: CCP4 (PF7)
- Port G: CCP5 (PG5)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with nine available pin assignments:

- Port F: CCP1 (PF6)
- Port G: CCP3 (PG4)

Step 10: Assign signals with 10 available pin assignments:

- Port E: CCP2 (PE4)
- Port J: CCP0 (PJ7)

Table 35 shows the final pin assignments for Example 17. **NA** appears in a column when a pin is not available on the microcontroller. — appears in a column when a pin is not used for an analog or alternate digital function.

Table 35. Final Pin Assignments for Example 17

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	U1Rx	TCK/SWCLK	I2S0RXSCK	EPI0S8	—	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	U1Tx	TMS/SWDIO	I2S0RXWS	EPI0S9	I2S0TXMCLK	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	—	—	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	—	—	EPI0S0	EPI0S19
4	SSI0Rx	EPI0S23	EPI0S2	I2S0RXSD	CCP2	EPI0S12	CCP3	EPI0S10	EPI0S28
5	SSI0Tx	EPI0S22	EPI0S3	I2S0RXMCLK	I2S0TXSD	EPI0S15	CCP5	EPI0S11	—
6	CAN0Rx	I2S0TXSCK	EPI0S4	EPI0S29	AIN1	CCP1	—	EPI0S26	EPI0S30
7	CAN0Tx	NMI	EPI0S5	I2S0TXWS	AIN0	CCP4	EPI0S31	EPI0S27	CCP0

4.18 Example 18: LM3S5B91

Example 18 uses the LM3S5B91 device with the modules and signals shown in Table 36.

Table 36. Example 18 Module and Signal List

Module	Signals	Notes
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
EPI interface to Host-Bus mode	EPI0S[31:0]	
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
I ² S	I2S0RXMCLK, I2S0RXSCK, I2S0RXSD, I2S0RXWS, I2S0TXMCLK, I2S0TXSCK, I2S0TXSD, I2S0TXWS	
ADC	AIN[1:0]	PE[7:6] used as analog functions.
Four timers, five CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: EPI0S29 (PD6)
- Port E: I2S0TXSD (PE5)
- Port F: I2S0TXMCLK (PF1), EPI0S12 (PF4), EPI0S15 (PF5)
- Port G: I2S0RXSCK (PG5), I2S0RXWS (PG6)
- Port J: EPI0S19 (PJ3), EPI0S28 (PJ4), EPI0S30 (PJ6)

Step 3: Assign signals with three available pin assignments:

- Port B: I2S0TXSCK (PB6)
- Port D: I2S0RXSD (PD4), I2S0RXMCLK (PD5), I2S0TXWS (PD7)

Step 4: Assign signals with four available pin assignments:

- Port D: CAN0Rx (PD0), CAN0Tx (PD1)

Step 5: Assign signals with five available pin assignments:

- Port A: USB0EPEN (PA6)

Step 6: Assign signals with six available pin assignments:

This configuration does not use any of the pins with six possible pin assignments.

Step 7: Assign signals with seven available pin assignments:

- Port A: USB0PFLT (PA7)
- Port F: CCP4 (PF7)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with nine available pin assignments:

- Port F: CCP1 (PF6)
- Port G: CCP3 (PG4)

Step 10: Assign signals with 10 available pin assignments:

- Port E: CCP2 (PE4)
- Port J: CCP0 (PJ7)

Table 37 shows the final pin assignments for Example 18. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 37. Final Pin Assignments for Example 18

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	CAN0Rx	EPI0S8	—	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/SWDIO	CAN0Tx	EPI0S9	I2S0TXMCLK	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	—	—	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	—	—	EPI0S0	EPI0S19
4	SSI0Rx	EPI0S23	EPI0S2	I2S0RXSD	CCP2	EPI0S12	CCP3	EPI0S10	EPI0S28
5	SSI0Tx	EPI0S22	EPI0S3	I2S0RXMCLK	I2S0TXSD	EPI0S15	I2S0RXSCK	EPI0S11	—
6	USB0EPEN	I2S0TXSCK	EPI0S4	EPI0S29	AIN1	CCP1	I2S0RXWS	EPI0S26	EPI0S30
7	USB0PFLT	NMI	EPI0S5	I2S0TXWS	AIN0	CCP4	EPI0S31	EPI0S27	CCP0

4.19 Example 19: LM3S5B91

Example 19 uses the LM3S5B91 device with the modules and signals shown in Table 38.

Table 38. Example 19 Module and Signal List

Module	Signals	Notes
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
EPI interface to Host-Bus mode	EPI0S[31:0]	
UART	U0Rx, U0Tx, U1Rx, U1Tx, U1CTS, U1DCD, U1DSR, U1DTR, U1RI, U1RTS	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers, six CCP inputs	CCP0, CCP1, CCP2, CCP3, CCP4, CCP5	
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: EPI0S28 (PD5), EPI0S29 (PD6)
- Port F: U1DSR (PF0), EPI0S12 (PF4), EPI0S15 (PF5)
- Port J: EPI0S19 (PJ3), EPI0S30 (PJ6)

Step 3: Assign signals with three available pin assignments:

- Port D: U1R1 (PD4), U1DTR (PD7)
- Port F: U1RTS (PF1)

Step 4: Assign signals with four available pin assignments:

- Port A: U1CTS (PA6), U1DCD (PA7)

Step 5: Assign signals with five available pin assignments:

- Port B: USB0EPEN (PB2)

Step 6: Assign signals with six available pin assignments:

- Port D: U1Rx (PD0), U1Tx (PD1)

Step 7: Assign signals with seven available pin assignments:

- Port B: USB0PFLT (PB3)
- Port F: CCP4 (PF7)
- Port G: CCP5 (PG5)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with nine available pin assignments:

- Port F: CCP1 (PF6)
- Port G: CCP3 (PG4)

Step 10: Assign signals with 10 available pin assignments:

- Port J: CCP2 (PJ5), CCP0 (PJ7)

Table 39 shows the final pin assignments for Example 19. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 39. Final Pin Assignments for Example 19

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	U1Rx	EPI0S8	U1SDR	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/SWDIO	U1Tx	EPI0S9	U1RTS	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	USB0EPEN	TDI	EPI0S20	EPI0S24	—	—	EPI0S1	EPI0S18
3	SSI0Fss	USB0PFLT	TDO/SWO	EPI0S21	EPI0S25	—	—	EPI0S0	EPI0S19
4	SSI0Rx	EPI0S23	EPI0S2	U1R1	AIN3	EPI0S12	CCP3	EPI0S10	—
5	SSI0Tx	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	CCP5	EPI0S11	CCP2
6	U1CTS	VREFA	EPI0S4	EPI0S29	AIN1	CCP1	—	EPI0S26	EPI0S30
7	U1DCD	NMI	EPI0S5	U1DTR	AIN0	CCP4	EPI0S31	EPI0S27	CCP0

4.20 Example 20: LM3S5B91

Example 20 uses the LM3S5B91 device with the modules and signals shown in Table 40.

Table 40. Example 20 Module and Signal List

Module	Signals	Notes
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
EPI interface to Host-Bus mode	EPI0S[31:0]	
PWM	PWM0, PWM1, PWM2, PWM3, Fault0, Fault1	
QEI	PhA0, PhB0, IDX0	

Table 40. Example 20 Module and Signal List (continued)

Module	Signals	Notes
CAN	CAN0Rx, CAN0Tx	
UART	U0Rx, U0Tx	
I ² C	I2C0SCL, I2C0SDA	
SSI	SSI0Clk, SSI0Fss, SSI0Rx, SSI0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1), SSI0Clk (PA2), SSI0Fss (PA3), SSI0Rx (PA4), SSI0Tx (PA5)
- Port B: I2C0SCL (PB2), I2C0SDA (PB3), EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: EPI0S19 (PD4), EPI0S28 (PD5)
- Port F: EPI0S12 (PF4), EPI0S15 (PF5)
- Port J: EPI0S29 (PJ5), EPI0S30 (PJ6)

Step 3: Assign signals with three available pin assignments:

This configuration does not use any of the pins with three possible pin assignments.

Step 4: Assign signals with four available pin assignments:

- Port D: CAN0Rx (PD0), CAN0Tx (PD1)
- Port F: PWM2 (PF2), PWM3 (PF3), PhA0 (PF6)

Step 5: Assign signals with five available pin assignments:

- Port A: USB0EPEN (PA6)
- Port F: Fault1 (PF7)

Step 6: Assign signals with six available pin assignments:

- Port D: IDX0 (PD7)
- Port F: PhB0 (PF0)
- Port G: PWM0 (PG2), PWM1 (PG3)

Step 7: Assign signals with seven available pin assignments:

- Port A: USB0PFLT (PA7)

Step 8: Assign signals with eight available pin assignments:

This configuration does not use any of the pins with eight possible pin assignments.

Step 9: Assign signals with nine available pin assignments:

- Port D: Fault0 (PD6)

Step 10: Assign signals with 10 available pin assignments:

This configuration does not use any of the pins with 10 possible pin assignments.

Table 41 shows the final pin assignments for Example 20. **NA** appears in a column when a pin is not available on the microcontroller. **—** appears in a column when a pin is not used for an analog or alternate digital function.

Table 41. Final Pin Assignments for Example 20

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	CAN0Rx	EPI0S8	PhB0	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/SWDIO	CAN0Tx	EPI0S9	—	EPI0S14	EPI0S7	EPI0S17
2	SSI0Clk	I2C0SCL	TDI	EPI0S20	EPI0S24	PWM2	PWM0	EPI0S1	EPI0S18
3	SSI0Fss	I2C0SDA	TDO/SWO	EPI0S21	EPI0S25	PWM3	PWM1	EPI0S0	—
4	SSI0Rx	EPI0S23	EPI0S2	EPI0S19	AIN3	EPI0S12	—	EPI0S10	—
5	SSI0Tx	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	—	EPI0S11	EPI0S29
6	USB0EPEN	VREFA	EPI0S4	Fault0	AIN1	PhA0	—	EPI0S26	EPI0S30
7	USB0PFLT	NMI	EPI0S5	IDX0	AIN0	Fault1	EPI0S31	EPI0S27	—

4.21 Example 21: LM3S5B91

Example 21 uses the LM3S5B91 device with the modules and signals shown in **Table 42**.

Table 42. Example 21 Module and Signal List

Module	Signals	Notes
USB OTG	USB0PFLT, USB0EPEN	USB0ID and USB0VBUS use PB0 and PB1 as analog functions; remaining signals have fixed locations.
EPI interface to general-purpose mode	EPI0S[31:0]	
PWM	PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7 Fault0	
QEI	PhA0, PhB0, IDX0	
CAN	CAN0Rx, CAN0Tx	
ADC	AIN[3:0], VREFA	PE[7:4] and PB6 used as analog functions.
Four timers		No signals.
System control	NMI	
JTAG/SWD	TCK/SWCLK, TMS/SWDIO, TDI, TDO/SWO	

Step 1: Assign signals with only one available pin assignment:

- Port A: U0Rx (PA0), U0Tx (PA1)
- Port B: EPI0S23 (PB4), EPI0S22 (PB5), NMI (PB7)
- Port C: TCK/SWCLK (PC0), TMS/SWDIO (PC1), TDI (PC2), TDO/SWO (PC3), EPI0S2 (PC4), EPI0S3 (PC5), EPI0S4 (PC6), EPI0S5 (PC7)
- Port D: EPI0S20 (PD2), EPI0S21 (PD3)
- Port E: EPI0S8 (PE0), EPI0S9 (PE1), EPI0S24 (PE2), EPI0S25 (PE3)
- Port G: EPI0S13 (PG0), EPI0S14 (PG1), EPI0S31 (PG7)
- Port H: EPI0S6 (PH0), EPI0S7 (PH1), EPI0S1 (PH2), EPI0S0 (PH3), EPI0S10 (PH4), EPI0S11 (PH5), EPI0S26 (PH6), EPI0S27 (PH7)
- Port J: EPI0S16 (PJ0), EPI0S17 (PJ1), EPI0S18 (PJ2)

Step 2: Assign signals with two available pin assignments:

- Port D: EPI0S19 (PD4), EPI0S28 (PD5), EPI0S29 (PD6), EPI0S30 (PD7)
- Port F: EPI0S12 (PF4), EPI0S15 (PF5)

Step 3: Assign signals with three available pin assignments:

This configuration does not use any of the pins with three possible pin assignments.

Step 4: Assign signals with four available pin assignments:

- Port D: CAN0Rx (PD0), CAN0Tx (PD1)
- Port F: PWM2 (PF2), PWM3 (PF3), PhA0 (PF6)

Step 5: Assign signals with five available pin assignments:

- Port A: USB0EPEN (PA6)

Step 6: Assign signals with six available pin assignments:

- Port B: IDX0 (PB2)
- Port F: PhB0 (PF0)
- Port G: PWM0 (PG2), PWM1 (PG3)

Step 7: Assign signals with seven available pin assignments:

- Port A: PWM4 (PA2), PWM5 (PA3), USB0PFLT (PA7)

Step 8: Assign signals with eight available pin assignments:

- Port A: PWM6 (PA4), PWM7 (PA5)

Step 9: Assign signals with nine available pin assignments:

- Port B: Fault0 (PB3)

Step 10: Assign signals with 10 available pin assignments:

This configuration does not use any of the pins with 10 possible pin assignments.

[Table 43](#) shows the final pin assignments for Example 21. **NA** appears in a column when a pin is not available on the microcontroller. — appears in a column when a pin is not used for an analog or alternate digital function.

Table 43. Final Pin Assignments for Example 21

Pin	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H	Port J
0	U0Rx	USB0ID	TCK/SWCLK	CAN0Rx	EPI0S8	PhB0	EPI0S13	EPI0S6	EPI0S16
1	U0Tx	USB0VBUS	TMS/SWDIO	CAN0Tx	EPI0S9	—	EPI0S14	EPI0S7	EPI0S17
2	PWM4	IDX0	TDI	EPI0S20	EPI0S24	PWM2	PWM0	EPI0S1	EPI0S18
3	PWM5	Fault0	TDO/SWO	EPI0S21	EPI0S25	PWM3	PWM1	EPI0S0	—
4	PWM6	EPI0S23	EPI0S2	EPI0S19	AIN3	EPI0S12	—	EPI0S10	—
5	PWM7	EPI0S22	EPI0S3	EPI0S28	AIN2	EPI0S15	—	EPI0S11	—
6	USB0EPEN	VREFA	EPI0S4	EPI0S29	AIN1	PhA0	—	EPI0S26	—
7	USB0PFLT	NMI	EPI0S5	EPI0S30	AIN0	—	EPI0S31	EPI0S27	—

5 Conclusion

The pin muxing capability of many Stellaris microcontrollers is highly flexible and easy to implement using the functions provided by the StellarisWare® Peripheral Driver Library. A system designer can choose the most efficient pin configuration targeted for specific system requirements.

6 References

- Stellaris LM3S9B92 Microcontroller Data Sheet ([SPMS180](#))
- Stellaris LM3S9B90 Microcontroller Data Sheet ([SPMS179](#))
- Stellaris LM3S5B91 Microcontroller Data Sheet ([SPMS098](#))
- Stellaris LM3S2B93 Microcontroller Data Sheet ([SPMS063](#))
- StellarisWare Driver Library. Available for download at www.ti.com/tool/sw-drl.
- Stellaris Peripheral Driver Library User's Manual, publication SW-DRL-UG (literature number [SPMU019](#))

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