TMS320C6000 System Clock Circuit Example

David Bell
Scott Chen

Digital Signal Processing Solutions

ABSTRACT

This document describes how to provide the Texas Instruments TMS320C6000™ DSP with a system clock. All of the clocks internal to the C6000™ are generated from a single source through the CLKIN pin. This source clock for the device is an external signal that, depending on the clock mode, either drives the on-chip Phase-Locked Loop (PLL) circuit, which multiplies the source clock in frequency to generate the internal CPU clock, or bypasses the PLL to become the internal clock. The source clock may be derived from either an oscillator chip or a clock synthesizer circuit and should be generated from a 3.3V source.

This document further describes how to provide the EMIF on Texas Instruments (TI) TMS320C6000 DSP through ECLKIN.

Contents

List of Figures

List of Tables

1 Design Problem

How do I provide the TMS320C6000 with a system clock?

2 Solution

2.1 Providing a System Clock Through CLKIN

2.1.1 PLL Modes

The internal CPU clock of the C6000 is generated from a single source through the CLKIN pin. This source clock for the device is an external signal that, depending on the clock mode, either drives the on-chip Phase-Locked Loop (PLL) circuit, which multiplies the source clock in frequency to generate the internal CPU clock, or bypasses the PLL to become the internal clock. The source clock may be derived from either an oscillator chip or a clock synthesizer circuit and should be generated from a 3.3V source. Ensure that all clock traces are as short as possible to minimize the distortion of the clock signal.

Each C6000 device has different PLL modes for the device operation. Table 1 is a summary of existing devices:

Table 1. PLL Mode for C6000 Devices

		CLKMODE (CLKIN Frequency Multiplier)								
Device	**Package**	**x1**	**x4**	**x6**	**x7**	**x8**	**x9**	**x10**	**x11**	**x12**
C6201	GJL / GJC	√	√							
C6202	GJL / GLS	√	√							
C6202B	GJL	√	√			√		√		
C6202B	GLS	√	√	√	√	√	√	√	√	
C6203	GJL	√	√			√		√		
C6203	GLS	√	√	√	√	√	√	√	√	
C6204	GLW / GHK	√	√							
C6205	GHK	√	√	√	√	√	√	√	√	
C6701	GJC	√	√							
C6211	GFN	√	√							
C6211B	GFN	√	√							
C6711	GFN	√	√							
C6712	GFN	√	√							
C6414	GLZ	√		√						√
C6415	GLZ	√		√						√
C6416	GLZ	√		√						√

For CLKMODE x1, the PLL is bypassed and all six external PLL components can be removed. For this case, the 3.3-V supply for PLLV must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}. In addition, PLLG and PLLF terminals should be tied together.

2.1.2 PLL Component Selection

Table 2 and Table 3 summarize the PLL component selection for the PLL external circuitry in the TMS320C62x™ (C62x™), TMS320C67x™ (C67x™), and TMS320C64x™ (C64x™) devices. Notice that under some operating conditions, the maximum PLL lock time may vary as much as 150% from the specified typical value. For example, if the typical lock time is specified as 100 μs, the maximum value may be as long as 250 μs.

TMS320C62x, TMS320C67x, TMS320C64x, C62x, C67x and C64x are trademarks of Texas Instruments.

Table 2. PLL Component Selection Table for C62x/C67x

DEVICE	CLKMODE	CLKIN RANGE (MHz)	CLKOUT RANGE (MHz)	CLKOUT2 RANGE (MHz)	R1 (Ω)	C1 (nF)	C2 (pF)	TYPICAL LOCK TIME (μs)
C6201	x4	12.5-50	50-200	25-100	60.4	27	560	75
C6202	x4	32.5-62.5	130-250	65-125	60.4	27	560	75
C6202B	X4	32.5-62.5	130-250	65-125	60.4	27	560	75
	X6	21.7-41.7						
	X7	18.6-35.7						
	X8	16.3-31.3						
	X9	14.4-27.8						
	X10	13-25						
	X11	11.8-22.7						
C6203	X4	32.5-75	130-300	65-150	60.4 (1.x) 45.3 (2.x)	27 (1.x) 47 (2.x)	560 (1.x) 10 (2.x)	75
	X6	21.7-50						
	X7	18.6-42.9						
	X8	16.3-37.5						
	X9	14.4-33.3						
	X10	13-30						
	X11	11.8-27.3						
C6204	X4	32.5-50	130-200	65-100	60.4	27	560	75
C6205	X4	32.5-50	130-200	65-100	60.4	27	560	75
	X6	21.7-33.3						
	X7	18.6-28.6						
	X8	16.3-25						
	X9	14.4-22.2						
	X10	13-20						
	X11	11.8-18.2						
C6701	X4	12.5-41.7	50-167	25-83.5	60.4	27	560	75
C6211	X4	16.3-41.6	65-167	32.5-83	60.4	27	560	75
C6711	X4	16.3-37.5	65-150	32.5-75	60.4	27	560	75
C6712	X4	16.3-37.5	65-150	32.5-75	60.4	27	560	75

Table 3. PLL Component Selection Table for C64x

Speed (MHz)	CLKMode	CLKIN RANGE (MHz)	CPU CLOCK FREQUENCY RANGE (MHz)	CLKOUT4 RANGE (MHz)	CLKOUT6 RANGE (MHz)	TYPICAL LOCK TIME (μs)
400	Bypass (x1)	30-75	30-75	7.5-18.8	5-12.5	N/A
	x6	30-66.7	180-400	45-100	30-66.7	75
	x12	30-33.3	360-400	90-100	60-66.7	75
500	Bypass (x1)	30-75	30-75	7.5-18.8	5-12.5	N/A
	x6	30-75	180-450	45-112.5	30-75	75
	x12	30-41.7	360-500	90-125	60-83.3	75
600	Bypass (x1)	30-75	30-75	7.5-18.8	5-12.5	N/A
	x6	30-75	180-450	45-112.5	30-75	75
	x12	30-50	360-600	90-150	60-100	75

It is recommended that 1% resistors be used in the PLL circuit, although 5% resistors are expected to work as well. Also, 10%-tolerance ceramic chip capacitors should be used for their low inductance.

For best performance, it is recommended that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown in Figures below. To reduce PLL jitter, lead length and the number of vias should be kept to a minimum, while spacing between switching signals and the PLL external components should be at maximum. Also, all PLL external components should be placed as close to the C6000 DSP as possible and isolated from all high-speed digital signal traces.

The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}. In multiple-C6000 designs, it is important to provide a separate EMI filter circuit to each DSP. Multiple chips on a single filter will not work properly. The DSP will not function properly (except in x1 mode) without an EMI filter. The EMI filter used in the figures below is TDK part number ACF451832333, 223, 153, 103 or Panasonic part number EXCCET103U.

2.1.3 CLKIN External Clock Source

Figure 1 shows a simple oscillator circuit providing a CLKIN signal to the C6000. If an oscillator is used, its output can be connected to the CLKIN pin of the DSP through a series resistor.

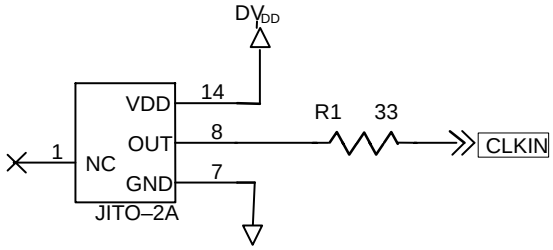


Figure 1. Oscillator Circuit for CLKIN

When selecting an oscillator, it is important to note that all rise/fall timings in the C6000 data sheet are based on 20% to 80%, while most oscillators base their timings on a 10% to 90% range. Table 4 lists some examples of compatible CLKIN external clock sources.

Table 4. Compatible CLKIN External Clock Sources

COMPATIBLE PARTS FOR EXTERNAL CLOCK SOURCES (CLKIN)	PART NUMBER	MANUFACTURER
Oscillators	JITO-2	Fox Electronix
	STA series, ST4100 series	SaRonix Corporation
	SG-636	Epson America
	342	Corning Frequency Control
PLL	MK1711-S, ICS525-02	Integrated Circuit Systems

The circuit shown in Figure 2 demonstrates how to generate the CLKIN signal using a clock synthesizer circuit rather than an oscillator chip. If a synthesizer circuit is used, the internal PLL must be bypassed in x1 mode. MicroClock[1] has developed a clock customized for use with TI's DSP products. It requires a single 20MHz crystal and generates a high quality clock signal with a frequency of 118MHz to 200MHz based on the value of CLK_SEL[2:0] (000b for 200MHz).

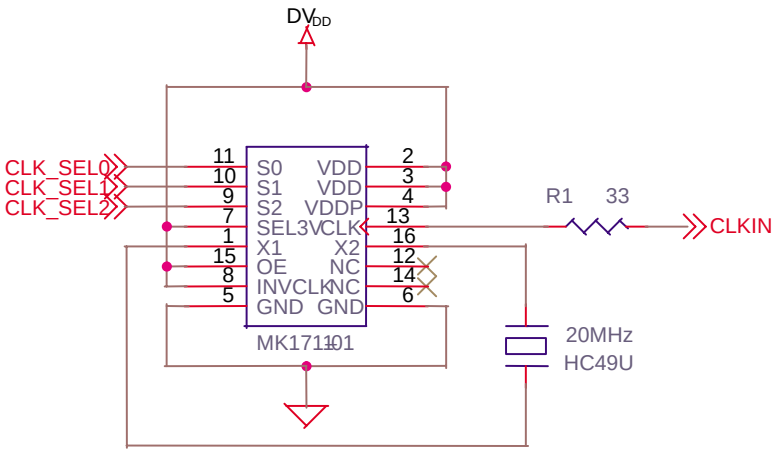
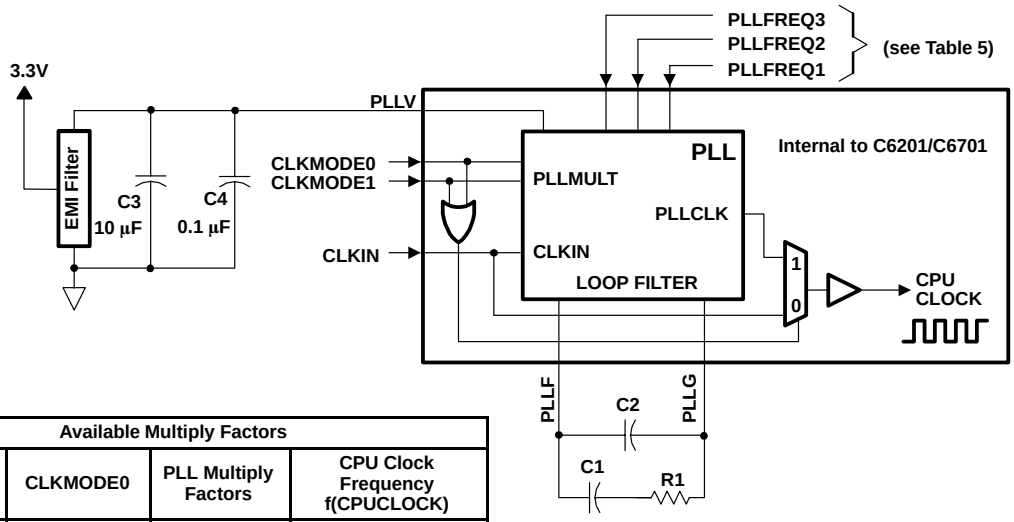


Figure 2. Clock Synthesizer Circuit for CLKIN

PLL Block Diagrams

The following figures show the locations within the device where each C6000 clock is generated. Essentially, the input clock either bypasses the PLL or is multiplied by a factor (CLKIN Frequency Multiplier) within it to generate the output clock (CLKOUT1), which serves as the internal clock to the device. This output clock (CLKOUT1) is then used to generate external clocks such as CLKOUT2, CLKOUT4, CLKOUT6, SSCLK, and SDCLK.

Figure 3 shows that on the C6201/C6701, CLKOUT1 serves as the internal clock for the rest of the DSP and is used to generate three other clock signals for memory interface: CLKOUT2, SDCLK, and SSCLK.



Available Multiply Factors			
CLKMODE1	**CLKMODE0**	**PLL Multiply Factors**	**CPU Clock Frequency f(CPUCLOCK)**
0	0	x1(BYPASS)	1 x f(CLKIN)
0	1	Reserved	Reserved
1	0	Reserved	Reserved
1	1	x4	4 x f(CLKIN)

Figure 3. Clock Signals for the TMS320C6201/C6701

[1] For more details on MicroClock, see their website at http://www.microclock.com.

On C6201/C6701, a target range for CLKOUT1 frequency has to be configured. The values of PLLFREQ[3:1] pins determine the frequency range when using x4 mode. Even though the frequency ranges given in Table 5 overlap, the lowest frequency range including the desired frequency is the one that should be used to maximize performance. For example, for CLKOUT1 = 133MHz, a PLLFREQ value of 000b should be used. Frequency ranges are slightly different on C6201 and C6701 due to device speed.

Table 5. CLKOUT1 Frequency Ranges On C6201/C6701

PLLFREQ3 (A9)	PLLFREQ2 (D11)	PLLFREQ1 (B10)	CLKOUT1 Frequency Range (MHz) for C6201	CLKOUT1 Frequency Range (MHz) for C6701
0	0	0	50-140	50-140
0	0	1	65-200	65-167
0	1	0	130-233	130-167

On the C6202/C6202B/C6203/C6204/C6205, CLKOUT1 serves as the internal clock for the rest of the DSP and is used to generate CLKOUT2, which is used for synchronous memory interface.

On the C621x/C671x the EMIF requires a separate external clock input (ECLKIN) to generate the memory clock (ECLKOUT). This allows the memory interface to operate at frequency independent of the CPU frequency. To drive the EMIF using CLKOUT2, this signal must be externally routed to ECLKIN.

Figure 4, Figure 5, and Figure 6 show the differences among C6202/02B/6203/6204, C6205, and C621x/C671x.

PLL circuitry diagrams are the same for C6202/C6202B/C6203/C6204, yet there are some differences in operation modes, as shown in Table 6.

Notice that:

- CLKMODE2 and CLKMODE1 are internally unconnected on C6202 GLS package and C6204 GLW package.
- CLKMODE2 and CLKMODE1 are not available on the C6204 GHK package.
- CLKMODE2 pin is NOT available on C6202B/C6203 GJL package, which means only x1 (Bypass), x4, x8, and x10 are applicable.

Table 6. PLL Multiplier Configurations on C6202/C6202B/C6203/C6204

			PLL Multiply Factors			
CLKMODE2	CLKMODE1	CLKMODE0	C6202	C6202B	C6203	C6204
0	0	0	Bypass (x1)	Bypass (x1)	Bypass (x1)	Bypass (x1)
0	0	1	x4	x4	x4	x4
0	1	0	Bypass (x1)	x8	x8	Bypass (x1)
0	1	1	x4	x10	x10	x4
1	0	0	Bypass (x1)	x6	x6	Bypass (x1)
1	0	1	x4	x9	x9	x4
1	1	0	Bypass (x1)	x7	x7	Bypass (x1)
1	1	1	x4	x11	x11	x4

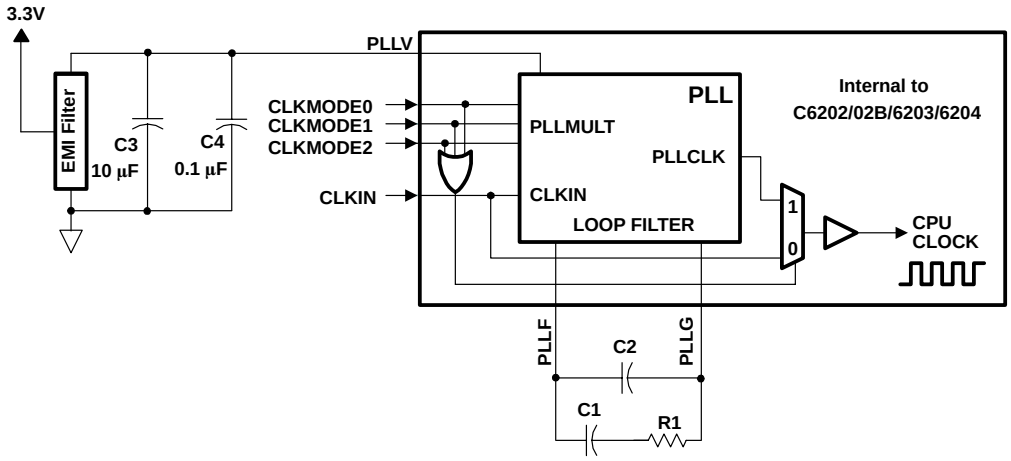
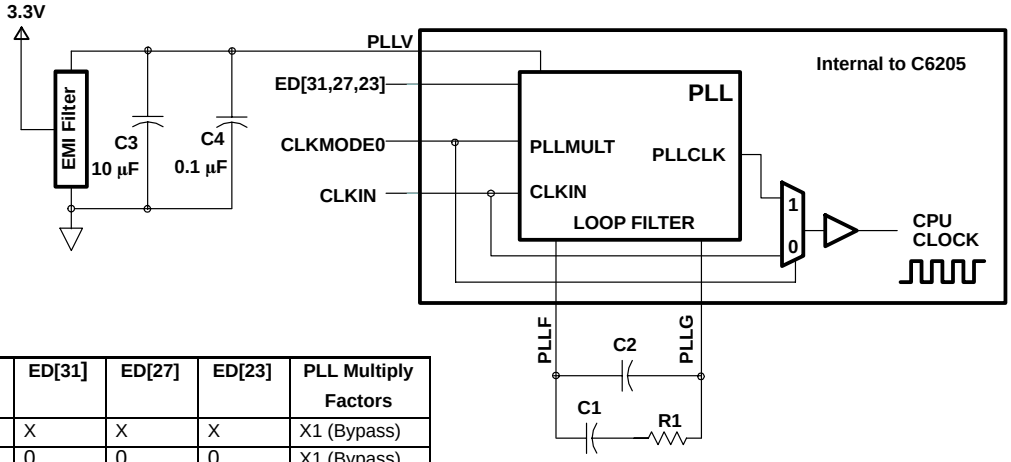


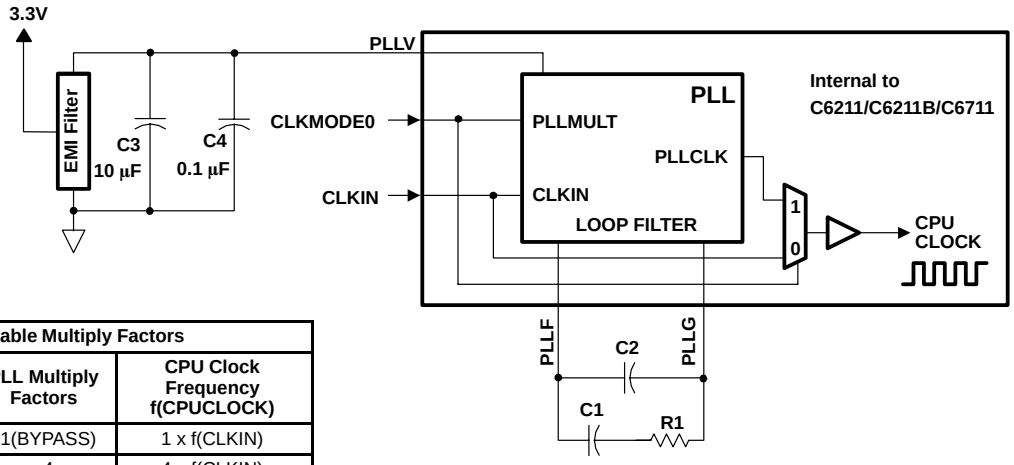
Figure 4. Clock Signals for the TMS320C6202/C6202B/C6203/C6204

On C6205, CLKMODE0 equal to 0 denotes on-chip PLL bypassed while CLKMODE0 equal to 1 denotes on-chip PLL used, except when configuration bits (ED[31], ED[27], and ED[13]) are 0 at reset. These on-chip PLL configuration bits (ED[31], ED[27], and ED[13]) are latched during device reset, along with the other boot configuration bits ED[31:0].



CLKMODE0	ED[31]	ED[27]	ED[23]	PLL Multiply Factors
0	X	X	X	X1 (Bypass)
1	0	0	0	X1 (Bypass)
1	0	0	1	X4
1	0	1	0	X8
1	0	1	1	X10
1	1	0	0	X6
1	1	0	1	X9
1	1	1	0	X7
1	1	1	1	X11

Figure 5. Clock Signals for the TMS320C6205

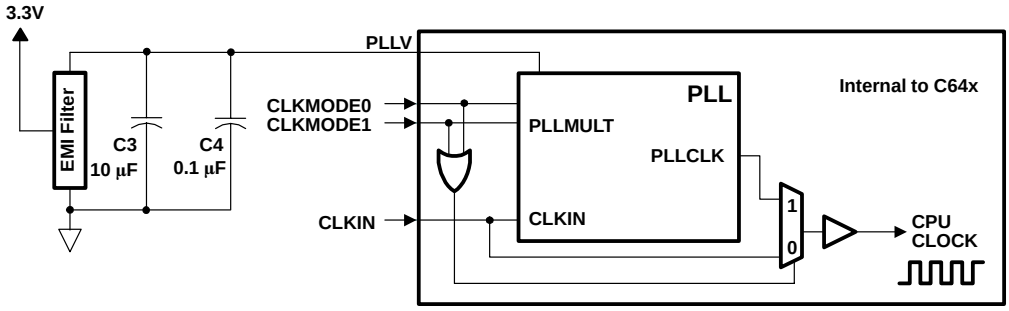


Available Multiply Factors		
CLKMODE0	**PLL Multiply Factors**	**CPU Clock Frequency f(CPUCLOCK)**
0	x1(BYPASS)	1 x f(CLKIN)
1	x4	4 x f(CLKIN)

Figure 6. Clock Signals for the TMS320C621x/C671x

On the C64x device, two external clocks, CLKOUT4 and CLKOUT6, are generated from the internal CPU clock. These two pins are muxed with the GPIO port pins and by default function as output clocks. One use of these two pins is to be externally routed back to ECLKIN for synchronous memory interface. Be aware of the ECLKIN max speed limit as discussed in the next section.

It is recommended to change the PLL multiply clock modes with external pullup resistors. CLKMODE1 and CLKMODE0 feature 30 kΩ internal pulldown resistors. To change the default PLL multiply clock mode (x1 Bypass) to either x6 or x12, use 1 kΩ external pullup resistors on the CLKMODE pins to pull up either signal to a logic ‘1’.



CLKMODE1	CLKMODE0	CLKMODE (PLL Multiply Factors)
0	0	Bypass (x1)
0	1	X6
1	0	X12
1	1	Reserved

Figure 7. Clock Signals for the TMS320C64x

2.2 Providing a Clock to EMIF Through ECLKIN

2.2.1 Clock Sources for C6000 EMIF

The external memory interface (EMIF) on C6000 DSP acquires clock signals from various sources. The C6201/C6701 DSP provides SDCLK for SDRAM and SSCLK for SBSRAM. On the remaining C620x devices, SDRAM and SBSRAM (only one of these two memory types can be used in a system) run off CLKOUT2 (EMIF clock cycle), which is equal to half the CPU clock rate (CPU/2).

The C621x/C671x EMIF requires that an external clock source (ECLKIN) be provided by the system. All of the memories interfacing with the C621x/C671x should operate off ECLKOUT (EMIF clock cycle) signal, which is produced internally (based on ECLKIN). If desired, the CLKOUT2 output can be routed back to the ECLKIN input.

There are two EMIFs (EMIFA and EMIFB) on C64x. These EMIFs are enhanced version of EMIF on C621x/C671x devices. In addition to ECLKIN, both EMIFs can be configured (at device reset via the pullup/pulldown resistors) to use internal CPU clock rate divide by 4 and divide by 6 as input clock. ECLKIN is the default for the EMIF input clock. All of the memories interfacing with the C64x DSP should operate off of ECLKOUT1 or ECLKOUT2 (EMIF clock cycle). The ECLKOUT1 frequency equals to EMIF input clock frequency. The ECLKOUT2 frequency is programmable to be EMIF input clock frequency divided by 1,2, or 4. ECLKIN is called AECLKIN for EMIFA and BECLKIN for EMIFB, while ECLKOUTx are called AECLKOUTx for EMIFA and BECLKOUTx for EMIFB.

According to the device datasheets, for C621x/C671x devices, ECLKIN speed is limited to 67MHz (15ns cycle time) for 100MHz devices or 100MHz (10ns cycle time) for 150MHz/160MHz devices, while on C64x devices, ECLKIN speed is limited to 133MHz (7.5ns cycle time) for 400MHz/500MHz/600MHz devices. With this limitation, connecting CLKOUT1 to ECLKIN is applicable only when the CPU is running at or lower than the ECLKIN speed limit.

3 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
2. *JITO–2 Specifications*, Fox Electronics.
3. *MK1711–01 200 MHz Selectable Clock Source Specifications*, MicroClock Division of ICS.
4. *TMS320C6201 Digital Signal Processor* (SPRS051).
5. *TMS320C6202, TMS320C6202B Fixed-Point Digital Signal Processors* (SPRS104).
6. *TMS320C6203 Fixed-Point Digital Signal Processor* (SPRS086).
7. *TMS320C6204 Fixed-Point Digital Signal Processor* (SPRS152).
8. *TMS320C6205 Fixed-Point Digital Signal Processor* (SPRS106).
9. *TMS320C6701 Floating-Point Digital Signal Processor* (SPRS067).
10. *TMS320C6211, TMS320C6211B Fixed-Point Digital Signal Processors* (SPRS073).
11. *TMS320C6712 Floating-Point Digital Signal Processor* (SPRS148).
12. *TMS320C6414 Fixed-Point Digital Signal Processor* (SPRS134).
13. *TMS320C6415 Fixed-Point Digital Signal Processor* (SPRS146).
14. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265