

High-Resolution Video Using the DM642 DSP and the THS8200 Triple DAC

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Device Applications

ABSTRACT

The DM642 DSP has three 20-bit video ports capable of high definition (HD) display. The video ports can be programmed to follow HDTV standards, such as SMPTE274M and SMPTE296M. These HDTV standards follow a 4:2:2 convention where luminance and chrominance signals are separated onto two different 8- or 10-bit data paths. This convention is more commonly called Y/C mode. Many new HD displays accept Y'P_bP_r component inputs (analog luminance and chrominance). The DM642 outputs digital luma and chroma (Y'C_bC_r) and must be converted to analog, which can be achieved using the THS8200 triple-video digital-to-analog converter (DAC). This application note gives a brief discussion on the HDTV standards and demonstrates the hardware requirements/implementation for interfacing the DM642 video port to a THS8200. A future revision of this application note will give software configurations, THS8200 drivers, and an example application proving the discussed system.

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1 Introduction

This application note describes the implementation of a high definition video using a video DAC, the Texas Instruments THS8200, and the DM642. The THS8200 is capable of capturing digital data via different formats: in 4:2:2 or 4:4:4 formats, through its 3 10-bit DACs. To achieve the necessary bandwidth for high resolution video, two 10-bit inputs on the THS8200 using the 4:2:2 format can be used. This mode, in conjunction with the DM642's Y/C mode, provides a simple solution to producing high-resolution analog video at 30 frames per second. Using SMPTE274M/296M standards, HDTV signals can be generated by the system for use in HD set-top boxes or other high resolution video applications.

2 HDTV Standards

2.1 SMPTE296M

SMPTE296M describes the scanning and timing information required for 1280 x 720 resolution with progressive scanning. This standard is commonly known as *720p*. Frame rates within this standard can vary from 23.976 f/s to 60 f/s. The sampling frequency, or pixel clock, stays fixed at ~74.25 MHz. Due to color and sound subcarrier frequency interactions, pixel clock rates may need to be modified by a 1.001 ratio, which decreases the pixel clock rate from 74.25 MHz to 74.176 MHz. In order to achieve various frame rates, the number of pixels per line varies accordingly; however, the number of actual lines remains constant at 750 lines per frame.

Table 1 provides a listing of frame rates given the pixel clock with 1280 x 720 resolution. The luminance and chrominance signals are transmitted across separate data lines to help maintain the required bandwidth. Synchronization can be embedded within the data lines; embedded sync signals (Start Active Video, SAV, and End Active Video, EAV) are transmitted as code words within the 8-/10-bit data streams. Both luminance and chrominance data are being transmitted using a 4:2:2 format. There are two luminance samples for every pair of chrominance samples. The chrominance signals (C_b and C_r) are multiplexed. Figure 4 provides an example of the multiplexing that occurs between the chrominance signals.

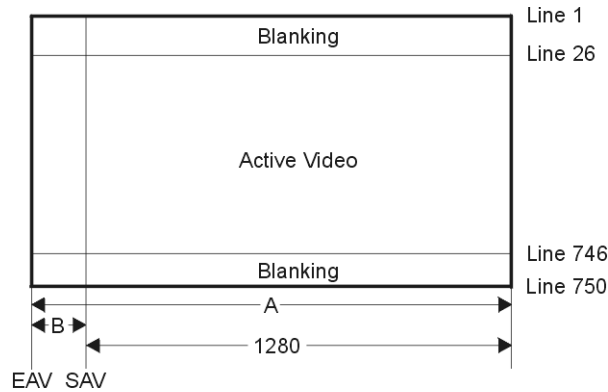


Figure 1. SMPTE296M Vertical and Horizontal Components

Refer to Table 1 for ‘A’ and ‘B’ pixel counts. Lines 26 – 746 make up the 720 horizontal lines of active video. The 1280 vertical lines of active video are defined by the total horizontal resolution (A) minus the horizontal blanking count (B).

Table 1. Various SMPTE296M Frame Rates

Active Horizontal Resolution	Frame Rate (Hz)	Sample Rate/ Pixel Clock (MHz)	Total Horizontal Resolution (A)	Horizontal Blanking (B)
1280	23.976	74.176	4125	2845
1280	24	74.25	4125	2845
1280	25	74.25	3960	2680
1280	29.97	74.176	3300	2020
1280	30	74.25	3300	2020
1280	50	74.25	1980	700
1280	59.94	74.176	1650	370
1280	60	74.25	1650	370

2.2 SMPTE274M

SMPTE274M varies slightly from SMPTE296M. The main difference between the two standards is the resolution. SMPTE274M describes the scanning and timing information required for 1920 x 1080 resolutions with both progressive and interlaced scanning. Table 2 and Table 3 provide listings of the various frame rates, pixel clocks, and resolutions for SMPTE274M, interlaced and progressive. The more common mode for this standard is 1920 x 1080 x 30 f/s interlaced, commonly known as *1080i*. Similar to SMPTE296M, frame rates vary from 23.976 f/s to 60 f/s. The total number of lines remains constant at 1125. The number of samples per line varies in order to achieve desired frame rates. Pixel clock rates double when high frame rates via progressive mode are desired. Embedded syncs and 4:2:2 formatting are also used with the SMPTE274M standard.

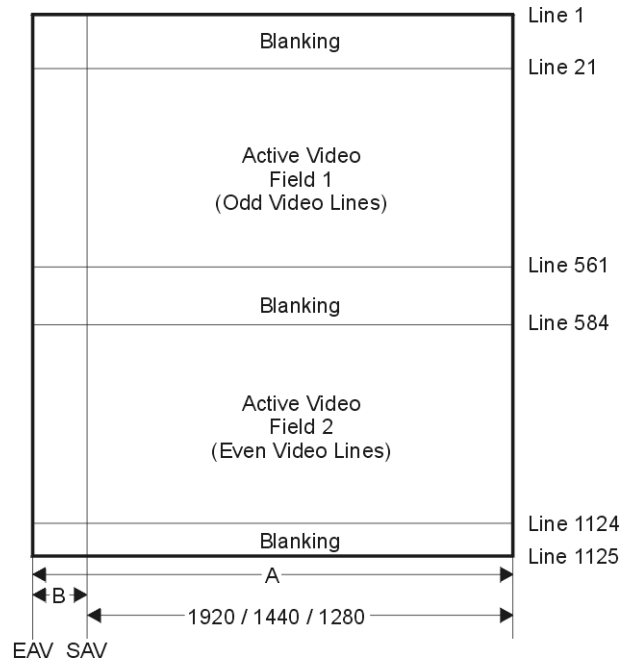


Figure 2. SMPTE274M Interlaced Vertical and Horizontal Components

Refer to Table 2 for 'A' and 'B' pixel counts. Lines 21 – 561 make up odd numbered horizontal lines of active video. Lines 584 – 1124 make up the even horizontal lines of active video. The vertical lines of active video are defined by the total horizontal resolution (A) minus the horizontal blanking count (B).

Table 2. Various SMPTE274M Interlaced Frame Rates

Active Horizontal Resolution	Frame Rate (Hz)	Sample Rate/ Pixel Clock (MHz)	Total Horizontal Resolution (A)	Horizontal Blanking (B)
1920	23.976	74.176	2750	830
1920	24	74.25	2750	830
1920	25	74.25	2640	720
1920	29.97	74.176	2200	280
1920	30	74.25	2200	280
1440	23.976	55.632	2062.5	622.5
1440	24	55.6875	2062.5	622.5
1440	25	55.6875	1980	540
1440	29.97	55.632	1650	210
1440	30	55.6875	1650	210
1280	23.976	49.451	1833.3	553.3
1280	24	49.5	1833.3	553.3
1280	25	49.5	1760	480
1280	29.97	49.451	1466.7	186.7
1280	30	49.5	1466.7	186.7

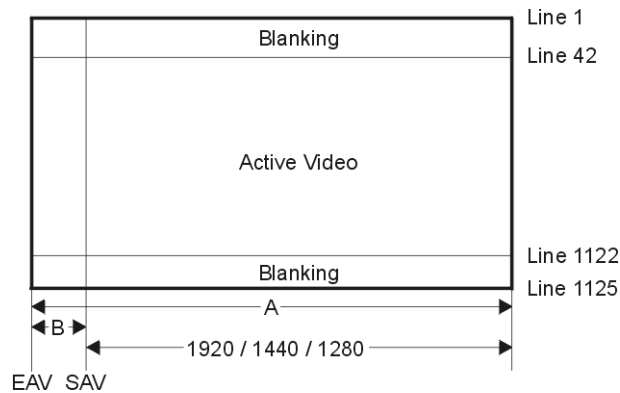


Figure 3. SMPTE274M Progressive Vertical and Horizontal Components

Refer to Table 3 for 'A' and 'B' pixel counts. Lines 42 – 1122 make up the 1080 horizontal lines of active video. The vertical lines of active video are defined by the total horizontal resolution (A) minus the horizontal blanking count (B).

Table 3. Various SMPTE274M Progressive Frame Rates

Active Horizontal Resolution	Frame Rate (Hz)	Sample Rate/ Pixel Clock (MHz)	Total Horizontal Resolution (A)	Horizontal Blanking (B)
1920	23.976	74.176	2750	830
1920	24	74.25	2750	830
1920	25	74.25	2640	720
1920	29.97	74.176	2200	280
1920	30	74.25	2200	280
1920	50	148.5	2640	720
1920	59.94	148.352	2200	280
1920	60	148.5	2200	280
1440	23.976	55.632	2062.5	622.5
1440	24	55.6875	2062.5	622.5
1440	25	55.6875	1980	540
1440	29.97	55.632	1650	210
1440	30	55.6875	1650	210
1440	50	111.375	1980	540
1440	59.94	111.264	1650	210
1440	60	111.375	1650	210
1280	23.976	49.451	1833.3	553.3
1280	24	49.5	1833.3	553.3
1280	25	49.5	1760	480
1280	29.97	49.451	166.7	186.7
1280	30	49.5	1466.7	186.7
1280	50	99	1760	480
1280	59.94	98.901	1466.7	186.7
1280	60	99	1466.7	186.7

Figure 4 shows the luminance and chrominance data signals using different data paths. Notice how the chrominance signals are multiplexed to achieve a 4:2:2 format.

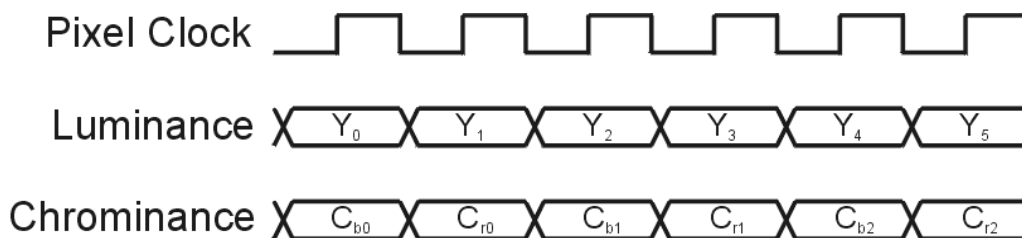


Figure 4. Digital Video Data Transfer

3 DM642 Video Port

The Texas Instruments DM642 has three 20-bit video ports that ports can be configured for different video standards, such as BT.656, SMPTE296M, or SMPTE274M, or can be used in a RAW data mode fashion. The video ports are capable of driving encoders for display purposes, or they can capture data from various decoders. Example applications for the DM642 using the video ports include security cameras, set-top boxes, or video conferencing.

One point to note here is the Y/C mode capability of the video port. Embedded synchronization capabilities of the DM642 video port can be used to synchronize the DM642 with the THS8200.

The DM642 also has an I²C port which can be used to communicate and set up various other programmable ICs within the system. In this case, the I²C port will be used to set-up the THS8200 for Y/C operation. Refer to the *THS8200 Data Manual* for a list of the THS8200 registers and their default values.

Table 4 provides a list of signal names and descriptions associated with the DM642 video port.

Table 4. DM642 Video Port Signal List

Signal Name	Driver	Description
VPxD[19..00]	I/O/Z	Video port x data lines VPxD[19..10] used for multiplexed chroma signals (C_b/C_r) VPxD[09..00] used for luma signals (Y')
VPxCLK1	I/O/Z	Video port x clock line Configured as output in display mode
VPxCLK0	I	Video port x clock line Configured as input in display mode
VPxCTL2	I/O/Z	Video port x control line Can be configured as <input type="checkbox"/> CBLNK – composite blanking (output) <input type="checkbox"/> FLD – field identification (input/output)
VPxCTL1	I/O/Z	Video port x control line Can be configured as <input type="checkbox"/> VSYNC – vertical synchronization (input/output) <input type="checkbox"/> VBLNK – vertical blanking (output) <input type="checkbox"/> CSYNC – composite synchronization (output) <input type="checkbox"/> FLD – field identification (output)
VPxCTL0	I/O/Z	Video port x control line Can be configured as <input type="checkbox"/> HSYNC – horizontal synchronization (input/output) <input type="checkbox"/> HBLNK – horizontal blanking (output) <input type="checkbox"/> AVID – active video signal (output) <input type="checkbox"/> FLD – field identification (output)

4 THS8200

The THS8200 is a Texas Instruments triple DAC, developed for the video industry, and which accepts a variety of digital input formats in both 4:4:4 and 4:2:2 formats. The THS8200 synchronizes to the incoming data via dedicated external synchronization inputs (HSYNC and VSYNC) or from embedded sync codes (SAV and EAV) inside the digital video stream.

Video processing flexibility is achieved through extensive programmability within the THS8200. This programmability is achieved through a fast mode I²C control interface. Its features include a fully programmable 3x3 matrix for color space conversion, and a programmable synchronous timing generator for various SDTV, HDTV, and non-standard video formats up to a maximum pixel clock of 205 MSPS. All video modes, up to an 80MHz clock rate, can be internally oversampled by 2x.

These modes and features of the THS8200 provide a clear, simplified path to high-resolution displays from the DM642. The DM642 can utilize the 20-bit $Y'C_bC_r$ 4:2:2 input capabilities of the THS8200 to convert the DM642's digital interface to $Y'P_bP_r$ for HD displays. Figure 5 shows the general connections between the DM642 and the THS8200.

Table 5 describes the digital video pin connections and functionality between the DM642 and the THS8200 as shown in Figure 5.

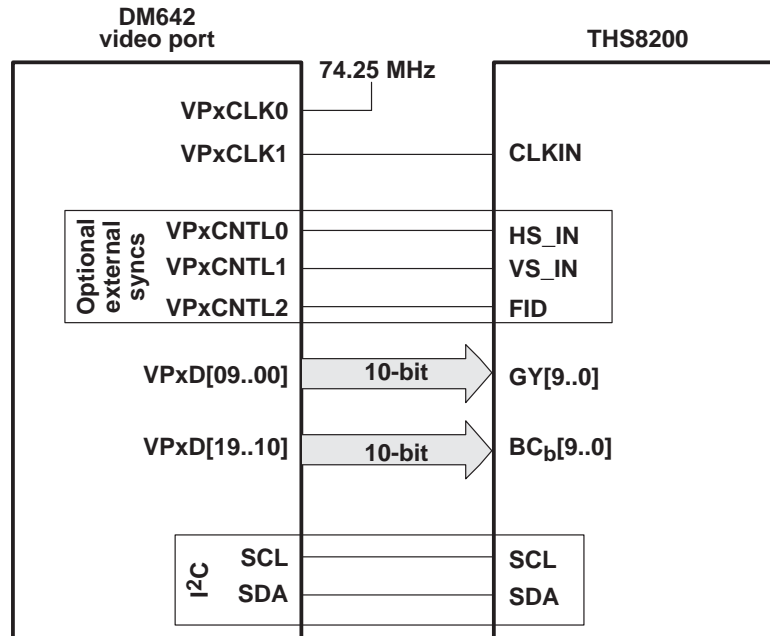


Figure 5. Interconnect between DM642 Video Port and the THS8200

Table 5. DM642 to THS8200 Signal Descriptions

Signal Name		
DM642	THS8200	Description
VPxD[9..0]	GY[9..0]	Luminance signal lines.
VPxD[19..10]	BCb[9..0]	Chrominance signal lines. Both Cb and Cr are multiplexed on this bus.
VPxCLK0	–	When the DM642 is mastering VPx (normal operation), this signal is used as an input of the pixel clock.
VPxCLK1	CLKIN	DM642 drives THS8200 clock line, keeping synchronization between CLKIN and data lines.
VPxCTL0	HS_IN	<i>Optional.</i> THS8200 is capable of using embedded synchronization. External syncs can be used for non-standard timings.
VPxCTL1	VS_IN	<i>Optional.</i> THS8200 is capable of using embedded synchronization. External syncs can be used for non-standard timings.
VPxCTL2	FID	<i>Optional.</i> THS8200 is capable of acquiring the field ID from the embedded data stream when interlaced video is present.
–	RCr[9..0]	Unused chrominance signals. Tied low to reduce THS8200 power consumption. These lines are used for 4:4:4 formatting, not capable by the DM642.

5 Video System Hardware Design Guidelines

To achieve good performance within the video system, some general guidelines have been given (the checklist format is for ease of implementation). These techniques provide a starting point for creating a low noise video system. Signal integrity analysis should be done using IBIS modeling to obtain optimum signal integrity and performance.

Table 6. DM642 Video Port to THS8200 Hardware Design Checklist

Completed (check box when done)	Description
	Power Supplies
<input type="checkbox"/>	Analog and digital power supplies should be separated.
<input type="checkbox"/>	The power supplies should have a high power supply rejection ratio (PSRR).
	Decoupling/Bypass Capacitance
<input type="checkbox"/>	Multiple decoupling capacitors should be located as close as possible to all digital ICs, especially the video DAC and DSP.
<input type="checkbox"/>	As many 0.01- μ F capacitors with low ESL/ESR should be placed near the ICs as feasible.
<input type="checkbox"/>	Bulk capacitors, on the order of 10- μ F, should also be used to help filter power supply fluctuations.
	Signal Integrity
<input type="checkbox"/>	Serial termination may be necessary on all data busses, address busses, and/or control/clock signals. Longer traces (>1.5 in.) generally require serial termination. Shorter traces may not require termination, but IBIS analysis can provide insight as to proper sizing and placement of termination resistors.
<input type="checkbox"/>	High speed interfaces should be kept within a reasonable length. Buses and control signals should not vary greatly in length.
<input type="checkbox"/>	Clock lines must have proper termination and not branch off several times on a given net.
	Analog Outputs of DAC
<input type="checkbox"/>	Analog video outputs should have similar trace characteristics, in order to help keep synchronization.
<input type="checkbox"/>	The analog outputs of the THS8200 should have EMI filtering in order to eliminate the high frequency components generated by the DAC. This filter acts as an anti-aliasing and reconstructive filter that smoothes the sharp edges generated by the video DAC. Depending on the output frequency used by the DAC, the filtering requirements may be different. Video specific filters can be purchased or a filter can be made from separate components. Quality, accuracy, and cost should be considered when choosing which option is best.

6 Conclusions

This application report provides a clear approach to obtaining high-resolution video using the DM642 and the THS8200. While focused on the THS8200 as the video DAC of choice, other video DACs that follow SMPTE274M and/or SMPTE296M can be used in a similar fashion. Appendix A provides schematics for a daughter card used to test the Y/C mode interface between the DM642 Video Port and the THS8200. The focus of the testing was done using embedded synchronization at ATSC standard resolutions of 480p, 720p, and 1080i. Appendix B provides a brief discussion of the example code and the THS8200 driver developed for the daughter card, shown in Appendix A. The THS8200 driver files can easily be ported to other applications.

7 References

1. *TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor Data Manual* (SPRS200)
2. *TMS320C64x DSP Video Port/VCXO Interpolated Control (VIC) Port Reference Guide* (SPRU629)
3. *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175)
4. Jack, Keith. *Video Demystified: A Handbook for the Digital Engineer*. Elsevier Science & Technology Books, April 2001.
5. Poynton, Charles. *Digital Video and HDTV Algorithms and Interfaces*. Elsevier Science & Technology, January 2003.

Appendix A THS8200 Daughtercard Schematics for DM642 EVM

The following pages contain schematics for a THS8200 daughtercard that can interface to the DM642 EVM. They should only be used as an example of how to interface the DM642 to a THS8200. This example is applicable to other video DACs having similar interfaces.

The schematics are shown for some different possible combinations. For example, the video port control lines are tied to the external synchronization signals, even though the DM642 and THS8200 are capable of using embedded synchronization. The clock routings are another example of possible variations. In general, the master will accept the pixel clock and then output it to the slave. Depending on the system, the clock can also branch to both the master and the slave on one net.

TEXAS INSTRUMENTS
THS8200 Daughter Card for DM642 Evaluation Module

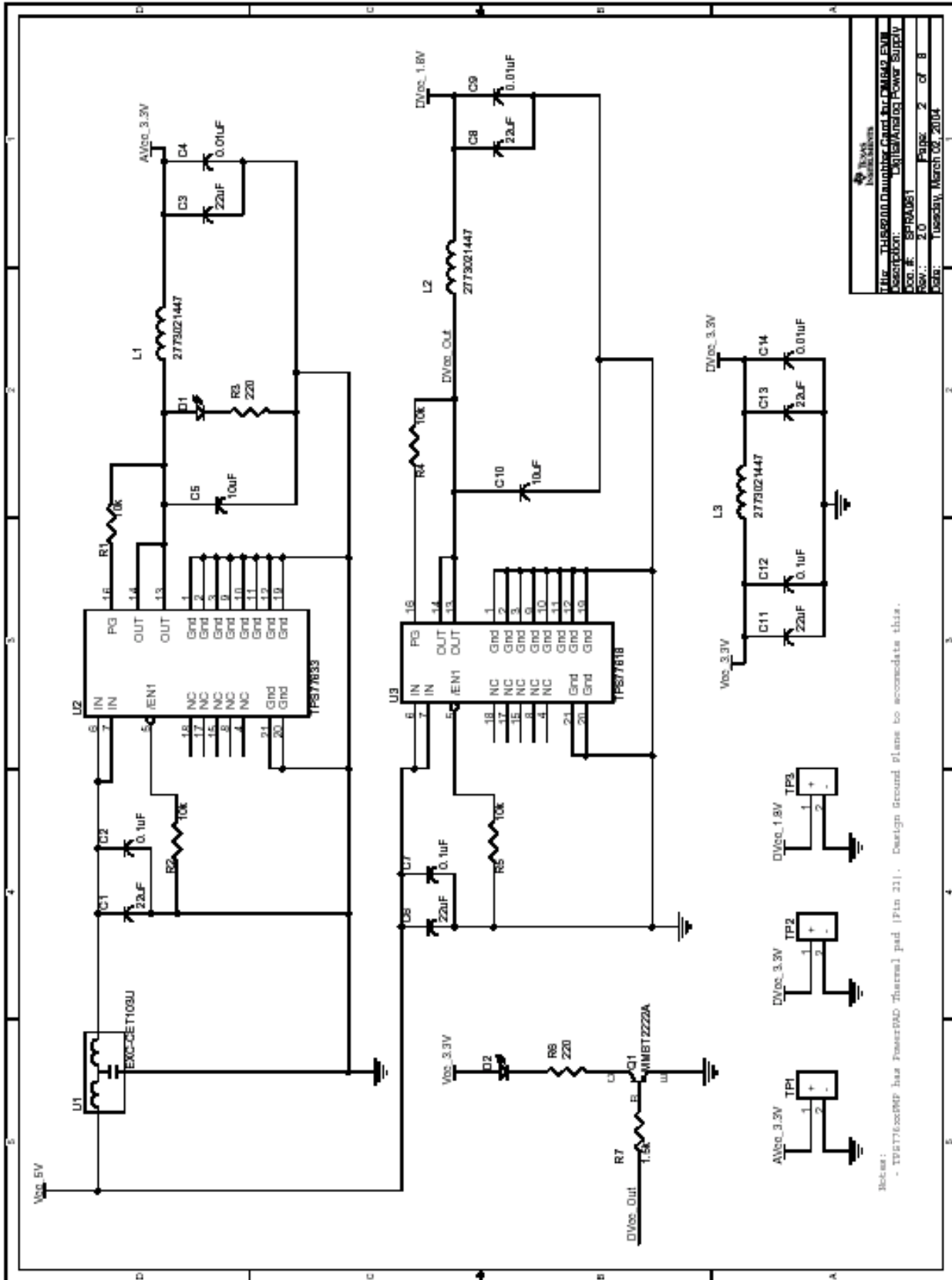
Table of Contents

- 1) Contents, Notes, & Revisions
- 2) Digital / Analog Power Supply
- 3) EMIF DC Connectors
- 4) VP2 DC Connectors
- 5) VP0/I DC Connectors
- 6) THS8200 - Control & Inputs
- 7) THS8200 - Power & Outputs
- 8) Clocking

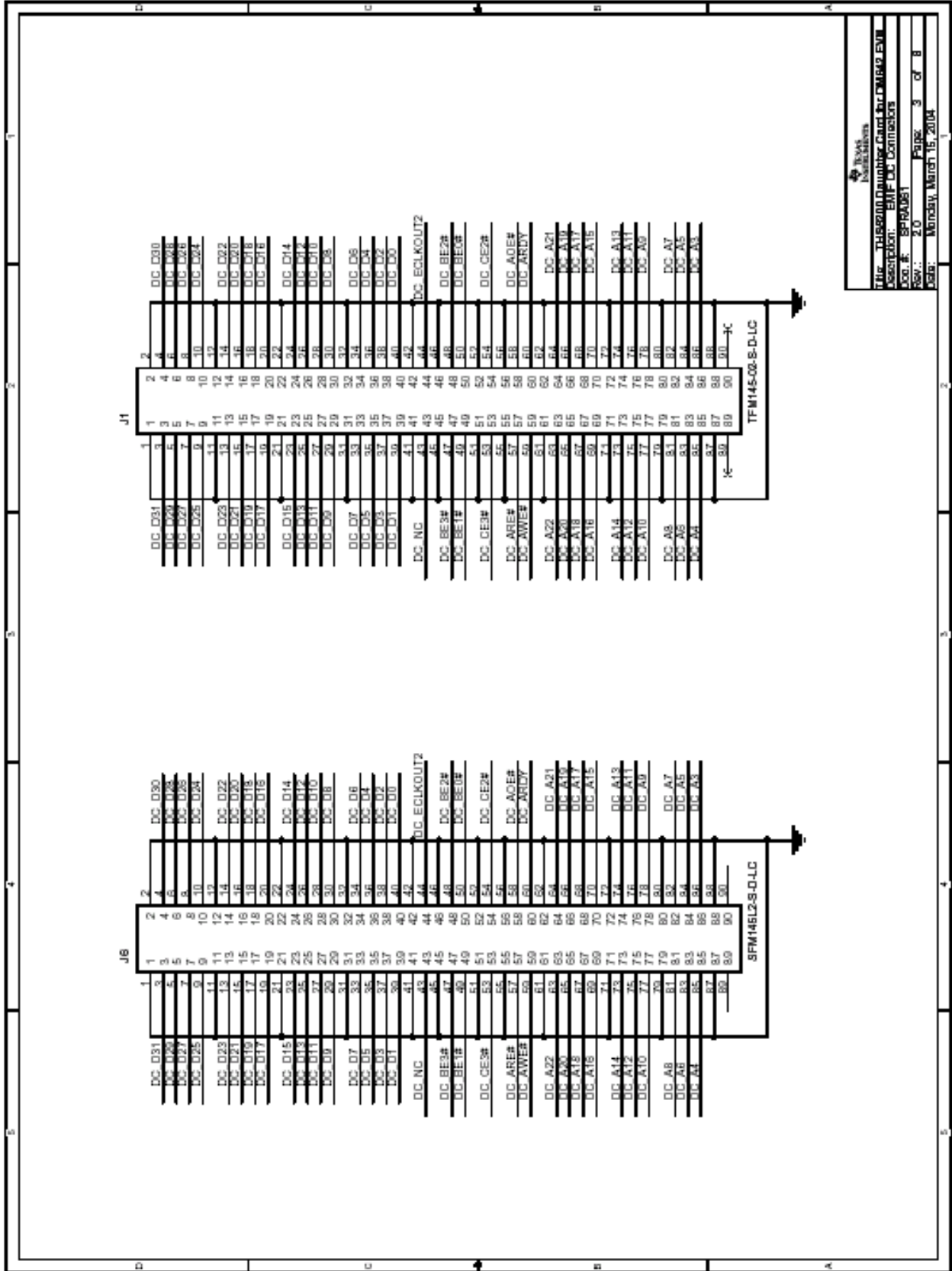
- Notes:
- 1) RESISTANCE VALUES ARE IN OHMS.
 - 2) CAPACITANCE VALUES ARE IN MICRO-FARADS (uF).
 - 3) BOARD PROPERTIES
 - A. BOARD TO WITHIN 10% OF MANUFACTURER DISTANCE.
 - B. 50 OHM MATCHED IMPEDANCE FOR DIGITAL LINES. 75 OHM MATCHED IMPEDANCE FOR ANALOG LINES.
 - C. CORE LAYERS 0.5 OZ CU & 0.5 OZ OR AU PLATING
 - D. INNER LAYERS 3.0 OZ CU
 - E. PRE BOARD MATERIAL
 - F. MINIMUM TRACE WIDTH/SPACING 4/8 MILS
 - G. MINIMUM VIA SIZE 10/13 MIL
 - H. APPROXIMATE BOARD SIZE 3.625 x 3.25 INCHES
 - I. U1, U2, & U5 HAVE POWERPAD PACKAGES, POWERPAD SHOULD BE CONNECTED TO APPROPRIATE GROUND.
 - J. THERMAL RELIEFS SHOULD NOT BE USED

Rev. #	Description	Date	Approval
0.6	Preliminary Schematics Completed	09/18/03	JBF
0.7	Modified Analog Output Filter Selection to resistors Added termination resistors to Digital Inputs Modified Clock Terminations Modified Switch for I2C and User I/O pins Changed Jumpers to Switches	10/07/03	JBF
1.0	Modified Power Supply Components Modified Clock Distribution Modified Bypass Caps to ICs Sent to Board Shop	10/20/03	JBF
1.01	Removed Pins 21, 22, 41, 42, 45, 46, 71, 72 of J1	11/03/03	JBF
1.02	Modified DVcc_1.8V Power Indicator Circuit Combined Ground Planes to Single Plane Modified Clocking Structure	11/10/03	JBF
1.1	Added IDT Clock Skew Generator Reannotated schematics	12/2/03	JBF
2.0	- Added Daughter Card Connectors to top of board - Fixed VP0/I Connector - Removed Logic Analyzer Connector - Added VESA Connector - Added HSYNC/VSYNC TestPoints - Removed HD Filters - Removed (R36, R37) Changed R40, R41 to 3.0k and 2.0k	2/27/04	JBF

TI Instruments	
Part Number	THS8200 Daughter Card for DM642 EV
Description	Contents, Notes, & Revisions
Doc. #	SPRA961
Rev.	2.0
Page	1 of 8
Date	Tuesday, March 02, 2004



TITLE: THIS DOCUMENT NUMBER: DM642 DSP DESCRIPTION: DM642 DSP Power Supply DOC. #.: SPRA961A REV.: 2.0 Page: 2 of 8 DATE: Tuesday, March 02, 2004



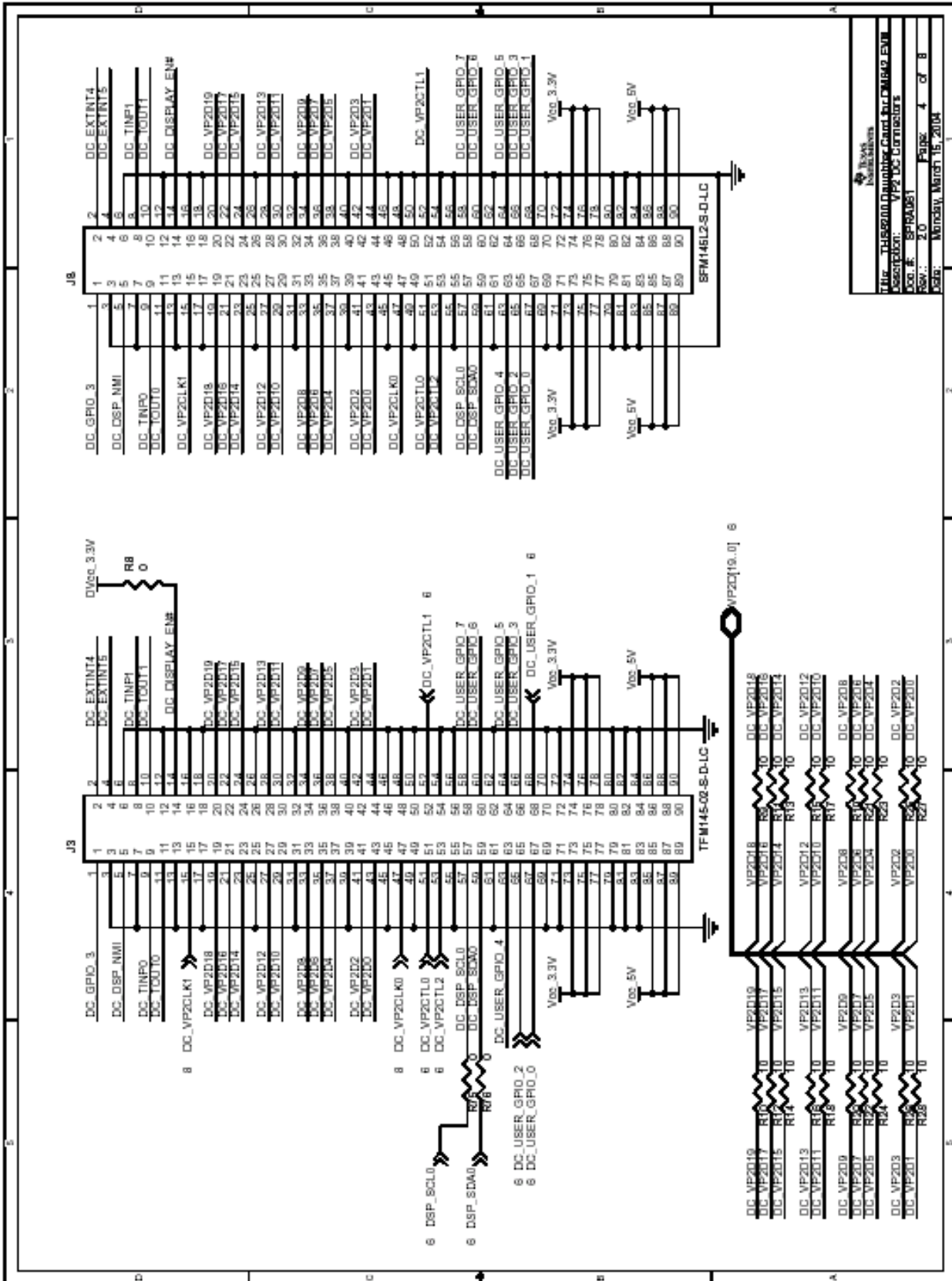
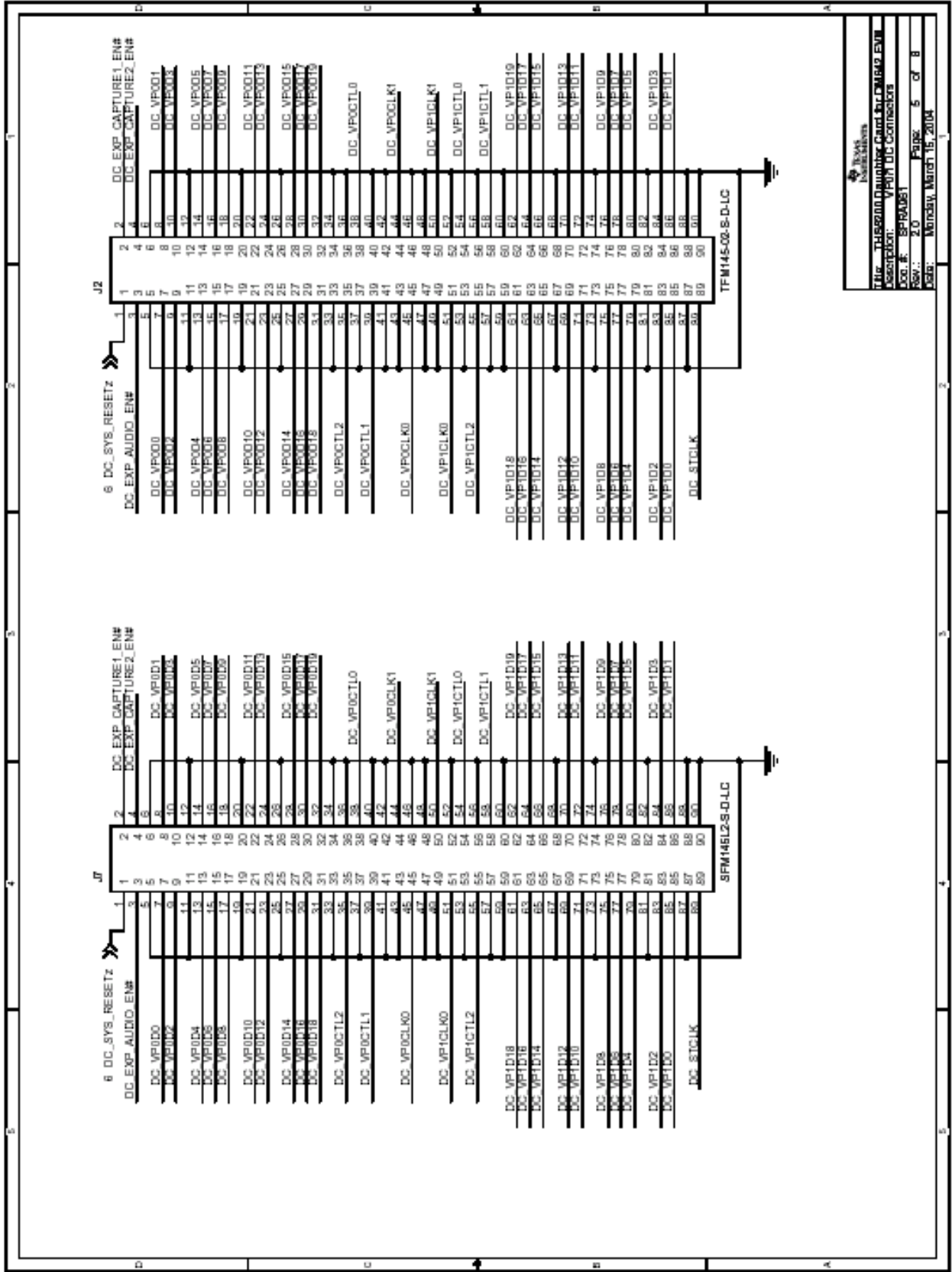


Table 1: Pin Connections

Pin #	Signal
1	DC_GPIO_3
2	DC_EXTINT4
3	DC_EXTINT5
4	DC_DSP_NMI
5	DC_TINP0
6	DC_TINP1
7	DC_TOUT0
8	DC_TOUT1
9	DC_TOUT2
10	DC_TOUT3
11	DC_TOUT4
12	DC_TOUT5
13	DC_TOUT6
14	DC_TOUT7
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64	DC_TOUT57
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66	DC_TOUT59
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73	DC_TOUT66
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87	DC_TOUT80
88	DC_TOUT81
89	DC_TOUT82
90	DC_TOUT83





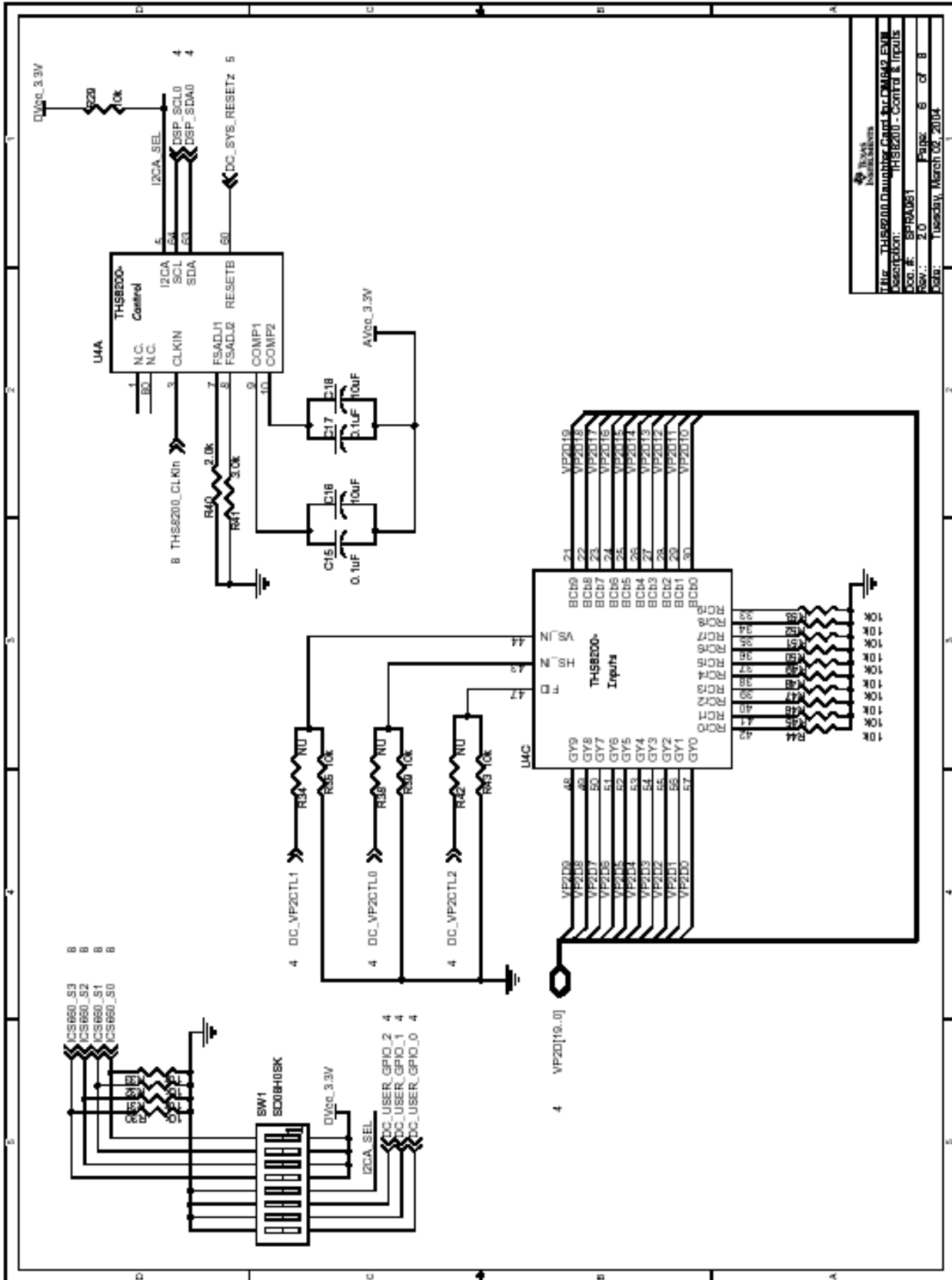
 THE TEXAS INSTRUMENTS COMPANY

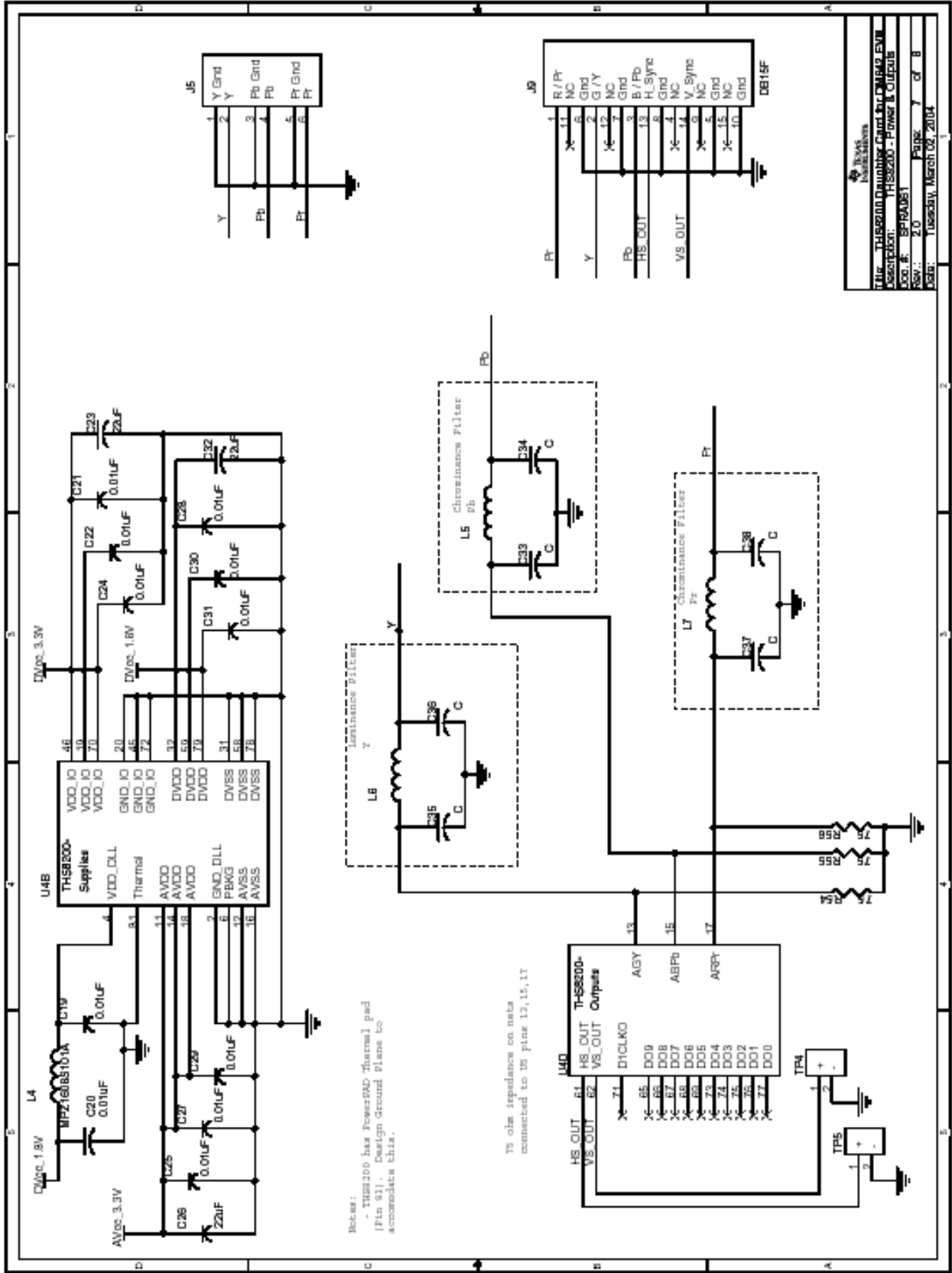
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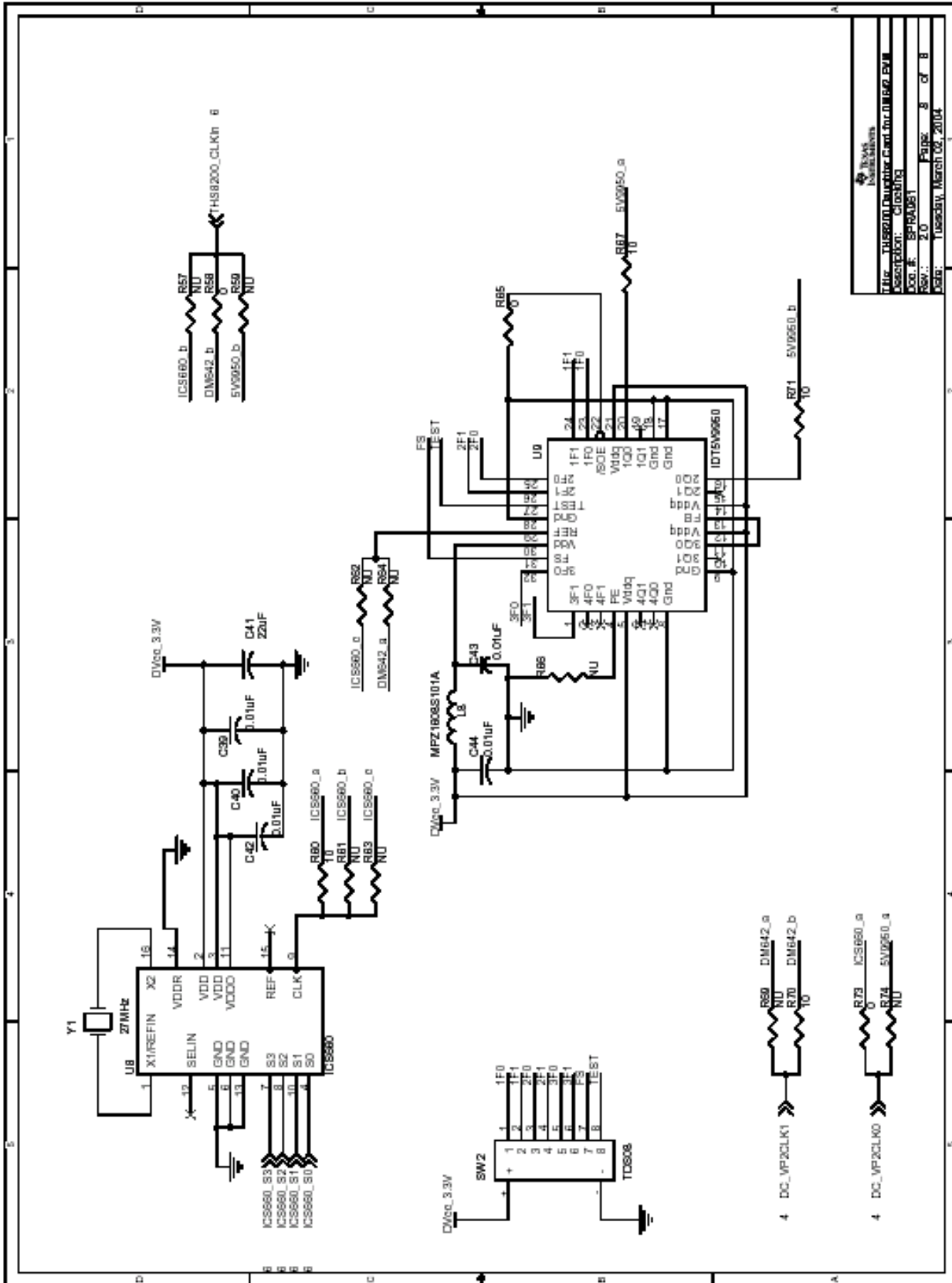
 Doc. # SPRA961

 Rev. 2.0 Page 5 of 8

 Date: Monday, March 15, 2014







File:	THS8200 Daughtice Card for DM642 EVM
Description:	Circuit
Doc #:	SPRA961
Rev.:	2.0
Page:	5 of 8
Date:	Tuesday, March 02, 2010

Appendix B THS8200 Driver Example

The example code given with this application note simply demonstrates the use of the THS8200 Driver to implement 480p, 720p, or 1080i resolution. The DM642 EVM with the THS8200 daughter card, shown in Appendix A, captures NTSC video via Video Port 0 and displays that video in a window within a high resolution format.

Frequency selection for 480p is different than for 720p and 1080i. 480p requires a 27MHz input clock frequency to the video port, while 720p and 1080i require ~74.25MHz, as described in section 2.

The THS8200 and the Philips SAA7115 use similar I2C addresses, 40h or 42h. Since the DM642 EVM has two SAA7115 decoders, only one SAA7115 can be used at a time with the THS8200. Because of this limitation, a picture-in-picture example is not possible. I2C multiplexers can be used to resolve conflicting addresses.

The THS8200 driver requires two parameters for initialization; an input mode parameter and an output mode parameter. The input parameter configures the **data_cntl** register, which sets the input format of data, and the **dtg2_cntl** register, which sets the input synchronization mode and polarity of synchronization signals. The output parameter configures several different registers related to the display timing generation. The dtg registers configure the pixel count, line count, synchronization levels, field and frame sizes, as well as the required processing delay. Most of these output parameters can easily be calculated from the particular video standard that is being used. The horizontal and vertical delay registers need to be set based on the amount of processing required by the THS8200 for processing and data conversion.

The THS8200 driver is set-up for 480p, 720p, and 1080i resolution. The THS8200 input format for 480p is BT .656, the output format is YP_bP_r component. The THS8200 input format for 720p and 1080i is 16-bit Y/C 4:2:2, the output format is YP_bP_r component.

The color space conversion registers and the clip/shift/multiplier registers provide the mean for higher quality video. These registers go beyond the scope of this example driver, but are easily implemented following the example functions within the example code.

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