Packet Transmission Basics

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Keywords

- *CC1100*
- *CC1101*
- *CC1100E*
- *CC1150*
- *CC2500*
- *CC2550*
- *FIFO*
- *Fixed Packet Length Mode*
- *Variable Packet Length Mode*
- *Infinite Packet Length Mode*

1 Introduction

The CC1100/CC1100E/CC1101/CC1150/ CC2500 /CC2500 all have extensive built-in packet handling support in hardware. This is to make it easier to implement packet oriented radio protocols in firmware. However, it can sometimes be difficult to know what features to use for a specific application. This design note will look into how the packet size will influence the complexity of the firmware, and how and when to use the different length configurations available.

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2 Packet Size

It is possible to send packets of all packet lengths, but the complexity of the code increases if the packet size is longer than 64 bytes (the FIFO size). Packet size is in this context all bytes that follow the sync word, except the optional CRC16 bytes.

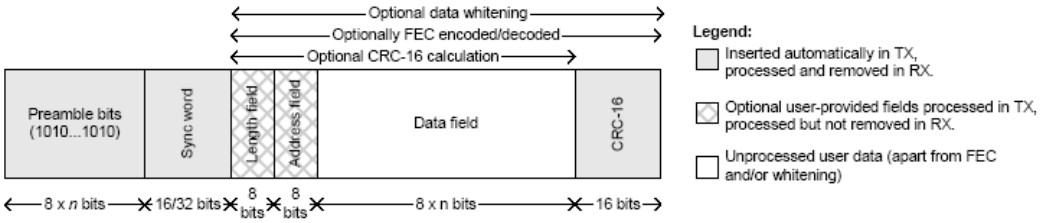

Figure 1. Packet Format

There are 3 different packet length modes supported; fixed, variable, and infinite. In fixed packet length mode, the PKTLEN register indicates the packet length. That means that if PKTLEN = 0x05, and 10 bytes are written to the TX FIFO, only 5 bytes will be transmitted. On the receiver side, 5 bytes will be received after a valid sync word has been detected. For variable packet length mode, the PKTLEN register has no meaning when in TX mode. In RX mode, however, it will give you the maximum allowed packet length to receive. That means that is PKTLEN = 0x05, and the first byte received after a valid sync word is greater than 5, the packet will be discarded.

2.1 Packet Size ≤ 64 Bytes

The easiest way to transmit and receive a packet, seen from a firmware point of view, is to not let the packet size exceed 64 bytes. To transmit a packet one only needs to write the packet to the TX FIFO, strobe TX, and wait for the packet to be transmitted. On the receiver side, one waits for the whole packet to be received before reading the FIFO. Both fixed and variable packet mode can be used.

```
//------------------------------------------------------------------
// TX (IOCFG0 = 0x06)

halSpiWriteBurstReg(CCxxx0_TXFIFO, txBuffer, sizeof(txBuffer));
halSpiStrobe(CCxxx0_STX);

// Wait for GDO0 to be set -> sync transmitted
while (!P0_6);

// Wait for GDO0 to be cleared -> end of packet
while (P0_6);

//------------------------------------------------------------------
// RX (IOCFG0 = 0x06)

halSpiStrobe(CCxxx0_SRX);

// Wait for GDO0 to be set -> sync received
while (!P0_6);

// Wait for GDO0 to be cleared -> end of packet
while (P0_6);

length = halSpiReadByte(CCxxx0_RXFIFO);
halSpiReadBurstReg(CCxxx0_RXFIFO, rxBuffer, length);
```

Be aware that even if the packet size can be 64 bytes, the size of the data field will vary depending on the register settings (address filtering, append status, etc).

	Fixed Packet Length Mode, TX	
Packet Size	**TX FIFO**	**Comment**
1 (min)	Addr	Address. No data bytes
1	D_0	No address, 1 data byte
64 (max)	Addr, D_0, D_1,.., D_{62}	Address + 63 data bytes
64	D_0, D_1,.., D_{63}	No address, 64 data bytes
	Fixed Packet Length Mode, RX	
1 (min)	**RX FIFO**	**Comment**
1	Addr	Address. No data bytes
64 (max)	D_0	No address, 1 data byte
64	Addr, D_0, D_1,.., D_{62}	Address + 63 data bytes
64	D_0, D_1,.., D_{63}	No address, 64 data bytes
64	Addr, D_0, D_1,.., D_{60}, RSSI, LQI	Address + 61 data bytes + 2 status bytes
64	D0, D1, D61, RSSI, LQI	No address, 62 data bytes + 2 status bytes
	Variable Packet Length, TX	
	TX FIFO	**Comment**
2 (min)	1, Addr	Length byte + address. No data bytes
2	1, D_0	Length byte + 1 data byte
64 (max)	63, Addr, D_0, D_1,.., D_{61}	Length byte + address + 62 data bytes
64	63, D_0, D_1,.., D_{62}	Length byte + 63 data bytes
	Variable Packet Length, RX	
	RX FIFO	**Comment**
2 (min)	1, Addr	Length byte + address. No data bytes
2	1, D_0	Length byte + 1 data byte
64 (max)	63, Addr, D_0, D_1,.., D_{61}	Length byte + address + 62 data bytes
64	63, D_0, D_1,.., D_{62}	Length byte + 63 data bytes
64	61, Addr, D_0, D_1,.., D_{59}, RSSI, LQI	Length byte + address + 60 data bytes + 2 status bytes
64	61, D_0, D_1,.., D_{60}, RSSI, LQI	Length byte + 61 data bytes + 2 status bytes

Table 1. Packet Size vs. Data Field Length

The Link example (see [1] and [2]) demonstrates how to transmit and receive packets with packet size ≤ 64 bytes (the example implements variable packet length mode and append status).

2.2 Packet Size ≤ 255 Bytes

It is fully possible to transmit and receive packets with packet size up to 255 bytes, but the firmware will be more complex since the TX FIFO will need to be refilled while in TX and the RX FIFO needs to be read while in RX. There are two different ways to implement this in firmware. One can either have the MCU poll status registers on the SPI or one can have an interrupt driven solution. Both fixed and variable packet length mode can be used.

2.2.1 SPI Polling

The status byte returned on the MISO line or the TXBYTES or RXBYTES register can be polled at a given rate after strobing TX or RX, to see if there is room for more bytes in the TX FIFO or more bytes to read from the RX FIFO.

TX:

1. Start by writing 64 bytes to the TX FIFO
2. Strobe TX
3. Poll the status byte or the TXBYTES register at a given rate to see if there is space available in the TX FIFO.
4. Write to the TX FIFO whenever there is room for more bytes
5. Repeat 3 and 4 until the whole packet is written to the TX FIFO

RX:

1. Strobe RX
2. Poll the status byte or the RXBYTES register at a given rate to see if there is bytes to read from the FIFO
3. Read the RX FIFO whenever there is something to read
4. Repeat 2 and 3 until the whole packet is received

Link1 demonstrates how to implement SPI polling and can be found on the TI website (see [1] and [2]).

2.2.2 Interrupt Driven Solution

In this case, GDO0 and GDO2 are used to give interrupt to the MCU. One of the pins gives an interrupt when the RX FIFO is filled above RXFIFO_THR in RX and when number of bytes in the TX FIFO is below the TXFIFO_THR in TX. The other pin gives an interrupt both when sync word has been received and when the whole packet has been received in RX, and when the packet has been transmitted in TX. The Link2 example implements an interrupt driven solution and can be found together with all the other software examples at the TI web site ([1]).

2.3 Packet Size > 255 bytes

Infinite packet length mode can be used if one wants to transmit and/or receive until TX or RX mode is turned off manually (can be used for all packet lengths, also packets with length less than 255). In this case, it will not be possible to have CRC automatically generated in TX or processed in RX, since the chip does not know the length of the packet. However, infinite packet length mode is most useful in combination with fixed packet length mode in cases where one wants to transmit or receive packets with packet size > 255, and have automatic CRC insertion and processing.

Assume a packet with packet size 452 is to be transmitted.

- Set PKTCTRL0.LENGTH_CONFIG = 2 (10) (Infinite packet length).
- Pre-program the PKTLEN register to mod(452,256) = 196.
- Transmit at least 197 bytes (less than 256 bytes left to transmit)
- Set PKTCTRL0.LENGTH_CONFIG = 0 (00) (Fixed packet length).
- The transmission ends when the packet counter reaches 196. A total of 452 bytes are transmitted.

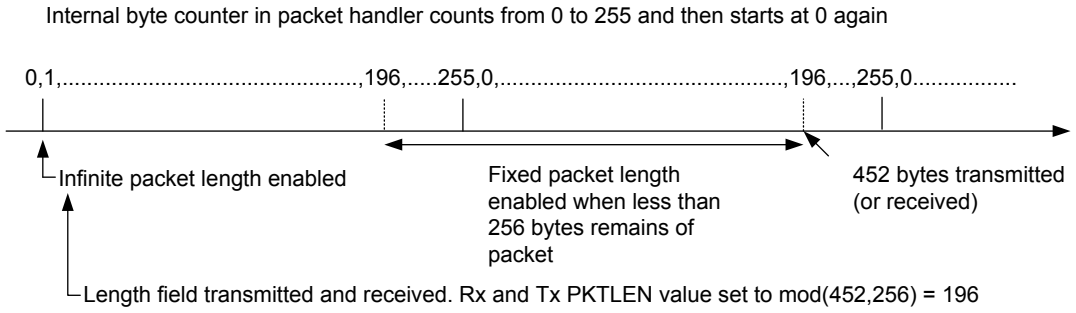

Figure 2. Infinite Packet Length Mode in Combination Fixed Packet Length Mode

With the infinite packet length example described here one can choose between using SPI polling or an interrupt driven solution. The InfiniteLink example demonstrates how an interrupt driven solution can be used for packets longer than 255 bytes. All the examples that

have been referred to are documented in the CC1100/CC1150DK & CC2500/CC2550DK Development Kit Examples and Libraries User Manual ([2]). Be aware that if using address filtering, PKTCTRL1.ADR_CHK = 1, 2, or 3, and the received address matches the address of the receiver, 0xFF will be written into the RX FIFO followed by the address byte and then the payload data.

3 Errata Notes

When using SPI polling, be aware that due to a bug affecting the synchronization mechanism between the SPI clock domain and the internal 26 MHz clock domain sometimes incorrect read values for register fields that are continuously updated will occur. It is also important to notice that for both methods (SPI polling and interrupt driven) one should also make sure that the RX FIFO is never emptied before the whole packet has been received (1 byte needs to be left in the RX FIFO). Please see [3], [4], [5], [6], [7], and [8]

4 References

[1] CC1100 CC2500 Examples Libraries (swrc021.zip)

[2] CC1100/CC1150DK & CC2500/CC2550DK Development Kit Examples & Libraries User Manual (swru109.pdf)

[3] CC1100 Errata Notes (swrz012.pdf)

[4] CC1100E Errata Notes (swrz029.pdf)

[5] CC1101 Errata Note (swrz020.pdf)

[6] CC1150 Errata Notes (swrz018.pdf)

[7] CC2500 Errata Notes (swrz002.pdf)

[8] CC2550 Errata Notes (swrz011.pdf)

5 General Information

5.1 Document History

Revision	Date	Description/Changes
SWRA109C	2009.04.01	Added CC110E.
SWRA109B	2007.10.22	Added chapter 4. Added CC1101. Removed logo in header.
SWRA109A	2006.10.20	Added info about address filtering when using infinite packet length mode.
SWRA109	2006.07.06	Initial release.

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