Steam-Age Evaluation of Nickel/Palladium Lead Finish for Integrated Circuits

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Contents

Title

Title	Page
Abstract	1
Background	1
Procedure and Test Results	2
Cross-Section After Board Mount	
Wetting-Balance Test	
Lead Pull	6
Surface-Mount Solderability Test	7
Surface Analysis	
Conclusion	
Acknowledgment	
References	10

List of Illustrations

Figure	Title	Page
1	51 Months of Shelf Storage	3
2	9 Months of Shelf Storage	3
3	9 Months of Shelf Storage + 1 Hour of Steam Aging	3
4	9 Months of Shelf Storage + 8 Hours of Steam Aging	3
5	Contact-Angle Measurements vs Age	4
6	Typical Wetting-Balance Curve	5
7	Average Time to Zero vs Age	6
8	Average Time to Zero vs Pd Thickness	6
9	Lead-Pull Force vs Shelf-Aging Time	7
10	51 Months of Shelf Storage	8
11	9 Months of Shelf Storage	8
12	9 Months of Shelf Storage + 1 Hour of Steam Aging	8
13	9 Months of Shelf Storage + 8 Hours of Steam Aging	8

Abstract

Removal of lead (Pb) from finished integrated-circuit (IC) packages, as well as IC package assembly and printed circuit board (PCB) assembly operations, is an ongoing effort by many electronics manufacturers. Toward this end, the semiconductor industry is converting to nickel/palladium (Ni/Pd)-finished leadframes in the assembly of integrated circuits. This technology eliminates Pb from the IC package. The best estimates are that more than 30 billion ICs are in the field with Ni/Pd-finished leads.

Historically, users of IC components have employed steam aging prior to solderability testing to simulate accelerated aging of devices, to stress devices to accentuate or magnify lead-finish defects, and to provide a "guard band" of performance for incoming product inspection. Preconditioning of IC leads by steam aging is well known and established for solderability testing of tin/lead (Sn/Pb)-finished leads. This study compares solderability performance of Ni/Pd-finished components, both after steam aging and shelf storage, to determine the relevance of steam aging for preconditioning Ni/Pd-finished IC packages.

Several groups of Ni/Pd-finished ICs were chosen for testing. Units that had been stored on a shelf in a warehouse environment for up to 51 months were used as a baseline for comparison. Recently built units (9 months old) were also tested with no steam aging, 1-hour steam aging, and 8-hour steam aging. Tests performed were wetting balance, measurement of the palladium thickness, cross-section after board mount, solderability test per ANSI/EIA-638, lead pull, and surface analysis using Auger electron spectroscopy.

Mechanical and solderability tests showed good results for all groups. However, the wetting-balance test showed delayed wetting for the steam-aged groups. Surface analysis of all groups showed that silicon (Si) and elevated carbon (C) were found on the surface of the steam-aged units. No Si was seen on shelf-aged units. These artifacts of the steam-aging test method do not correlate with normal aging or normal stressing of the package leads and can contribute to erroneous solderability test results. Previous studies have shown that constituents of the mold compound are picked up in the steam during steam aging and deposited onto the surface of the leads. Silicon and carbon are major components of the mold compound and hinder dissolution of the palladium when deposited onto the leads during steam-aging exposure.

Background

Ni/Pd finished leads offer several advantages to the IC maker and the end user ^{1,2,3,4}. This finish eliminates Pb from the IC manufacturing process and, when used with a Pb-free solder paste, allows elimination of Pb from the final electronic product ^{5,6,7,8}. Other advantages that accrue to the leadframe maker are elimination of cyanide from the process flow, elimination of selective plating, and use of simplified, high-speed manufacturing flow. For the IC assembly operation this finish removes the need for solder-plating equipment and associated personnel, waste treatment, process water supply, and floor space required for these operations. Use of Ni/Pd plated leadframes also reduces cycle time, eliminates solder flakes and burrs in the trim/form operation, and improves lead tip planarity. At the board level, this finish was designed to be a drop-in replacement for Sn/Pb-finished leads.

The process of steam aging consists of placing IC units above boiling water inside a test chamber for a specified period of time. Typically, the test specimens are located 1.5 to 3 inches above the boiling water. There are two types of steam-aging systems in use. One type is a glass beaker that sits on a hot plate and is filled with deionized water to a specified level. The ICs rest on a perforated plastic or ceramic plate suspended above the water. The second type of steam-aging system is a rectangular box made of Teflon[™]-coated stainless steel. With this system, the units are placed in drawers that are inserted into the chamber. Each drawer has a perforated bottom panel that allows the steam to pass through. After steam aging by either system, the IC units are tested for solderability using various standard test methods.

Currently, in ANSI/J-STD-002 ⁹ Ni/Pd-finished components are considered "Category 2: ...non Sn/Pb finishes," requiring 1 hour of steam aging prior to testing for solderability. The default steam aging time for Sn and Sn/Pb finished components is 8 hours.

Teflon is a trademark of E. I. du Pont de Nemours and Company.

A major issue encountered during the implementation of Ni/Pd finish at a new user (IC assembly site or PCB assembly house) is solderability test performance after steam aging. When performed with well-controlled equipment and procedures, steam aging presents no problems for Ni/Pd-finished components. However, when control is lacking, either in the performance of the test or maintenance of the equipment, solderability test performance after steam aging can be impacted negatively.

Historically, dip-and-look solderability testing of steam-aged Ni/Pd-finished components can result in small solder voids on the surface of the leads. When analyzed using Auger electron spectroscopy, these voids show a layer of C covering Pd at the bottom of the nonwet area. The reason is that a C-rich coating is deposited during the steam-aging process. The C layer masks the Pd surface from contact with the molten solder and prevents dissolution of the Pd and contact with the Ni by the solder.

This study was undertaken to evaluate board-mount and solderability test performance of Ni/Pd-finished components of various ages and after steam aging.

Procedure and Test Results

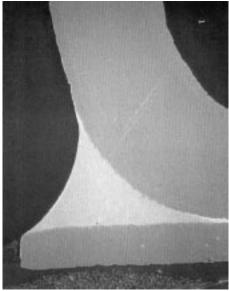
Seven groups of 20-pin small-outline integrated-circuit (SOIC) packages were tested in this evaluation (see Table 1). The units tested included four groups of Ni/Pd finished components that had been stored on a shelf in a warehouse environment for various times. Recently built units also were tested with no steam aging, 1-hour steam aging, and 8-hour steam aging.

GROUP	AGE
1	51 months
2	38 months
3	25 months
4	23 months
5	9 months
6	9 months + 1 hour of steam aging
7	9 months + 8 hours of steam aging

Table 1. Aging Time of 20-Pin SOIC Packages Used in the Evaluation

Cross-Section After Board Mount

Units from each of the seven groups were mounted on PCBs using an industry-standard water-soluble solder paste ¹⁰. The reflow oven used was a BTU model VIP98A convection reflow with no nitrogen purge. After board mounting, individual units from each group were sectioned to document the contact angle to the backside of the lead. The contact angle is the angle formed by the tangent to the backside of the lead and the tangent to the solder fillet at the point of contact of the lead with the fillet. In general, lower contact angles indicate a soldering condition that has produced good results; higher contact angles indicate either a situation where the wetting rate has been decreased or where the equilibrium wetting point has changed ¹¹. Typical cross-section results for groups 1, 5, 6, and 7 are shown in Figures 1, 2, 3, and 4. Visual results show good solder wetting on all seven groups independent of shelf storage time or steam exposure.



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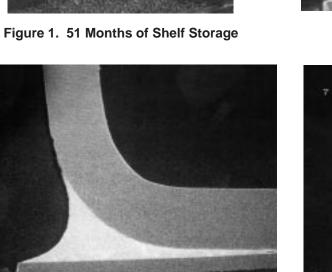


Figure 3. 9 Months of Shelf Storage + 1 Hour of Steam Aging

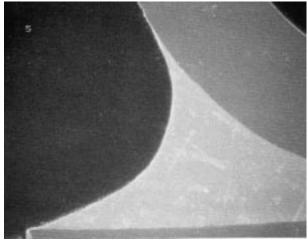


Figure 2. 9 Months of Shelf Storage

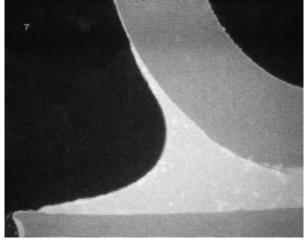
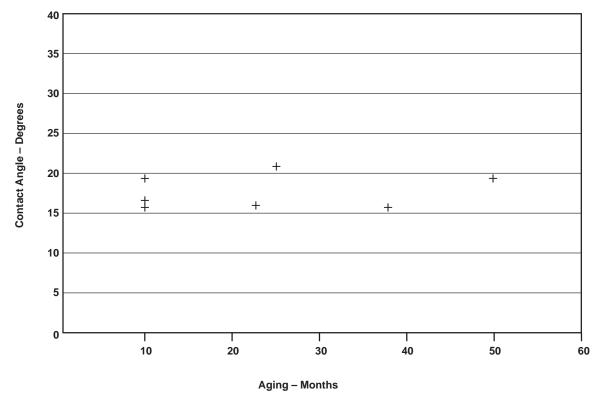


Figure 4. 9 Months of Shelf Storage + 8 Hours of Steam Aging



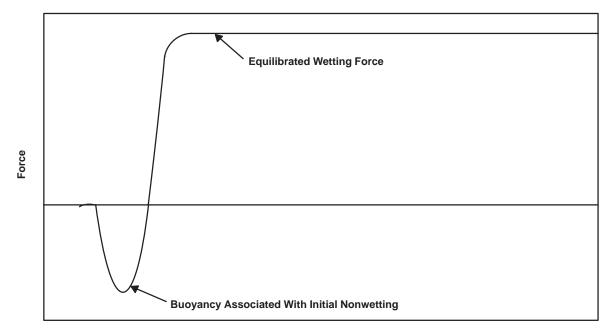
Contact-angle measurements were taken for each of the seven groups and the average for each group is shown in Figure 5. Steam aging or shelf aging appeared to have no effect on contact angle.

Figure 5. Contact-Angle Measurements vs Age

Wetting-Balance Test

The wetting-balance test can be used to test wettability of IC leads. The wetting-balance test is classified in ANSI/J-STD-002 as a "Test Without Established Accept/Reject Criterion." This test method is recommended for engineering evaluations only, not as a production pass/fail monitor.

The wetting-balance test measures the forces imposed by the molten solder on the test specimen (IC lead) as the specimen is dipped into and held in the solder bath. This wetting force is measured as a function of time and plotted. A typical wetting-balance curve is shown in Figure 6.



Time



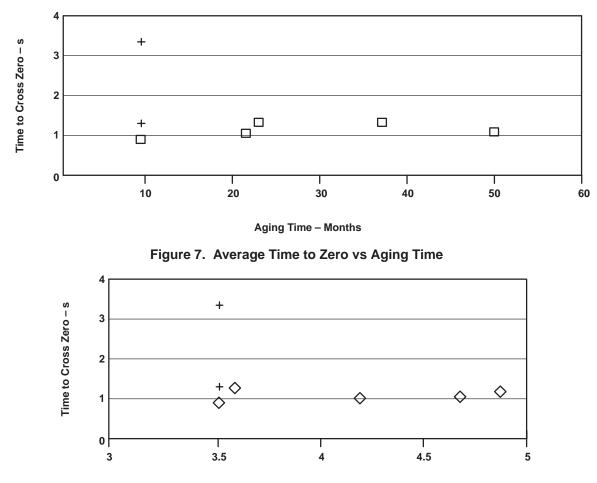
Initially, the force is negative, indicating that the solder has not begun to wet the specimen and, in fact, shows a bouyancy effect. The force exerted by the solder approaches zero as the solder begins to wet to the specimen. One commonly used performance measure is the time to cross the zero axis of wetting force. This point indicates the transition from nonwetting (F<0) to wetting (F0).

Wetting-balance measurements were taken for each group. Ten readings were taken per group and the average time to zero for each group was recorded. Palladium-thickness readings also were taken on each group to see if the thickness of the palladium had any impact on wetting time. Palladium-thickness measurements and wetting-balance readings are shown in Table 2.

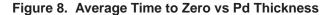
GROUP	AGING (months)	Pd THICKNESS (microinches)	TIME TO CROSS ZERO (seconds)		
1	51	4.7	1.09		
2	38	4.9	1.41		
3	25	3.6	1.35		
4	23	4.2	1.02		
5	9	3.5	0.75		
6	9 months + 1 hour of steam aging	3.5	1.38		
7	9 months + 8 hours of steam aging	3.5	3.37		

Table 2. Palladium-Thickness Measurements and Wetting-Balance Readings

Time-to-zero is plotted against aging time and palladium thickness in Figures 7 and 8.



Palladium Thickness – Microinches



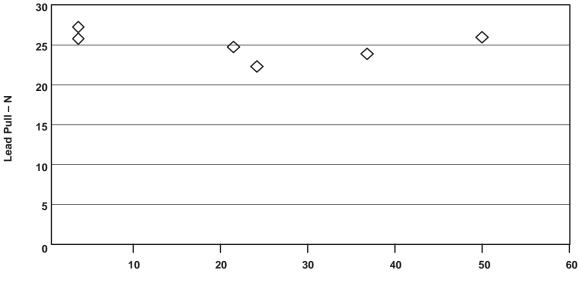
The time-to-zero values for the steam-aged groups are shown with a "+". Results indicate that wetting time is not affected by normal shelf storage. However, steam aging did have a dramatic impact on wetting time for both 1-hour and 8-hour steam aging. Palladium thickness for these samples had no impact on wetting time.

Lead Pull

Lead-pull testing was performed to determine the mechanical force needed to pull the individual IC leads from the PCB land pattern after soldering. First, to allow for access to an individual lead on the PCB, the leads are cut near the package body. Next, with the leads separated from the package body, the PCB is fastened in a test fixture. Then the lead is pulled until it separates from the PCB. The force needed to pull the lead from the PCB is measured and recorded.

Lead pull was performed on ten units from each of the seven groups. The average lead-pull value for each group is plotted against shelf-aging time of the components in Figure 9.

Lead-pull values for groups 5, 6, and 7 overlap, indicating that steam age had no impact on lead-pull strength, contrary to the impact on wetting-balance performance. In fact, there is no significant difference between any of the seven groups in lead-pull results, indicating good adhesion to the PCB, independent of shelf age.



Shelf-Aging Time – Months

Figure 9. Lead-Pull Force vs Shelf-Aging Time

Surface-Mount Solderability Test

Solderabilility testing was performed per the ANSI/EIA-638 Surface Mount Solderability Test method ¹². This test procedure begins with screening solder paste onto a 0.035-inch-thick ceramic plate using a solder stencil. The paste print mirrors the pattern of the leads to be tested. The devices to be tested are then placed onto the solder paste print. The ceramic substrate is processed through a reflow cycle, then allowed to cool. After reflow, the units are removed from the ceramic and inspected. The benefit of this test method is that the IC devices are subjected to the same reflow environment as used in actual processing, and use of a ceramic substrate allows for inspection of the surface to be soldered.

Pass/fail criteria indicated in ANSI/EIA-638 says "all terminations shall exhibit a continuous solder coating free from defects for a minimum of 95% of the critical surface area of any individual termination. Anomalies other than dewetting, nonwetting, and pinholes are not cause for rejection." The critical surface area for gull-wing components is defined as the underside of the lead up to $1\times$ the thickness of the lead and the edges (sides) also up to $1\times$ the lead thickness. Units from all seven groups were tested and inspected per ANSI/EIA-638. Typical solderability test results for groups 1, 5, 6, and 7 are shown in Figures 10, 11, 12, and 13. No failures were seen on any of the groups when this solderability test method was used.

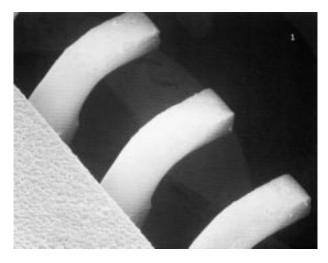


Figure 10. 51 Months of Shelf Storage

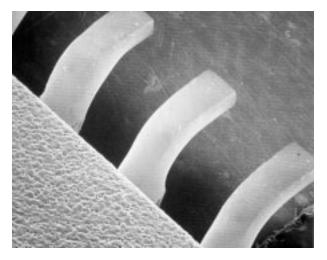


Figure 11. 9 Months of Shelf Storage

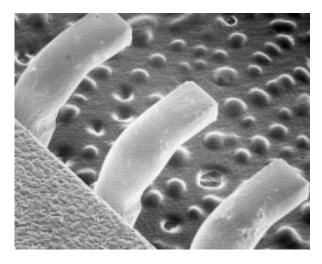


Figure 12. 9 Months of Shelf Storage + 1 Hour of Steam Aging

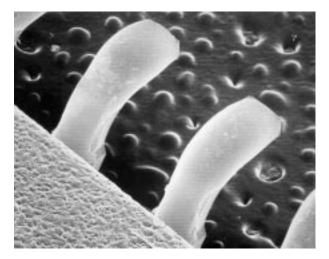


Figure 13. 9 Months of Shelf Storage + 8 Hours of Steam Aging

Surface Analysis

Surface analysis of the leads was performed on units from each group. Auger electron spectroscopy was used to scan the surface of the leads and identify the chemicals present. This surface analytical technique is widely applied to determine chemical composition of solid-state surfaces and interfaces in various fields of materials research. Results are presented in Table 3.

		ELEMENTAL CONTENT ON SURFACE (ATOMIC %)							
GROUP	AGE	S	С	Pd	N	0	Ni	Cu	Si
1	51 months	6.9	46.7	26.4	7.4	12.6	0	0	0
2	38 months	10.9	27.8	47.6	6.0	7.7	0	0	0
3	25 months	11.2	46.4	35.4	3.0	4.1	0	0	0
4	23 months	5.0	44.7	34.5	5.7	10.1	0	0	0
5	9 months	4.3	63.1	25.1	2.8	4.7	0	0	0
6	9 months + 1 hour of steam aging	0.5	80.7	1.0	2.9	4.8	0	0	10.1
7	9 months + 8 hours of steam aging	2.3	55.4	14.1	3.2	8.7	0.2	0.8	15.2

Table 3. Auger Electron Spectroscopy Surface-Analysis Results

The Auger spectra were taken on the foot of the leads from each group. All of the data on the groups that were not subjected to steam aging is fairly consistent, with Pd in the range of 25-50%, carbon (C) being 25-65%, and the balance was small amounts of sulfur (S) and nitrogen (N). For the steam-aged samples, the Pd levels are less than 15%, C in the range of 50-80%, and significant silicon (Si) in the range of 10-15%. No Si was seen on any of the shelf-aged units, only on the steam-aged units. Silicon is a major component of the mold compound used to encapsulate the package and, along with carbon, hinders dissolution of the palladium when deposited onto the leads during steam-aging.

Occasionally, failures are seen during dip-and-look solderability testing of Pd-finished components. Previous work has shown that the majority of steam-aged palladium solderability nonwets result from the palladium adsorbing an organic compound by during the steam-aging process. The organic has been identified as mold compound or some constituent of the mold compound using Fourier Transform Infrared Spectroscopy (FTIR). The same organic also has been found in the steam-aging water. The silicon seen on steam-aged units during this study correlates with this previous work that identified mold compound constituents on the leads and in the steam-aging water. The fact that the steam-aging process can cause the leads to be coated with mold compound residue, thus inhibiting dissolution of the palladium, indicates that steam aging is not a valid preconditioning method for Pd-finish IC packages.

Conclusion

All of the tests performed, except wetting balance and Auger electron spectroscopy analysis, showed good correlation between the steam-aged samples and the natural shelf-aged samples. The wetting-balance test showed a marked degradation in wetting time for the steam-aged samples. The Auger results show the presence of atypical Si contamination and elevated C on the surface of the steam-aged samples when compared to shelf-aged samples.

From the results shown in this application report and the experience noted with steam-age testing of both solder finished and Ni/Pd finished parts in commercial use, it can be concluded that steam-age exposure inordinately affects solderability test performance of Ni/Pd-finished units. This statement particularly applies if pass/fail is based on either wetting-balance or dip-and-look testing. Steam aging is not a proper preconditioning treatment for Ni/Pd-finished components because constituents of the mold compound can be deposited on the surface of the leads, a phenomenon which does not occur naturally. This view is supported by the wholly different mechanisms of soldering for the two finishes — dissolution of Pd versus reflow of Sn/Pb — that render leads more susceptible to solderability test failures caused by contamination of the lead surface during steam aging.

Acknowledgment

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