

## SN74AUP1T97 Single-Supply Voltage-level Translator With Nine Configurable Gate Logic Functions

### 1 Features

- Available in the Texas Instruments NanoStar™ Packages
- Single-Supply Voltage Translator
- 1.8 V to 3.3 V (at  $V_{CC} = 3.3$  V)
- 2.5 V to 3.3 V (at  $V_{CC} = 3.3$  V)
- 1.8 V to 2.5 V (at  $V_{CC} = 2.5$  V)
- 3.3 V to 2.5 V (at  $V_{CC} = 2.5$  V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- $I_{off}$  Supports Partial-Power-Down Mode With Low Leakage Current (0.5  $\mu$ A)
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SON (DRY or DSF), SOT-23 (DBV), SC-70 (DCK), and NanoStar WCSP
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Related Devices: SN74AUP1T98, SN74AUP1T57, and SN74AUP1T58

### 2 Description

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T97 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V  $V_{CC}$  supply.

The wide  $V_{CC}$  range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ( $\Delta V_T = 210$  mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T97 can be easily configured to perform a required gate function by connecting A, B, and C inputs to  $V_{CC}$  or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.

$I_{off}$  is a feature that allows for powered-down conditions ( $V_{CC} = 0$  V) and is important in portable and mobile applications. When  $V_{CC} = 0$  V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

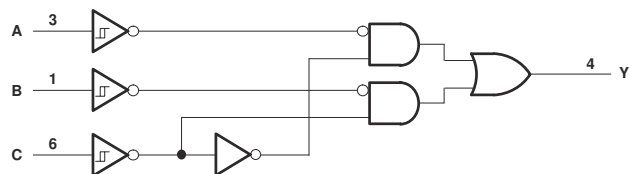
The SN74AUP1T97 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74AUP1T97DBV	SOT-23 (6)	2.9mm x 1.6mm
SN74AUP1T97DCK	SC70 (6)	2.0mm x 1.25mm
SN74AUP1T97DRY	SON (6)	1.45mm x 1.0mm
SN74AUP1T97DSF	SON (6)	1.0mm x 1.0mm
SN74AUP1T97YFP	DSBGA (6)	1.0mm x 1.4mm
SN74AUP1T97YZP	DSBGA (6)	1.75mm x 1.25mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



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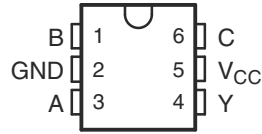
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### 3 Revision History

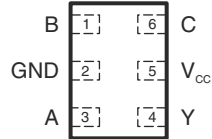
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision I (May 2010) to Revision J (September 2020)</b>	<b>Page</b>
• Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table, see <i>Mechanical, Packaging, and Orderable Information</i> at the end of the data sheet.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

## 4 Pin Configuration and Functions



**Figure 4-1. DBV OR DCK Package 6-Pin SOT-23 or SC70 Top View**



**Figure 4-2. DRY OR DSF Package 6-Pin SON Top View**



**Figure 4-3. YFP OR YZP Package 6-Pin DSBGA Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	4.6	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>		-0.5	4.6	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		-0.5	4.6	V
V <sub>O</sub>	Output voltage range in the high or low state <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±20	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

See<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>I</sub>	Input voltage		0	3.6	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V		-3.1	mA
		V <sub>CC</sub> = 3 V		-4	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V		3.1	mA
		V <sub>CC</sub> = 3 V		4	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AUP1T97				UNIT
	DBV (SOT-23)	DCK (SC70)	DRY (SON)	DSF (SON)	
	6 PINS	6 PINS	6 PINS	6 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	165	259	340	300	°C/W
R <sub>θJC(top)</sub> Junction-to-case (top) thermal resistance					°C/W
R <sub>θJB</sub> Junction-to-board thermal resistance					°C/W
ψ <sub>JT</sub> Junction-to-top characterization parameter					°C/W
ψ <sub>JB</sub> Junction-to-board characterization parameter					°C/W
R <sub>θJC(bot)</sub> Junction-to-case (bottom) thermal resistance					°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AUP1T97		UNIT
	YFP (DSBGA)	YZP (DSBGA)	
	6 PINS	6 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	123	123	°C/W
R <sub>θJC(top)</sub> Junction-to-case (top) thermal resistance			°C/W
R <sub>θJB</sub> Junction-to-board thermal resistance			°C/W
ψ <sub>JT</sub> Junction-to-top characterization parameter			°C/W
ψ <sub>JB</sub> Junction-to-board characterization parameter			°C/W
R <sub>θJC(bot)</sub> Junction-to-case (bottom) thermal resistance			°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
		3 V to 3.6 V	0.75		1.16	0.75	1.19	
V <sub>T-</sub> Negative-going input threshold voltage		2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
		3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
		3 V to 3.6 V	0.25		0.56	0.15	0.56	
V <sub>OH</sub>	I <sub>OH</sub> = -20 μA	2.3 V to 3.6 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1		V
	I <sub>OH</sub> = -2.3 mA	2.3 V	2.05			1.97		
	I <sub>OH</sub> = -3.1 mA		1.9			1.85		
	I <sub>OH</sub> = -2.7 mA	3 V	2.72			2.67		
	I <sub>OH</sub> = -4 mA		2.6			2.55		
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	2.3 V to 3.6 V				0.1		V
	I <sub>OL</sub> = 2.3 mA	2.3 V				0.33		

## 5.6 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
	I <sub>OL</sub> = 3.1 mA	3 V			0.44		0.45	
	I <sub>OL</sub> = 2.7 mA				0.31		0.33	
	I <sub>OL</sub> = 4 mA				0.44		0.45	
I <sub>I</sub>	All inputs V <sub>I</sub> = 3.6 V or GND	0 V to 3.6 V			0.1		0.5	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V			0.1		0.5	μA
ΔI <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0 V to 0.2 V			0.2		0.5	μA
I <sub>CC</sub>	V <sub>I</sub> = 3.6 V or GND, I <sub>O</sub> = 0	2.3 V to 3.6 V			0.5		0.9	μA
ΔI <sub>CC</sub>	One input at 0.3 V or 1.1 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	2.3 V to 2.7 V					4	μA
	One input at 0.45 V or 1.2 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	3 V to 3.6 V					12	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.5				pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		3				pF

## 5.7 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 1.8 V ± 0.15 V (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

## 5.8 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

## 5.9 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	

### 5.9 Switching Characteristics (continued)

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_I = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

### 5.10 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

### 5.11 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

### 5.12 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

### 5.13 Operating Characteristics

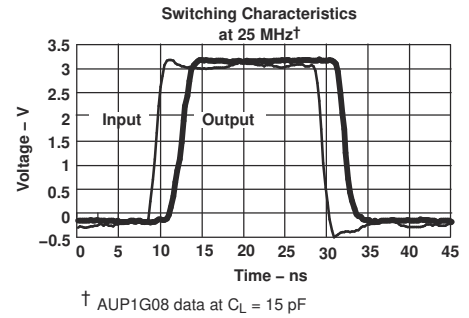
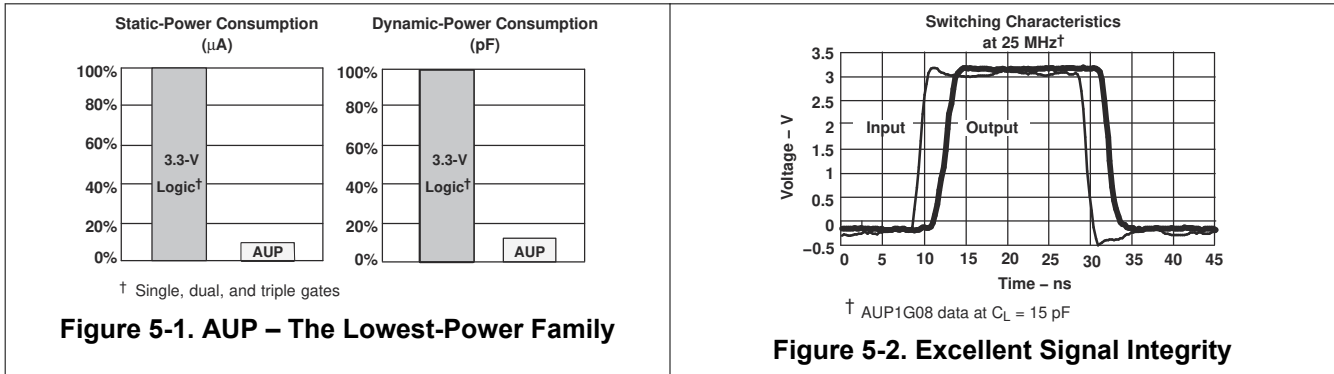
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	4	5	pF

**SN74AUP1T97**

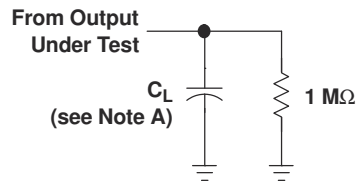
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**5.14 Typical Characteristics**



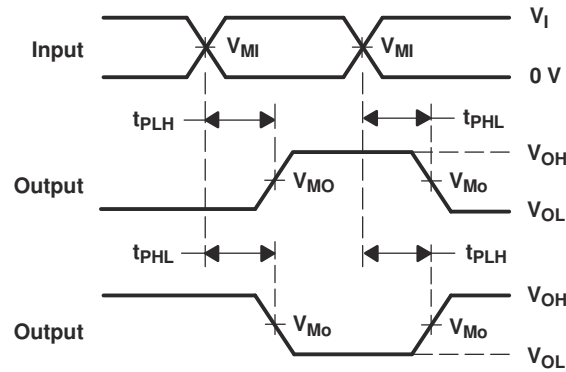


## 6 Parameter Measurement Information



LOAD CIRCUIT

	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_{MI}$	$V_I/2$	$V_I/2$
$V_{MO}$	$V_{CC}/2$	$V_{CC}/2$



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ , slew rate  $\geq$  1 V/ns.  
 C. The outputs are measured one at a time, with one transition per measurement.  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Functional Block Diagram

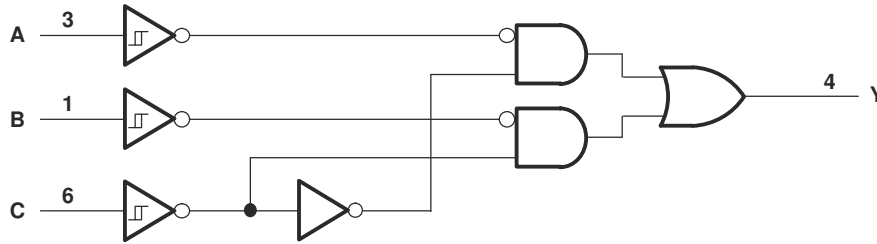


Figure 7-1. Logic Diagram (Positive Logic)

### 7.2 Feature Description

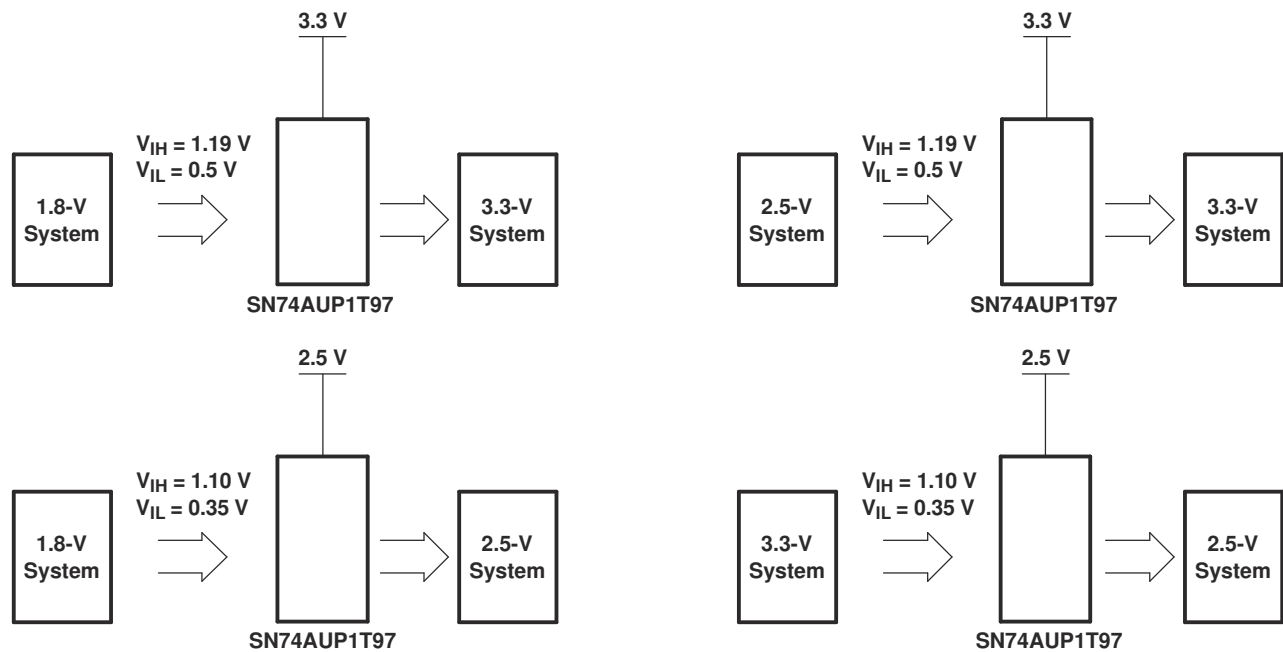


Figure 7-2. Possible Voltage-Translation Combinations

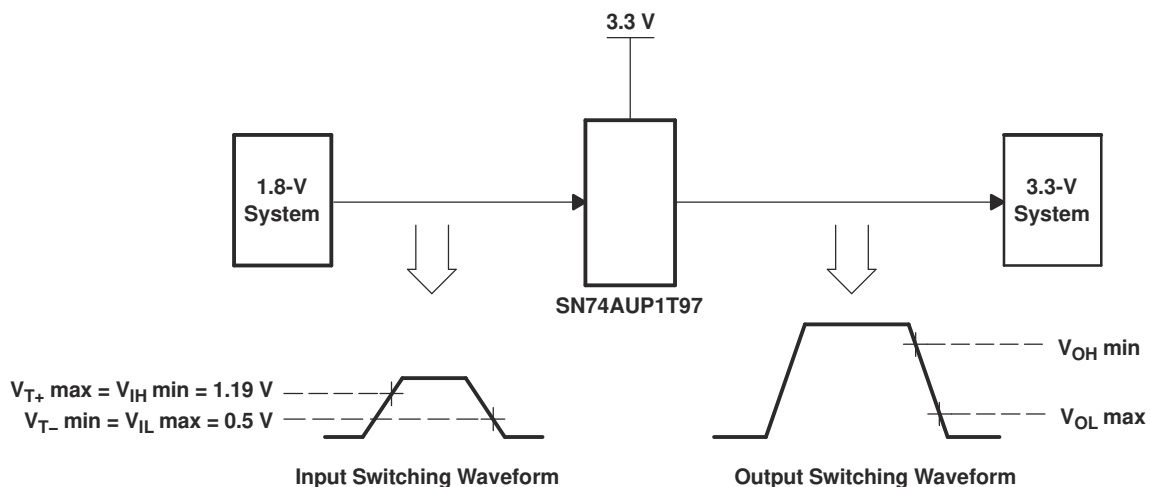


Figure 7-3. Switching Thresholds for 1.8-V to 3.3-V Translation

### 7.3 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AUP1T97.

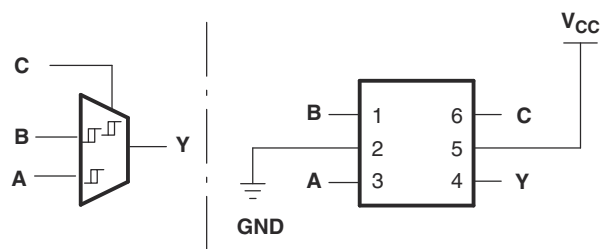
**Table 7-1. Function Table**

INPUTS			OUTPUT Y
C	B	A	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

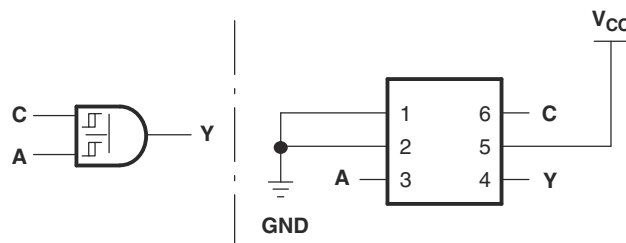
#### 7.3.1 Logic Configurations

**Table 7-2. Function Selection Table**

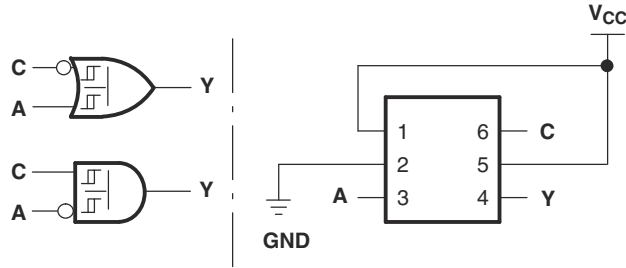
LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	7-4
2-input AND gate	7-5
2-input OR gate with one inverted input	7-6
2-input NAND gate with one inverted input	7-6
2-input AND gate with one inverted input	7-7
2-input NOR gate with one inverted input	7-7
2-input OR gate	7-8
Inverter	7-9
Noninverted buffer	7-10



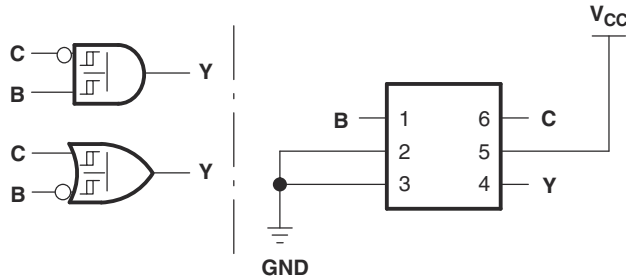
**Figure 7-4. 157: 2-to-1 Data Selector/MUX**  
 When C is L, Y = B  
 When C is H, Y = A



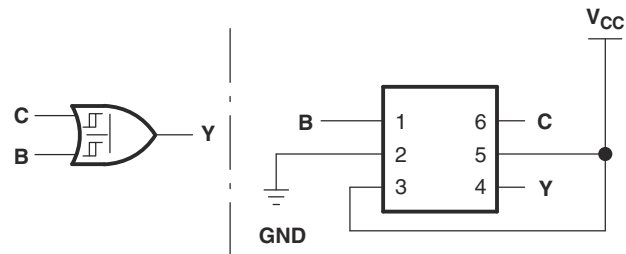
**Figure 7-5. 08: 2-Input AND Gate**



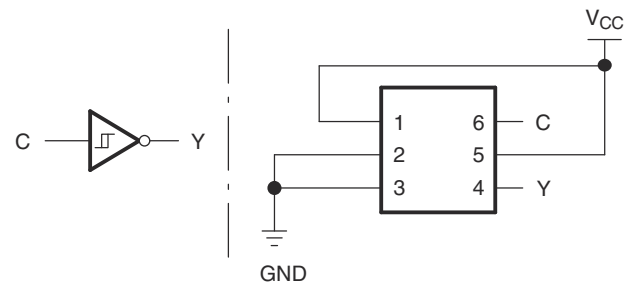
**Figure 7-6. 14+32/14+00: 2-Input OR/NAND Gate With One Inverted Input**



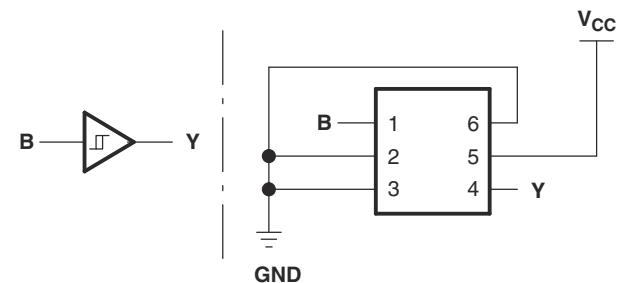
**Figure 7-7. 14+08/14+02: 2-Input AND/NOR Gate With One Inverted Input**



**Figure 7-8. 32: 2-Input OR Gate**



**Figure 7-9. 04/14: Inverter**



**Figure 7-10. 17/34: Noninverted Buffer**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

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All other trademarks are the property of their respective owners.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T97DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT4R	<a href="#">Samples</a>
SN74AUP1T97DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HT4F, HT4R)	<a href="#">Samples</a>
SN74AUP1T97DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(THF, THR)	<a href="#">Samples</a>
SN74AUP1T97DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(THF, THR)	<a href="#">Samples</a>
SN74AUP1T97DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TH	<a href="#">Samples</a>
SN74AUP1T97DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TH	<a href="#">Samples</a>
SN74AUP1T97YFPR	ACTIVE	DSBGA	YFP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TH2, THN)	<a href="#">Samples</a>
SN74AUP1T97YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TH2, THN)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T97DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T97DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T97DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T97DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T97DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1T97DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1T97DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1T97YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1T97YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T97DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T97DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T97DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T97DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T97DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1T97DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1T97DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1T97YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1T97YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

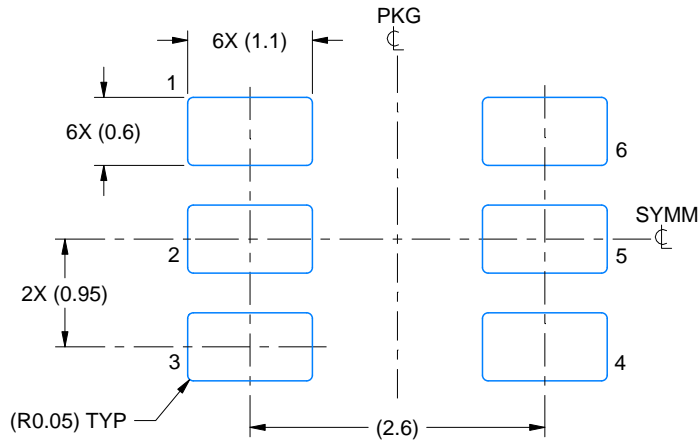


# EXAMPLE BOARD LAYOUT

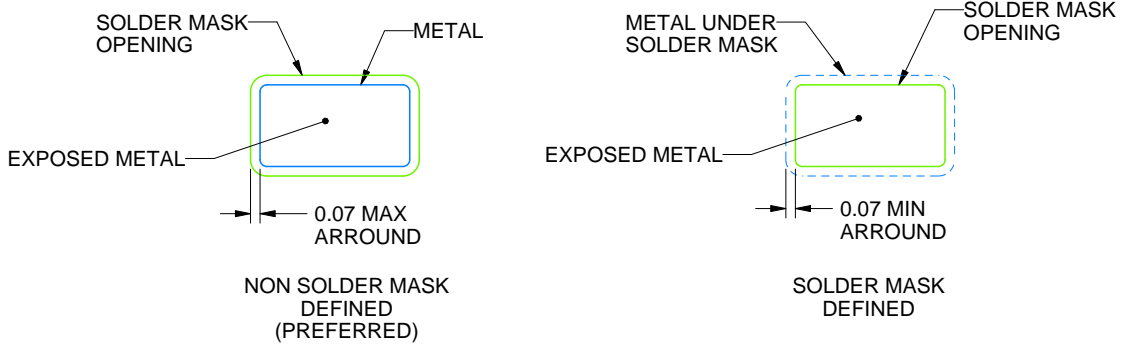
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

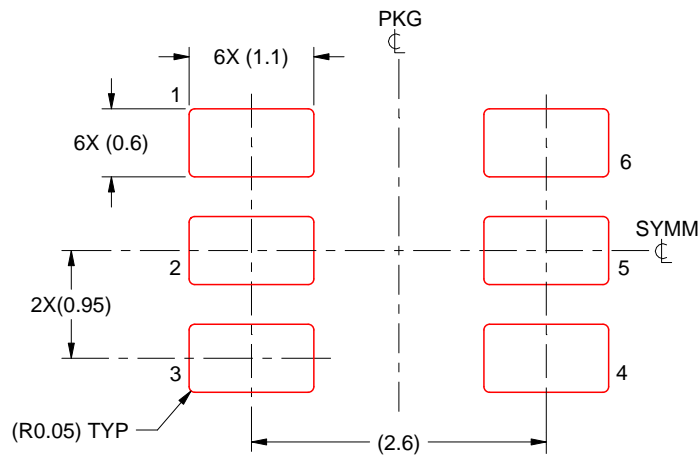
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.

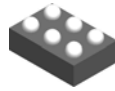
DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

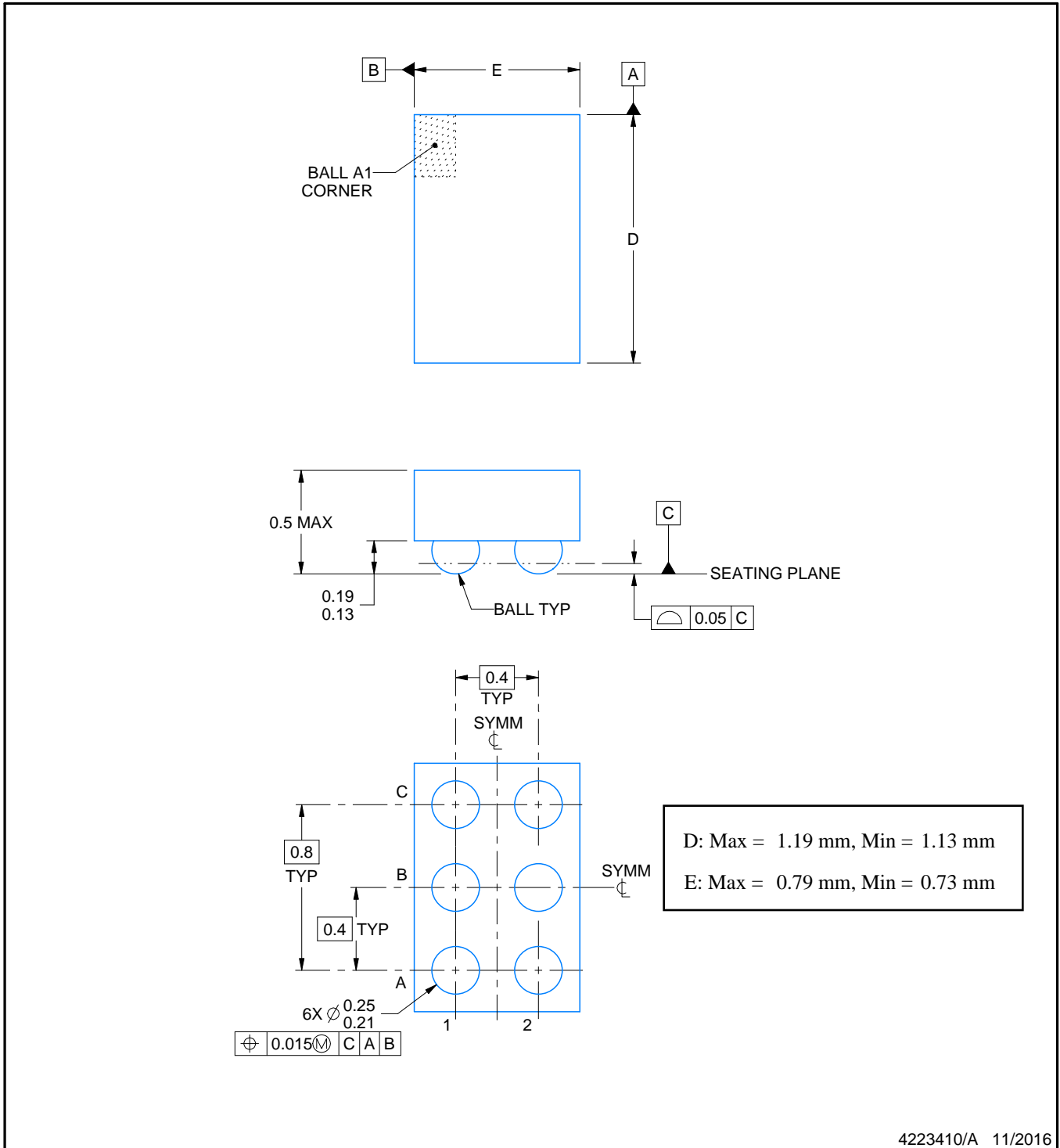
YFP0006



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

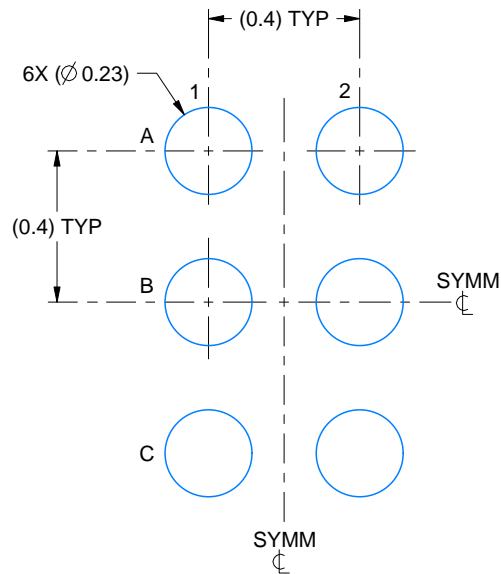
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

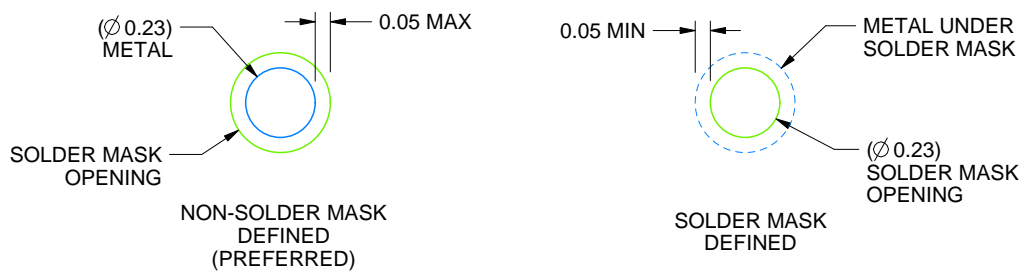
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:50X



SOLDER MASK DETAILS  
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

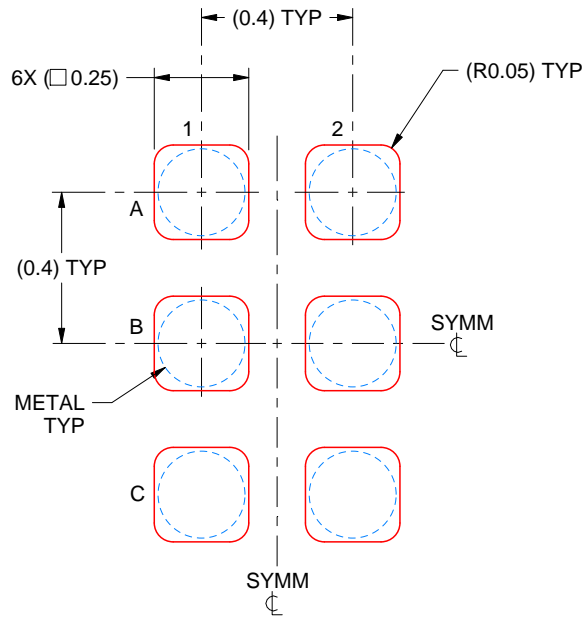


# EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



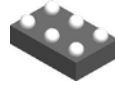
SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

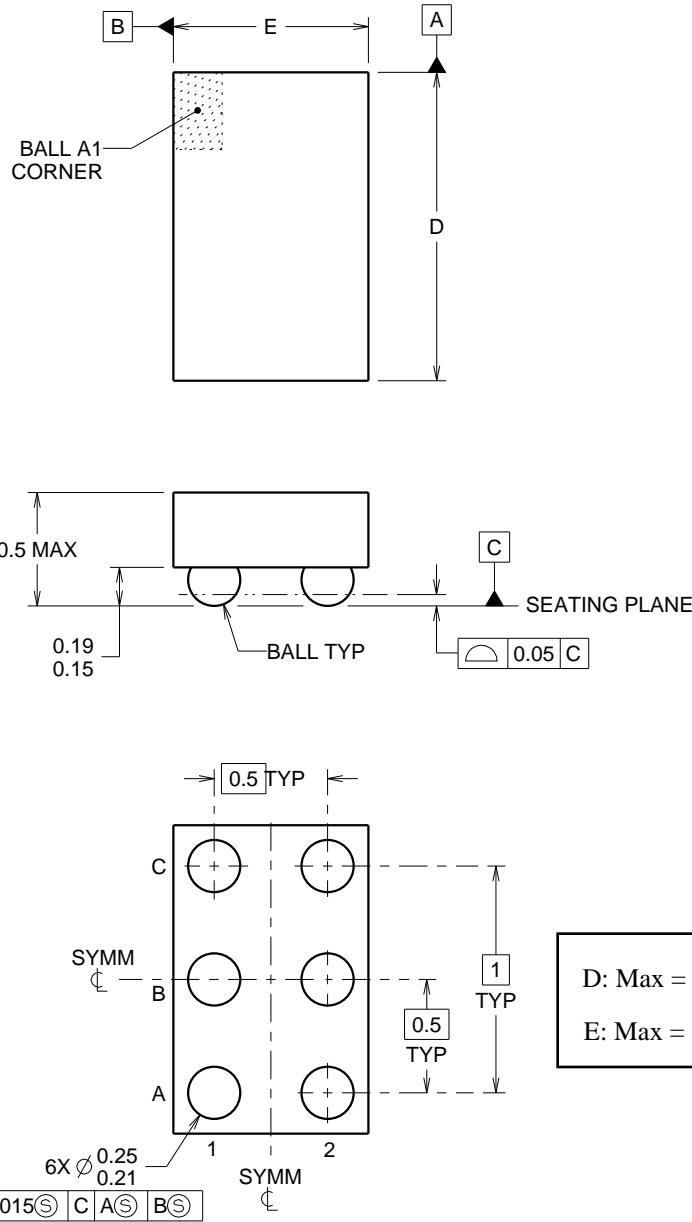
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm  
 E: Max = 0.918 mm, Min = 0.858 mm

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

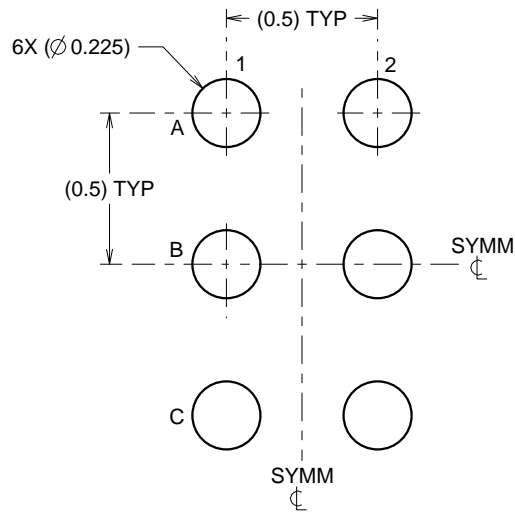
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

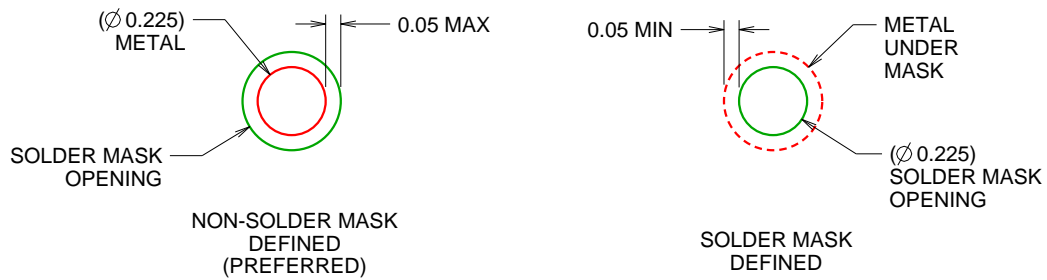
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

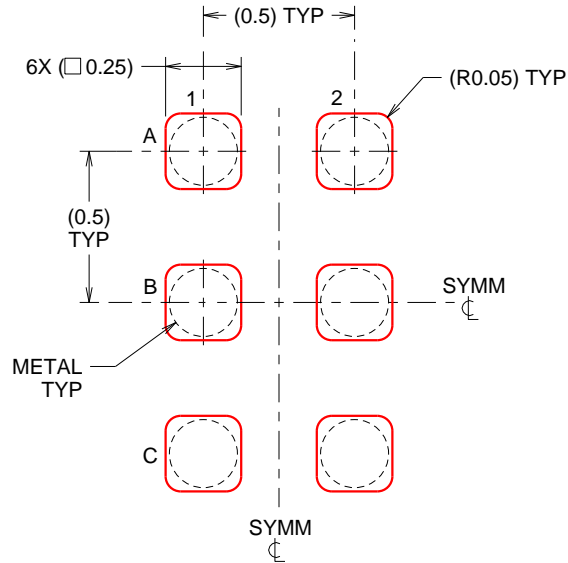
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

# EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

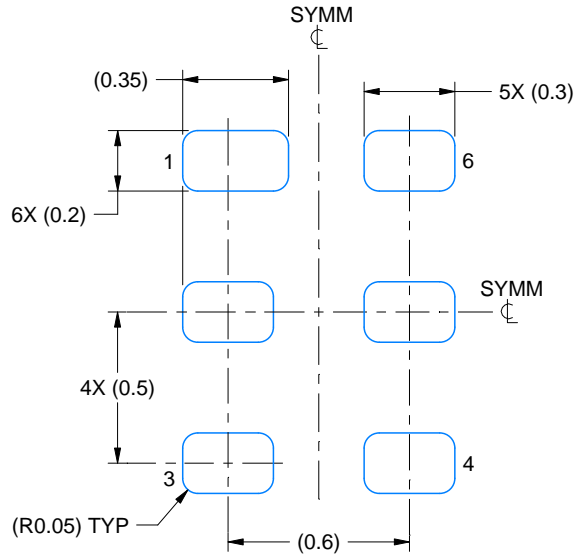


# EXAMPLE BOARD LAYOUT

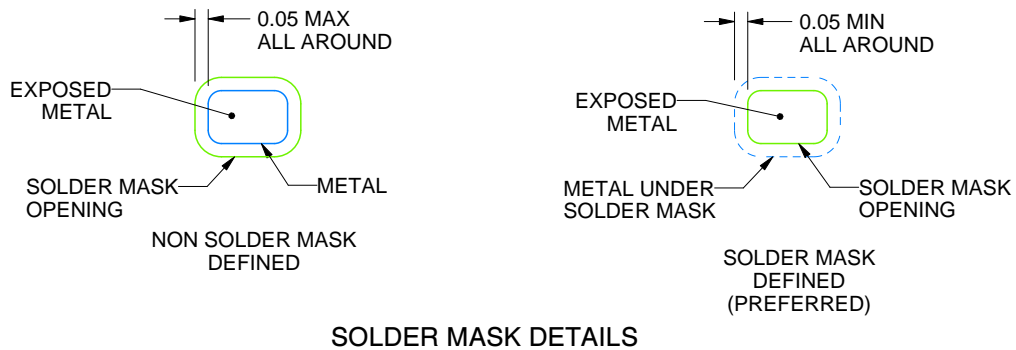
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
 1:1 RATIO WITH PKG SOLDER PADS  
 EXPOSED METAL SHOWN  
 SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

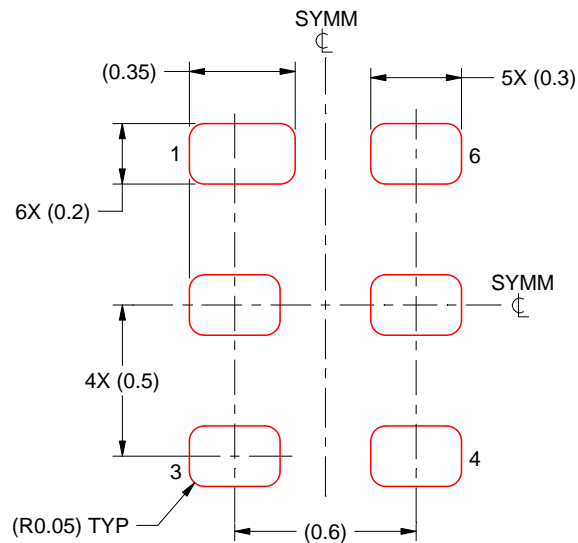
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





# EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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