

Data sheet acquired from Harris Semiconductor

CMOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

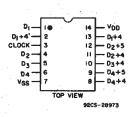
■ CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output (D1+4') that is delayed one-half clockcycle, is provided (see Truth Table for Output from Term. 2).

The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

TERMINAL ASSIGNMENT





ALL INPUTS (TERMINALS 1,3,4,5,6)
PROTECTED BY CMOS PROTECTION
NETWORK

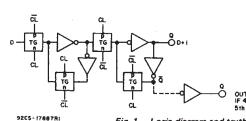
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Features:

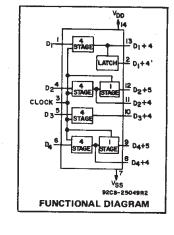
- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature 1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial shift registers F requency division
- Time delay circuits



CD4006B Types



TRUTH TABLE FOR SHIFT REGISTER STAGE

| D | CL♣ | D + 1 |
|---|-----|-------|
| 0 | 7 | 0 |
| 1 | 7 | 1 |
| х | | NC |

TRUTH TABLE FOR OUTPUT FROM TERM2

| D ₁ +4 | CL≜ | D ₁ +4' |
|-------------------|----------|--------------------|
| 0 | | 0 |
| 1 | | . 1 |
| Х | | NC |
| | <u> </u> | NC |

= DON'T CARE = HIGH = LEVEL CHANGE 0 = LOW NC = NO CHANGE

Fig. 1 - Logic diagram and truth table (one register stage).

RECOMMENDED OPERATING CONDITIONS at TA = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V _{DD} | LIN | UNITS | | |
|--|-----------------|-----------------|---------------|-----|--|
| | (V) | Min. | Max. | | |
| Supply-Voltage Range (For T _A = Full Package Temperature Range) | _ | 3 | 18 | V | |
| Clock Pulse Width, t _W | 5 10 15 | 180 80 50 | <u>-</u> ' | ns | |
| Data Setup Time, t _S | 5 10 15 | 100 50 40 | - - - | ns | |
| Data Hold Time, t _H | 5 10 15 | 60 40 30 | - - - | ns | |
| Clock Rise or Fall Time: t _r , t _f | 5,10, 15 | _ | 15 | μS | |
| Clock Input Frequency, f _{CL} | 5 10 15 | _ _ _ | 2.5 5 7 | MHz | |

CD4006B Types

| MAXIMUM RATINGS, Absolute-Maximum Values: | |
|--|--------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (VDD) | |
| Voltages referenced to VSS Terminal) | 0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | 0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | |
| POWER DISSIPATION PER PACKAGE (PD): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearity at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package | Types)100mW |
| OPERATING-TEMPERATURE RANGE (TA) | 55°C to +125°C |
| STORAGE TEMPERATURE RANGE (Tstg) | |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s m | ax+265°C |

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER- | CONE | OITION | ıs | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|------------------------------|----------|--------|----------|---------------------------------------|-------|-------|-------|-------|-----------------------|------|--|
| ISTIC | Vo | VIN | VDD | _55 _40 +85 +125 | | | | | +25 Min. Typ. Max. | | |
| 0 | (V) | (V) | (V) 5 | 5 | 5 | 150 | 150 | | | - | |
| Quiescent Device Current. | | 0,5 | | | | | | | 0.04 | 5 | μΑ |
| IDD Max. | | 0,10 | 10 | 10 | 10 | 300 | 300 | | 0.04 | 10 | |
| | - | 0,15 | 15 | 20 | 20 | 600 | 600 | | 0.04 | 20 | |
| | _ | 0,20 | 20 | 100 | 100 | 3000 | 3000 | | 0.08 | 100 | |
| Output Low | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | _ | |
| (Sink) Current IOL Min. | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | | |
| IOL MIII. | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3 4 | 6.8 | - | |
| Output High | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | _1 | - | mA |
| (Source) Current, IOH Min. | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | 2.4 | -3.4 | -6.8 | - | |
| Output Voltage: | _ | 0,5 | 5 | | 0 | .05 | | - | 0 | 0.05 | |
| Low-Level, VOL Max. | _ | 0,10 | 10 | | 0 | .05 | | - | 0 | 0.05 | V |
| VOL Wax. | | 0,15 | 15 | | 0 | .05 | | _ | 0 | 0.05 | |
| Output Voltage: | _ | 0,5 | 5 | | 4 | .95 | | 4.95 | 5 | - | · |
| High-Level, | _ | 0,10 | 10 | | 9 | .95 | | 9.95 | 10 | - | |
| VOH Min. | | 0,15 | 15 | | 14 | .95 | | 14.95 | 15 | - | |
| Input Low | 0.5, 4.5 | _ | 5 | | 1 | .5 | | _ | | 1.5 | |
| Voltage, | 1, 9 | _ | 10 | | | 3 | | | _ | 3 | |
| VIL Max. | 1.5,13.5 | _ | 15 | | | 4 | | _ | = | 4 | |
| Input High Voltage, | 0.5, 4.5 | _ | 5 | | 3 | 3.5 | | 3.5 | _ | | v |
| | 1, 9 | _ | 10 | 7 | | | | 7 | | - | |
| VIH Min. | 1.5,13.5 | - | 15 | 11 | | | | 11 | - | _ | |
| Input Current IIN Max. | - | 0,18 | 18 | ±0.1 ±0.1 ±1 ±1 | | | | _ | ±10-5 | ±0.1 | μА |

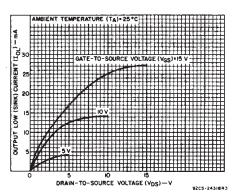


Fig. 2 – Typical output low (sink) current characteristics.

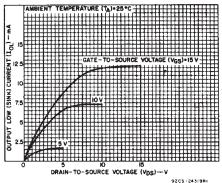


Fig. 3 — Minimum output low (sink) current characteristics.

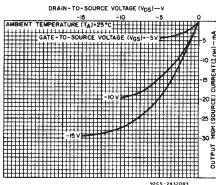


Fig. 4 — Typical output high (source) current characteristics.

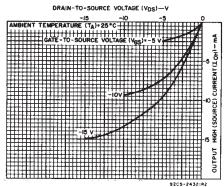


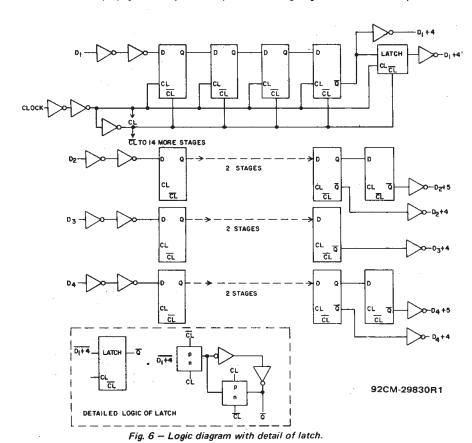
Fig. 5 — Minimum output high (source) current characteristics.

CD4006B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_{\rm A}$ = 25°C; Input $t_{\rm t}$, $t_{\rm t}$ = 20 ns, $C_{\rm L}$ = 50 pF, $R_{\rm L}$ = 200 k Ω

| CHARACTERISTIC | TEST CONDITIONS | | UNITS | | | |
|-------------------------------------|---------------------|--------------|-------|------|-------|--|
| CHARACTERISTIC | V _{DD} (V) | MIN. | TYP. | MAX. | UNITS | |
| Propagation Delay Time, | 5 | _ | 200 | 400 | | |
| tent, teth | 10 | _ | 100 | 200 | ns | |
| | - 15 | _ | 80 | 160 | | |
| Transition Time, | 5 | | 100 | 200 | | |
| t _{THL} , t _{TLH} | 10 | _ | 50 | 100 | ns | |
| | 15 | _ | 40 | 80 | : | |
| Minimum Data Setup Time, | 5 | - | 50 | 100 | | |
| ts | 10 | _ | 25 | 50 | ns | |
| | 15 | _ | 20 | 40 | | |
| Minimum Clock Pulse Width, | 5 | | 100 | 200 | | |
| t _w . | 10 | _ | 45 | 90 | ns | |
| | 15 | _ | 30 | 60 | | |
| Maximum Clock Input | 5 | 2.5 | 5 | _ | | |
| Frequency, fcL | 10 | 5 | 10 | _ | MHz | |
| | 15 | 7 | 14 | _ | | |
| Maximum Clock Input Rise or | 5 | | | 15 | | |
| Fall Time, trCL, trCL* | 10 | – | [- | 15 | μs | |
| | 15 | – | _ | 15 | | |
| Input Capacitance, Cin | Any Input | | 5 | 7.5 | ρF | |

^{*}If more than one unit is cascaded t_iCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.



AMBIENT TEMPERATURE (TA)-25°C

Fig. 7 — Typical transition time as a function of load capacitance.

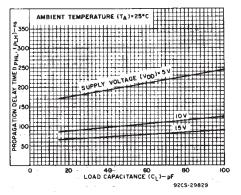


Fig. 8 — Typical propagation delay time as a function of load capacitance.

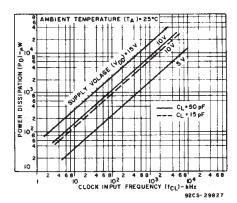


Fig. 9 — Typical dyanamic power dissipation as a function of clock frequency.

CD4006B Types

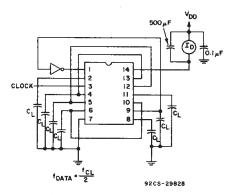


Fig. 10 - Dynamic power dissipation test circuit.

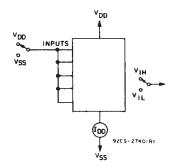


Fig. 11 - Quiescent device current test circuit.

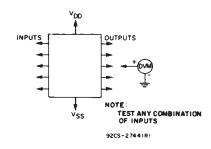


Fig. 12 - Input voltage test circuit.

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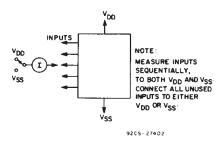
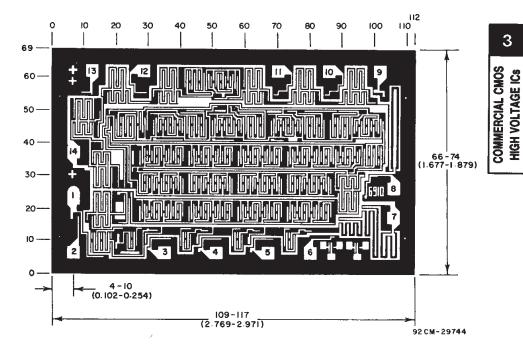


Fig. 13 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

Dimensions and pad layout for CD4006BH.



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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan | Lead finish/ Ball material | MSL Peak Temp | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|------------|--------------|--------------------|------|----------------|---------------------|-------------------------------|--------------------|--------------|----------------------|---------|
| CD4006BF3A | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD4006BF3A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

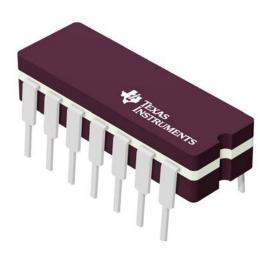
Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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CERAMIC DUAL IN LINE PACKAGE



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4040083-5/G





CERAMIC DUAL IN LINE PACKAGE

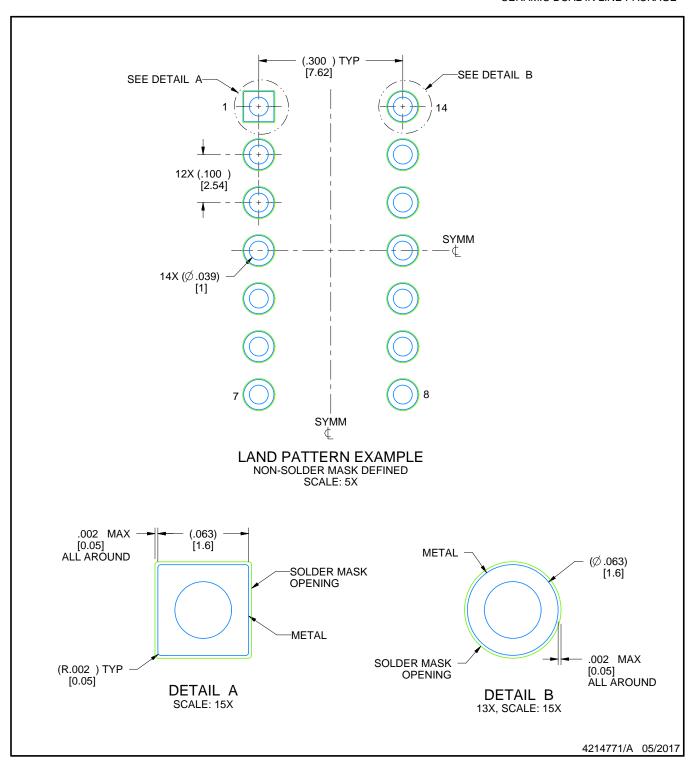


NOTES:

- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



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