

OPA244
OPA2244
OPA4244

MicroPower, Single-Supply OPERATIONAL AMPLIFIERS MicroAmplifier™ Series

FEATURES

- **MicroSIZE PACKAGES**
 OPA244 (Single): SOT-23-5
 OPA2244 (Dual): MSOP-8
 OPA4244 (Quad): TSSOP-14
- **MicroPOWER:** $I_Q = 50\mu\text{A}/\text{channel}$
- **SINGLE SUPPLY OPERATION**
- **WIDE BANDWIDTH:** 430kHz
- **WIDE SUPPLY RANGE:**
 Single Supply: 2.2V to 36V
 Dual Supply: $\pm 1.1\text{V}$ to $\pm 18\text{V}$

APPLICATIONS

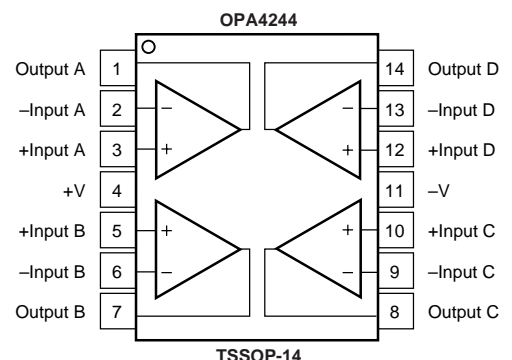
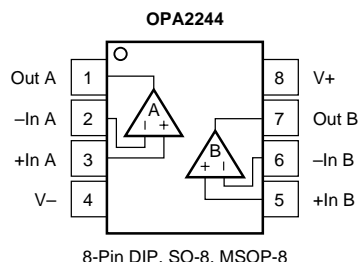
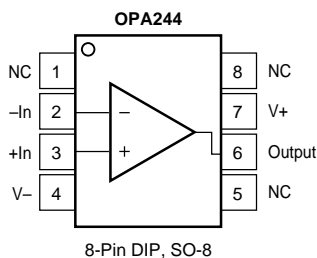
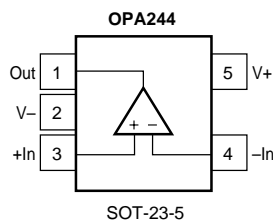
- **BATTERY POWERED SYSTEMS**
- **PORTABLE EQUIPMENT**
- **PCMCIA CARDS**
- **BATTERY PACKS AND POWER SUPPLIES**
- **CONSUMER PRODUCTS**

DESCRIPTION

The OPA244 (single), OPA2244 (dual), and OPA4244 (quad) op amps are designed for very low quiescent current ($50\mu\text{A}/\text{channel}$), yet achieve excellent bandwidth. Ideal for battery powered and portable instrumentation, all versions are offered in micro packages for space-limited applications. The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The OPA244 series is easy to use and free from phase inversion and overload problems found in some other op amps. These amplifiers are stable in unity gain and excellent performance is maintained as they swing to their specified limits. They can be operated from single (+2.2V to +36V) or dual supplies ($\pm 1.1\text{V}$ to $\pm 18\text{V}$). The input common-mode voltage range includes ground—ideal for many single supply applications. All versions have similar performance. However, there are some differences, such as common-mode rejection. All versions are interchangeable in most applications.

All versions are offered in miniature, surface-mount packages. OPA244 (single version) comes in the tiny 5-lead SOT-23-5 surface mount, SO-8 surface mount, and 8-pin DIP. OPA2244 (dual version) is available in the MSOP-8 surface mount, SO-8 surface-mount, and 8-pin DIP. The OPA4244 (quad) comes in the TSSOP-14 surface mount. They are fully specified from -40°C to $+85^\circ\text{C}$ and operate from -55°C to $+125^\circ\text{C}$. A SPICE Macromodel is available for design analysis.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
 Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = +2.6V$ to $+36V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

At $T_A = +25^{\circ}C$, $R_L = 20k\Omega$ connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA244NA, PA, UA			UNITS
		MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^{\circ}C$ to $85^{\circ}C$ vs Temperature vs Power Supply $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_{OS} $V_S = \pm 7.5V, V_{CM} = 0$ dV_{OS}/dT $PSRR$ $T_A = -40^{\circ}C$ to $85^{\circ}C$ $V_S = +2.6V$ to $+36V$ $V_S = +2.6V$ to $+36V$		± 0.7 ± 4 5	± 1.5 ± 2 50 50	mV mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current Input Offset Current	I_B I_{OS} $V_{CM} = V_S/2$ $V_{CM} = V_S/2$		-10 ± 1	-25 ± 10	nA nA
NOISE Input Voltage Noise, $f = 0.1kHz$ to $10kHz$ Input Voltage Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$	e_n i_n		0.4 22 40		$\mu Vp-p$ nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_{CM} CMRR $V_S = \pm 18V, V_{CM} = -18V$ to $+17.1V$ $V_S = \pm 18V, V_{CM} = -18V$ to $+17.1V$	0 84 84	98	$(V+) - 0.9$	V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^6 \parallel 2$ $10^9 \parallel 2$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain $T_A = -40^{\circ}C$ to $85^{\circ}C$	A_{OL} $V_O = 0.5V$ to $(V+) - 0.9$ $V_O = 0.5V$ to $(V+) - 0.9$	86 86	106		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% Overload Recovery Time	GBW SR $G = 1$ 10V Step $V_{IN} \cdot \text{Gain} = V_S$		430 -0.1/+0.16 150 8		kHz V/ μs μs μs
OUTPUT Voltage Output, Positive $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Negative $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Positive $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Negative $T_A = -40^{\circ}C$ to $85^{\circ}C$ Short-Circuit Current Capacitive Load Drive	V_O $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground I_{SC} C_{LOAD}	$(V+) - 0.9$ $(V+) - 0.9$ 0.5 0.5 0.1 0.1 -25/+12	$(V+) - 0.75$ $(V+) - 0.75$ 0.2 0.2 $(V+) - 0.75$ $(V+) - 0.75$ 0.1 0.1 -25/+12		V V V V V V V V mA
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Quiescent Current $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_S I_Q $T_A = -40^{\circ}C$ to $85^{\circ}C$ $I_O = 0$ $I_O = 0$	+2.6	+2.2 50	+36 60 70	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT-23-5 Surface-Mount SO-8 Surface-Mount 8-Pin DIP	θ_{JA}	-40 -55 -65		85 125 150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$

NOTE: (1) $V_S = +15V$.

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SPECIFICATIONS: $V_S = +2.6V$ to $+36V$

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$

At $T_A = +25^\circ C$, $R_L = 20k\Omega$ connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA2244EA, PA, UA			UNITS
		MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^\circ C$ to $85^\circ C$ vs Temperature vs Power Supply $T_A = -40^\circ C$ to $85^\circ C$ Channel Separation	V_{OS} $V_S = \pm 7.5V, V_{CM} = 0$ dV_{OS}/dT $PSRR$ $T_A = -40^\circ C$ to $85^\circ C$ $V_S = +2.6V$ to $+36V$ $V_S = +2.6V$ to $+36V$		± 0.7 ± 4 5 140	± 1.5 ± 2 50 50	mV mV $\mu V/^\circ C$ $\mu V/V$ $\mu V/V$ dB
INPUT BIAS CURRENT Input Bias Current Input Offset Current	I_B I_{OS} $V_{CM} = V_S/2$ $V_{CM} = V_S/2$		-10 ± 1	-25 ± 10	nA nA
NOISE Input Voltage Noise, $f = 0.1kHz$ to $10kHz$ Input Voltage Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$	e_n i_n		0.4 22 40		$\mu Vp-p$ nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection $T_A = -40^\circ C$ to $85^\circ C$	V_{CM} CMRR $V_S = \pm 18V, V_{CM} = -18V$ to $+17.1V$ $V_S = \pm 18V, V_{CM} = -18V$ to $+17.1V$	0 72 72	98	$(V+) - 0.9$	V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^6 \parallel 2$ $10^9 \parallel 2$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain $T_A = -40^\circ C$ to $85^\circ C$	A_{OL} $V_O = 0.5V$ to $(V+) - 0.9$ $V_O = 0.5V$ to $(V+) - 0.9$	86 86	106		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% Overload Recovery Time	GBW SR G = 1 10V Step $V_{IN} \cdot \text{Gain} = V_S$		430 -0.1/+0.16 150 8		kHz V/ μs μs μs
OUTPUT Voltage Output, Positive $T_A = -40^\circ C$ to $85^\circ C$ Voltage Output, Negative $T_A = -40^\circ C$ to $85^\circ C$ Voltage Output, Positive $T_A = -40^\circ C$ to $85^\circ C$ Voltage Output, Negative $T_A = -40^\circ C$ to $85^\circ C$ Short-Circuit Current Capacitive Load Drive	V_O I_{SC} C_{LOAD} $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground See Typical Curve	$(V+) - 0.9$ $(V+) - 0.9$ 0.5 0.5 0.1 0.1 -25/+12	$(V+) - 0.75$ $(V+) - 0.75$ 0.2 0.2 $(V+) - 0.75$ $(V+) - 0.75$ 0.1 0.1		V V V V V V V V mA
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Quiescent Current (per amplifier) $T_A = -40^\circ C$ to $85^\circ C$	V_S I_Q $T_A = -40^\circ C$ to $85^\circ C$ $I_O = 0$ $I_O = 0$	+2.6	+2.2 40	+36 50 63	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance MSOP-8 Surface-Mount SO-8 Surface-Mount 8-Pin DIP	θ_{JA}	-40 -55 -65		85 125 150	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

NOTE: (1) $V_S = +15V$.

SPECIFICATIONS: $V_S = +2.6V$ to $+36V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

At $T_A = +25^{\circ}C$, $R_L = 20k\Omega$ connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA4244EA			UNITS
		MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^{\circ}C$ to $85^{\circ}C$ vs Temperature vs Power Supply $T_A = -40^{\circ}C$ to $85^{\circ}C$ Channel Separation	V_{OS} $V_S = \pm 7.5V, V_{CM} = 0$ dV_{OS}/dT $PSRR$ $T_A = -40^{\circ}C$ to $85^{\circ}C$ $V_S = +2.6V$ to $+36V$ $V_S = +2.6V$ to $+36V$		± 0.7 ± 4 5 140	± 1.5 ± 2 50 50	mV mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$ dB
INPUT BIAS CURRENT Input Bias Current Input Offset Current	I_B I_{OS} $V_{CM} = V_S/2$ $V_{CM} = V_S/2$		-10 ± 1	-25 ± 10	nA nA
NOISE Input Voltage Noise, $f = 0.1kHz$ to $10kHz$ Input Voltage Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$	e_n i_n		0.4 22 40		$\mu Vp-p$ nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_{CM} CMRR $V_S = \pm 18V, V_{CM} = -18V$ to $+17.1V$ $V_S = \pm 18V, V_{CM} = -18V$ to $+17.1V$	0 82 82		$(V+) - 0.9$ 104	V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^6 \parallel 2$ $10^9 \parallel 2$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain $T_A = -40^{\circ}C$ to $85^{\circ}C$	A_{OL} $V_O = 0.5V$ to $(V+) - 0.9$ $V_O = 0.5V$ to $(V+) - 0.9$	86 86	106		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% Overload Recovery Time	GBW SR $G = 1$ 10V Step $V_{IN} \cdot \text{Gain} = V_S$		430 $-0.1/+0.16$ 150 8		kHz $V/\mu s$ μs μs
OUTPUT Voltage Output, Positive $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Negative $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Positive $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Negative $T_A = -40^{\circ}C$ to $85^{\circ}C$ Short-Circuit Current Capacitive Load Drive	V_O I_{SC} C_{LOAD} $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB, R_L = 20k\Omega$ to Ground See Typical Curve	$(V+) - 0.9$ $(V+) - 0.9$ 0.5 0.5 0.5 0.5 0.1 0.1 $-25/+12$	$(V+) - 0.75$ $(V+) - 0.75$ 0.2 0.2 $(V+) - 0.75$ $(V+) - 0.75$ 0.1 0.1 $-25/+12$		V V V V V V V V mA
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Quiescent Current (per amplifier) $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_S I_Q $T_A = -40^{\circ}C$ to $85^{\circ}C$ $I_O = 0$ $I_O = 0$	+2.6	+2.2 40	+36 60 70	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance TSSOP-14 Surface Mount	θ_{JA}	-40 -55 -65		85 125 150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$

NOTE: (1) $V_S = +15V$.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	36V
Input Voltage Range ⁽²⁾	(V-) – 0.3V to (V+) + 0.3V
Input Current ⁽²⁾	10mA
Output Short-Circuit ⁽³⁾	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Capability	2000V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Inputs are diode-clamped to the supply rails and should be current-limited to 10mA or less if input voltages can exceed rails by more than 0.3V. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

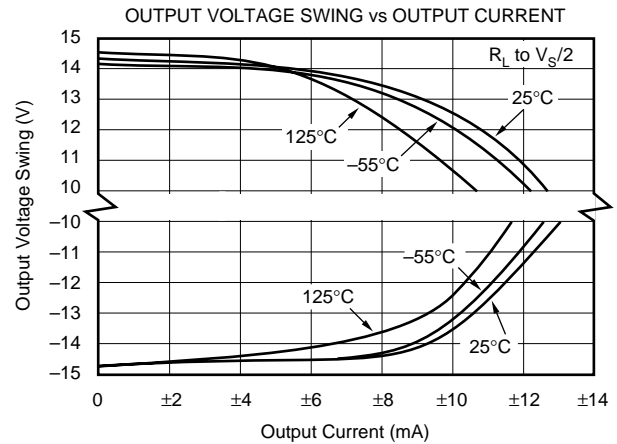
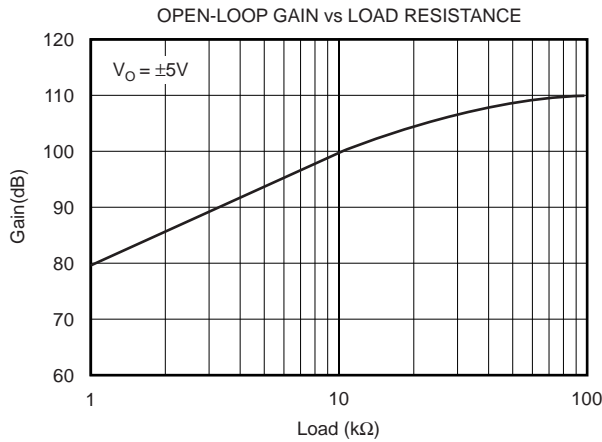
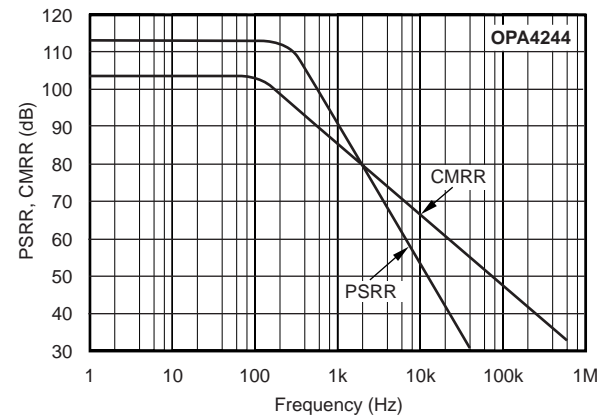
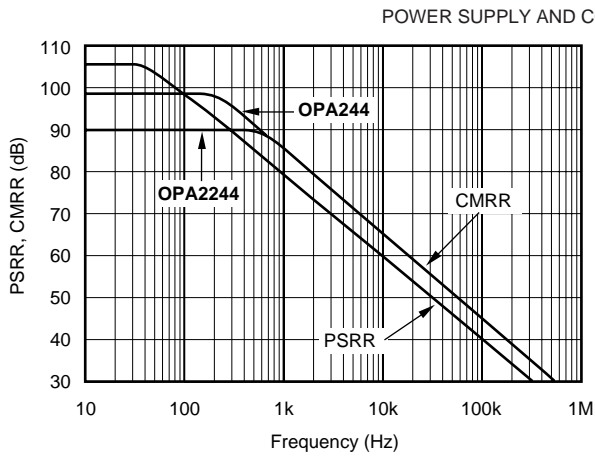
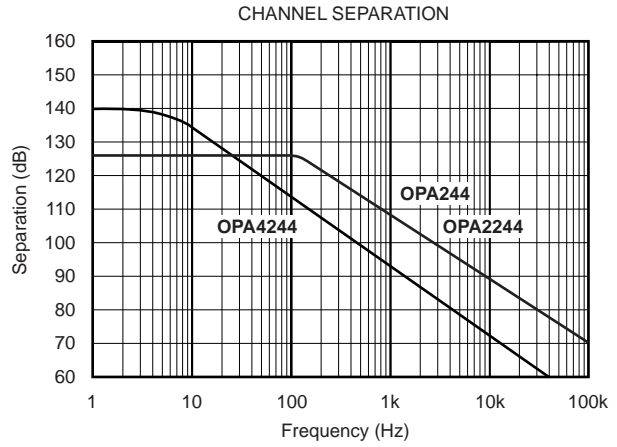
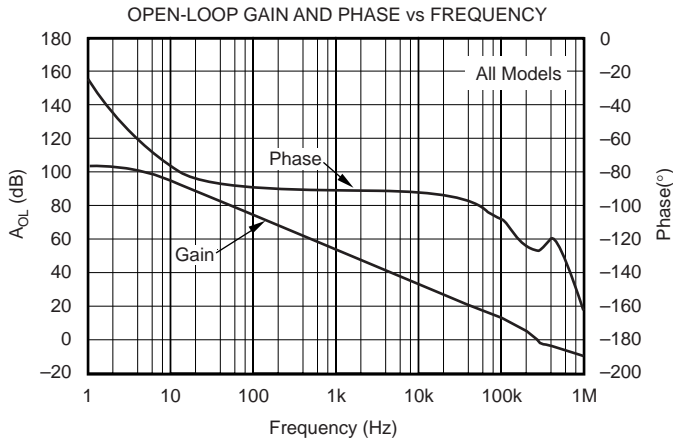
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
Single						
OPA244NA "	SOT-23-5 Surface-Mount "	331 "	–40°C to +85°C "	A44 "	OPA244NA/250	Tape and Reel
OPA244PA OPA244UA "	8-Pin DIP SO-8 Surface-Mount "	006 182 "	–40°C to +85°C –40°C to +85°C "	OPA244PA OPA244UA "	OPA244NA/3K OPA244PA OPA244UA OPA244UA/2K5	Tape and Reel Rails Rails Tape and Reel
Dual						
OPA2244EA "	MSOP-8 Surface-Mount "	337 "	–40°C to +85°C "	A44 "	OPA2244EA/250	Tape and Reel
OPA2244PA OPA2244UA "	8-Pin DIP SO-8 Surface-Mount "	006 182 "	–40°C to +85°C –40°C to +85°C "	OPA2244PA OPA2244UA "	OPA2244EA/2K5 OPA2244PA OPA2244UA OPA2244UA/2K5	Tape and Reel Rails Rails Tape and Reel
Quad						
OPA4244EA "	TSSOP-14 Surface-Mount "	357 "	–40°C to +85°C "	OPA4244EA "	OPA4244EA/250 OPA4244EA/2K5	Tape and Reel Tape and Reel

NOTE: (1) Products followed by a slash (/) are only available in Tape and Reel in the quantities indicated (e.g., /250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA244NA/3K" will get a single 3000 piece Tape and Reel.

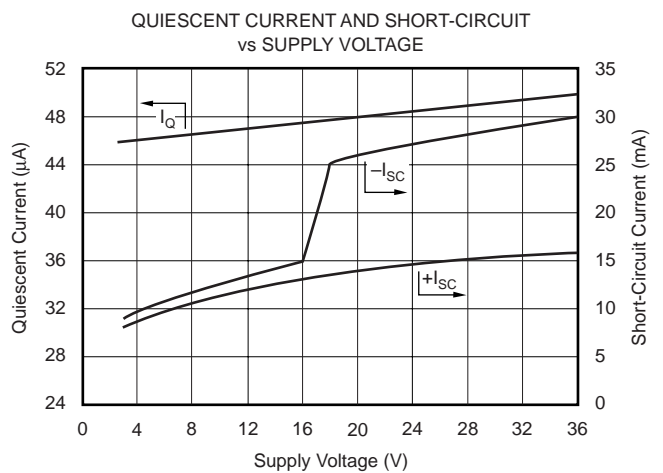
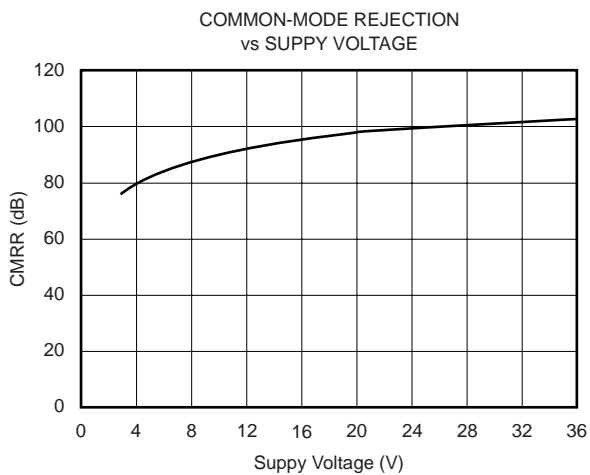
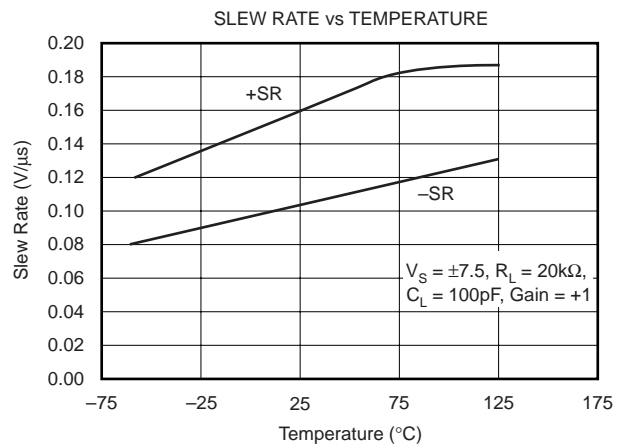
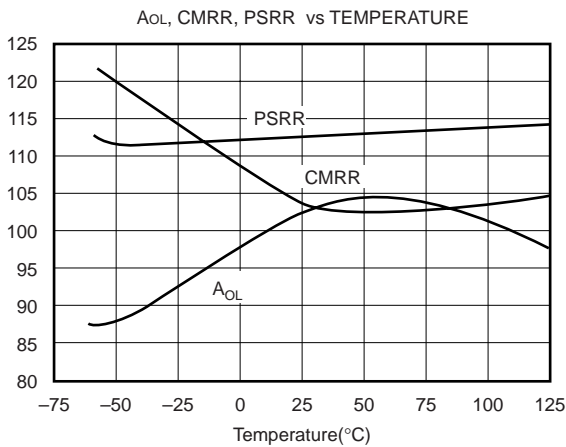
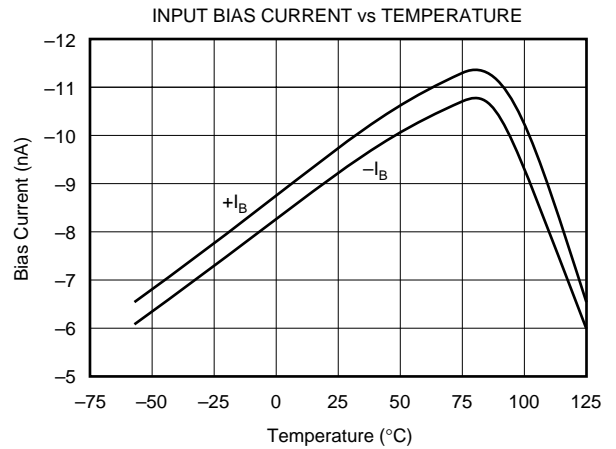
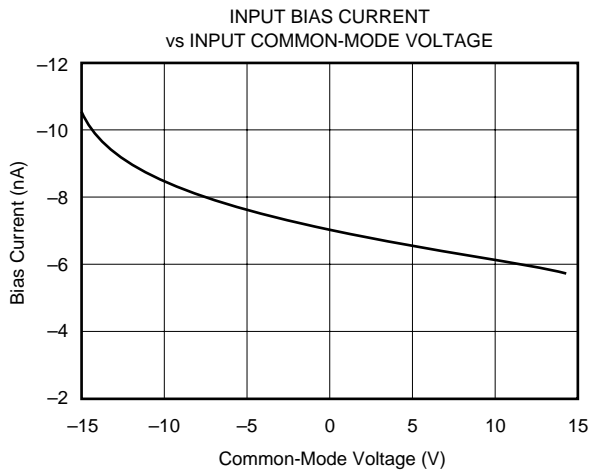
TYPICAL PERFORMANCE CURVES

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Cont.)

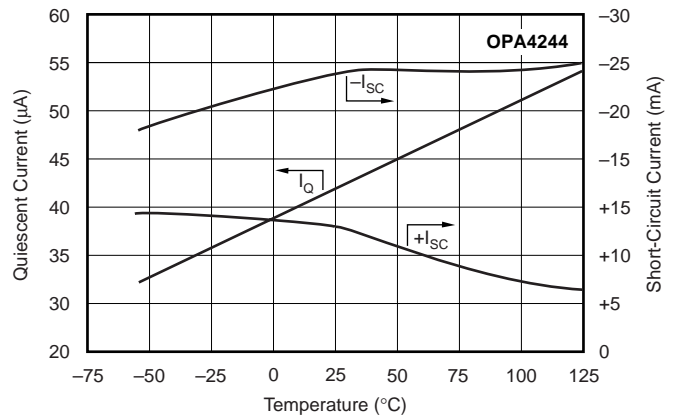
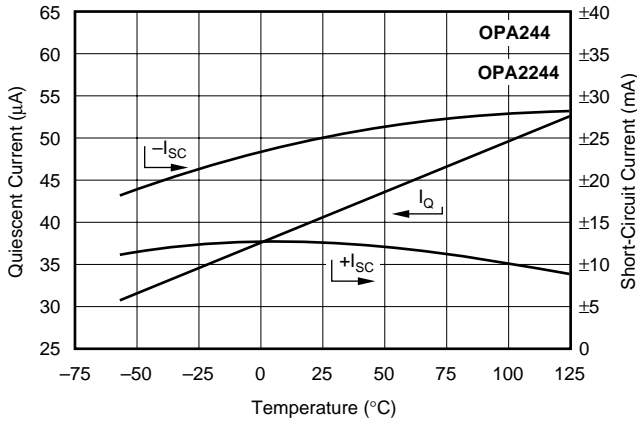
At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.



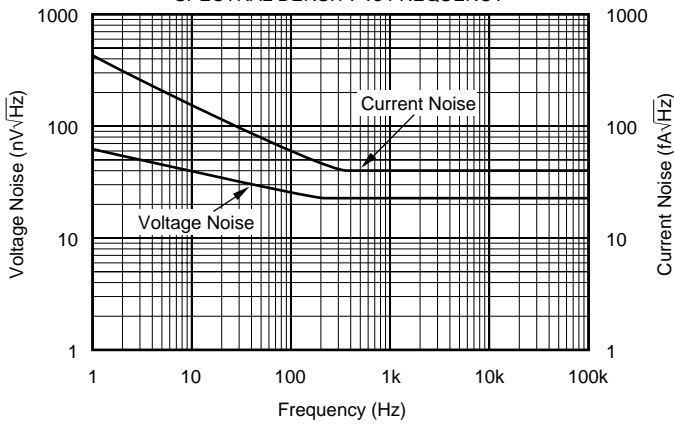
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.

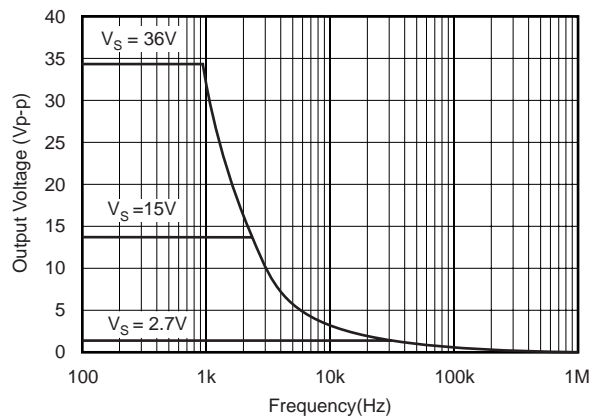
QUIESCENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



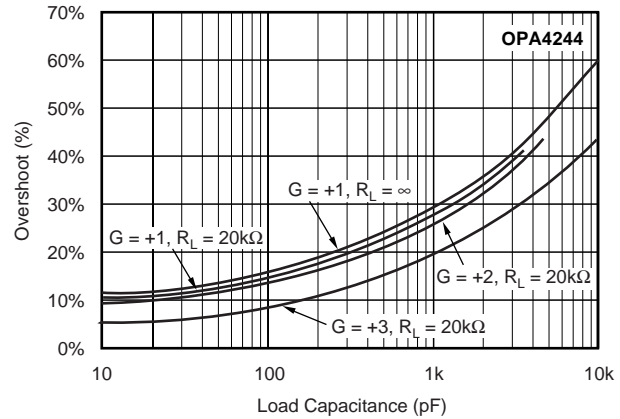
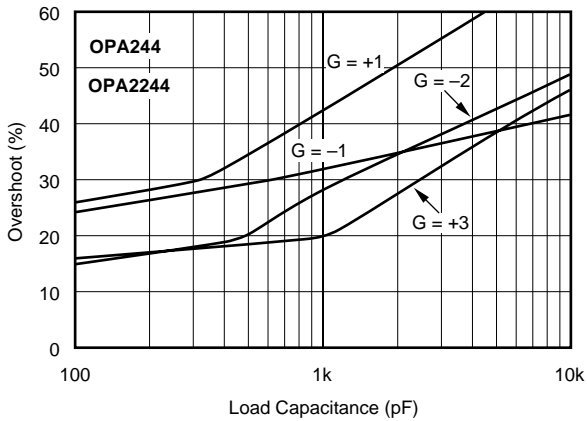
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



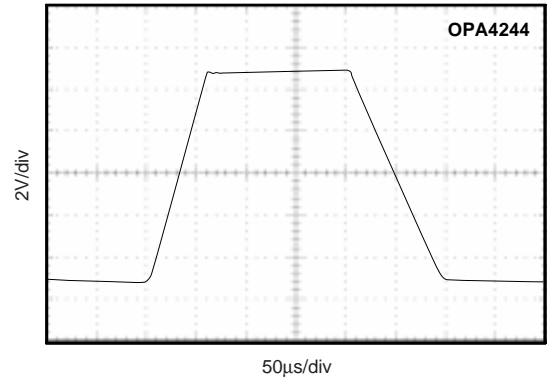
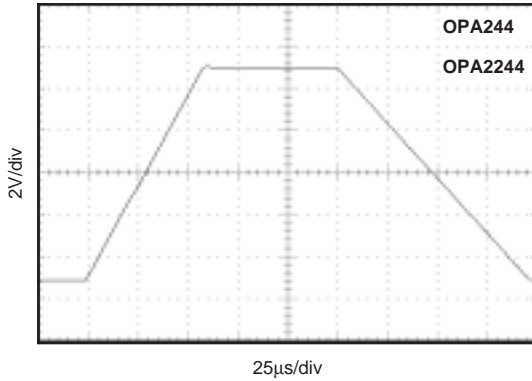
SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE



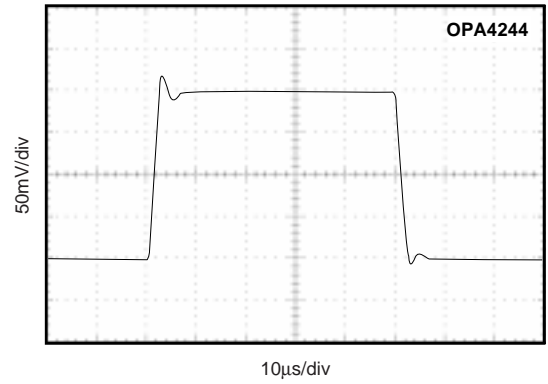
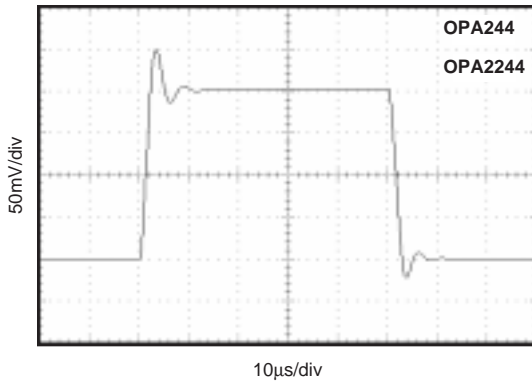
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.

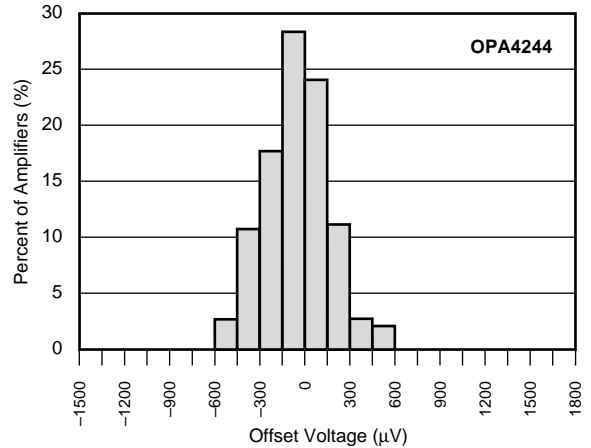
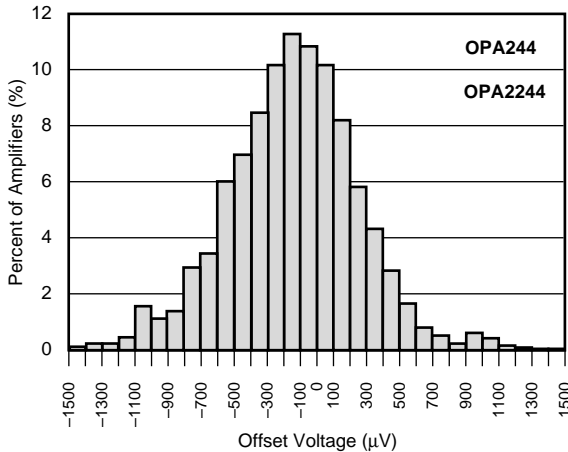
LARGE-SIGNAL STEP RESPONSE, $G = 1$, $C_L = 100\text{pF}$



SMALL-SIGNAL STEP RESPONSE, $G = 1$, $C_L = 100\text{pF}$



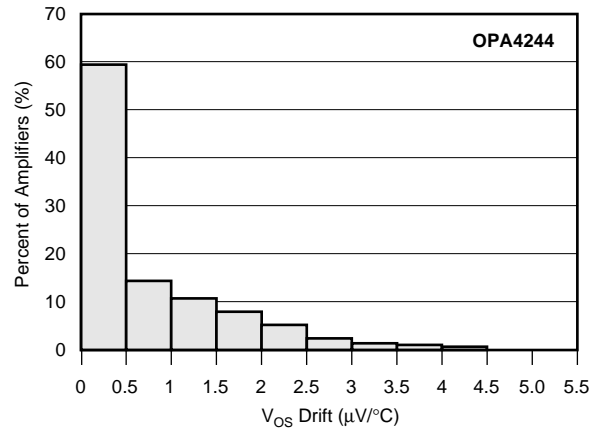
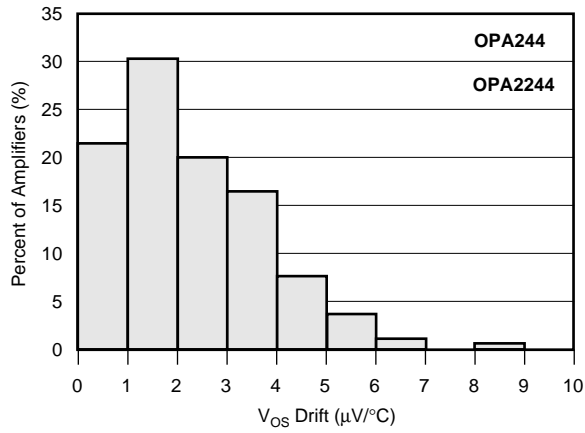
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION



APPLICATIONS INFORMATION

The OPA244 is unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with 0.01µF ceramic capacitors.

OPERATING VOLTAGE

The OPA244 can operate from single supply (+2.2V to +36V) or dual supplies (±1.1 to ±18V) with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA244 is specified for real world applications; a single set of specifications applies throughout the +2.6V to +36V (±1.3 to ±18V) supply range.

This allows a designer to have the same assured performance at any supply voltage within this range. In addition, many key parameters are guaranteed over the specified temperature range, -40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

Useful information on solder pad design for printed circuit boards can be found in Burr-Brown's Application Bulletin AB-132B, "Solder Pad Recommendations for Surface-Mount Devices," easily found at Burr-Brown's web site (<http://www.burr-brown.com>).

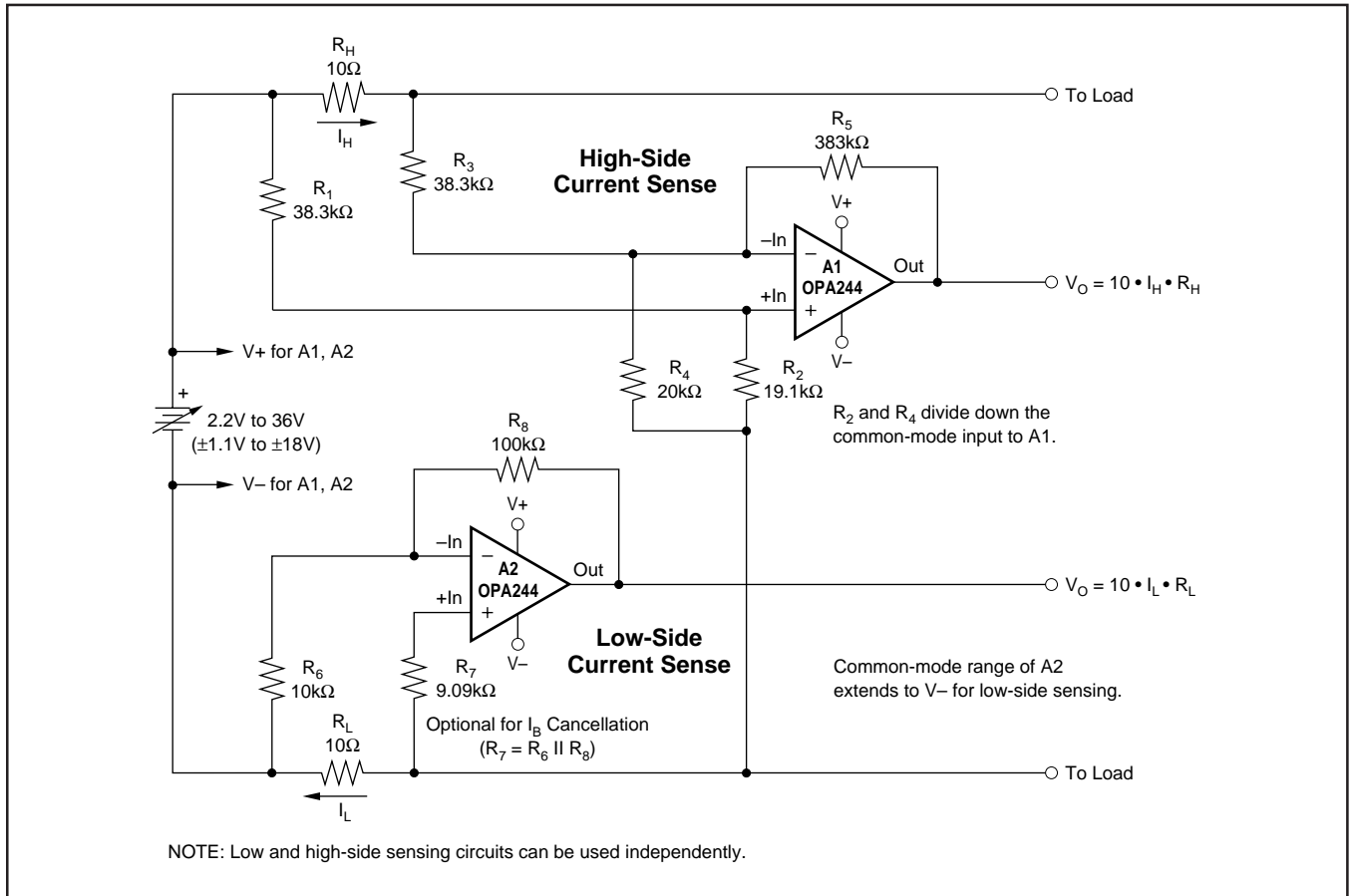


FIGURE 1. Low and High-Side Battery Current Sensing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2244EA/250	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA2244EA/250G4	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA2244EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA2244EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
OPA2244PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA2244PA	Samples
OPA2244UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2244UA	
OPA2244UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2244UA	Samples
OPA2244UAG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2244UA	
OPA244NA/250	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA244NA/250G4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA244NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA244UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 244UA	
OPA244UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 244UA	Samples
OPA4244EA/250	LIFEBUY	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	
OPA4244EA/2K5	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	Samples

(1) The marketing status values are defined as follows:

LIFEBUY: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2244EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2244EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2244UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA244NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA244NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA244UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4244EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4244EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2244EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2244EA/2K5	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2244UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA244NA/250	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA244NA/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA244UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4244EA/250	TSSOP	PW	14	250	210.0	185.0	35.0
OPA4244EA/2K5	TSSOP	PW	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2244PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2244UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2244UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA244UA	D	SOIC	8	75	506.6	8	3940	4.32

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

4214839/J 02/2024

EXAMPLE BOARD LAYOUT

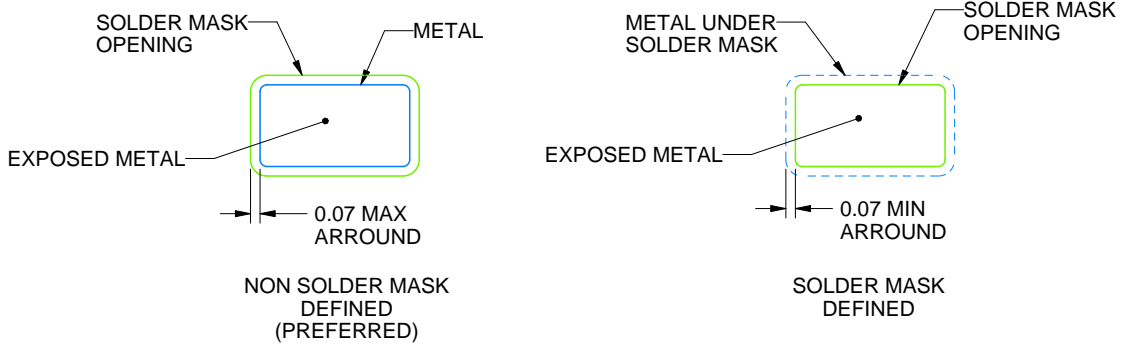
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G14)

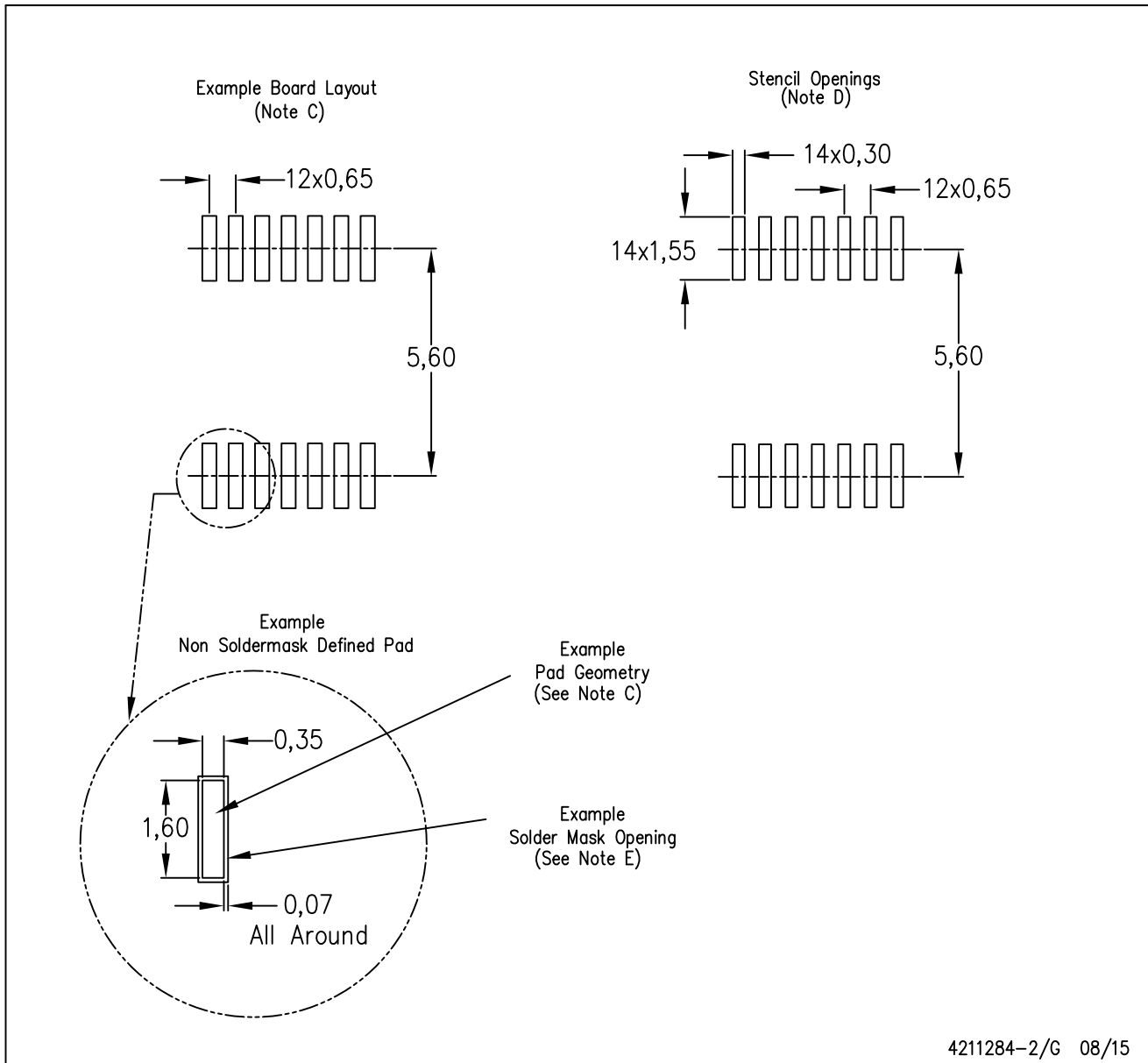
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

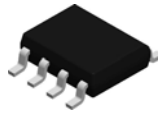
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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