

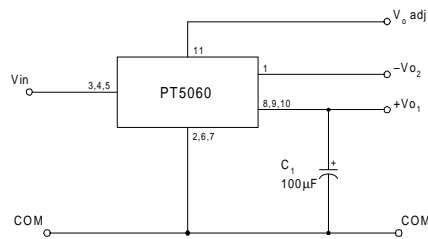
### Features

- Single Device: +5V Input
- Complimentary Dual Output:  $\pm 12V$ ,  $\pm 15V$
- Wide Input Voltage Range
- 85% Efficiency
- Adjustable Output Voltage
- Laser-trimmed

### Description

The PT5060 series of dual-output Integrated Switching Regulators (ISRs) provide a complimentary  $\pm 12V$  or  $\pm 15V$  from a single +5V input. Applications include systems that require power for analog interface circuitry, such as D/A and A/D converters, and Op Amps. The output voltage can be adjusted with an external resistor. These ISRs are made available in a 12-pin single in-line pin (SIP) package. Note that these modules are not short-circuit protected.

### Standard Application



$C_1$  = Required 100µF electrolytic

### Pin-Out Information

Pin	Function
1	$-V_{O2}$
2	GND
3	$V_{in}$
4	$V_{in}$
5	$V_{in}$
6	GND
7	GND
8	$+V_{O1}$
9	$+V_{O1}$
10	$+V_{O1}$
11	$V_o$ Adj
12	Do Not Connect

### Ordering Information

PT5061□ =  $\pm 12$  Volts

PT5062□ =  $\pm 15$  Volts

### PT Series Suffix (PT1234 x)

Case/Pin Configuration	Order Suffix	Package Code *
Vertical	<b>N</b>	(ECD)
Horizontal	<b>A</b>	(ECA)
SMD	<b>C</b>	(ECC)
Vertical, Side Tabs	<b>R</b>	(ECE)
Horizontal, Side Tabs	<b>G</b>	(ECG)
SMD, Side Tabs	<b>B</b>	(ECK)

\* Previously known as package style 300.

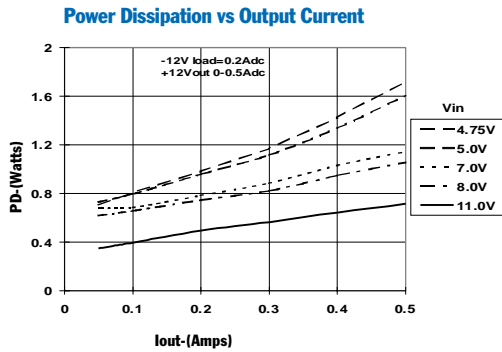
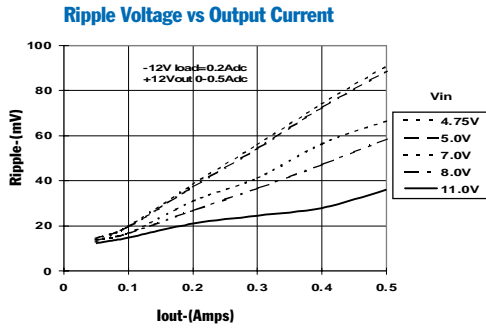
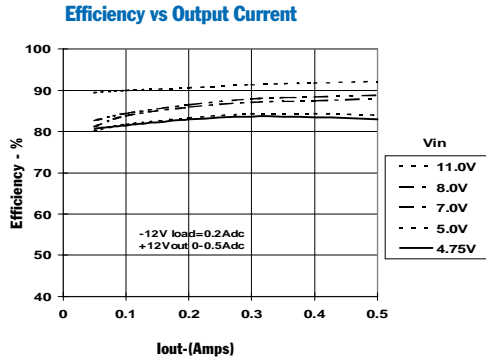
(Reference the applicable package code drawing for the dimensions and PC board layout)

### Specifications (Unless otherwise stated, $T_a = 25^\circ C$ , $V_{in} = +5V$ , $I_o = I_{o,max}$ , $C_1 = 100\mu F$ )

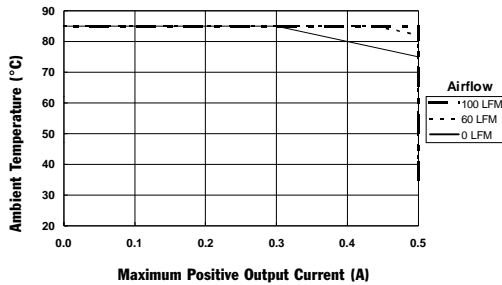
Characteristics	Symbol	Conditions	PT5060 SERIES			Units	
			Min	Typ	Max		
Output Current	$I_o$	Over $V_{in}$ range	$V_{O1} = +12V$ $V_{O2} = -12V$	0.05 0.05 (1)	— —	0.50 0.25	A
Current Limit	$I_{lim}$			—	150 (2)	—	% $I_{o,max}$
Inrush Current	$I_{ir}$	On start up		—	5.5 (3)	—	A
	$t_{tr}$			—	2	—	mSec
Input Voltage Range	$V_{in}$	Over $I_o$ range		4.75	—	$+V_o - 1$	V
Output Voltage Tolerance	$\Delta V_o$	Over $V_{in}$ and $I_o$ ranges $T_a = 0^\circ C$ to SOA limit (3)	$+V_{O1}$ $-V_{O2}$	— —	$\pm 1.5$ $\pm 5$	$\pm 3.0$ $\pm 10$	% $V_o$
Line Regulation	$Reg_{line}$	Over $V_{in}$ range		—	$\pm 0.5$	$\pm 1.0$	% $V_o$
Load Regulation	$Reg_{load}$	$0.1 \leq I_o \leq I_{o,max}$		—	$\pm 0.5$	$\pm 1.0$	% $V_o$
$V_o$ Ripple (pk-pk)	$V_n$	20MHz bandwidth	$+V_{O1}$ $-V_{O2}$	— —	$\pm 1.5$ $\pm 2$	$\pm 3$ $\pm 3$	% $V_o$
Transient Response	$t_{tr}$ $V_{os}$	25% load change $V_o$ over/undershoot		— —	100 3	— 5	$\mu$ Sec % $V_o$
Efficiency	$\eta$	$I_o = 0.2A$ each output		—	85	—	%
Switching Frequency	$f_s$	Over $V_{in}$ and $I_o$ ranges		—	650	—	kHz
Operating Temperature Range	$T_a$	—		0	—	$+85$ (4)	$^\circ C$
Storage Temperature	$T_s$	—		-40	—	$+125$	$^\circ C$
Mechanical Shock		Per Mil-STD-883D, Method 2002.3, 1 msec, Half Sine, mounted to a fixture	—	500	—	G's	
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2 20-2000 Hz, Soldered in a PC board	—	15	—	G's	
Weight				—	6.5	—	grams

- Notes:**
- (1) Do not operate the negative output rail of these ISRs below the minimum load.
  - (2) ISRs based on a boost topology are not short-circuit protected.
  - (3) The inrush current stated is above the normal input current for the associated output load.
  - (4) See Safe Operating Area curves or consult the factory for the appropriate derating.

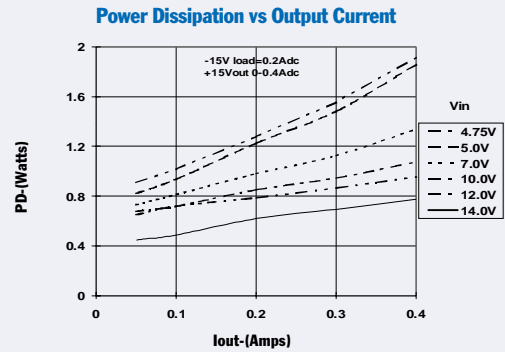
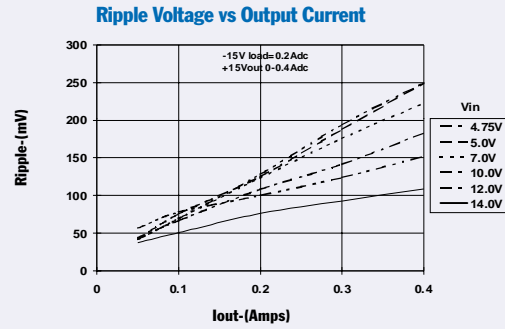
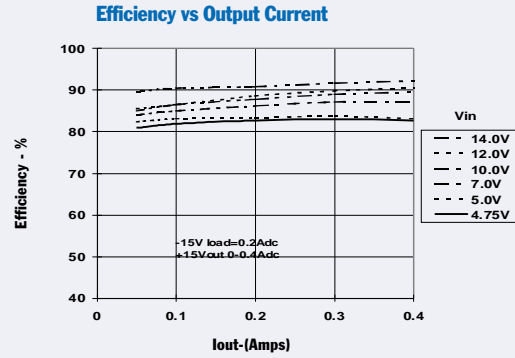
**PT5061 +/- 12VDC** (See Note A)



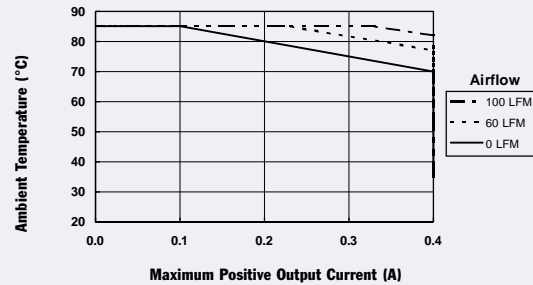
**Safe Operating Area,  $V_{in} = 5.0V$ ;  $I_{o2} = 0.25A$**  (See Note B)



**PT5062 +/- 15V** (See Note A)



**Safe Operating Area  $V_{in} = 5.0V$ ,  $I_{o2} = 0.2A$**  (See Note B)



**Note A:** Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.  
**Note B:** Thermal derating graphs are developed in free-air convection cooling, which corresponds to approximately 40-60 LFM of airflow.

## Adjusting the Output Voltage of the PT5060 Dual-Output Boost Converter Series

The dual output voltage of the PT5060 series modules can be adjusted higher or lower than the factory pre-set voltage with the addition of a single external resistor. Table 1 gives the applicable adjustment range for each model in the series as  $V_a$  (min) and  $V_a$  (max).

**Adjust Up:** An increase in the output voltage is obtained by adding a resistor  $R_2$ , between pin 11 ( $V_o$  adj) and pins 2, 6, or 7 (GND).

**Adjust Down:** Add a resistor ( $R_1$ ), between pin 11 ( $V_o$  adj) and pins 8, 9 or 10 ( $V_{o1}$ ).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either ( $R_1$ ) or  $R_2$  as appropriate.

### Notes:

- Both the positive and negative voltage outputs from the ISR are adjusted simultaneously.
- Use only a single 1% resistor in either the ( $R_1$ ) or  $R_2$  location. Place the resistor as close to the ISR as possible.
- Never connect capacitors from  $V_o$  adj to either GND or  $V_{o1}$ . Any capacitance added to the  $V_o$  adjust pin will affect the stability of the ISR.
- An increase in the output voltage must be accompanied by a corresponding reduction in the specified maximum current at each output. For  $V_{o1}$  and  $-V_{o2}$ , the revised maximum output current must be reduced to the equivalent of 6 watts and 3 watts respectively. i.e.

$$I_{o1}(\text{max}) = \frac{6}{V_a} \text{ A dc}$$

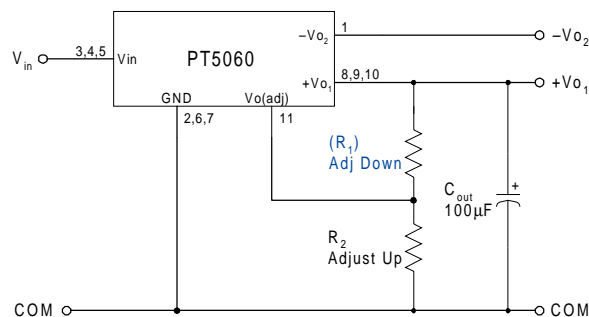
and

$$I_{o2}(\text{max}) = \frac{3}{V_a} \text{ A dc,}$$

where  $V_a$  is the adjusted output voltage.

- Adjustments to the output voltage will also limit the maximum input voltage that can be applied to the ISR. The maximum input voltage that may be applied is limited to  $(V_o - 1)\text{Vdc}$  or 14Vdc, whichever is less.

Figure 1



The values of ( $R_1$ ) [adjust down], and  $R_2$  [adjust up], can also be calculated using the following formulas.

$$(R_1) = \frac{3.65 (V_a - 2.5)}{(V_o - V_a)} - 0.1 \quad \text{k}\Omega$$

$$R_2 = \frac{9.125}{V_a - V_o} - 0.1 \quad \text{k}\Omega$$

Where:  $V_o$  = Original output voltage  
 $V_a$  = Adjusted output voltage

Table 1

PT5060 ADJUSTMENT AND FORMULA PARAMETERS		
Series Pt #	PT5061	PT5062
$V_o$ (nom)	$\pm 12.0\text{V}$	$\pm 15.0\text{V}$
$V_a$ (min)	$\pm 7.5\text{V}$	$\pm 7.5\text{V}$
$V_a$ (max)	$\pm 14.0\text{V}$	$\pm 20.0\text{V}$

Table 2

PT5060 ADJUSTMENT RESISTOR VALUES		
Series Pt #	PT5061	PT5062
Current	0.5/0.25A dc	0.4/0.2A dc
$V_o$ (nom)	$\pm 12.0\text{Vdc}$	$\pm 15.0\text{Vdc}$
$V_a$ (req'd)		
7.0		
7.5	(4.0)k $\Omega$	(2.3)k $\Omega$
8.0	(4.9)k $\Omega$	(2.8)k $\Omega$
8.5	(6.2)k $\Omega$	(3.3)k $\Omega$
9.0	(7.8)k $\Omega$	(3.9)k $\Omega$
9.5	(10.1)k $\Omega$	(4.6)k $\Omega$
10.0	(13.6)k $\Omega$	(5.4)k $\Omega$
10.5	(19.4)k $\Omega$	(6.4)k $\Omega$
11.0	(30.9)k $\Omega$	(7.7)k $\Omega$
11.5	(65.6)k $\Omega$	(9.3)k $\Omega$
12.0		(11.5)k $\Omega$
12.5	18.2k $\Omega$	(14.5)k $\Omega$
13.0	9.0k $\Omega$	(19.1)k $\Omega$
13.5	6.0k $\Omega$	(26.7)k $\Omega$
14.0	4.5k $\Omega$	(41.9)k $\Omega$
14.5		(87.5)k $\Omega$
15.0		
15.5		18.2k $\Omega$
16.0		9.0k $\Omega$
16.5		6.0k $\Omega$
17.0		4.5k $\Omega$
17.5		3.6k $\Omega$
18.0		2.9k $\Omega$
18.5		2.5k $\Omega$
19.0		2.2k $\Omega$
19.5		1.9k $\Omega$
20.0		1.7k $\Omega$

$R_1$  = (Blue)       $R_2$  = Black

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PT5061A	NRND	SIP MOD ULE	ECA	12	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT5061C	NRND	SIP MOD ULE	ECC	12	12	Pb-Free (RoHS)	Call TI	Level-1-215C-UNLIM
PT5061N	NRND	SIP MOD ULE	ECD	12	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT5061R	NRND	SIP MOD ULE	ECE	12	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT5062A	NRND	SIP MOD ULE	ECA	12	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT5062C	NRND	SIP MOD ULE	ECC	12	12	Pb-Free (RoHS)	Call TI	Level-1-215C-UNLIM
PT5062CT	NRND	SIP MOD ULE	ECC	12	200	Pb-Free (RoHS)	Call TI	Level-1-215C-UNLIM
PT5062G	NRND	SIP MOD ULE	ECG	12	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT5062N	NRND	SIP MOD ULE	ECD	12	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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