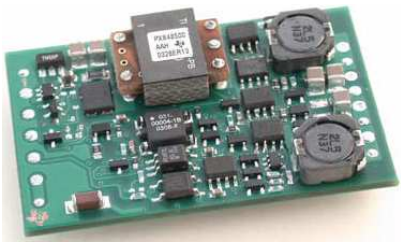
DUAL-OUTPUT, 48-V INPUT ISOLATED DC/DC CONVERTER for xDSL

FEATURES

- **Dual Outputs (Independently Regulated)**
- **Input Voltage Range: 36 V to 75 V**
- **Power-Up/Down Sequencing**
- **1500 VDC Isolation**
- **Over-Current Protection**
- **Over-Temperature Shutdown**
- **Under-Voltage Lockout**
- **Fixed Frequency Operation**
- **Temp Range: –40°C to 85°C**
- **Industry Standard Outline**
- **Operates with PTB4851x for Complete AC7 Power Solution**
- **Powers up to 64 DSL Ports**
- **Safety Approvals:**
  - **– UL/cUL 60950**
  - **– EN 60950**



DESCRIPTION

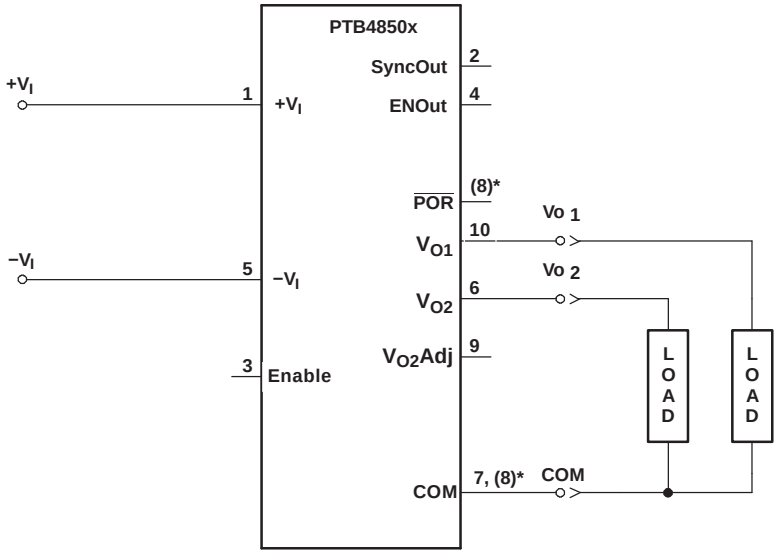
The PTB4850x power modules are a dual-output isolated DC/DC converter, designed to provide the logic supply voltages for AC-7 based xDSL applications. The PTB48500 is rated for 13 A of total output current, making it suitable for 32-channel xDSL applications. The PTB48501 and PTB48502 provide output current for powering up to 64 xDSL channels. The PTB48501 is rated for 16.5 A total output current, and the PTB48502, 21 A. The PTB48502 incorporates 10 W of additional capacity for powering peripheral circuitry. Any of these converters can be used for other applications with similar power requirements.

The modules operate from a standard telecom (–48 V) central office (CO) supply and include an *on/off* enable control, output current limit, over-temperature protection, input under-voltage lockout (UVLO). The PTB48500 and PTB48501 also incorporates a power-up reset (POR) output.

The modules are designed to operate with one of the PTB4851x DC/DC converter modules. The combination of PTB4850x and PTB4851x converter provides the complete the power supply for an AC7 chipset. The *EN Out* and *Sync Out* pins provide compatible output signals for controlling both the power up sequence and switching frequency the PTB48510.

The PTB4850x modules employ double-sided surface mount construction, and are an industry standard size.

STAND-ALONE APPLICATION



* Pin 8 is COM on PTB48502

ORDERING INFORMATION

Base Part No. (PTB4850_xxx)			Output Voltage (PTB4850x_xx)		Package Options (PT4850xx_ _)		
Order Prefix	**Description**		**Code**	**Voltage**	**Code**	**Description**	**Pkg Ref.(1)**
PTB48500xxx	13 A	(32-Ports)	A	3.3 V / 1.2 V	AH	Horiz. T/H	(ERH)
PTB48501xxx	16.5 A	(48/64-Ports)			AS	SMD, Standard(2)	(ERJ)
PTB48502xx	21 A	(64-Ports + 10 W)			AZ	SMD, Pb-free	(ERJ)

(1) Reference the applicable package reference drawing for the dimensions and PC board layout.
(2) *Standard* option specifies 63/37, Sn/Pb pin solder material.

Environmental and General Specifications

(Unless otherwise stated, all voltages are with respect to $-V_I$)

				VALUE	UNIT
V_I	Input Voltage Range	Over output load range		36 to 75	VDC
	Isolation Voltage	Input-output/input/case		1500	V
	Capacitance	Input to output		1500	pF
	Resistance	Input to output		10	mΩ
T_A	Operating Temperature Range	Over V_{in} Range		–40 to 85	° C
OTP	Over-Temperature Protection	Shutdown threshold		115	°C
		Hysterisis		10	
T_{reflow}	Solder Reflow Temperature	Surface temperature of module body or pins		235(1)	°C
T_S	Storage Temperature			–40 to 125	°C
	Mechanical Shock	Per Mil-STD-883D, Method 2002.3 1 msec, 1/2 Sine, mounted		500	G
	Mechanical Vibration Mil-STD-883D	Method 2007.2	Suffix H	20	G
		20-2000 Hz	Suffix C	5	
	Weight				grams
	Flammability	Meets UL 94V-O			

(1) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS (PTB48500A)

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, C_I = 0 µF, C_O = 0 µF, and I_O = 50% $I_o$max)

PARAMETER		TEST CONDITIONS		PTB48500A			UNIT
				MIN	TYP	MAX	
Po_1, Po_2	Output Power		Vo_1 (3.3 V)			19.8	W
			Vo_2 (1.2 V)			8.4	
Po_{total}	Both outputs					28	W
Io_1, Io_2	Output Current	Over V_I range	Vo_1 (3.3 V)	0		6 (1)	A
			Vo_2 (1.2 V)	0		7 (1)	
$Io_1 + Io_2$		Total (both outputs)		0		13	A
Vo_1	Output Voltage	Includes set point, line, load, –40°C ≤ T_A ≤ 85°C		3.2	3.3	3.4	V
Vo_2				1.16	1.2	1.24	
ΔReg_{temp}	Temperature Variation	–40°C ≤ T_A ≤ 85°C, I_O = I_O min	Vo_1		±0.5		%V_O
			Vo_2		±0.8		
ΔReg_{line}	Line Regulation	Over V_I range	Vo_1, Vo_2		±1	±10	mV
ΔReg_{load}	Load Regulation	Over $_{IO}$ range	Vo_1, Vo_2		±3	±12	mV
ΔReg_{cross}	Cross Regulation	I_O min ≤ Io_2≤ $I_o$max, Io_1 = 1 A	ΔVo_1			10	mV
		I_O min ≤ Io_1≤ $I_o$max, Io_2 = 1 A	ΔVo_2			10	
η	Efficiency	Io_1, Io_2 = $I_o$max			82%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth	Vo_1		20	50	mV_{pp}
			Vo_2		20	50	
t_{tr}	Transient Response	1 A/µs load step, 50% to 100% $I_o$max			30		µs
ΔV_{tr}		Vo_1, Vo_2 over/undershoot			±2.0		%V_O
$I_o$trip	Over Current Threshold	V_I = 36 V, reset followed by auto-recovery	$Io_1 + Io_2$	13.5	16		A
Vadj	Output Voltage Adjust Range	Vo_2 only		–10		20	%V_o
f_S	Switching Frequency	Over V_I and I_O ranges		500	550	600	kHz
V_I on	Under-Voltage Lockout	V_I increasing			34		V
V_I off		V_I decreasing			32		
V_{IH}	On/Off Enable (pin 3) Input High Voltage	Referenced to –V_I (pin 5)		3.6		75 (2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–1		mA
I_I standby	Standby Input Current	Pins 3 and 5 connected			2		mA
C_I	Internal Input Capacitance				2		µF
Co_1	External Output Capacitance			0 (3)		5000	µF
Co_2				0 (3)		5000	
MTBF	Reliability	Per Telcordia SR-332 50% stress, T_A = 40°C, ground benign		1.5			10^6 Hrs

(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to +V_I. The maximum open-circuit voltage is 7 V. If it is left open circuit the converter will operate when input power is applied.
(3) An output capacitor is not required.

ELECTRICAL CHARACTERISTICS (PTB48501A)

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, C_I = 0 µF, C_O = 0 µF, and I_O = 50% $I_o$max)

PARAMETER		TEST CONDITIONS		PTB48501A			UNIT
				MIN	TYP	MAX	
Po_1, Po_2	Output Power		Vo_1 (3.3 V)			19.8	W
			Vo_2 (1.2 V)			12.6	
Po_{total}	Both outputs					32.4	W
Io_1, Io_2	Output Current	Over V_I range	Vo_1 (3.3 V)	0		6 (1)	A
			Vo_2 (1.2 V)	0		10.5 (1)	
$Io_1 + Io_2$		Total (both outputs)		0		16.5	A
Vo_1	Output Voltage	Includes set point, line, load, –40°C ≤ T_A ≤ 85°C		3.2	3.3	3.4	V
Vo_2				1.16	1.2	1.24	
ΔReg_{temp}	Temperature Variation	–40°C ≤ T_A ≤ 85°C, I_O = I_O min	Vo_1		±0.5		%V_O
			Vo_2		±0.8		
ΔReg_{line}	Line Regulation	Over V_I range	Vo_1, Vo_2		±1	±10	mV
ΔReg_{load}	Load Regulation	Over $_{IO}$ range	Vo_1, Vo_2		±3	±12	mV
ΔReg_{cross}	Cross Regulation	I_O min ≤ Io_2≤ $I_o$max, Io_1 = 1 A	ΔVo_1			10	mV
		I_O min ≤ Io_1≤ $I_o$max, Io_2 = 1 A	ΔVo_2			10	
η	Efficiency	Io_1, Io_2 = $I_o$max			81%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth	Vo_1		20	50	mV_{pp}
			Vo_2		20	50	
t_{tr}	Transient Response	1 A/µs load step, 50% to 100% $I_o$max			30		µs
ΔV_{tr}		Vo_1, Vo_2 over/undershoot			±2.0		%V_O
$I_o$trip	Over Current Threshold	V_I = 36 V, reset followed by auto-recovery	$Io_1 + Io_2$		24		A
Vadj	Output Voltage Adjust Range	Vo_2 only		–20		10	%V_o
f_S	Switching Frequency	Over V_I and I_O ranges		500	550	600	kHz
V_I on	Under-Voltage Lockout	V_I increasing			34		V
V_I off		V_I decreasing			32		
V_{IH}	On/Off Enable (pin 3) Input High Voltage	Referenced to –V_I (pin 5)		3.6		75 (2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–1		mA
I_I standby	Standby Input Current	Pins 3 and 5 connected			2		mA
C_I	Internal Input Capacitance				2		µF
Co_1	External Output Capacitance			0 (3)		5000	µF
Co_2				0 (3)		5000	
MTBF	Reliability	Per Telcordia SR-332 50% stress, T_A = 40°C, ground benign		1.5			10^6 Hrs

(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to +V_I. The maximum open-circuit voltage is 7 V. If it is left open circuit the converter will operate when input power is applied.
(3) An output capacitor is not required.

ELECTRICAL CHARACTERISTICS (PTB48502A)

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, C_I = 0 µF, C_O = 0 µF, and I_O = 50% $I_o$max)

PARAMETER		TEST CONDITIONS		PTB48502A			UNIT
				MIN	TYP	MAX	
Po_1, Po_2	Output Power		Vo_1 (3.3 V)			33	W
			Vo_2 (1.2 V)			15.6	
Po_{total}	Both outputs					45	W
Io_1, Io_2	Output Current	Over V_I range	Vo_1 (3.3 V)	0		10(1)	A
			Vo_2 (1.2 V)	0		13(1)	
$Io_1 + Io_2$		Total (both outputs)		0		21	A
Vo_1	Output Voltage	Includes set point, line, load, –40°C ≤ T_A ≤ 85°C		3.2	3.3	3.4	V
Vo_2				1.16	1.2	1.24	
ΔReg_{temp}	Temperature Variation	–40°C ≤ T_A ≤ 85°C, I_O = I_O min	Vo_1		±0.5		$\%V_O$
			Vo_2		±0.8		
ΔReg_{line}	Line Regulation	Over V_I range	Vo_1, Vo_2		±1	±10	mV
ΔReg_{load}	Load Regulation	Over $_{IO}$ range	Vo_1, Vo_2		±3	±12	mV
ΔReg_{cross}	Cross Regulation	I_O min ≤ Io_2≤ $I_o$max, Io_1 = 1 A	ΔVo_1			10	mV
		I_O min ≤ Io_1≤ $I_o$max, Io_2 = 1 A	ΔVo_2			10	
η	Efficiency	Io_1, Io_2 = $I_o$max			82%		
V_r	V_O Ripple (pk-pk)	20 MHz bandwidth	Vo_1		20	50	mV_{pp}
			Vo_2		20	50	
t_{tr}	Transient Response	1 A/µs load step, 50% to 100% $I_o$max			30		µs
ΔV_{tr}		Vo_1, Vo_2 over/undershoot			±2.0		$\%V_O$
$I_o$trip	Over Current Threshold	V_I = 36 V, reset followed by auto-recovery	$Io_1 + Io_2$		24		A
Vadj	Output Voltage Adjust Range	Vo_2 only		–20		10	$\%V_o$
f_S	Switching Frequency	Over V_I and I_O ranges		500	550	600	kHz
V_I on	Under-Voltage Lockout	V_I increasing			34		V
V_I off		V_I decreasing			32		
V_{IH}	On/Off Enable (pin 3) Input High Voltage	Referenced to –V_I (pin 5)		3.6		75(2)	V
V_{IL}	Input Low Voltage			–0.2		0.8	
I_{IL}	Input Low Current				–1		mA
I_I standby	Standby Input Current	Pins 3 and 5 connected			2		mA
C_I	Internal Input Capacitance				2		µF
Co_1	External Output Capacitance			0(3)		5000	µF
Co_2				0(3)		5000	
MTBF	Reliability	Per Telcordia SR-332 50% stress, T_A = 40°C, ground benign		1.5			10^6 Hrs

(1) See Safe Operating Area curves or contact the factory for the appropriate derating.
(2) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to +V_I. The maximum open-circuit voltage is 7 V. If it is left open circuit the converter will operate when input power is applied.
(3) An output capacitor is not required.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
$+V_I$ (1)	1	The positive input supply for the module with respect to $-V_I$. When powering the module from a –48 V telecom central office supply, this input is connected to the primary system ground.
$-V_I$	5	The negative input supply for the module, and the 0 VDC reference for the *Enable*, *EN Out*, and *Sync Out* signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.
V_O1	10	The higher regulated power output voltage, which is referenced to the COM node.
V_O2	6	The lower regulated power output voltage, which is referenced to the COM node.
COM	7	The secondary return reference for the module's two regulated output voltages. It is dc isolated from the input supply pins.
V_O2 Adjust	9	Using a single resistor, this pin allows V_O2 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.
Enable (2)	3	This is an open-collector (open-drain) positive logic input that enables the module output. This pin is referenced to $-V_I$. A logic 0 at this pin disables the module's outputs, and a high impedance enables the outputs. If not used the pin should be left unconnected.
EN Out	4	This open-collector output may be used to enable the output of other DC/DC converters in applications where the power-up sequence of the related voltages must be precisely controlled. The output is used principally to control the startup up of a PTB4851xx module when powering ADSL circuits based on the AC7 chipset. The signal is referenced to $-V_I$, and is active low. It is initially *off* (high impedance), and turns *on* when the output voltage, V_O1, has risen to its nominal set-point voltage.
Sync Out	2	The signal generated by this pin is designed to be used exclusively with the PTB48510 in AC7 ADSL applications. When the *Sync Out* of this converter is connected directly to the *Sync In* pin of the PTB48510, both modules will operate at the same switch conversion frequency.
POR (3)/COM (4)	8	(POR: Available to PTB48500 and PTB48501 only.) This pin produces an active-low power-on reset signal that may be used to reset logic circuitry. The output is set low during power up just as the output voltage from V_O1 starts to rise. It remains low for 10 ms after the voltage at V_O1 has reached its nominal set-point voltage. This signal is referenced to the COM node, and has a 3.3-kΩ internal pull-up resistor to V_O1.

(1) Shaded functions indicate signals that are referenced to $-V_I$.
(2) Denotes positive logic: Open = Normal operation, $-V_I$ = Outputs Off
(3) Denotes negative logic: High = Normal operation, Low = Reset
(4) This pin is COM on the PTB48502.

TYPICAL CHARACTERISTICS (1)(2)(3)

CHARACTERISTIC DATA (PTB48500A)

EFFICIENCY vs LOAD CURRENT

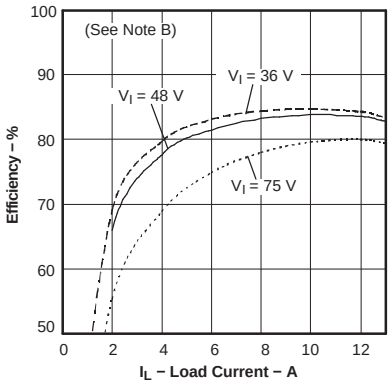


Figure 1.

POWER DISSIPATION vs LOAD CURRENT

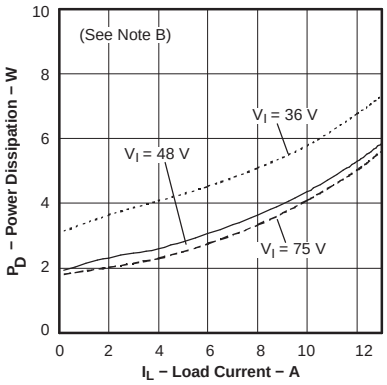


Figure 2.

CROSS REGULATION ΔVo_x vs Io_y Io_x = 1 A and V_I = 48 V

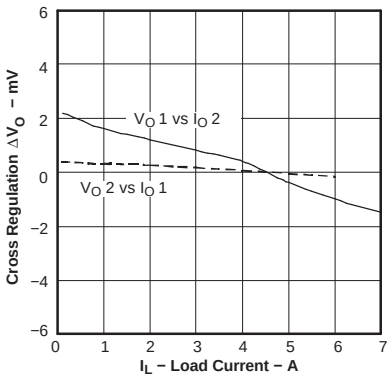


Figure 3.

SAFE OPERATING AREA V_I = 48 VDC

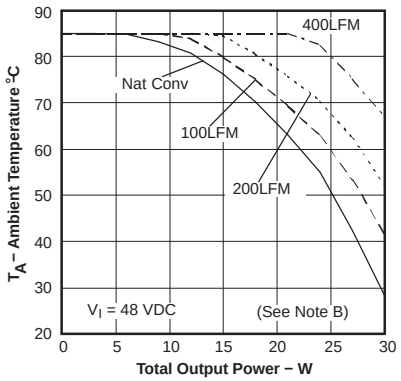


Figure 4.

(1) A. Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.
(2) B. Load current is increased proportionally from both outputs, up to the indicated maximum value of each respective output.
(3) C. SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

TYPICAL CHARACTERISTICS (1)(2)(3)

PTB48501A CHARACTERISTIC DATA (PTB48501A)

EFFICIENCY vs LOAD CURRENT

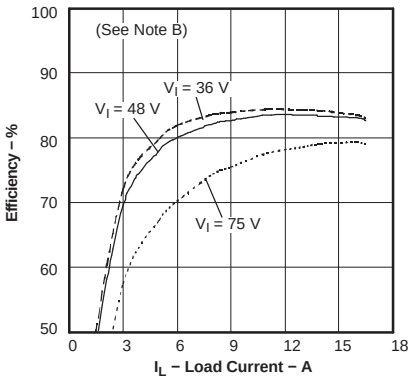


Figure 5.

POWER DISSIPATION vs LOAD CURRENT

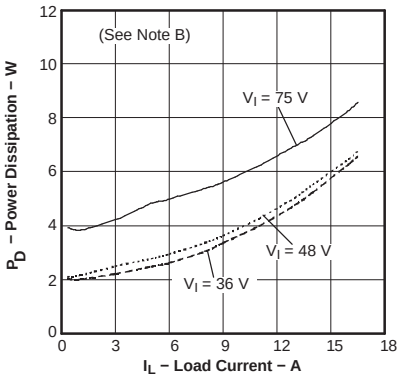


Figure 6.

CROSS REGULATION ΔVo_x vs Io_y Io_x = 1 A and V_I = 48 V

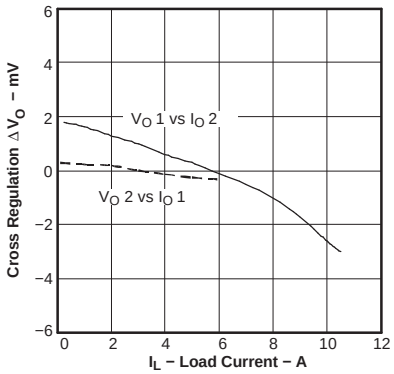


Figure 7.

SAFE OPERATING AREA V_I = 48 VDC

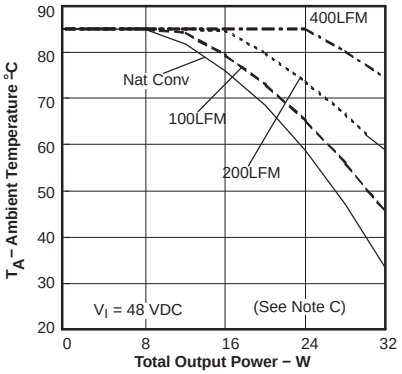


Figure 8.

(1) A. Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.
(2) B. Load current is increased proportionally from both outputs, up to the indicated maximum value of each respective output.
(3) C. SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

TYPICAL CHARACTERISTICS (1)(2)(3)

CHARACTERISTIC DATA (PTB48502A)
[Io_1 = 10 A, Io_2 = 10 A represents 100% load]

EFFICIENCY vs LOAD CURRENT

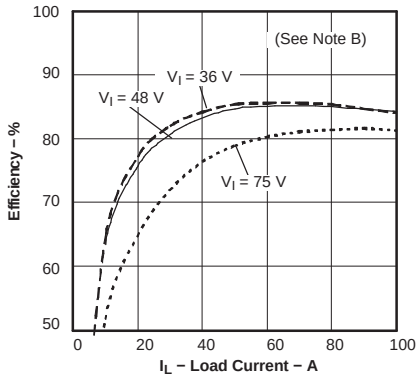


Figure 9.

POWER DISSIPATION vs LOAD CURRENT

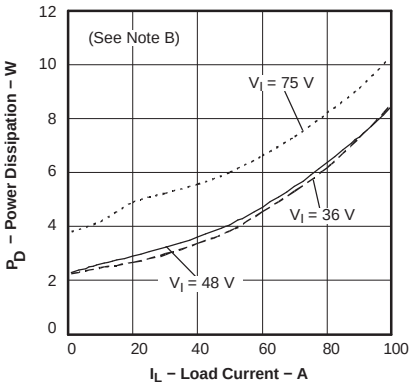


Figure 10.

CROSS REGULATION
ΔVo_x vs Io_y
Io_x = 1 A and V_I = 48 V

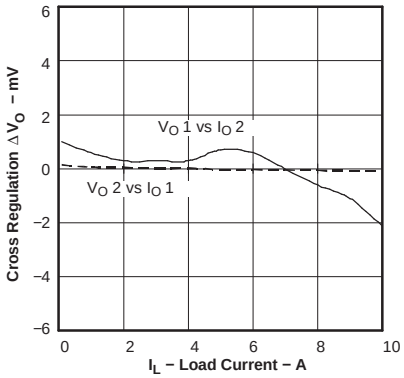


Figure 11.

SAFE OPERATING AREA
V_I = 48 V

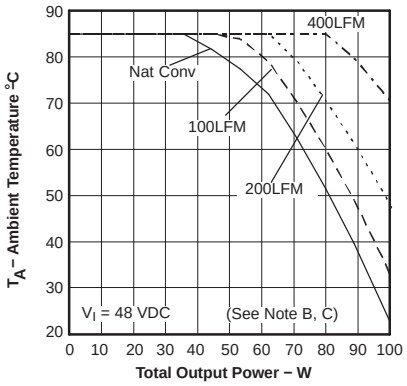


Figure 12.

(1) A. Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.
(2) B. Load current is increased proportionally from both outputs, up to the indicated maximum value of each respective output.
(3) C. SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

TYPICAL CHARACTERISTICS (1)(2)(3)

CHARACTERISTIC DATA (PTB48502A)
[Io_1 = 8 A, Io_2 = 10 A represents 100% load]

EFFICIENCY vs LOAD CURRENT

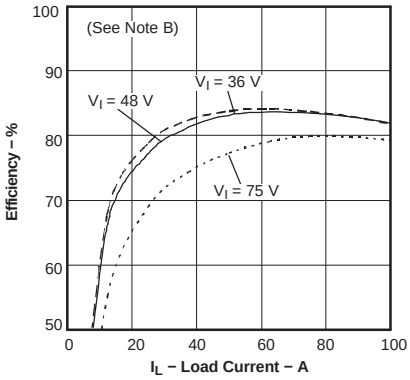


Figure 13.

POWER DISSIPATION vs LOAD CURRENT

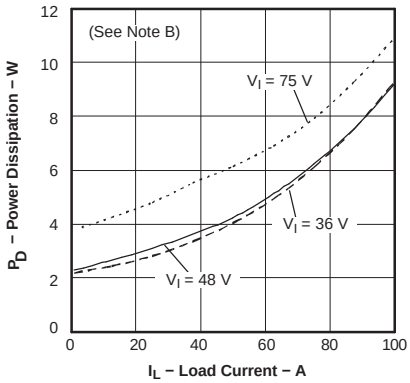


Figure 14.

CROSS REGULATION
ΔVo_x vs Io_y
Io_x = 1 A and V_I = 48 V

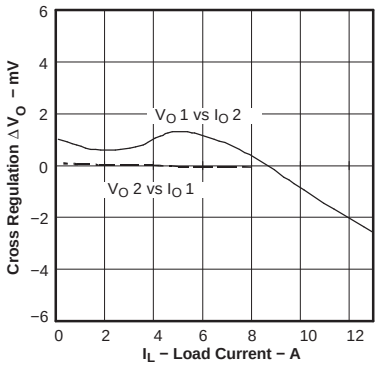


Figure 15.

SAFE OPERATING AREA
V_I = 48 V

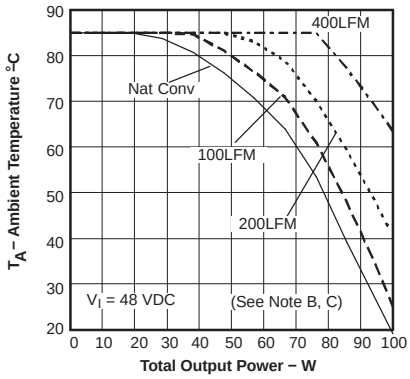


Figure 16.

(1) A. Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.
(2) B. Load current is increased proportionally from both outputs, up to the indicated maximum value of each respective output.
(3) C. SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

APPLICATION INFORMATION

ADJUSTING THE LOWER OUTPUT VOLTAGE OF THE PTB4850x

The PTB4850x series of DC/DC converters are designed to produce two logic-level supply voltages for use with the AC-7 ADSL chipset. The magnitude of lowest output voltage (Vo_2) can be adjusted higher or lower by up to 10% or —20% of the nominal. The adjustment method uses a single external resistor.[1] The value of the resistor determines the amount of adjustment, and its placement determines whether the voltage is increased or decreased. The resistor values can be calculated using the appropriate formula (see Equation 1 and Equation 2), or simply selected from the range of values given in Table 2. The placement of each resistor is as follows.

Adjust Up: To increase the magnitude of both output voltages, place a resistor R_1 between *Vo_2 Adj* (pin 9) and the *Vo_2* (pin 6) voltage rail; see Figure 17.

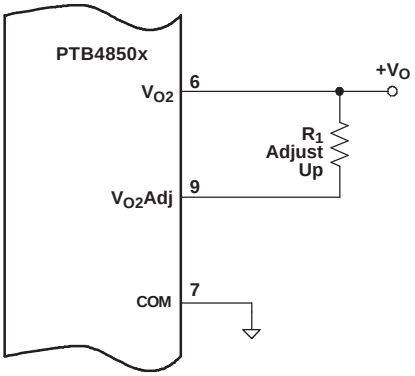


Figure 17. Adjust Up

Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R_2), between *Vo_2 Adj* (pin 9) and the *COM* (pin 7) voltage rail; see Figure 18.

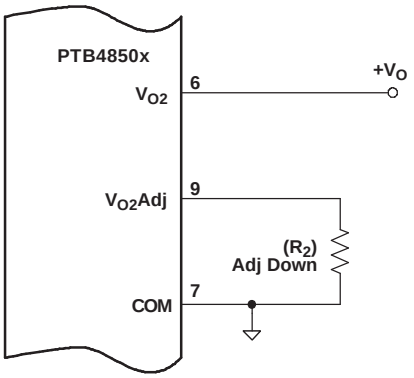


Figure 18. Adjust Down

CALCULATION OF THE ADJUST RESISTOR

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R_1 to adjust up, or (R_2) to adjust down.

$$R_1\ [\text{Adjust Up}] = R_p \times \frac{V_a}{(V_a - V_o)} - R_s\ k\Omega \quad (1)$$

$$(R_2)\ [\text{Adjust Down}] = R_n \times \frac{V_a}{(V_o - V_a)} - R_s\ k\Omega \quad (2)$$

Where:

V_o = Magitude of the original output voltage
V_a = Magnitude of the adjusted voltage
R_p = Adjust-up constant from Table 1
R_n = Adjust-down constant from Table 1
R_s = Internal series resistor from Table 1

Table 1. Adjustment Range and Formula Parameters

Part No.	PTB48500(1)A	PTB48502A
V_o(nom)	1.2 V	1.2 V
V_a(min)	0.96 V	0.84 V
V_a(max)	1.32 V	1.32 V
R_p (kΩ)	1.648	1.196
R_n (kΩ)	4.624	3.598
R_s (kΩ)	18.2V	13.0

NOTES:

1. A 0.05 W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the R_1 or (R_2) location, as close to the converter as possible.
2. Never connect capacitors to the *Vo_2 Adj* pin. Capacitance added to this pin can affect the stability of the regulated output.

Table 2. Adjust Resistor Values

Part No.		PTB4850xA	PTB48502A
% Adjust	V_a (V)	R_1 / (R_2)(1)	R_1 / (R_2)(1)
–21	0.848	N/A	(0.5) kΩ
–20	0.960	(0.3) kΩ	(1.4) kΩ
–19	0.972	(1.5) kΩ	(2.3) kΩ
–18	0.984	(2.9) kΩ	(3.4) kΩ
–17	0.996	(4.4) kΩ	(4.6) kΩ
–16	1.008	(6.1) kΩ	(5.9) kΩ
–15	1.020	(8.0) kΩ	(7.4) kΩ
–14	1.032	(10.2) kΩ	(9.1) kΩ

(1) R_1 =Adjust up, (R_2) =Adjust down

Table 2. Adjust Resistor Values (continued)

Part No.		PTB4850xA	PTB48502A
% Adjust	V_a (V)	R_1 / (R_2)(1)	R_1 / (R_2)(1)
–13	1.044	(12.7) kΩ	(11.1) kΩ
–12	1.056	(15.7) kΩ	(13.4) kΩ
–11	1.068	(19.2) kΩ	(16.1) kΩ
–10	1.080	(23.4) kΩ	(19.4) kΩ
– 9	1.092	(28.6) kΩ	(23.4) kΩ
– 8	1.104	(35) kΩ	(28.4) kΩ
–7	1.116	(43.2) kΩ	(34.8) kΩ
–6	1.128	(54.2) kΩ	(43.4) kΩ
–5	1.140	(69.7) kΩ	(55.4) kΩ
–4	1.152	(92.8) kΩ	(73.4) kΩ
–3	1.164	(131) kΩ	103.0) kΩ
–2	1.176	(208) kΩ	163.0) kΩ
–1	1.188	(440) kΩ	343.0) kΩ
0	1.200		
+ 1	1.212	148 kΩ	108.0 kΩ
+ 2	1.224	65.8 kΩ	48.0 kΩ
+ 3	1.236	38.4 kΩ	28.1 kΩ
+ 4	1.248	24.6 kΩ	18.1 kΩ
+ 5	1.260	16.4 kΩ	12.1 kΩ
+ 6	1.272	10.9 kΩ	8.1 kΩ
+ 7	1.284	7 kΩ	5.3 kΩ
+ 8	1.296	4.1 kΩ	3.2 kΩ
+ 9	1.308	1.8 kΩ	1.5 kΩ
+10	1.320	0 kΩ	0.2 kΩ

CONFIGURING THE PTB4850X AND PTB4851X FOR DSL APPLICATIONS

When operated as a pair, the PTB4850x and PTB4851x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB4851x produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB4851x may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 20 shows the required cross-connects between the two converters to enable these two features.

SWITCHING FREQUENCY SYNCHRONIZATION

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

POWER-UP SEQUENCING

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be guaranteed if the PTB4850x and PTB4851x are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the *EN Out* pin of the PTB4850x is directly connected to the activelow *Enable* input of the PTB4851x (see Figure 20). This allows the PTB4850x to momentarily hold off the outputs from the PTB4851x until the logic-level voltages have risen first. Figure 19 shows the power-up waveforms of all four supply voltages from the schematic of Figure 20.

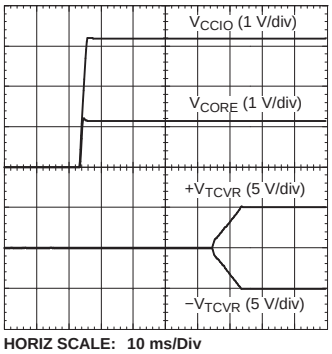


Figure 19. Power-Up Sequencing Waveforms

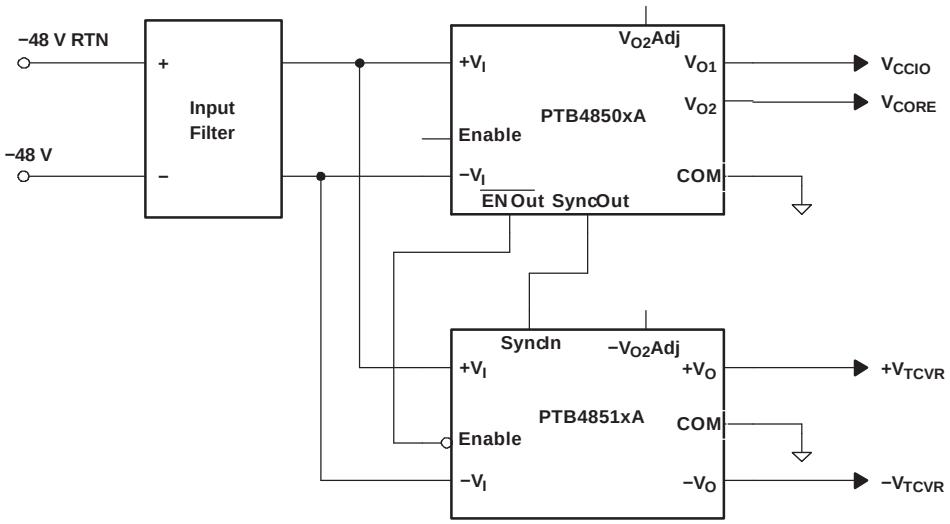


Figure 20. Example of PTB4850x and PTB4851x Modules Configured for DSL Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTB48502AAZ	NRND	Surface Mount Module	ERJ	10	9	RoHS (In Work) & non-Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

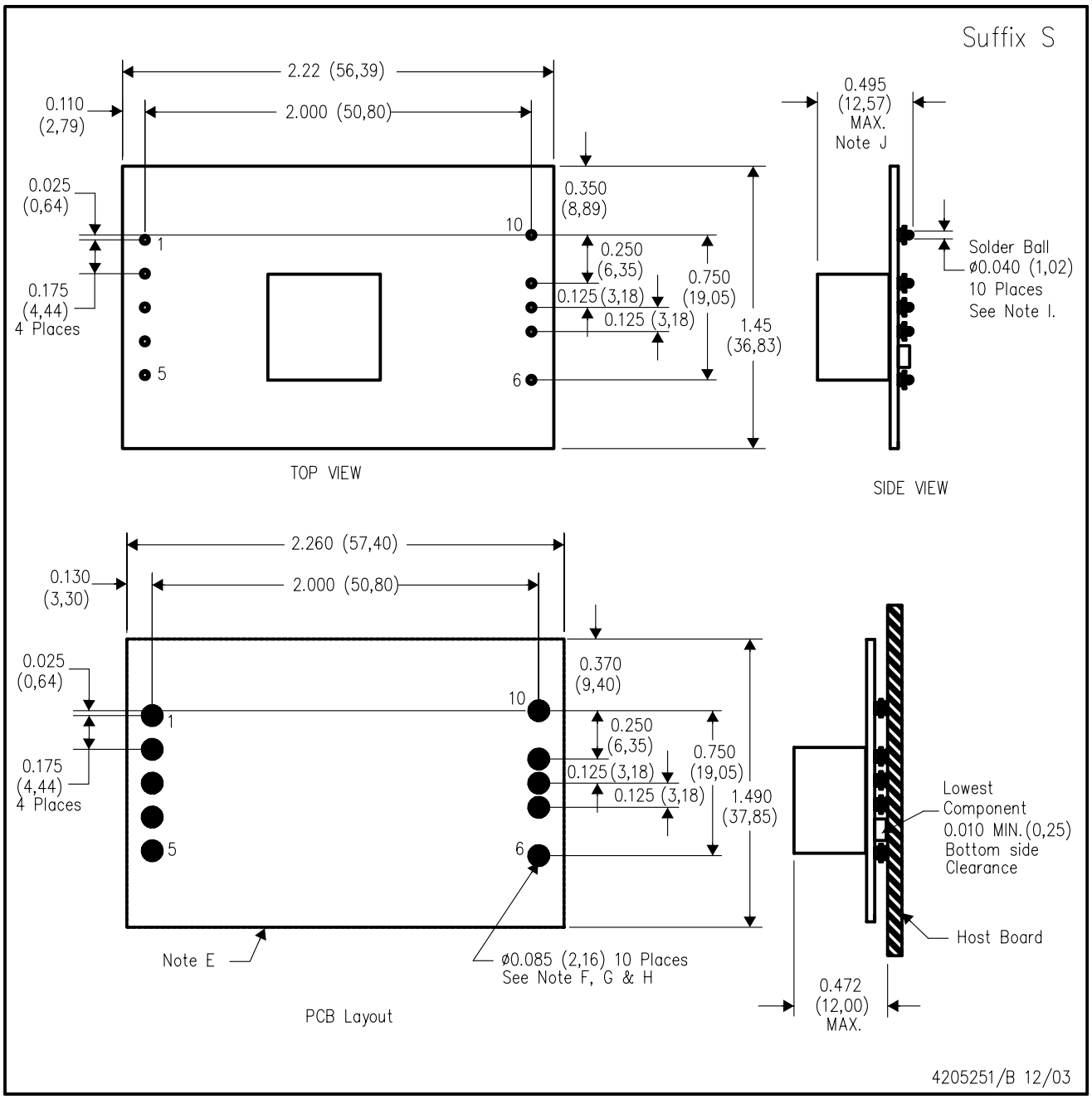
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ERJ (R–PDSS–B10) DOUBLE SIDED MODULE



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ±0.020 (±0,51mm).
- D. 3 place decimals are ±0.010 (±0,25mm).
- E. Recommended keep out area for user components.
- F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material – Copper Alloy
  Finish – Tin (100%) over Nickel plate
  Solder Ball – See product data sheet.
- J. Dimension prior to reflow solder.

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