

# SN54AHCT132, SN74AHCT132 Quadruple Positive-NAND Gates With Schmitt-trigger Inputs

## 1 Features

- Operating range of 4.5 V to 5.5 V
- Low power consumption, 10-μA maximum  $I_{CC}$
- ±8-mA output drive at 5 V
- Operation from very slow input transitions
- Temperature-compensated threshold levels
- High noise immunity
- Same pinouts as 'AHCT00
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)

## 3 Description

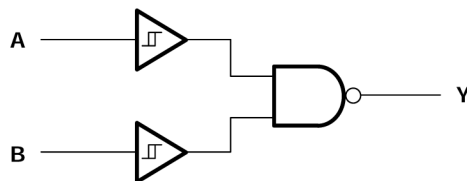
The 'AHCT132 devices are quadruple positive-NAND gates. These devices perform the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	PACKAGE SIZE	BODY SIZE (NOM)
SN74AHCT132	D (SOIC, 14)	8.7 mm × 6 mm	8.7 mm × 3.9 mm
	DB (SSOP, 14)	6.2 mm × 7.8 mm	6.2 mm × 5.3 mm
	DGV (TVSOP, 14)	3.6 mm × 6.4 mm	3.6 mm × 4.4 mm
	N (PDIP, 14)	19.3 mm × 8 mm	19.3 mm × 6.3 mm
	NS (SOP, 14)	10.3 mm × 7.8 mm	10.3 mm × 5.3 mm
	PW (TSSOP, 14)	5 mm × 6.4 mm	5 mm × 4.4 mm
	BQA (WQFN, 14)	3 mm × 2.5 mm	3 mm × 2.5 mm
SN54AHCT132	J (CDIP, 14)	21.3 mm × 7.6 mm	19.56 mm × 6 mm
	W (CFP, 14)	9.9 mm × 6.3 mm	9.2 mm × 6.3 mm
	FK (LCCC, 20)	8.9 mm × 8.9 mm	8.9 mm × 8.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram, Each Gate (Positive Logic)



## Table of Contents

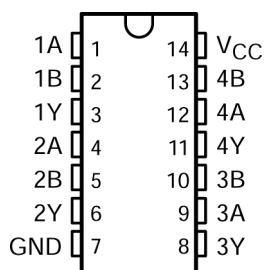
<b>1 Features</b> .....	<b>1</b>	8.1 Overview.....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	8.2 Functional Block Diagram.....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	8.3 Feature Description.....	<b>9</b>
<b>4 Revision History</b> .....	<b>2</b>	8.4 Device Functional Modes.....	<b>10</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Application and Implementation</b> .....	<b>11</b>
<b>6 Specifications</b> .....	<b>5</b>	9.1 Application Information.....	<b>11</b>
6.1 Absolute Maximum Ratings.....	<b>5</b>	9.2 Typical Application.....	<b>11</b>
6.2 ESD Ratings.....	<b>5</b>	9.3 Power Supply Recommendations.....	<b>14</b>
6.3 Recommended Operating Conditions.....	<b>5</b>	9.4 Layout.....	<b>14</b>
6.4 Thermal Information.....	<b>5</b>	<b>10 Device and Documentation Support</b> .....	<b>15</b>
6.5 Electrical Characteristics.....	<b>6</b>	10.1 Receiving Notification of Documentation Updates.....	<b>15</b>
6.6 Switching Characteristics.....	<b>6</b>	10.2 Support Resources.....	<b>15</b>
6.7 Noise Characteristics.....	<b>6</b>	10.3 Trademarks.....	<b>15</b>
6.8 Operating Characteristics.....	<b>7</b>	10.4 Electrostatic Discharge Caution.....	<b>15</b>
6.9 Typical Characteristics.....	<b>7</b>	10.5 Glossary.....	<b>15</b>
<b>7 Parameter Measurement Information</b> .....	<b>8</b>	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>
<b>8 Detailed Description</b> .....	<b>9</b>		

## 4 Revision History

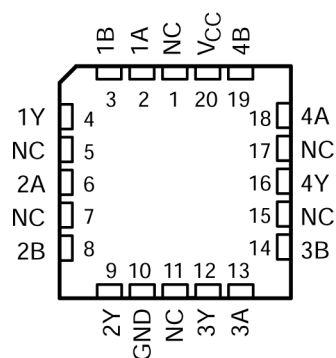
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision H (May 2023) to Revision I (October 2023)</b>	<b>Page</b>
• Updated RθJA values: D = 86 to 124.5, PW = 113 to 147.7, all values in °C/W .....	<b>5</b>
<b>Changes from Revision G (May 1997) to Revision H (May 2023)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	<b>1</b>
• Added BQA package information to the data sheet.....	<b>1</b>

## 5 Pin Configuration and Functions

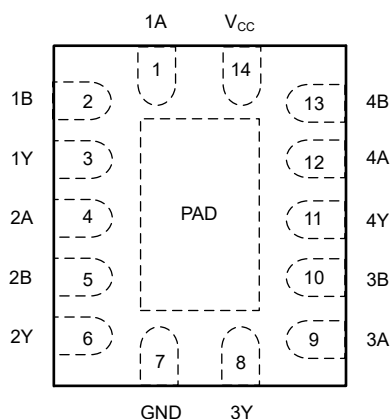


**Figure 5-1. SN54AHCT132 J or W Package  
SN74AHCT132 D, DB, DGV, N, NS, or PW Package  
(Top View)**



NC – No internal connection

**Figure 5-2. SN54AHCT132 FK Package (Top View)**



**Figure 5-3. SN74AHCT132 BQA Package (Top View)**

**Table 5-1. Pin Functions**

PIN					TYPE <sup>(1)</sup>	DESCRIPTION
NAME	SN74AHCT132		SN54AHCT132			
	D, DB, DGV, N, NS, PW	BQA	J, W	FK		
1A	1	1	1	2	I	1A Input
1B	2	2	2	3	O	1Y Output
1Y	3	3	3	4	I	2A Input
2A	4	4	4	6	O	2Y Output
2B	5	5	5	8	I	3A Input
2Y	6	6	6	9	O	3Y Output
3A	9	9	9	13	I	4A Input
3B	10	8	8	14	O	4Y Output
3Y	8	11	11	12	I	5A Input
4A	12	10	10	18	I	5Y Output
4B	13	13	13	19	I	6A Input
4Y	11	12	12	16	O	6Y Output
GND	7	7	7	—	—	Ground Pin
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No Connection

Table 5-1. Pin Functions (continued)

PIN					TYPE <sup>(1)</sup>	DESCRIPTION
NAME	SN74AHCT132		SN54AHCT132			
	D, DB, DGV, N, NS, PW	BQA	J, W	FK		
V <sub>CC</sub>	14	14	14	20	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	–0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage	–0.5	7	V
V <sub>O</sub> <sup>(2)</sup>	Output voltage	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0)	–20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHCT132		SN74AHCT132		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–8		–8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 6.4 Thermal Information

		SNx4AHCT132						UNIT
		D	DB	DGV	N	NS	PW	
THERMAL METRIC <sup>1</sup>		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.5	96	127	80	76	147.7	88.3

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25 °C			SN54AHCT132		SN74AHCT132		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		4.5 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		5.5 V	1		2.1	1	2.1	1	2.1	
V <sub>T-</sub> Negative-going input threshold voltage		4.5 V	0.5		1.5	0.5	1.5	0.5	1.5	V
		5.5 V	0.6		1.7	0.6	1.7	0.6	1.7	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		4.5 V	0.3		1.4	0.3	1.4	0.3	1.4	V
		5.5 V	0.3		1.5	0.3	1.5	0.3	1.5	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20		20	μA
ΔI <sub>CC</sub> <sup>(2)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10				10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCT132		SN74AHCT132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5.5 <sup>(1)</sup>	8 <sup>(1)</sup>		1 <sup>(1)</sup>	9 <sup>(1)</sup>	1	9	ns
t <sub>PHL</sub>				4.5 <sup>(1)</sup>	6 <sup>(1)</sup>		1 <sup>(1)</sup>	7 <sup>(1)</sup>	1	7	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	6.5	9		1	10	1	10	ns
t <sub>PHL</sub>				5.5	7		1	8	1	8	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.7 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C<sup>(1)</sup>

PARAMETER		SN74AHCT132			UNIT
		MIN	TYP	MAX	
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.5	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.28	-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		5		V
V <sub>IH(D)</sub>	High-level dynamic input voltage		2		V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

## 6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	15	pF

## 6.9 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

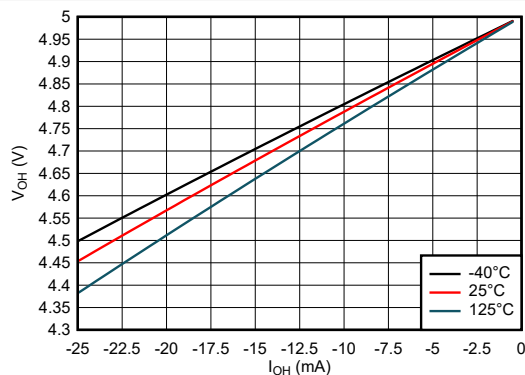


Figure 6-1. Output Voltage vs Current in HIGH State; 5-V Supply

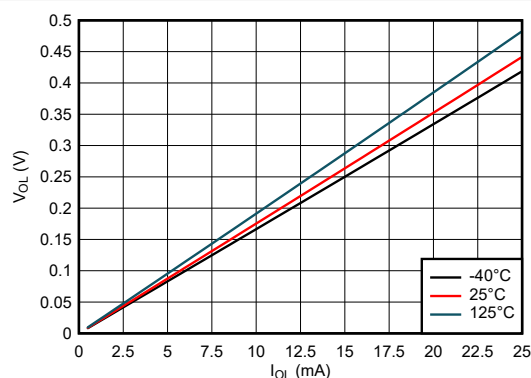
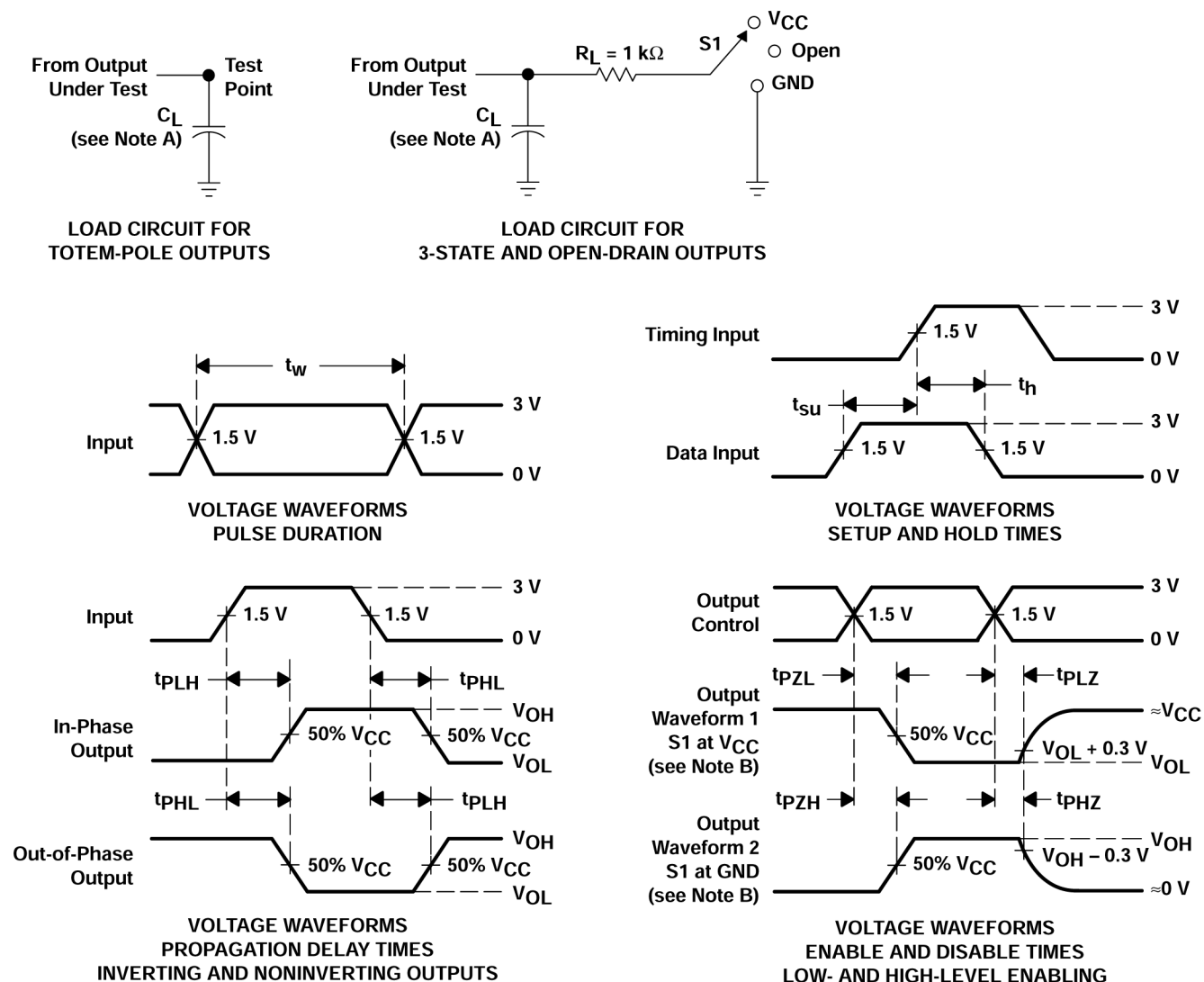


Figure 6-2. Output Voltage vs Current in LOW State; 5-V Supply

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

**Figure 7-1. Load Circuit and Voltage Waveforms**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



## 8 Detailed Description

### 8.1 Overview

The 'AHCT132 devices are quadruple positive-NAND gates.

These devices perform the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

### 8.2 Functional Block Diagram

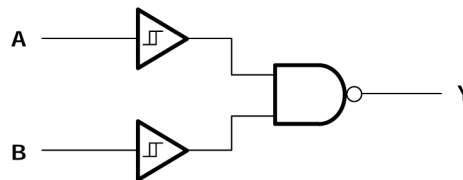


Figure 8-1.

### 8.3 Feature Description

#### 8.3.1 TTL-Compatible Schmitt-Trigger CMOS Inputs

This device includes TTL-compatible CMOS inputs with Schmitt-trigger architecture. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage thresholds.

TTL-compatible Schmitt-trigger CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10-k $\Omega$  resistor is recommended and will typically meet all requirements.

#### 8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.3 Clamp Diode Structure

As Figure 8-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

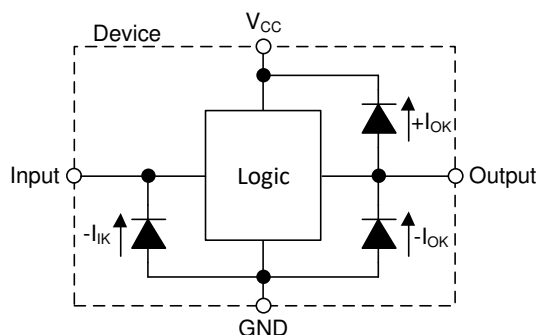


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

Table 8-1. Function Table  
(Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

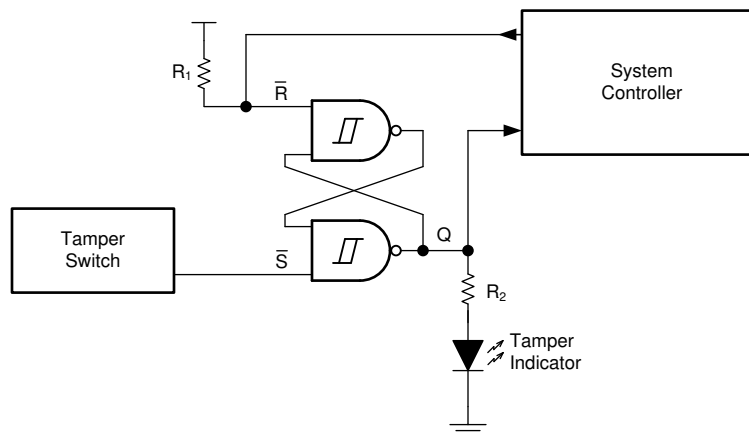
### 9.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in *Typical Application*. The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The AHCT132 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the  $\bar{R}$  input which returns the Q output back to LOW.

The inputs of this active-low SR latch can often be driven by open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z. This makes the AHCT132 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

### 9.2 Typical Application



**Figure 9-1. Typical Application Block Diagram**

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SNx4AHCT132 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4AHCT132 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground

connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SNx4AHCT132 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SNx4AHCT132 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Input signals must cross  $V_{t-(min)}$  to be considered a logic LOW, and  $V_{t+(max)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4AHCT132 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SNx4AHCT132 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the  $\Delta V_{T(min)}$  in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than  $V_{CC}$  or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.

2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4AHCT132 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.3 Application Curves

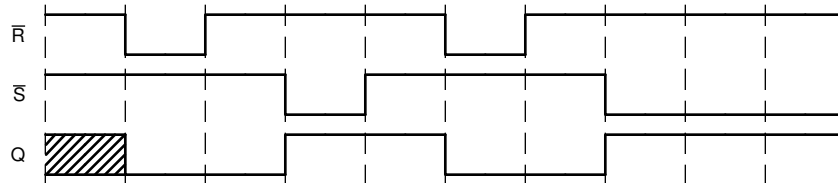


Figure 9-2. Application Timing Diagram

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 9.4.2 Layout Example

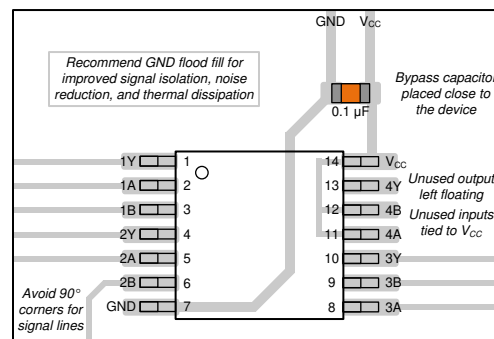


Figure 9-3. Example layout for the SN74AHCT132

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.3 Trademarks

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### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT132BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHT132	<a href="#">Samples</a>
SN74AHCT132DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB132	<a href="#">Samples</a>
SN74AHCT132DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB132	<a href="#">Samples</a>
SN74AHCT132DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT132	<a href="#">Samples</a>
SN74AHCT132N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT132N	<a href="#">Samples</a>
SN74AHCT132NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT132	<a href="#">Samples</a>
SN74AHCT132PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB132	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT132BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT132DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT132DGV	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT132NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT132PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT132PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT132BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT132DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHCT132DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHCT132DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHCT132DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHCT132NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHCT132PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT132PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT132N	N	PDIP	14	25	506	13.97	11230	4.32

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