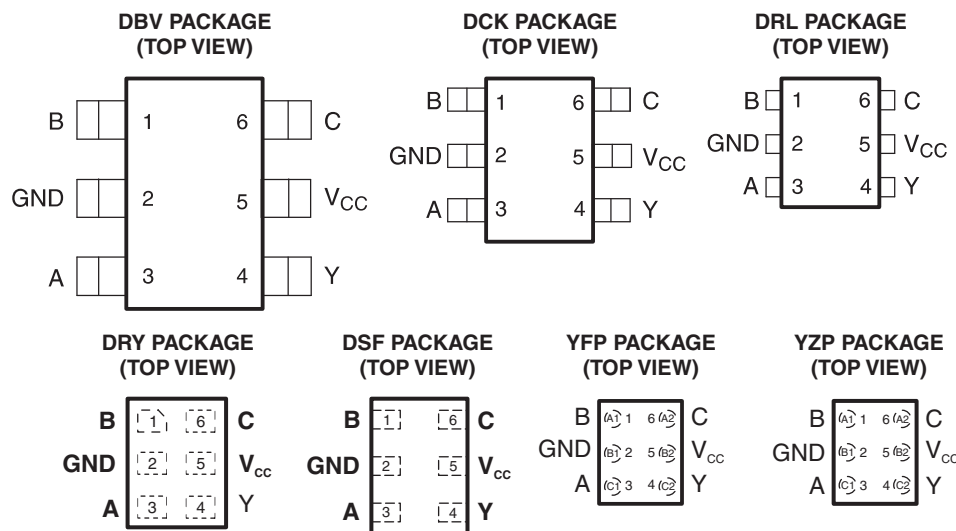


LOW-POWER CONFIGURABLE MULTIPLE-FUNCTION GATE

Check for Samples: [SN74AUP1G98](#)

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A Max}$)
- Low Dynamic-Power Consumption ($C_{pd} = 4.6 \text{ pF Typ at } 3.3 \text{ V}$)
- Low Input Capacitance ($C_i = 1.5 \text{ pF Typ}$)
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.3 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 2](#)).

The SN74AUP1G98 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

The device functions as an independent gate with Schmitt-trigger inputs, which allow for slow input transition and better switching-noise immunity at the input.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

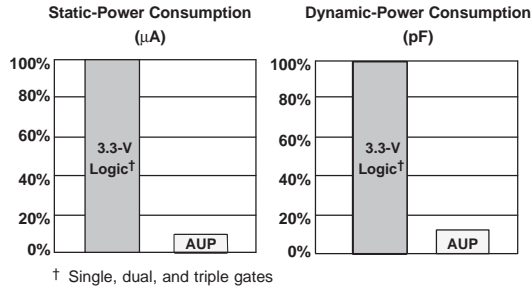


Figure 1. AUP – The Lowest-Power Family

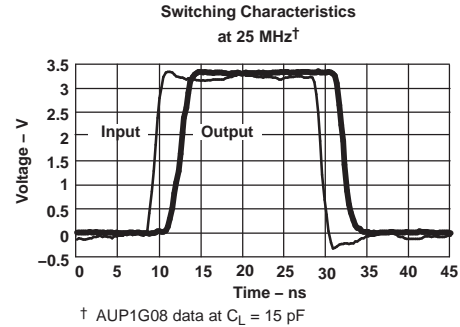


Figure 2. Excellent Signal Integrity

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G98YFPR	___ H R _
	NanoStar – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G98YZPR	___ H R _
	QFN – DRY	Reel of 5000	SN74AUP1G98DRYR	HR
	uQFN – DSF	Reel of 5000	SN74AUP1G98DSFR	HR
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G98DBVR	H98_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G98DCKR	HR_
SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G98DRLR		

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

FUNCTION TABLE

INPUTS			OUTPUT Y
C	B	A	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)

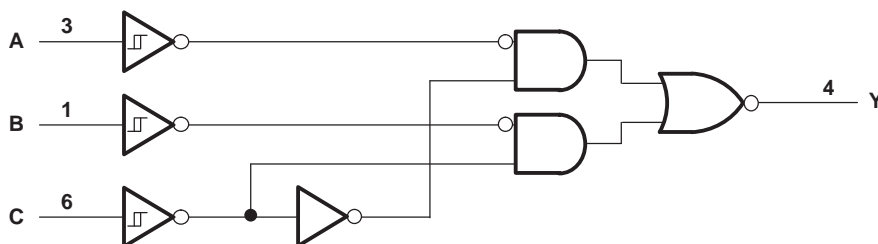


Table 1. FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector with inverted output	Figure 3
2-input NAND gate	Figure 4
2-input NOR gate with one inverted input	Figure 5
2-input AND gate with one inverted input	Figure 5
2-input NAND gate with one inverted input	Figure 6
2-input OR gate with one inverted input	Figure 6
2-input NOR gate	Figure 7
Noninverted buffer	Figure 8
Inverter	Figure 9

LOGIC CONFIGURATIONS

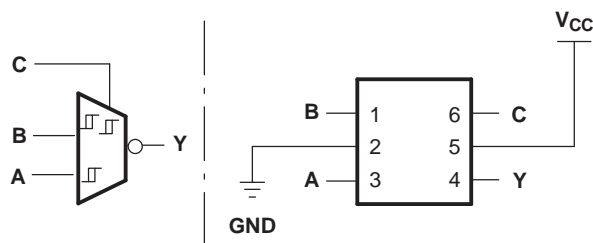


Figure 3. 2-to-1 Data Selector With Inverted Output
 When C is L, $Y = \overline{B}$
 When C is H, $Y = \overline{A}$

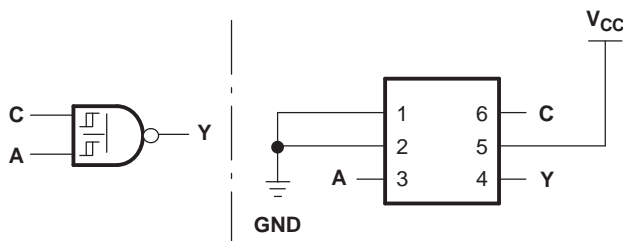


Figure 4. 2-Input NAND Gate

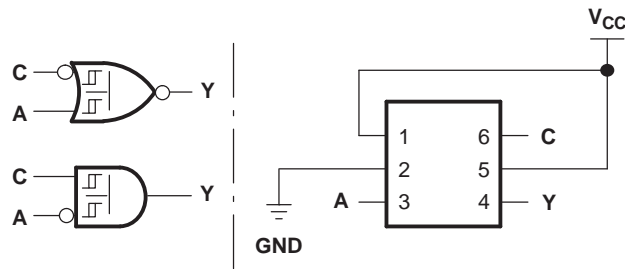


Figure 5. 2-Input NOR Gate With One Inverted Input
2-Input AND Gate With One Inverted Input

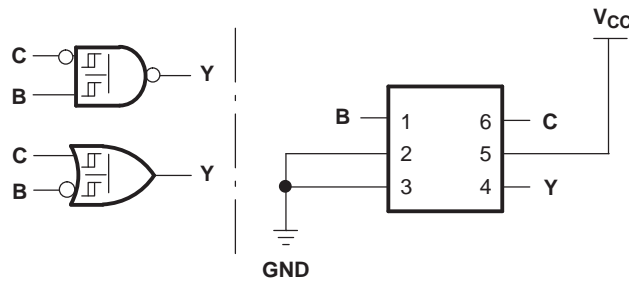


Figure 6. 2-Input NAND Gate With One Inverted Input
2-Input OR Gate With One Inverted Input

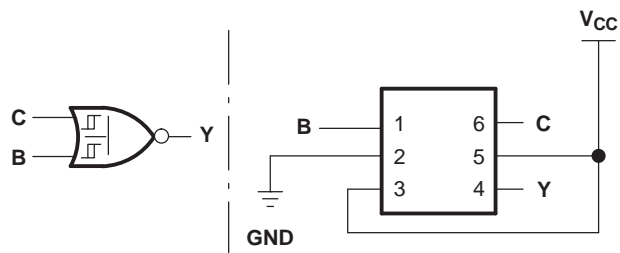


Figure 7. 2-Input NOR Gate

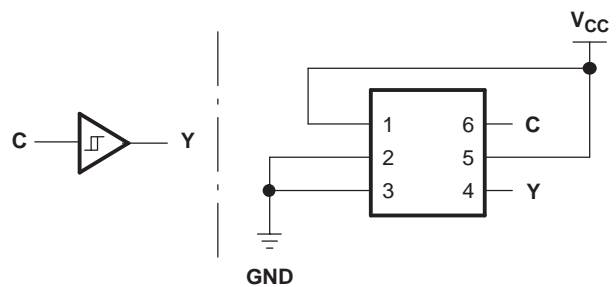


Figure 8. Noninverted Buffer

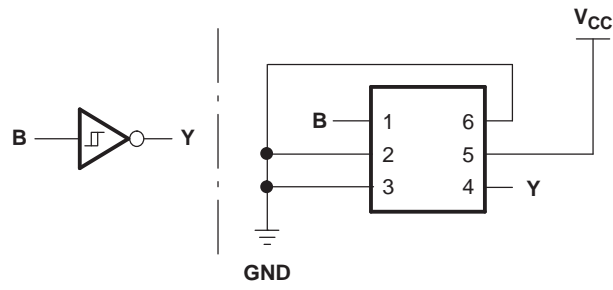


Figure 9. Inverter

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 20	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	165	°C/W
		DCK package	259	
		DRL package	142	
		DSF package	300	
		DRY package	234	
		YFP/YZP package	123	
T_{stg}	Storage temperature range	-65	.	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8$ V	-20	mA
		$V_{CC} = 1.1$ V	-1.1	
		$V_{CC} = 1.4$ V	-1.7	
		$V_{CC} = 1.65$	-1.9	
		$V_{CC} = 2.3$ V	-3.1	
		$V_{CC} = 3$ V	-4	
I_{OL}	Low-level output current	$V_{CC} = 0.8$ V	20	mA
		$V_{CC} = 1.1$ V	1.1	
		$V_{CC} = 1.4$ V	1.7	
		$V_{CC} = 1.65$ V	1.9	
		$V_{CC} = 2.3$ V	3.1	
		$V_{CC} = 3$ V	4	
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		0.8 V	0.3		0.6	0.3	0.6	V
		1.1 V	0.53		0.9	0.53	0.9	
		1.4 V	0.74		1.11	0.74	1.11	
		1.65 V	0.91		1.29	0.91	1.29	
		2.3 V	1.37		1.77	1.37	1.77	
		3 V	1.88		2.29	1.88	2.29	
V _{T–} Negative-going input threshold voltage		0.8 V	0.1		0.6	0.1	0.6	V
		1.1 V	0.26		0.65	0.26	0.65	
		1.4 V	0.39		0.75	0.39	0.75	
		1.65 V	0.47		0.84	0.47	0.84	
		2.3 V	0.69		1.04	0.69	1.04	
		3 V	0.88		1.24	0.88	1.24	
ΔV _T Hysteresis (V _{T+} – V _{T–})		0.8 V	0.07		0.5	0.07	0.5	V
		1.1 V	0.08		0.46	0.08	0.46	
		1.4 V	0.18		0.56	0.18	0.56	
		1.65 V	0.27		0.66	0.27	0.66	
		2.3 V	0.53		0.92	0.53	0.92	
		3 V	0.79		1.31	0.79	1.31	
V _{OH}	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1		V _{CC} – 0.1		V	
	I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}			
	I _{OH} = –1.7 mA	1.4 V	1.11		1.03			
	I _{OH} = –1.9 mA	1.65 V	1.32		1.3			
	I _{OH} = –2.3 mA	2.3 V	2.05		1.97			
	I _{OH} = –3.1 mA		1.9		1.85			
	I _{OH} = –2.7 mA	3 V	2.72		2.67			
	I _{OH} = –4 mA		2.6		2.55			
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V			0.1	0.1	V	
	I _{OL} = 1.1 mA	1.1 V			0.3 × V _{CC}	0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V			0.31	0.37		
	I _{OL} = 1.9 mA	1.65 V			0.31	0.35		
	I _{OL} = 2.3 mA	2.3 V			0.31	0.33		
	I _{OL} = 3.1 mA				0.44	0.45		
	I _{OL} = 2.7 mA	3 V			0.31	0.33		
	I _{OL} = 4 mA				0.44	0.45		
I _I	All inputs	V _I = GND to 3.6 V	0 V to 3.6 V		0.1	0.5	μA	
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.2	0.6	μA	
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V		0.2	0.6	μA	
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V		0.5	0.9	μA	
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V		40	50	μA	
C _i	V _I = V _{CC} or GND	0 V		1.5			pF	
		3.6 V		1.5				
C _O	V _O = GND	0 V		3			pF	

 (1) One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND.

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	22.2					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	2.7	9.1	13.6	2.2	17	
			$1.5\text{ V} \pm 0.1\text{ V}$	2	6.4	9.2	1.5	11.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.4	5.2	7.2	0.9	8.9	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.2	3.8	5.3	0.7	6.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	3.1	4.5	0.5	5.3	

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	25.4					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5.2	10.4	15.4	4.7	19	
			$1.5\text{ V} \pm 0.1\text{ V}$	4	7.4	10.5	3.5	12.6	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.1	6	8.3	2.6	10.2	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.7	4.5	6.1	2.2	7.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.5	3.7	5	2	6	

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	28.7					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.7	11.5	17	3.2	21.1	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.8	8.3	11.6	2.3	14	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.1	6.7	9.2	1.6	11.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.8	5	6.7	1.3	8.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.6	4.1	5.5	1.1	6.6	

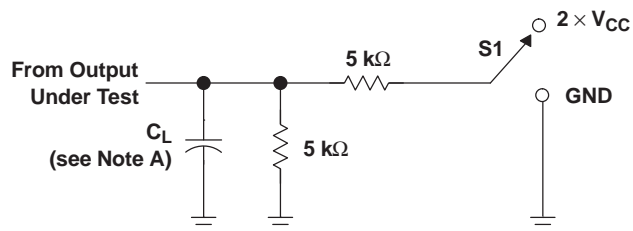
SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	39.7					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5.1	15.3	21.6	4.6	26.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.9	10.9	14.6	3.4	17.6	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.1	8.9	11.5	2.6	14.1	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.6	6.7	8.4	2.1	10.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.3	5.5	6.9	1.8	8.3	

OPERATING CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	4	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	4	
			$1.5\text{ V} \pm 0.1\text{ V}$	4	
			$1.8\text{ V} \pm 0.15\text{ V}$	4	
			$2.5\text{ V} \pm 0.2\text{ V}$	4.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	4.6	

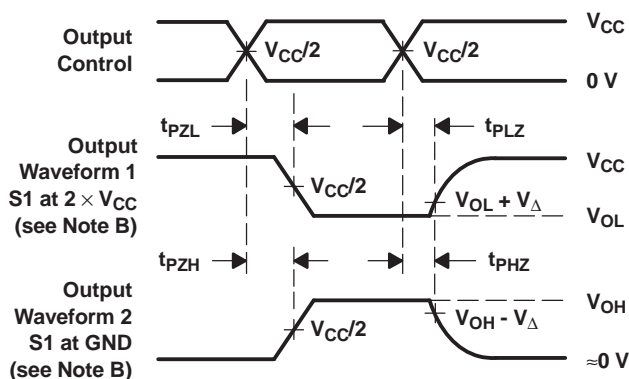
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 11. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G98DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H98R	Samples
SN74AUP1G98DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HRR	Samples
SN74AUP1G98DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HRR	Samples
SN74AUP1G98DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1KE, HR7, HRR)	Samples
SN74AUP1G98DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HR	Samples
SN74AUP1G98DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HR	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G98DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G98DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1G98DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1G98DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G98DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74AUP1G98DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G98DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G98DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1G98DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1G98DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1G98DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74AUP1G98DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74AUP1G98DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G98DSFR	SON	DSF	6	5000	210.0	185.0	35.0

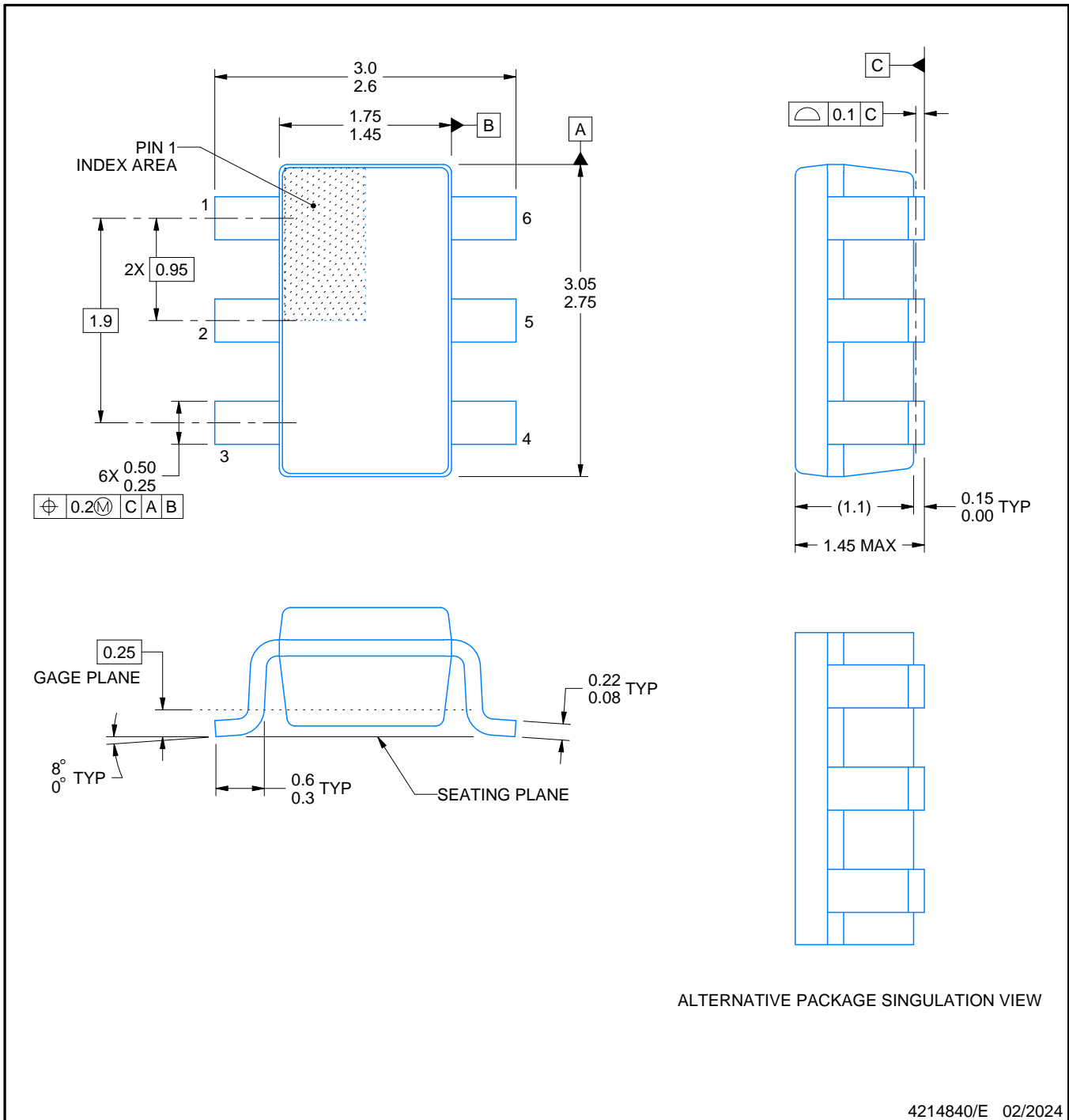


DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/E 02/2024

NOTES:

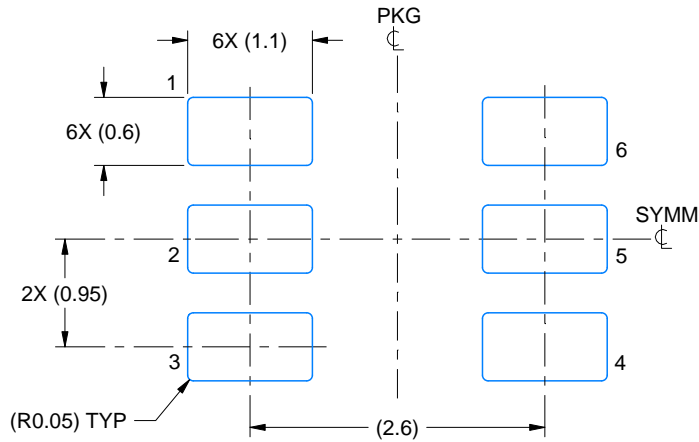
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

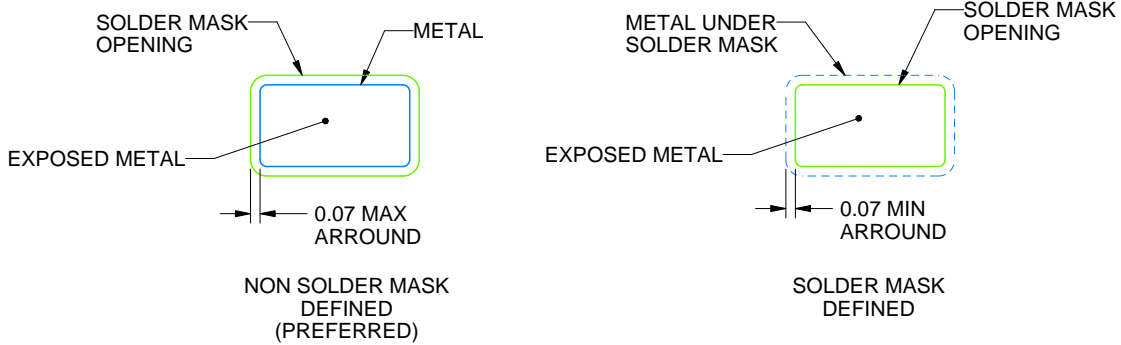
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

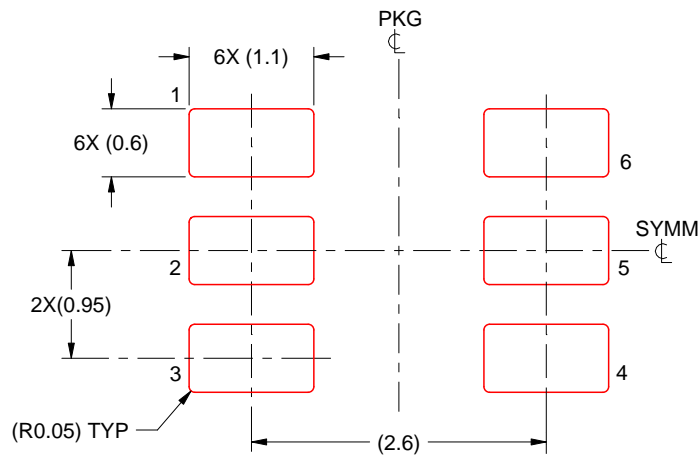
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G6)

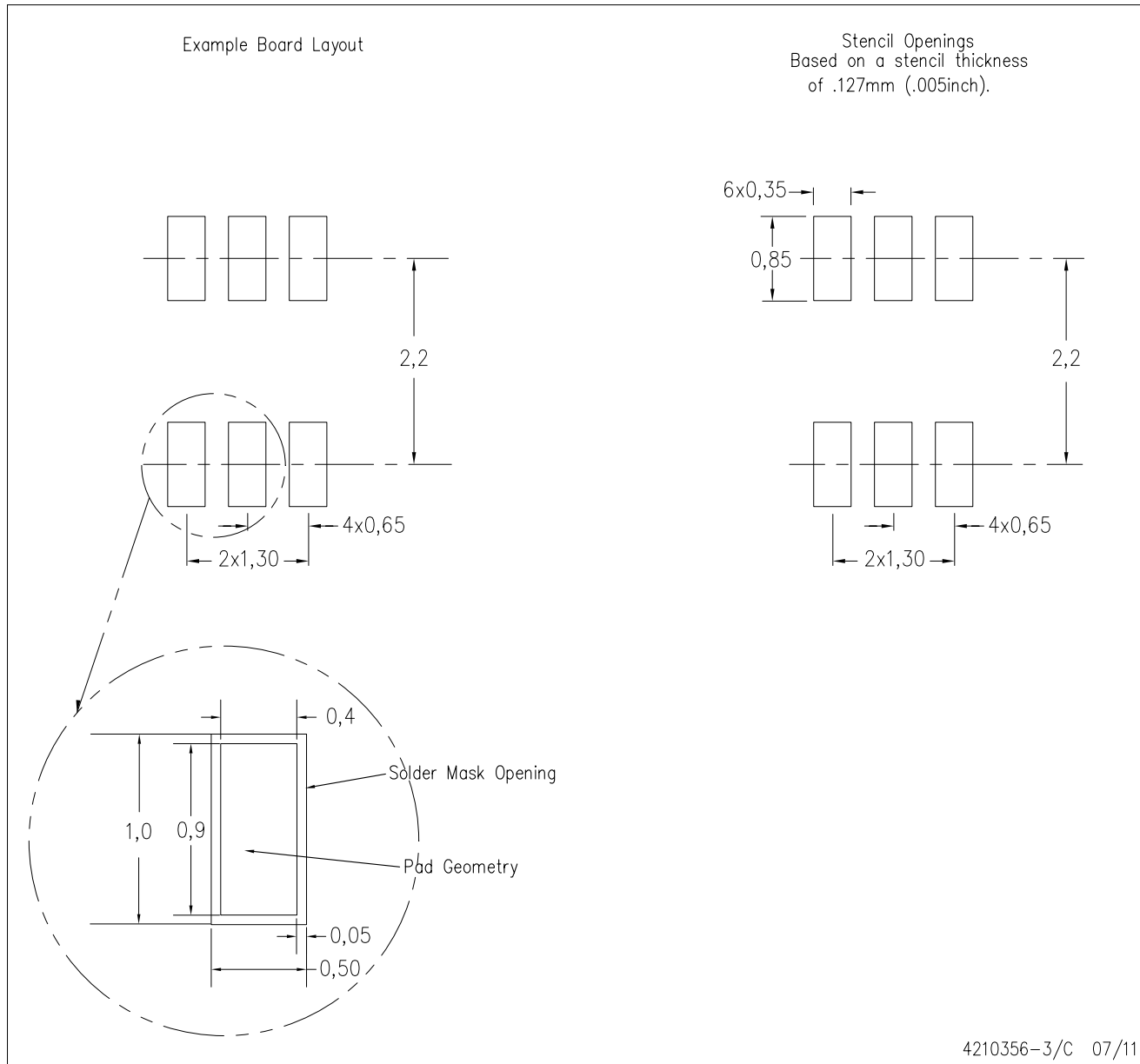
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



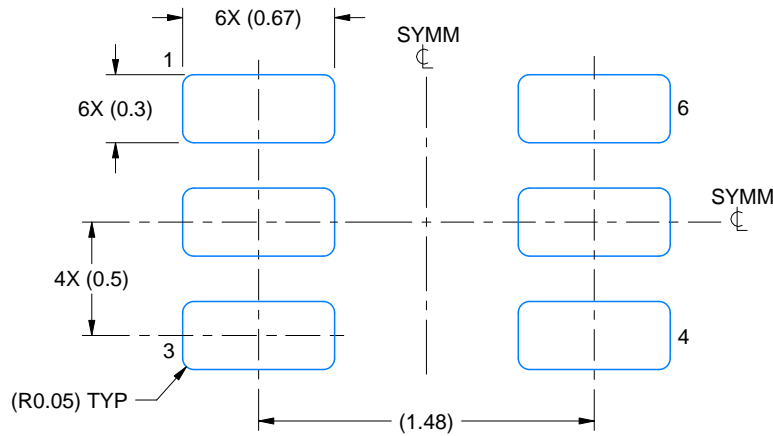
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

EXAMPLE BOARD LAYOUT

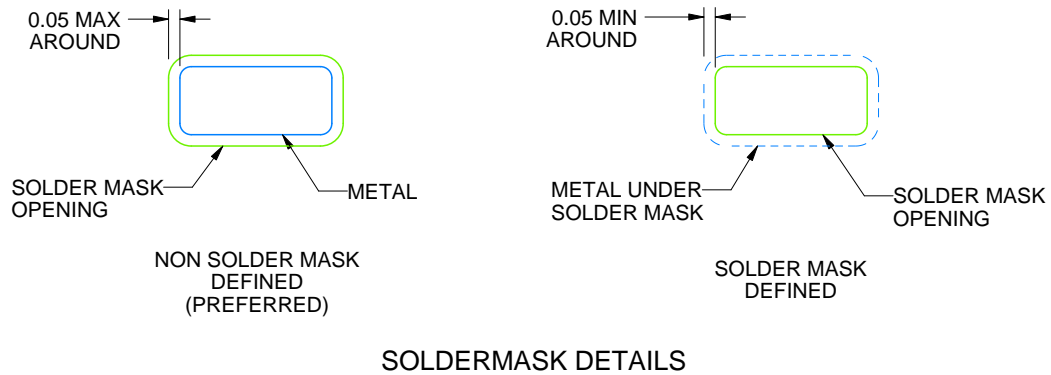
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

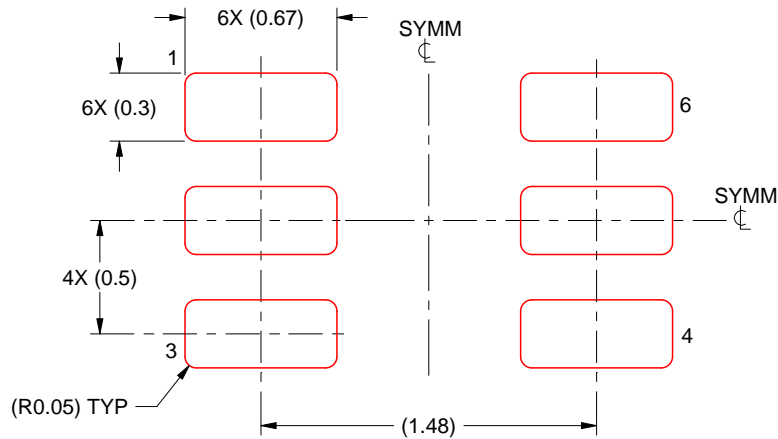
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

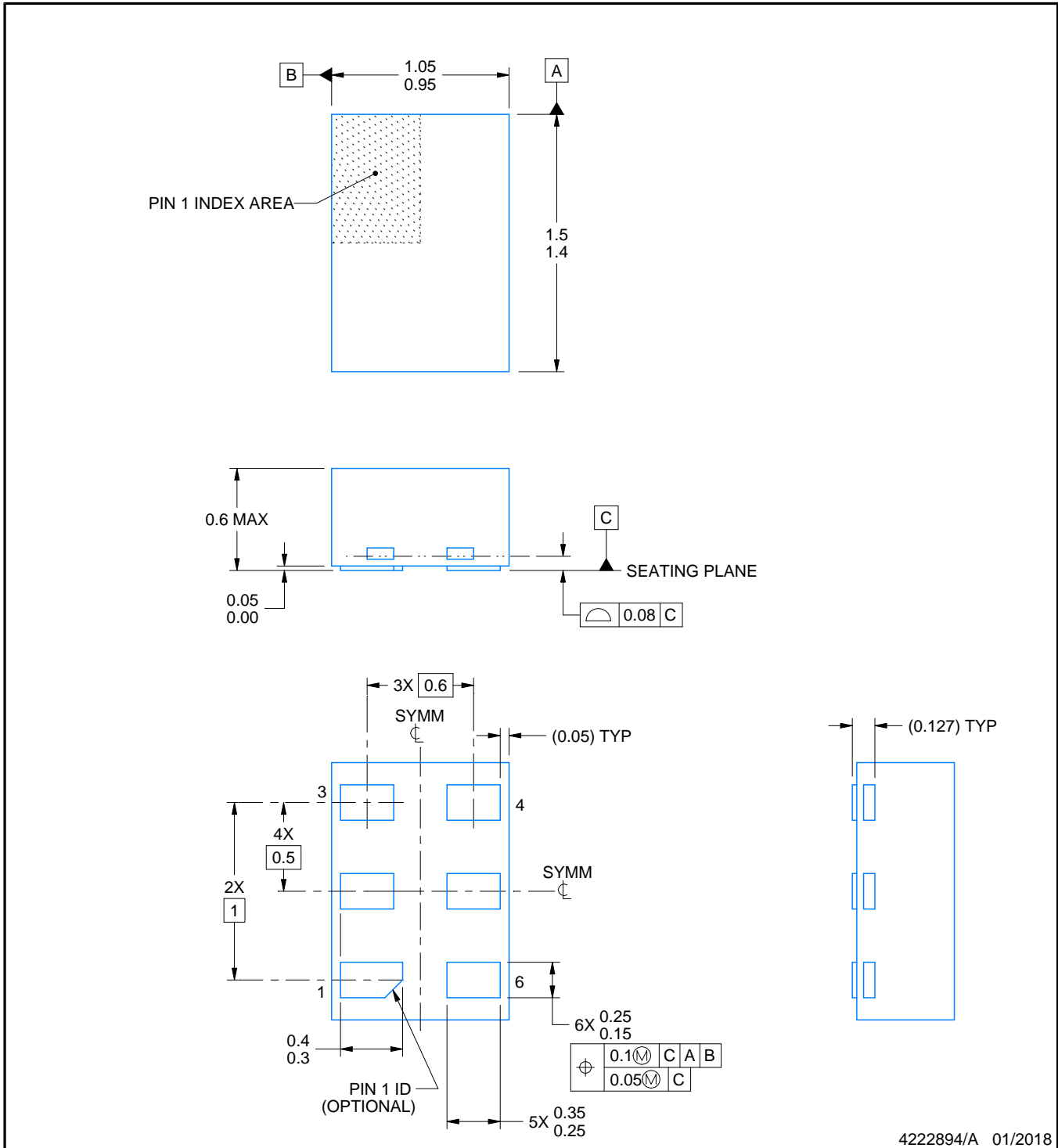
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

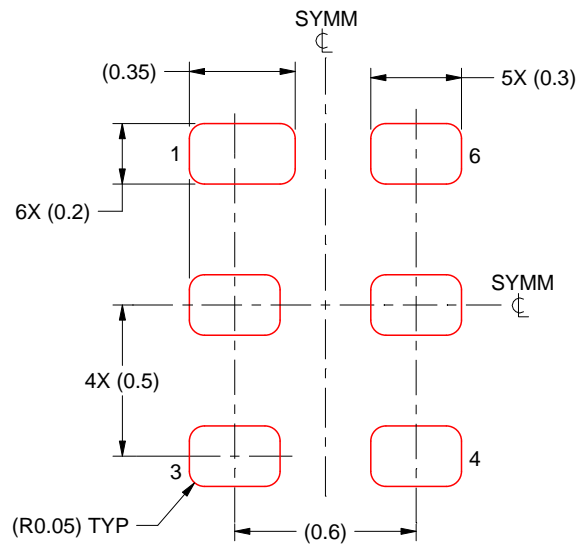
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

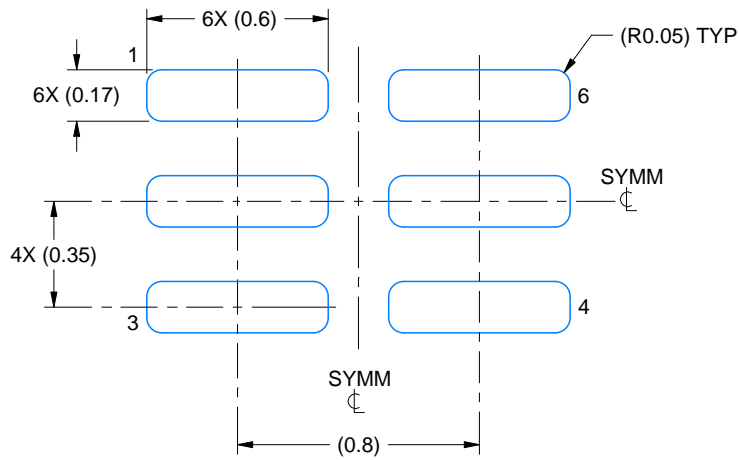
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated