Internal Frequency Compensation

High Slew Rate ... 18 V/us Typ

Low Total Harmonic Distortion

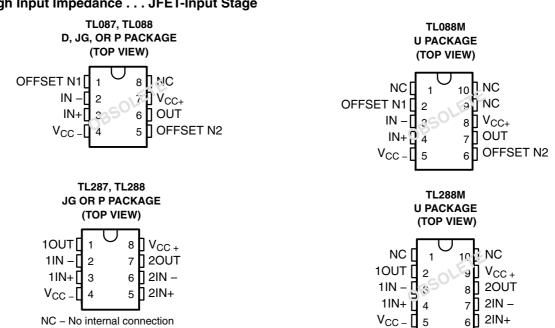
Latch-Up-Free Operation

0.003% Typ

The TL087, TL088, and TL287 are obsolete and are no longer supplied.

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- Low Input Offset Voltage . . . 0.5 mV Max
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- High Input Impedance . . . JFET-Input Stage



#### description/ordering information

These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset currents, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

The C-suffix devices are characterized for operation from 0°C to 70°C, and the I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

O	RDERING INFORMATION	1

T <sub>A</sub>	TYPE	V <sub>IO</sub> MAX AT 25°C	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	Dual	1 mV	PDIP (P)	Tube of 50	TL288CP	TL288CP

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

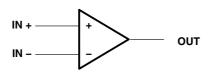
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



The TL087, TL088, and TL287 are obsolete and are no longer supplied.

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#### symbol (each amplifier)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, VCC+ (see Note 1)		18	18	18	V
Supply voltage, V <sub>CC</sub> – (see Note 1)		-18	-18	-18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)	±15	±15	±15	V	
Input current, I <sub>I</sub> (each Input)	±1	±1	±1	mA	
Output current, I <sub>O</sub> (each output)		±80	±80	±80	mA
Total V <sub>CC</sub> + terminal current		160	160	160	mA
Total V <sub>CC</sub> - terminal current		-160	- 160	- 160	mA
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation		S	See Dissipation R	ating Table	
Maximum junction temperature, T <sub>J</sub>			150	150	°C
Package thermal impedance, $\theta_{\text{JA}}$ (see Notes 5 and 6)	P package		85	85	°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	300	°C
Storage temperature range, T <sub>stg</sub>		-65 to 150	-65 to 150	-65 to 150	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.

2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

- 4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- 5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is PD =  $(T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- 6. The package thermal impedance is calculated in accordance with JESD 51-7.
- 7. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- 8. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is PD =  $(T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- 9. The package thermal impedance is calculated in accordance with JESD 51-7.

#### DISSIPATION RATING TABLE

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A =</sub> 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING						
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW						
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW						



# The TL087, TL088, and TL287 are obsolete and are no longer supplied.

# TL087, TL088, TL287, TL288 JFET-INPUT OPERATIONAL AMPLIFIERS

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#### recommended operating conditions

			C-SU	FFIX	I-SUI	FIX	M-SU	FFIX	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
$V_{CC}$	Supply voltage		±5	±5	±5	±5	±5	±15	V
		$V_{CC\pm} = \pm 5 V$	-1	4	-1	4	-1	4	
V <sub>IC</sub>	Common-mode input voltage	$V_{CC\pm} = \pm 15 \text{ V}$	- 11	11	-11	11	-11	11	V
	land to the sec	$V_{CC\pm} = \pm 5 V$	-1	4	-1	4	-1	4	
VI	Input voltage	$V_{CC\pm} = \pm 15 \text{ V}$	- 11	11	-11	11	-11	11	V
T <sub>A</sub>	Operating free-air temperature		0	70	-40	85	-55	125	°C

### operating characteristics $V_{CC}$ = $\pm 15$ V, $T_{A}$ = $25^{\circ}C$

	PARAMETER	TEST CO	TEST CONDITIONS			88M	TL087I, TL087C TL088I, TL088C			UNIT
			MIN	TYP	MAX	MIN	TYP	МАХ		
SR	Slew rate at unity gain	V <sub>I</sub> = 10 V, C <sub>L</sub> = 100 pF,	$R_L = 2 k\Omega,$ $A_{VD} = 1$		18		8	18		V/µs
t <sub>r</sub>	Rise time	V <sub>I</sub> = 20 mV,	$R_L = 2 k\Omega$ ,		55			55		ns
	Overshoot factor	C <sub>L</sub> = 100 pF,	$A_{VD} = 1$		25			25		%
Vn	Equivalent input noise voltage	R <sub>S</sub> = 100 Ω,	f = 1 kHz		19			19		nV/√Hz



#### electrical characteristics, V<sub>CC $\pm$ </sub> = $\pm$ 15 V

	PARAMETER	TEST C		TL088M TL288M			TL087I TL088I TL287I TL288I			TL087C TL088C TL287C TL288C				
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
		$R_S = 50 \Omega$ ,	TL087, TL287					0.1	0.5		0.1	0.5		
		$V_O = 0$ $T_A = 25^{\circ}C$	TL088, TL288		0.1	3		0.1	1		0.1	1	mV	
V <sub>IO</sub>	Input offset voltage	$R_{S} = 50 \Omega$ ,	TL087, TL287						2			1.5	mv	
	$V_O = 0,$ $T_A = $ full range	TL088, TL288			6			3			2.5			
<sup>α</sup> VIO	Temperature coefficient of input offset voltage	$R_{S} = 50 \Omega,$	$T_A = 25^{\circ}C$ to MAX		10			8			8		μV/°C	
ha	Input offset current	$T_A = 25^{\circ}C$			5			5	100		5	100	pА	
IIO	-	$T_A = $ full range				25			3			2	nA	
I <sub>IB</sub>	Input bias current <sup>‡</sup>	$T_A = 25^{\circ}C$			30			30	200		30	200	pА	
		$T_A = $ full range				100			20			7	nA	
	Common-mode input		(V <sub>CC</sub> _) ·	+ 4		(V <sub>CC</sub> _)	+4		(V <sub>CC</sub> _)	+4				
V <sub>ICR</sub>	voltage range	$T_A = 25^{\circ}C$		t (V <sub>CC+</sub> )			(V <sub>CC+</sub> )	to 4		to (V <sub>CC+</sub> )	-4		V	
	$T_A = 25^{\circ}C,$		$R_L = 10 \ k\Omega$	24	27		24	27		24	27			
V <sub>O(PP)</sub>	Maximum-peak-to-peak output voltage swing	T <sub>A</sub> = full range	$R_L \ge 10 \ k\Omega$	24			24			24			V	
	output voltage owing	_	$R_L \ge 2 k\Omega$	20			20			20				
Δ	Large-signal differential	$\begin{aligned} R_L &\geq 2 \ k\Omega, \\ T_A &= 25^\circ C \end{aligned}$	$V_{O} = \pm 10 V$ ,	50	105		50	105		50	105		V/mV	
A <sub>VD</sub>	voltage amplification	$R_L \ge 2 k\Omega$ , $T_A = full range$	$V_{O} = \pm 10 V$ ,	25			25			25			v/IIIv	
B <sub>1</sub>	Unity-gain bandwidth	$T_A = 25^{\circ}C$			3			3			3		MHz	
r <sub>i</sub>	Input resistance	$T_A = 25^{\circ}C$			10 <sup>12</sup>			10 <sup>12</sup>			10 <sup>12</sup>		Ω	
CMRR	Common-mode rejection ratio	$\label{eq:R_S} \begin{split} R_{S} &= 50\;\Omega,\\ V_{IC} &= V_{ICR}\;min, \end{split}$	V <sub>O</sub> = 0 V, T <sub>A</sub> = 25°C	80	93		80	93		80	93		dB	
k <sub>SVR</sub>	Supply voltage rejection ratio ( $\Delta V_{CC} \pm \Delta V_{IO}$ )	$\begin{aligned} R_{S} &= 50 \ \Omega, \\ V_{CC\pm} &= \pm 9 \ V \ to \\ T_{A} &= 25^\circC \end{aligned}$	V <sub>O</sub> = 0 V,	80	99		80	99		80	99		dB	
I <sub>CC</sub>	Supply current (per amplifier)	No load, T <sub>A</sub> = 25°C	V <sub>O</sub> = 0 V,		26	2.8		2.6	2.8		2.6	2.8	mA	

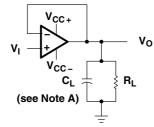
<sup>+</sup> All characteristics are measured under open–loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T<sub>A</sub> is –55°C to 125°C for TL\_88M; -40°C to 85°C for TL\_8\_I; and 0°C to 70°C for TL\_8\_C.

<sup>‡</sup> Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

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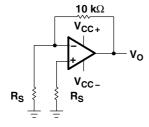
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#### PARAMETER MEASUREMENT INFORMATION

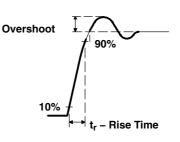


NOTE A: CL includes fixture capacitance.

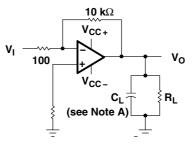
#### Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit







#### Figure 2. Rise Time and Overshoot Waveform



NOTE A: C<sub>L</sub> includes fixture capacitance.

#### Figure 4. Unity-Gain Brandwidth and Phase Margin Test Circuit

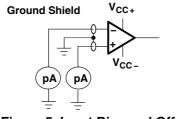


Figure 5. Input Bias and Offset Current Test Circuit



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#### typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

#### input bias and offset current

At the picoamp bias current level typical of these JFET operational amplifiers, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device then is inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements then are subtracted algebraically to determine the bias current of the device.



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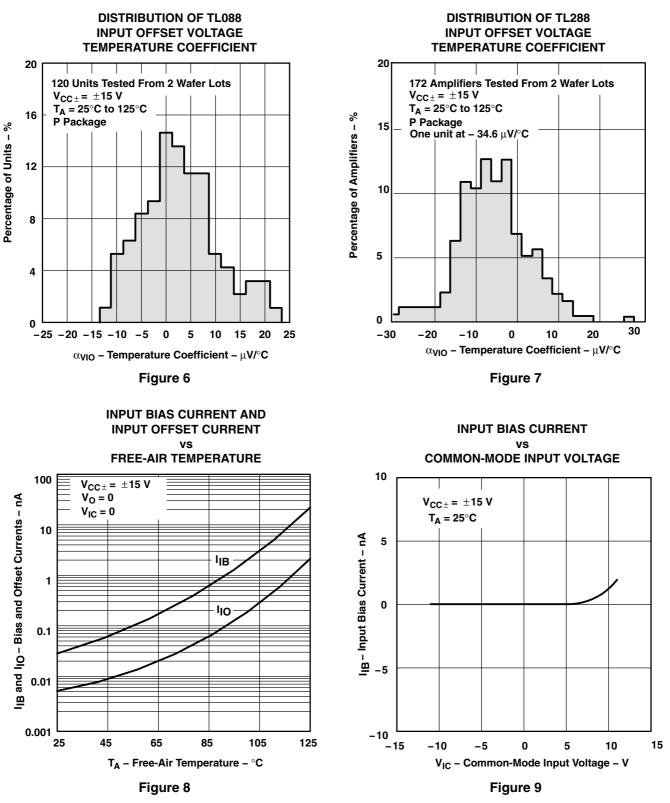
#### **TYPICAL CHARACTERISTICS**

# table of graphs

			FIGURE
<sup>α</sup> vio	Temperature coefficient of input offset voltage	Distribution	6, 7
I <sub>IO</sub>	Input offset current	vs Temperature	8
I <sub>IB</sub>	Input bias current	vs V <sub>IC</sub> vs Temperature	9 8
VI	Common-mode input voltage range limits	vs V <sub>CC</sub> vs Temperature	10 11
V <sub>ID</sub>	Differential input voltage	vs Output voltage	12
V <sub>OM</sub>	Maximum peak output voltage swing	vs V <sub>CC</sub> vs Output current vs Frequency vs Temperature	13 17 14, 15, 16 18
A <sub>VD</sub>	Differential voltage amplification	vs R <sub>L</sub> vs Frequency vs Temperature	19 20 21
z <sub>o</sub>	Output impedance	vs Frequency	24
CMRR	Common-mode rejection ratio	vs Frequency vs Temperature	22 23
k <sub>SVR</sub>	Supply-voltage rejection ratio	vs Temperature	25
I <sub>OS</sub>	Short-circuit output current	vs V <sub>CC</sub> vs Time vs Temperature	26 27 28
I <sub>CC</sub>	Supply current	vs V <sub>CC</sub> vs Temperature	29 30
SR	Slew rate	vs R <sub>L</sub> vs Temperature	31 32
	Overshoot factor	vs C <sub>L</sub>	33
Vn	Equivalent input noise voltage	vs Frequency	34
THD	Total harmonic distortion	vs Frequency	35
B <sub>1</sub>	Unity-gain bandwidth	vs V <sub>CC</sub> vs Temperature	36 37
φ <sub>m</sub>	Phase margin	vs V <sub>CC</sub> vs C∟ vs Temperature	38 39 40
	Phase shift	vs Frequency	20
	Pulse response	Small-signal Large-signal	41 42



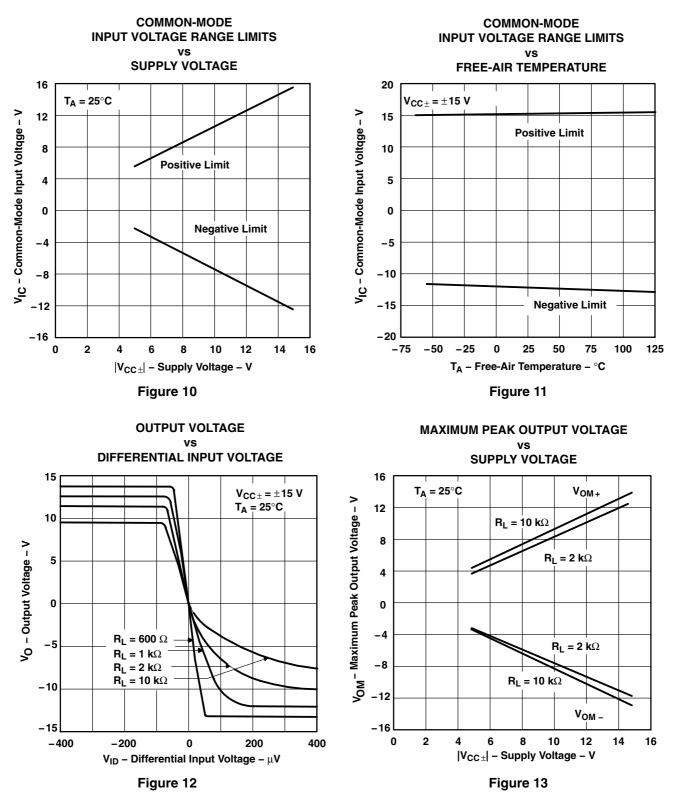
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 



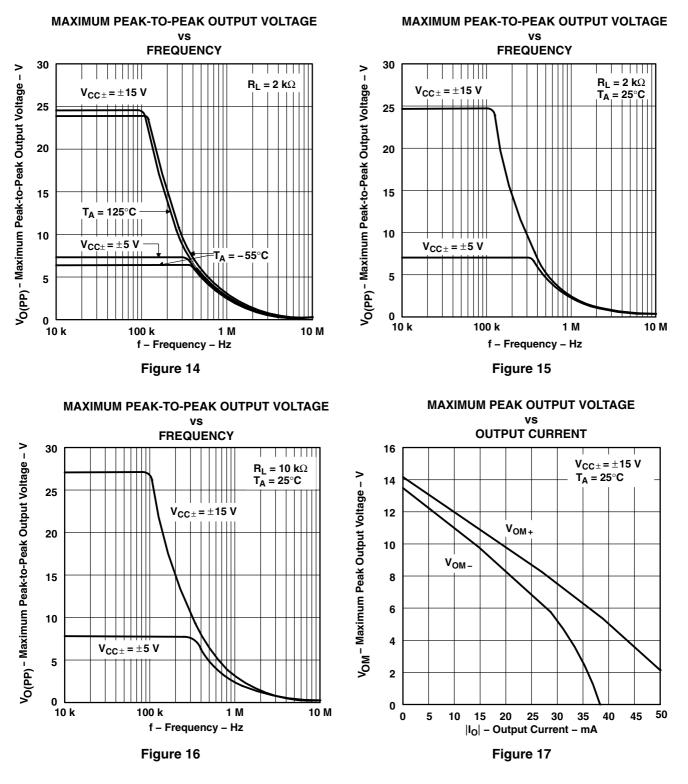
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 



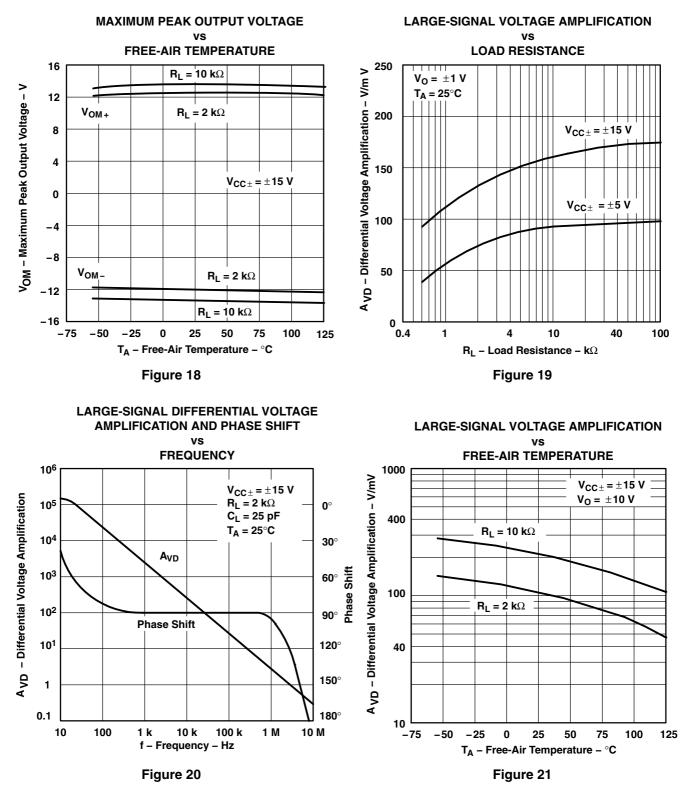
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 



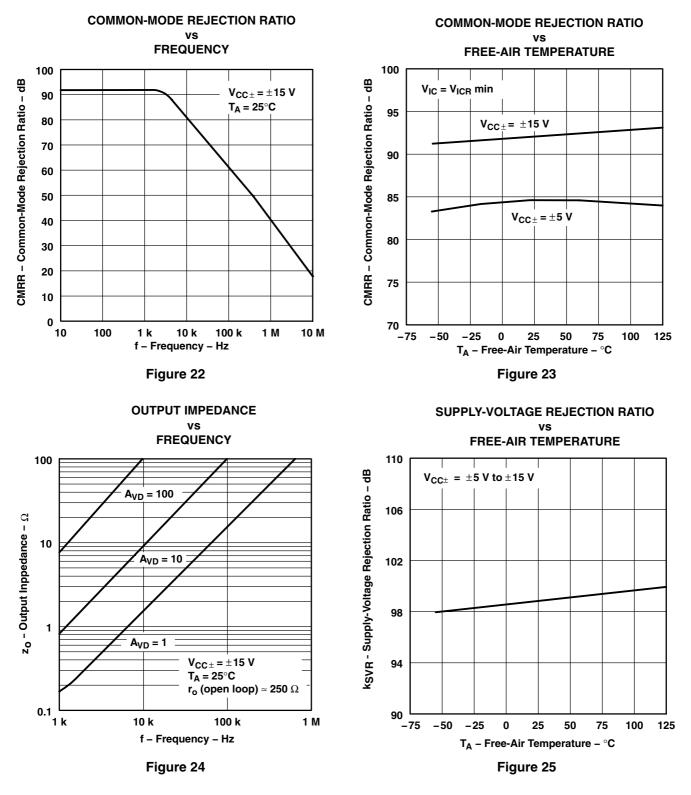
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 



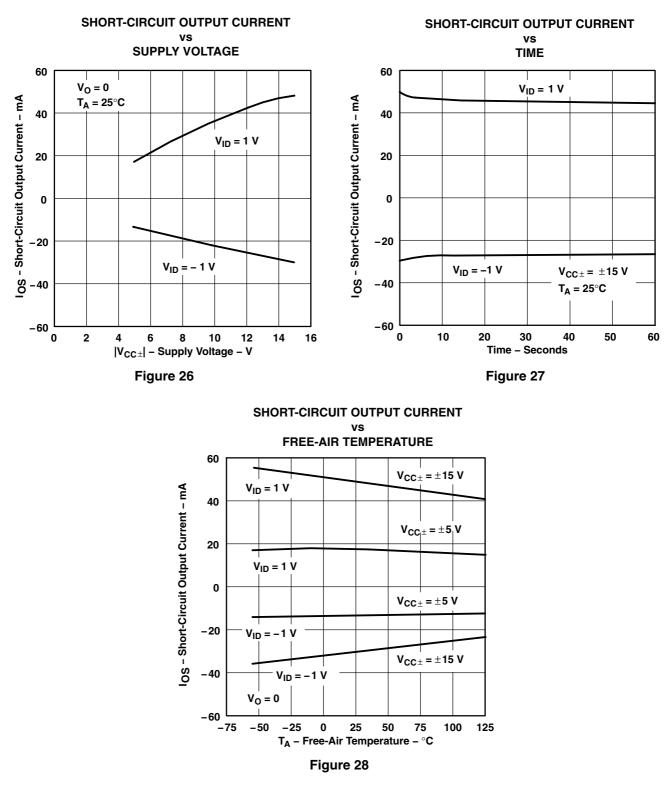
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 



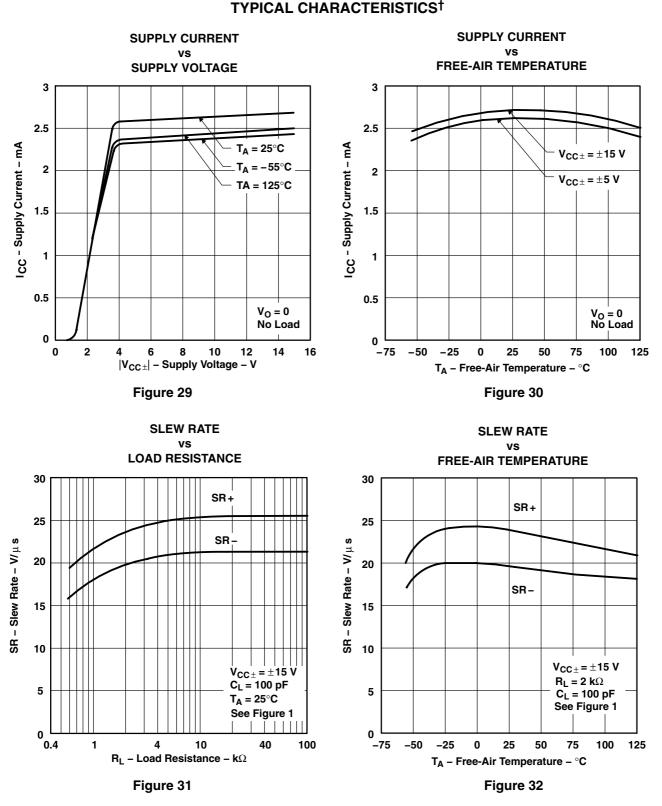
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 

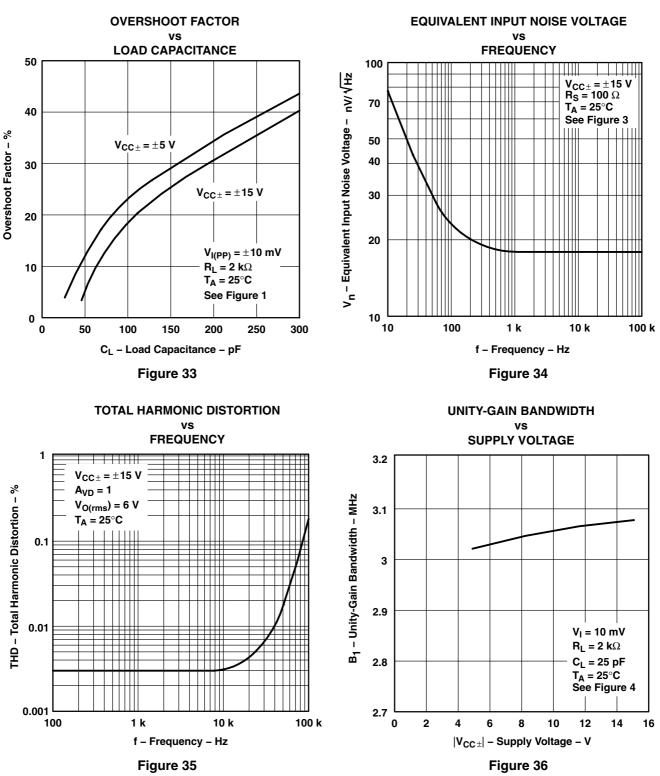


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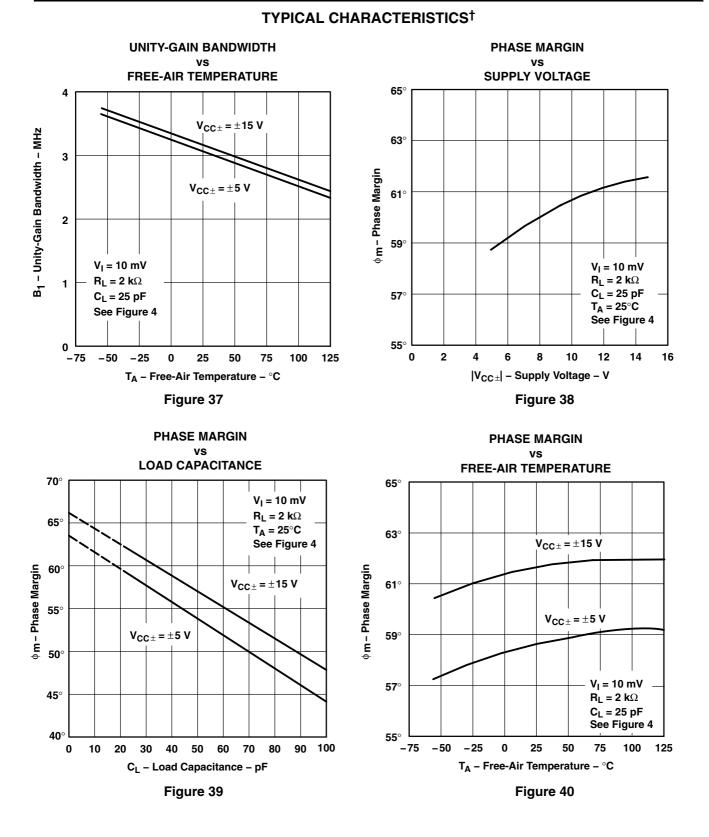
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**TYPICAL CHARACTERISTICS<sup>†</sup>** 

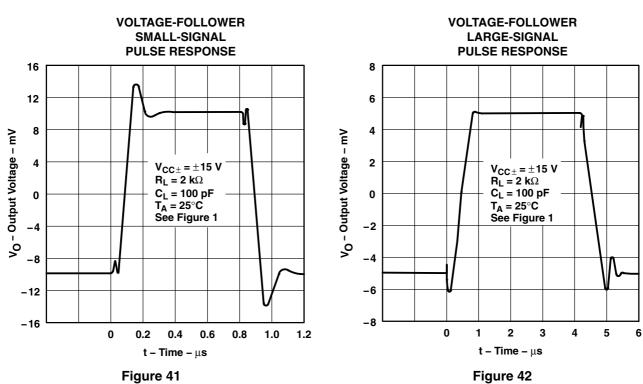


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#### **TYPICAL CHARACTERISTICS**

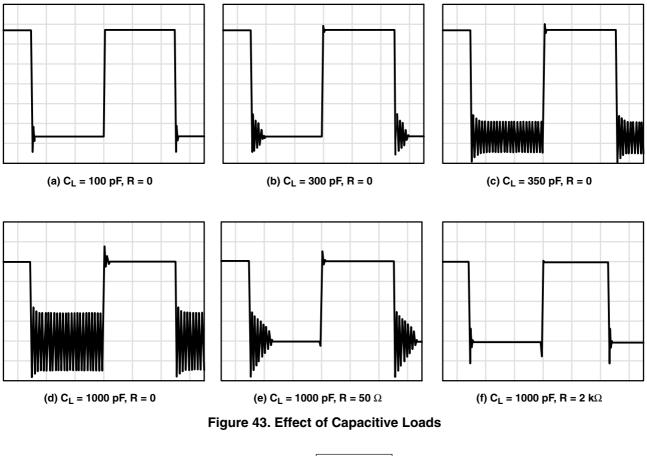


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### **TYPICAL APPLICATION DATA**

#### output characteristics

All operating characteristics are specified with 100-pF load capacitance. These amplifiers will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF, and larger, may be driven if enough resistance is added in series with the output (see Figure 43).



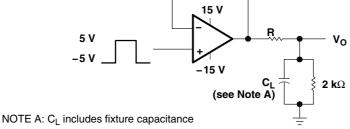


Figure 44. Test Circuit for Output Characteristics

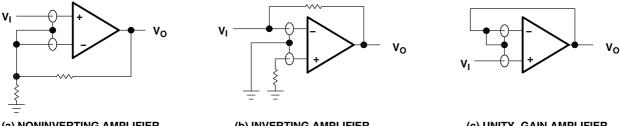


#### TYPICAL APPLICATION DATA

#### input characteristics

These amplifiers are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, these amplifiers are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets easily can exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 45). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER

(b) INVERTING AMPLIFIER

Figure 45. Use of Guard Rings



#### noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of these amplifiers result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k $\Omega$ .





#### PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL288CP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL288CP	Samples
TL288CPE4	ACTIVE	PDIP	Р	8	50	TBD	Call TI	Call TI	0 to 70		Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE OPTION ADDENDUM

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### TEXAS INSTRUMENTS

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### TUBE



### - B - Alignment groove width

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
TL288CP	Р	PDIP	8	50	506	13.97	11230	4.32

P(R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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