TLC3702-Q1 Dual Micropower LinCMOS™ Voltage Comparators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Devce CDM ESD Classification Level C4B
- Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, I_O = ± 8 mA
- Very Low Power…100 µW Typical at 5 V
- Fast Response Time… t_{PLH} = 2.7 µs Typical With 5-mV Overdrive
- Single-Supply Operation…3 V to 16 V
- On-Chip ESD Protection

2 Applications

- Transmission Control Unit
- Braking
- Engine Control

3 Description

The TLC3702-Q1 consists of two independent micropower voltage comparators. Compared to similar devices, the TLC3702-Q1 uses one-twentieth of the power for similar response times. This allows the device to react quickly to fast changing signals while extending the battery life.

The push-pull CMOS output stage drives capacitive loads directly without a power consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation but also saves board space and component cost. Additionally, the output stage is fully compatible with all TTL and CMOS logic requirements.

Texas Instruments' LinCMOS™ process offers superior analog performance versus standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance and low bias currents, the LinCMOS process offers extremely stable input/offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

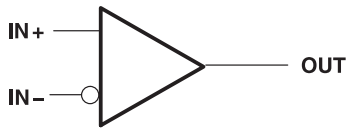
The TLC3702-Q1 has a wide supply range from 3 V to 16 V, allowing design flexibility. The voltage range also allows the device to handle start-stop applications and be connected directly to a standard 12-V battery. All of these features make the TLC3702-Q1 suitable for HEV/EV and powertrain system such as transmission control unit (TCU) and engine control.

Device Information[1]

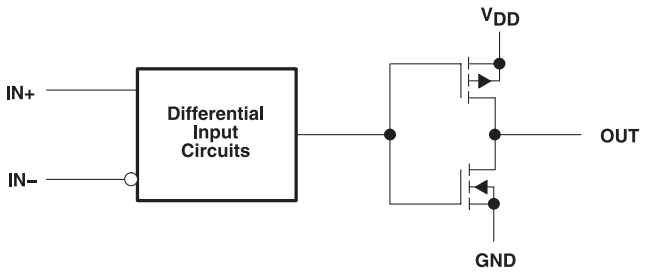
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC3702-Q1	SOIC (8)	4.90 mm × 3.91 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Symbol (Each Comparator)



Functional Block Diagram (Each Comparator)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2012) to Revision F **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table; see POA at the end of the datasheet. ... 1
- Changed the *Description* section ... 1
- Changed Equation 2 in *Detailed Design Procedure* from "R2 + R1//R" to "R1 + R2//R" ... 17
- Changed "Output is high" to "Output is low" ... 17
- Deleted *Enhanced Supply Supervisor* schematics and *Pulse-Width-Modulated Motor Speed Controller* schematic ... 17
- Added missing resistors to *Two-Phase Non-Overlapping Clock Generator* schematic and changed in NOTES A: from "1.85" to "2 × 1.71" ... 18
- Deleted the *Micropower Switching Regulator* image ... 19

Changes from Revision D (February 2012) to Revision E **Page**

- Changed part numbers from TLC3702 to TLC3702-Q1 ... 1
- Changed units for I_{IB} from dB to pA and nA ... 4

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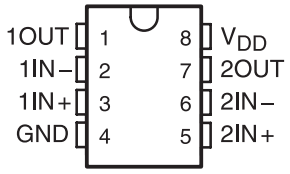
5 Pin Configuration and Functions

D or PW Package
8-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	3	I	Non-Inverting input channel 1
1IN-	2	I	Inverting input channel 1
2IN+	5	I	Non-Inverting input channel 2
2IN-	6	I	Inverting input channel 2
1OUT	1	O	Output, Channel 1
1OUT	7	O	Output, Channel 2
GND	4	-	Negative (lowest) power supply
VDD	8	-	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_{DD} (2)		−0.3	18	V
Differential input voltage, V_{ID} (3)			±18	V
Input voltage, V_I		−0.3	V_{DD}	V
Output voltage, V_O		−0.3	V_{DD}	V
Input current, I_I			±5	mA
Output current, I_O (each output)			±20	mA
Total supply current into V_{DD}			40	mA
Total current out of GND			40	mA
Continuous total power dissipation		See *Thermal Information*		
Operating free-air temperature, T_A		−40	125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D package		260	°C
	PW package		260	
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Differential voltages are at IN+ with respect to IN−.

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6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except 1, 4, 5, and 8	±500	
			Pins 1, 4, 5, and 8	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4	5	16	V
V_{IC}	Common-mode input voltage	0		V_{DD} - 1.5	V
I_{OH}	High-level output current			–20	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLC3702-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.7	181.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	49.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.8	110.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.3	108.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at specified operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted). See (1)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min, See (2)	25°C		1.2	5	mV
			−40°C to +125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to +125°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			−40°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			−40°C		82		

(1) All characteristics are measured with zero common-mode voltage unless otherwise noted.
(2) The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

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Electrical Characteristics (continued)

at specified operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted). See (1)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5			V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		19	40	µA
			−40°C to +125°C			90	

6.6 Switching Characteristics

at recommended operating conditions, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(PLH)}$	Propagation response time, low-to-high-level output (1)	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4 V step at IN+			1.1		µs
$t_{(PHL)}$	Propagation response time, high-to-low-level output (1)	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

(1) Simultaneous switching of inputs causes degradation in output response.

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6.7 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	Figure 1
I_{IB}	Input bias current	vs Free-air temperature	Figure 2
CMRR	Common-mode rejection ratio	vs Free-air temperature	Figure 3
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	Figure 4
V_{OH}	High-level output current	vs Free-air temperature	Figure 5
		vs High-level output current	Figure 6
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 7
		vs Free-air temperature	Figure 8
t_t	Transition time	vs Load capacitance	Figure 9
	Supply current response	vs Time	Figure 10
	Low-to-high-level output response	Low-to-high level output propagation delay time	Figure 11
	High-to-low level output response	High-to-low level output propagation delay time	Figure 12
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	Figure 13
t_{PHL}	High-to-low level output propagation delay time	vs Supply voltage	Figure 14
I_{DD}	Supply current	vs Frequency	Figure 15
		vs Supply voltage	Figure 16
		vs Free-air temperature	Figure 17

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

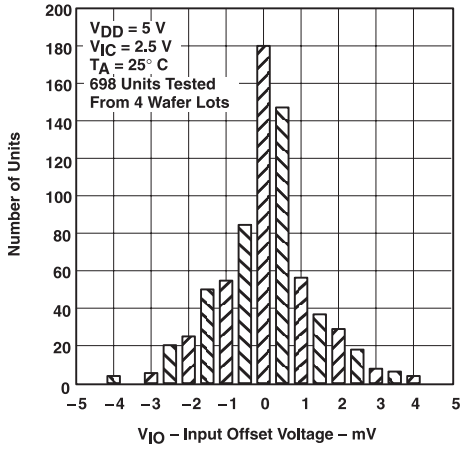

Figure 1. Distribution of Input Offset Voltage

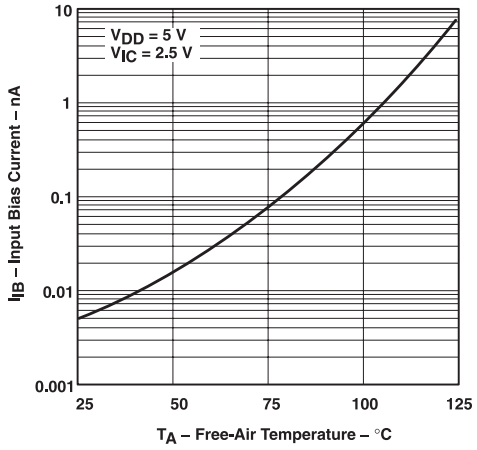

Figure 2. Input Bias Current vs Free-Air Temperature

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

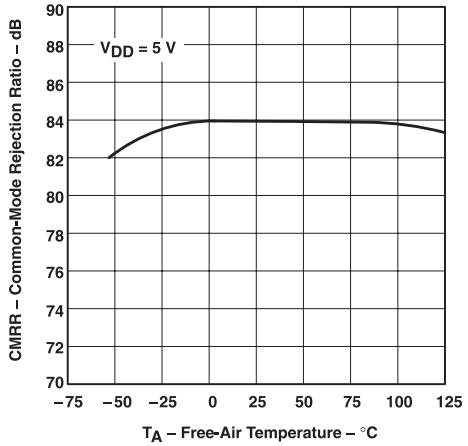

Figure 3. Common-Mode Rejection Ratio vs Free-Air Temperature

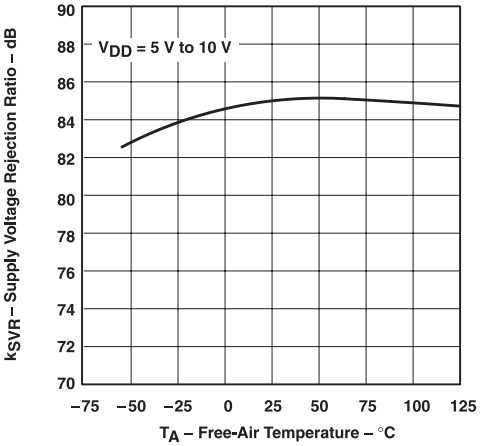

Figure 4. Supply-Voltage Rejection Ratio vs Free-Air Temperature

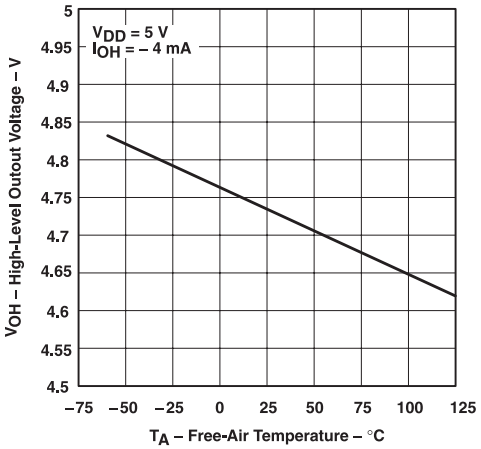

Figure 5. High-Level Output Current vs Free-Air Temperature

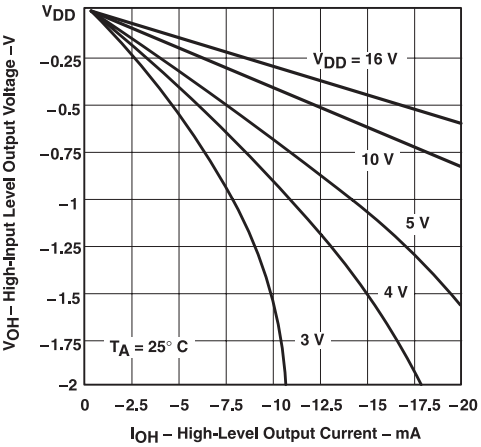

Figure 6. High-Level Output Current vs High-Level Output Current

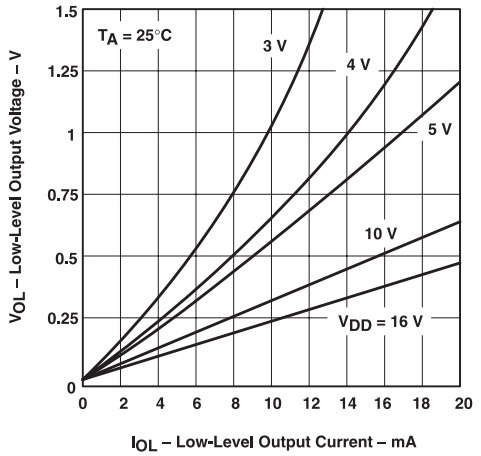

Figure 7. Low-Level Output Voltage vs Low-Level Output Current

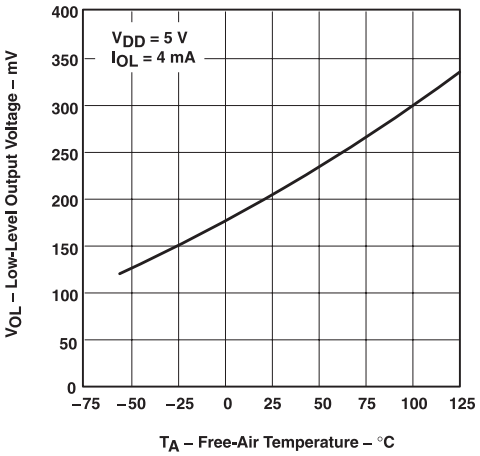

Figure 8. Low-Level Output Voltage vs Free-Air Temperature

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

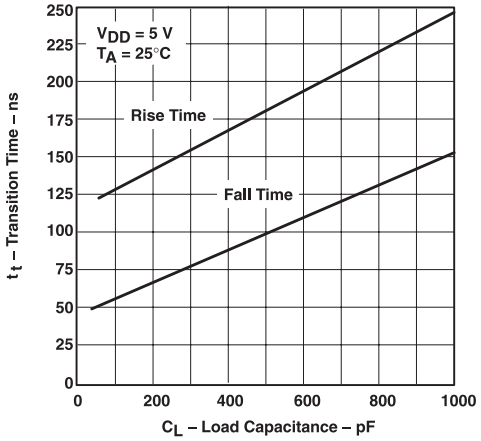

Figure 9. Output Transition Time vs Load Capacitance

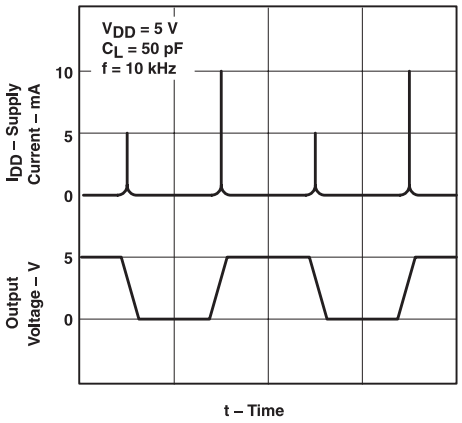

Figure 10. Supply Current Response to an Output Voltage Transition

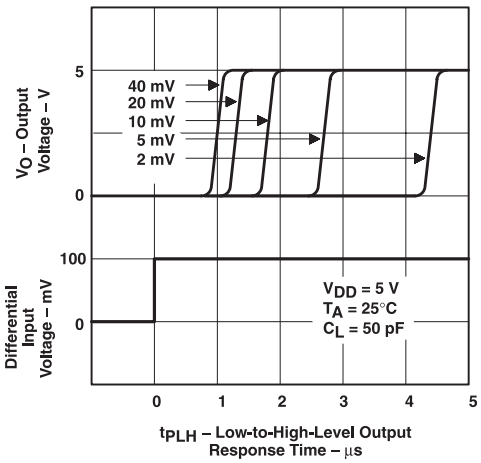

Figure 11. Low-to-High-Level Output Response for Various Input Overdrives

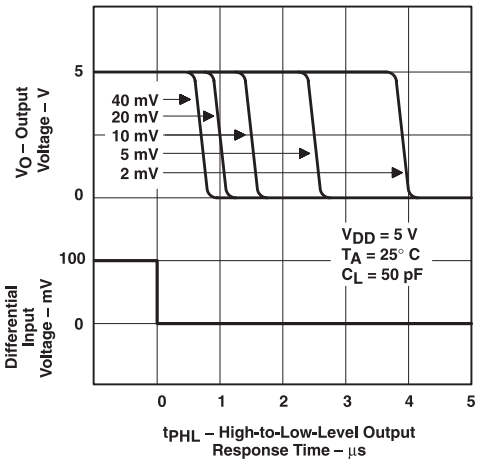

Figure 12. High-to-Low-Level Output Response for Various Input Overdrives

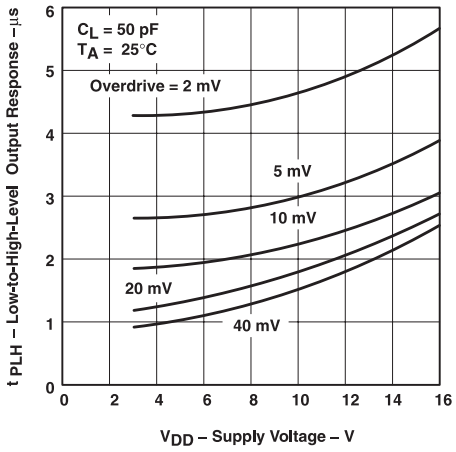

Figure 13. Low-to-High-Level Output Response Time vs Supply Voltage

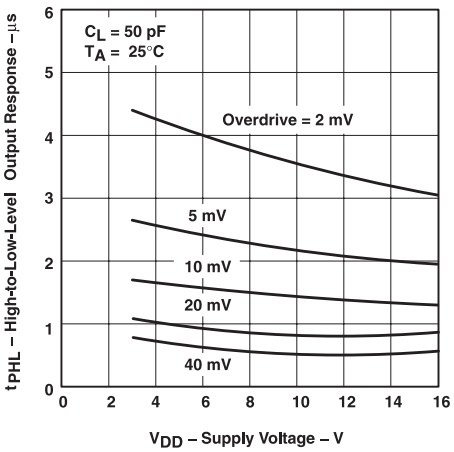

Figure 14. High-to-Low-Level Output Response Time vs Supply Voltage

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Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

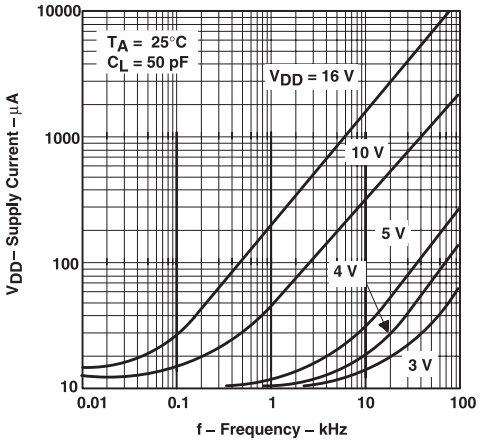


Figure 15. Average Supply Current (per Comparator) vs Frequency

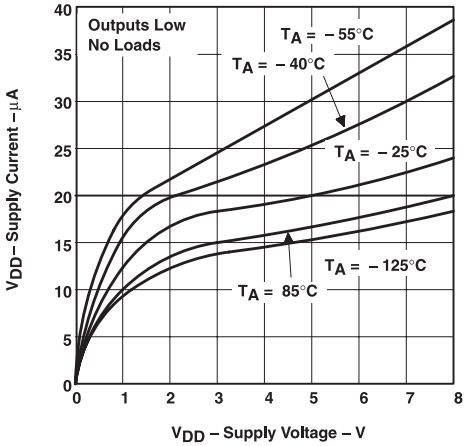


Figure 16. Supply Current vs Supply Voltage

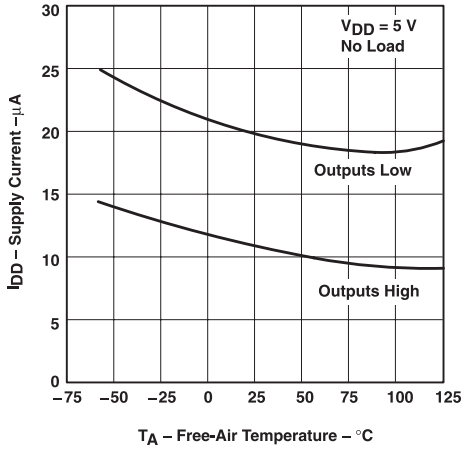


Figure 17. Supply Current vs Free-Air Temperature

7 Parameter Measurement Information

CAUTION

The TLC3702-Q1 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device.

Conventional operational amplifier and comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Because the servo-loop method of testing cannot be used, the following alternatives are offered for measuring parameters such as input offset voltage, common-mode rejection, and so forth.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 18(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

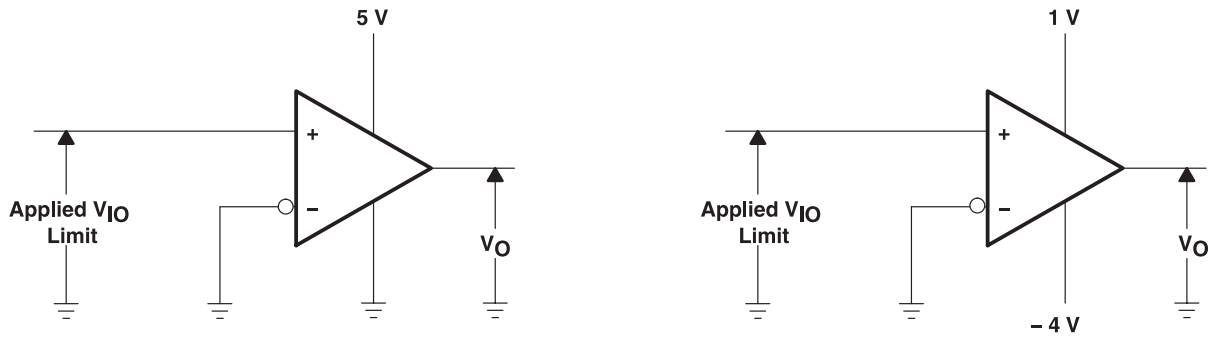
A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed to provide greater accuracy, as shown in Figure 18(b) for the V_{ICR} test. This slewing is done instead of changing the input voltages.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 19 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R8 and R9 provide an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, TI recommends that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 18. Method for Verifying That Input Offset Voltage Is Within Specified Limits

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Parameter Measurement Information (continued)

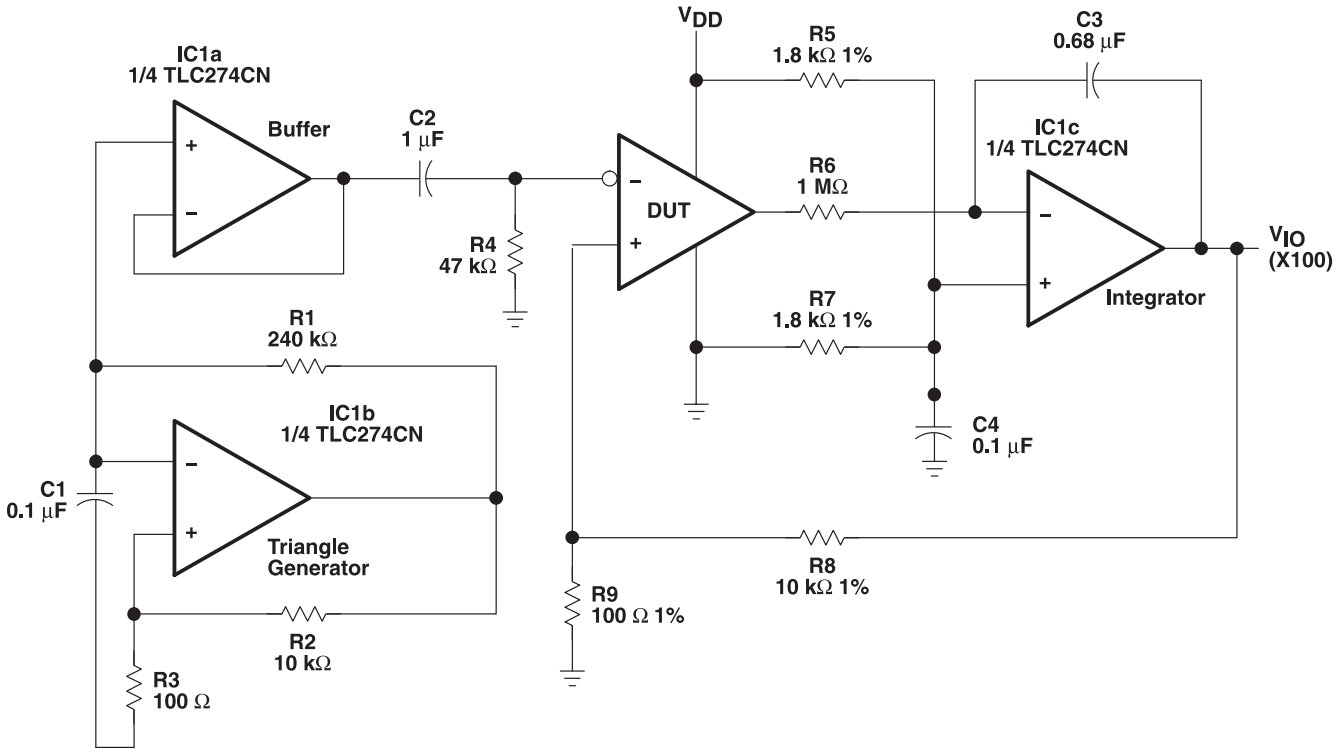

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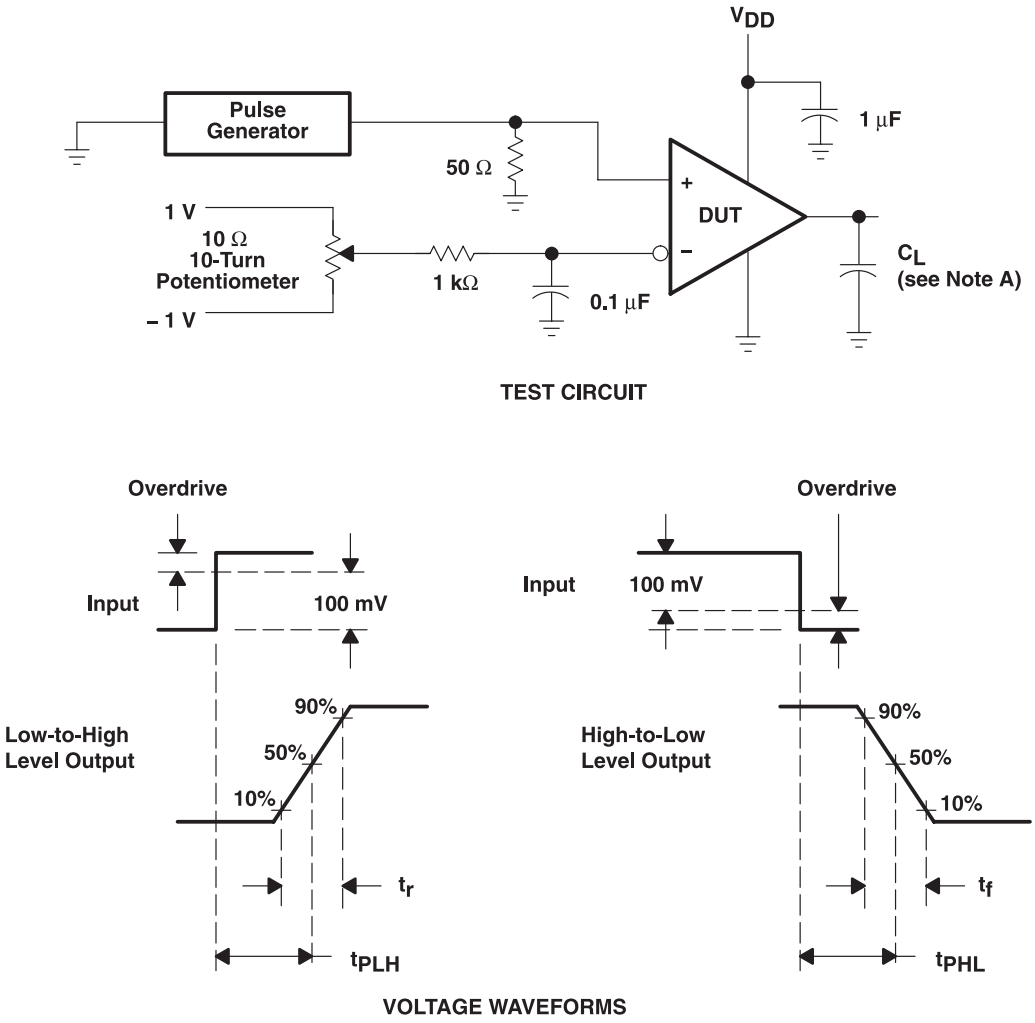
Figure 19. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 20, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state

Parameter Measurement Information (continued)



NOTE A: C_L includes probe and jig capacitance.

Figure 20. Response, Rise, and Fall Times Circuit and Voltage Waveforms

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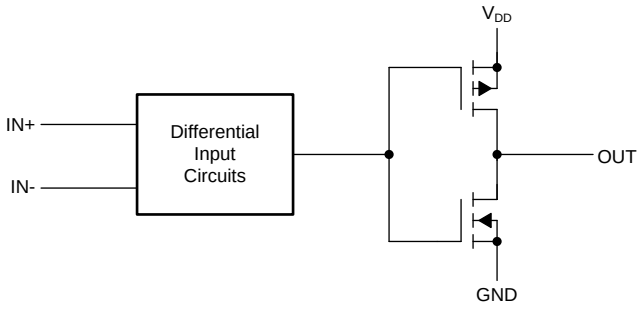
8 Detailed Description

8.1 Overview

The TLC3702-Q1 push-pull output comparator features a low quiescent current 20 uA and operation from 4 V to 16 V. The push-pull CMOS output stage drives capacitive loads directly without a power consuming pull-up resistor to achieve the stated response time.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 LinCMOS™ Process

The LinCMOS process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Further questions should be directed to the nearest TI field sales office.

8.3.2 Electrostatic Discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, for example, during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits effectively shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 21. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented in the following sections.

All input and output pins on LinCMOS and Advanced LinCMOS products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

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Feature Description (continued)

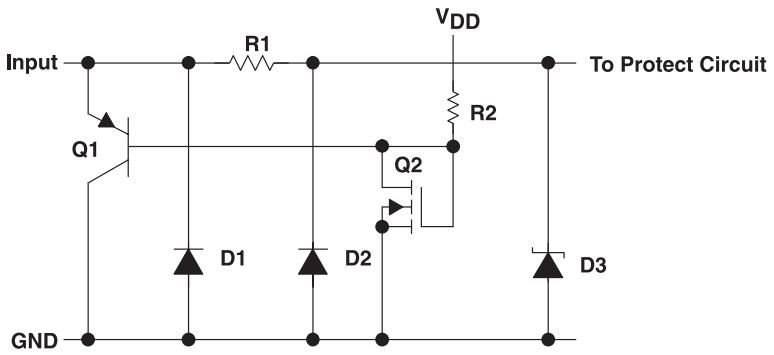

Figure 21. LinCMOS™ ESD-Protection Schematic

8.3.3 Input Protection Circuit Operation

TI's patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

8.3.4 Positive ESD Transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the N-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

8.3.5 Negative ESD Transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is −0.3 V to −1 V (the forward voltage of D1 and D2).

8.3.6 Circuit-Design Considerations

LinCMOS products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figure 22 and Figure 23 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 22. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

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Feature Description (continued)

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 24).

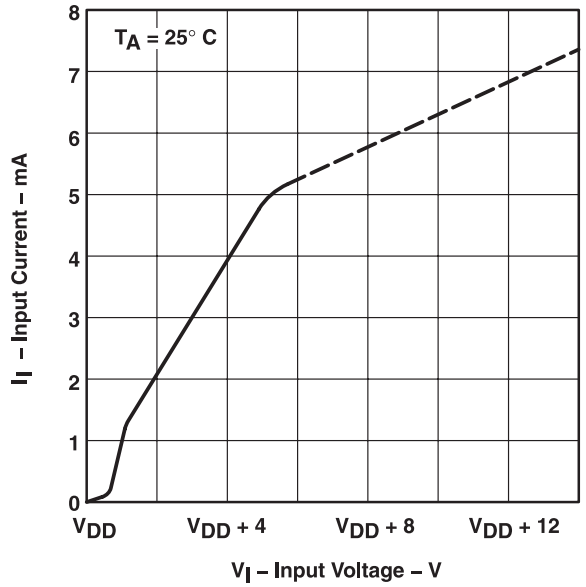


Figure 22. Input Current vs Input Voltage

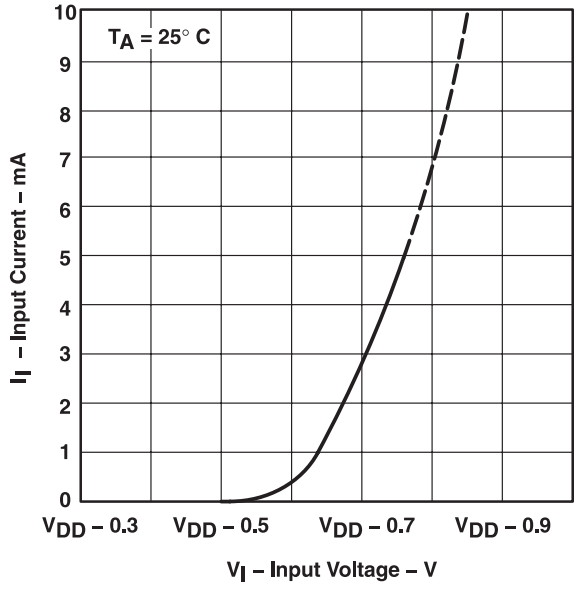
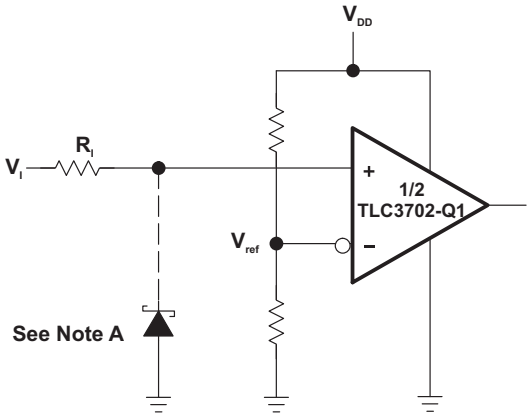


Figure 23. Input Current vs Input Voltage



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

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A. If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

Figure 24. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

8.4 Device Functional Modes

The TLC3702-Q1 is powered on when the supply is connected. The device can operate with single or dual supply, depending on the application. The device is in its full performance once the supply is above the recommended value.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The inputs should always remain within the supply rails to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between –0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) that is positioned as close to the device as possible.

The TLC3702-Q1 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

9.2 Typical Applications

9.2.1 Achieving Greater Noise Immunity

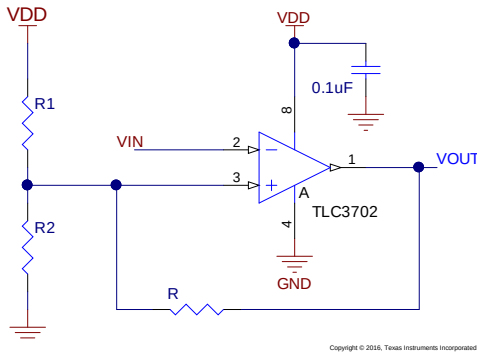

Figure 25. Application Adding Hysteresis to the TLC3702-Q1

9.2.1.1 Design Requirements

Figure 25 shows a typical topology used to introduce additional hysteresis. The additional hysteresis depends on the external resistors value and the supply voltage VDD.

Table 2. Design Parameters

PARAMETER	VALUE
Supply voltage	5 V
VIN	2.5 V and 50 mV noise on top
Ceramic capacitor	XR5 or XR7 50V
Hysteresis V+(H) – V+(-)	70 mV
R1, R2	27K 1%
R	1MΩ 1%

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9.2.1.2 Detailed Design Procedure

This circuit is designed for stabilizing the output in a noisy environment by adding external hysteresis. The hysteresis is added by connecting a feedback resistor between positive input V+ and output VOUT. Output is high and VOUT = VDD, the positive input V+(H) =

$$\frac{R2}{R2 + R1 // R} VDD \quad (1)$$

Output is low and VOUT = GND, the positive input V+(L) =

$$\frac{R2 // R}{R1 + R2 // R} VDD \quad (2)$$

From Equation 1 and Equation 2:

$$\frac{R}{R1} = \frac{V+(L)}{V+(H) - V+(L)} \quad (3)$$

$$\frac{R2}{R1} = \frac{V+(L)}{VDD - V+(H)} \quad (4)$$

9.2.1.3 Application Curves

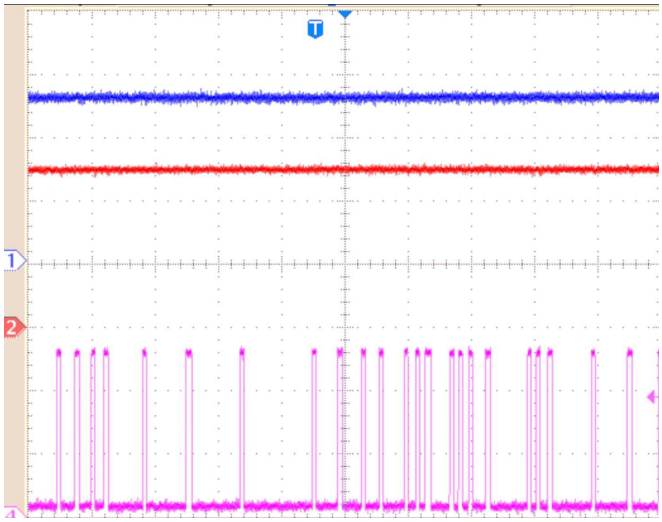


Figure 26. Output Voltage With No Hysteresis, R is Omitted

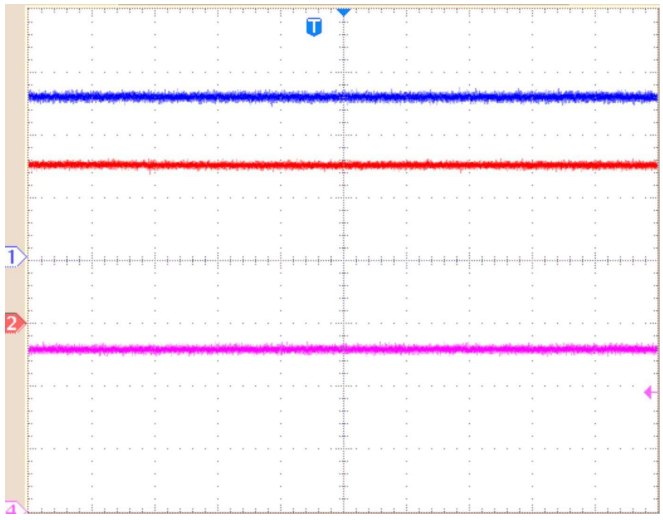
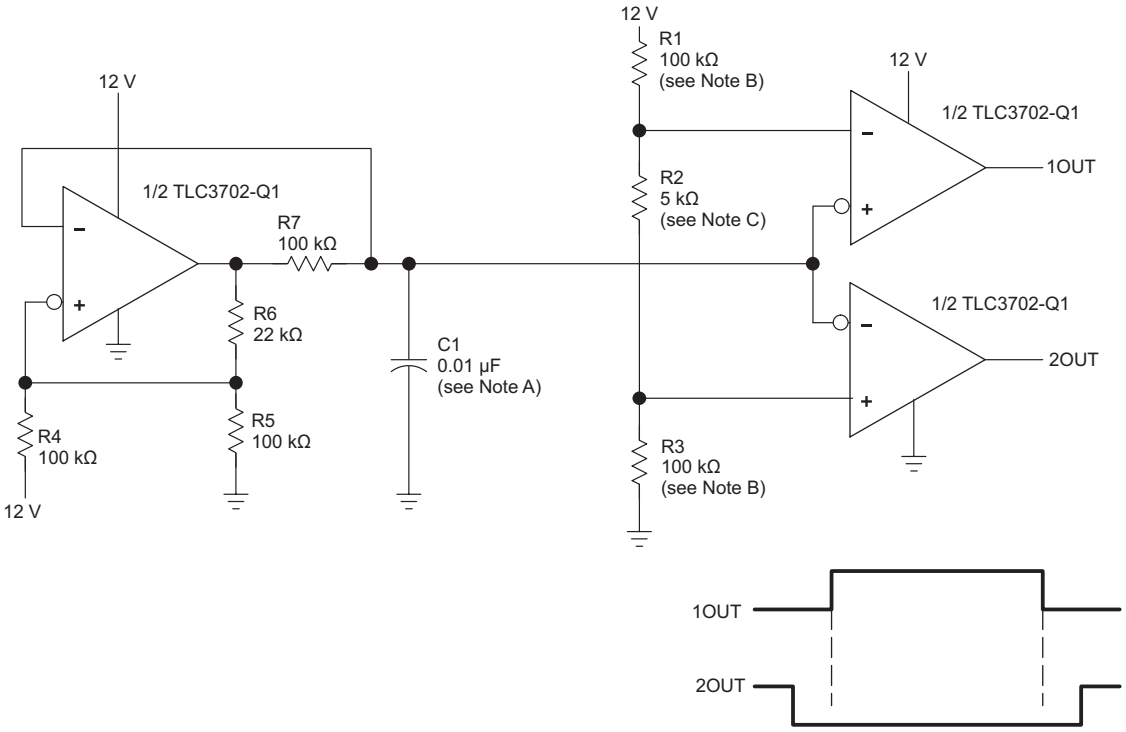


Figure 27. Output Voltage With Hysteresis

9.2.2 Two-Phase Non-Overlapping Clock Generator



NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 2 \times 1.71\,(100\ k\Omega)C1$
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

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Figure 28. Two-Phase Non-Overlapping Clock Generator

9.2.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage	3 V to 12 V
Ceramic capacitor	XR5 or XR7 50 V
Resistors	1%

9.2.2.2 Detailed Design Procedure

The first stage is a window comparator with positive feedback by connecting R6 between the comparator output and the positive input. That creates an external hysteresis depending on resistors R4, R5, R6 value and the supply voltage VDD.

Comparator output is high gives V+(H) =

$$\frac{R5}{R5 + R4 \,//\, R6}\,VDD \tag{5}$$

Comparator output is low gives V+(L) =

$$\frac{R5 \,//\, R6}{R4 + R5 \,//\, R6}\,VDD \tag{6}$$

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The negative feedback between capacitor C1 and the comparator negative input allows the capacitor to charge between 2 threshold V+(H) and V+(L). The charging and discharging is exponential with time constant of R7C1. The charging and discharging have the same duration.

C1 is charging during the time when output is high and the voltage across it is:

$$Vc(t) = VDD\left(1 - e^{-\frac{t}{R7C1}}\right) \tag{7}$$

The charging time is:

$$R7C1 \times Ln\left(\frac{VDD - V+(L)}{VDD - V+(H)}\right) \tag{8}$$

The charging and discharging time is:

$$T = 2 \times R7C1 \times Ln\left(\frac{VDD - V+(L)}{VDD - V+(H)}\right) \tag{9}$$

and the oscillator frequency is:

$$F = \frac{1}{2 \times R7C1 \times Ln\left(\frac{VDD - V+(L)}{VDD - V+(H)}\right)} \tag{10}$$

For the circuit of Figure 28, V+(L) = 1.83 V, V+(H) = 10.17 V and period T = 3.43 mS

This circuit can also be used for Frequency Dithering in switch mode power supply to pass EMC compliance.

The second stage forms 2 window comparators with complementary outputs. One output 1OUT is high when

$$Vc > \frac{R2 + R3}{R1 + R2 + R3} VDD \tag{11}$$

VDD and 2OUT is high when

$$Vc < \frac{R3}{R1 + R2 + R3} VDD \tag{12}$$

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10 Power Supply Recommendations

The TLC3702-Q1 comparator is specified for use on a single supply from 3 V to 16 V (or a dual supply from ±1.5 V to ±8 V) over a temperature range of –40°C to +125°C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

For any high-speed comparator or amplifier, proper design and printed-circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

- Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLC3702-Q1 device along with stray capacitance from an input pin to ground results in several picofarads of capacitance.
- The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2-µF tantalum capacitor do not need to be as close to the device as the 0.1-µF capacitor, and may be shared with other devices. The 2.2-µF capacitor buffers the power-supply line against ripple, and the 0.1-µF capacitor provides a charge for the comparator during high frequency switching.
- In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.
- Figure 29 shows an evaluation layout for the TLC3702-Q1 SOIC-8 package. C1 and C2 are power-supply bypass capacitors. Place the 0.1-µF capacitor closest to the comparator. Figure 25 shows a schematic of this circuit.

11.2 Layout Example

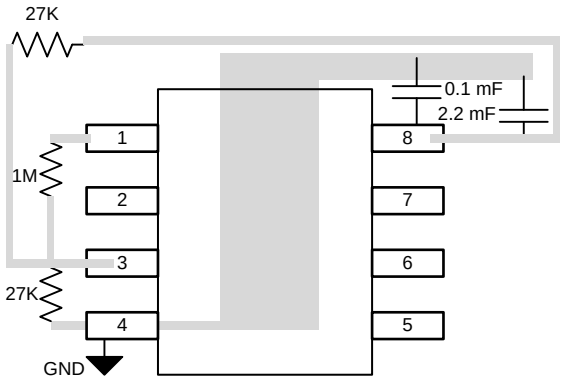

Figure 29. Layout Example

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

LinCMOS, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC3702QDRG4Q1	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702Q1	
TLC3702QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702Q1	Samples
TLC3702QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	3702Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC3702-Q1 :

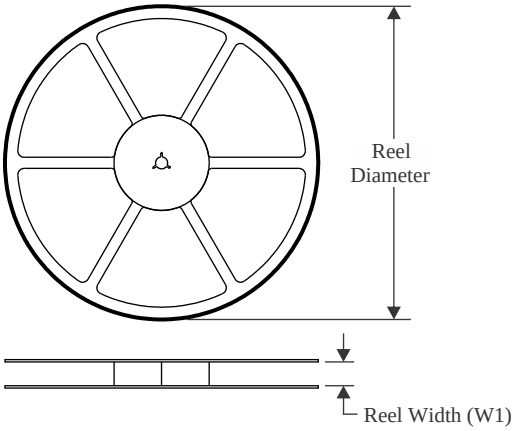
- Catalog : TLC3702
- Enhanced Product : TLC3702-EP
- Military : TLC3702M

NOTE: Qualified Version Definitions:

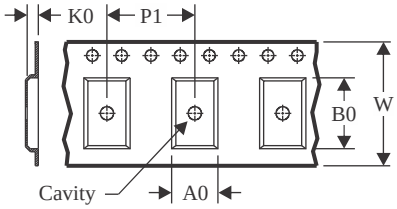
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

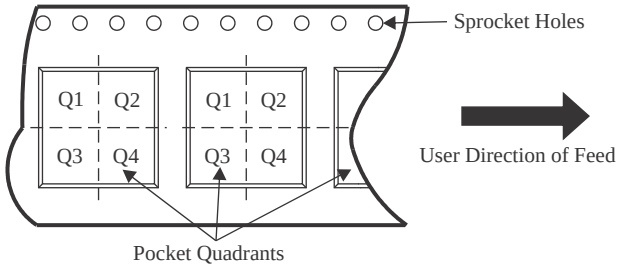


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

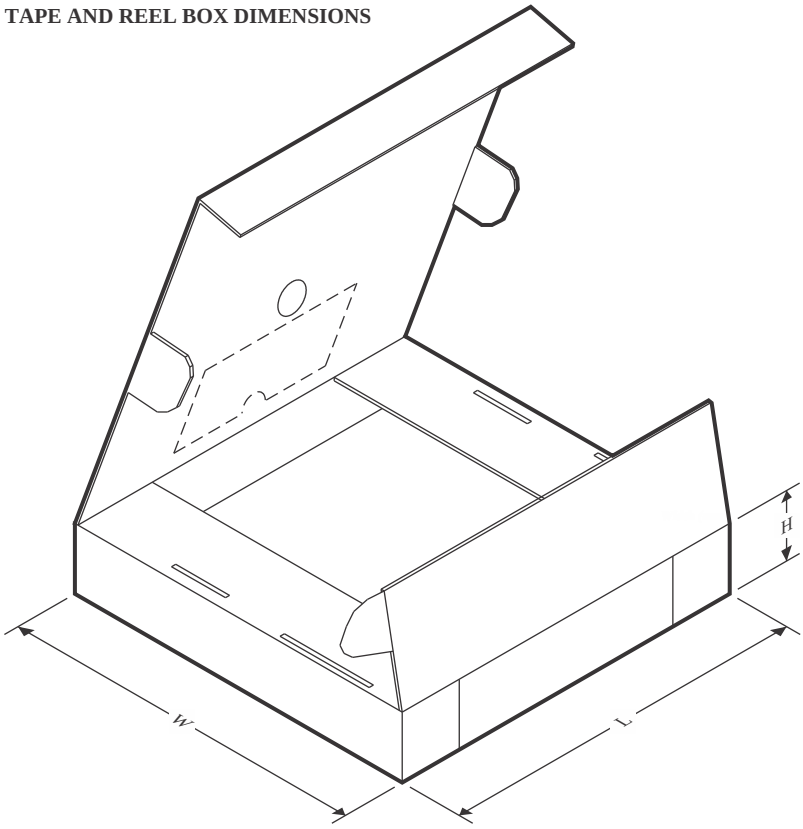
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

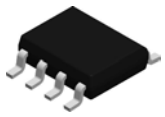
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3702QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3702QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

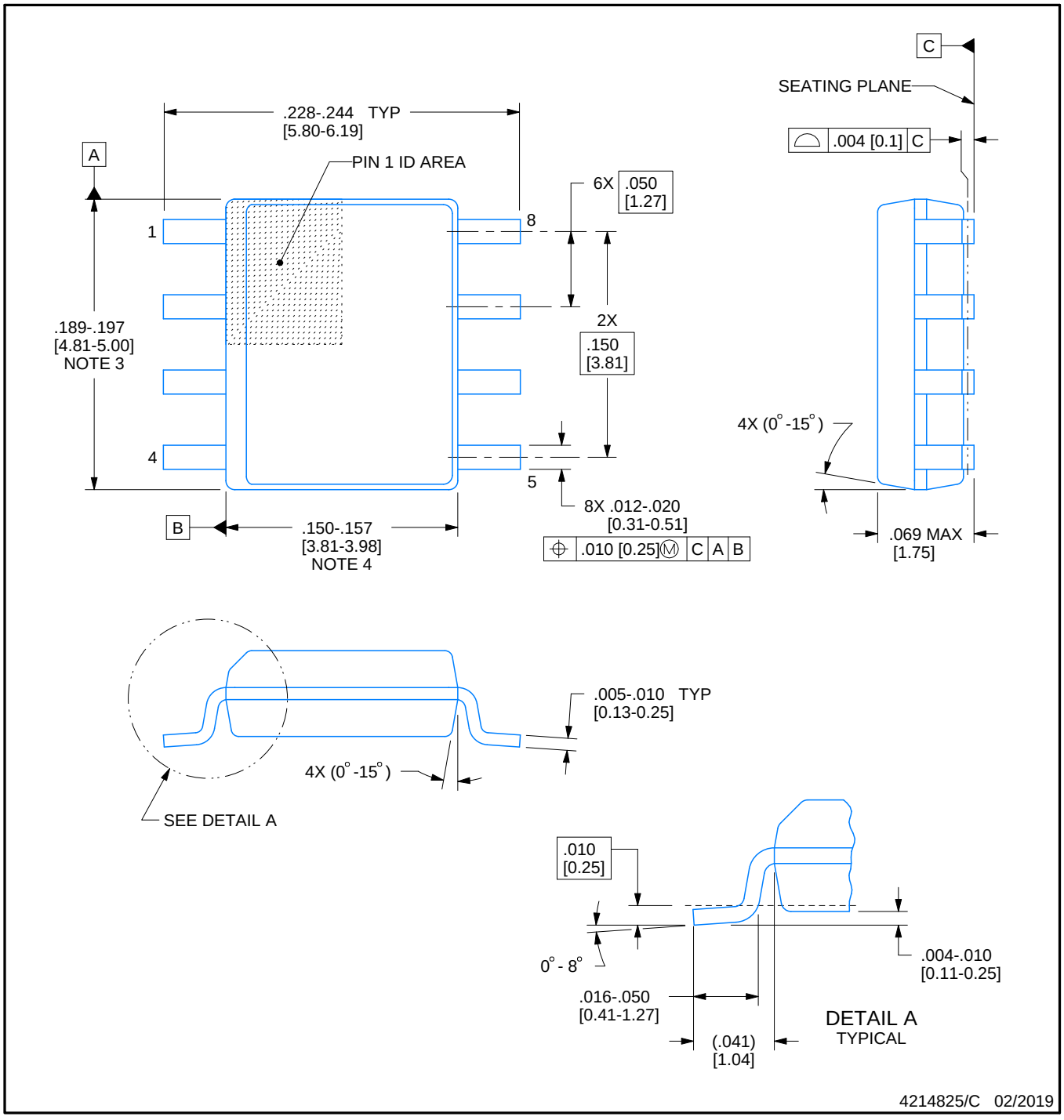


PACKAGE OUTLINE

D0008A

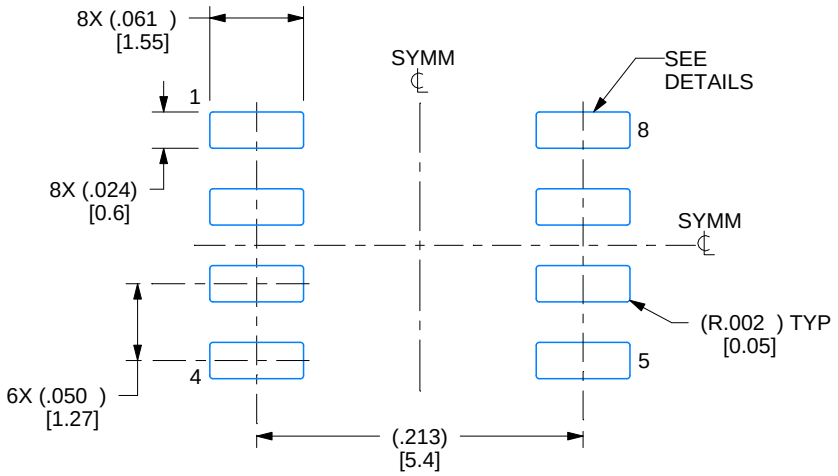
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

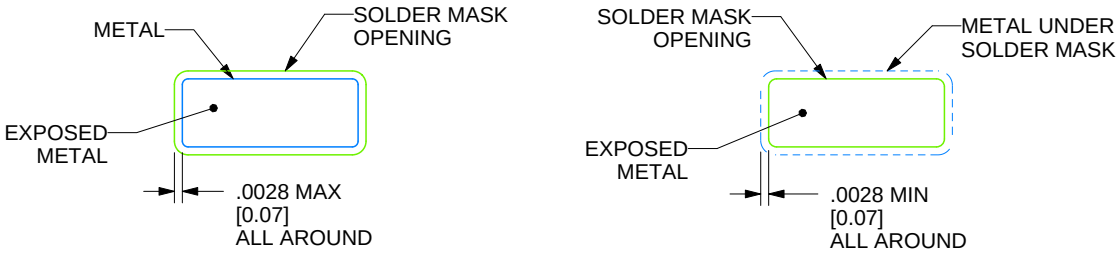


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

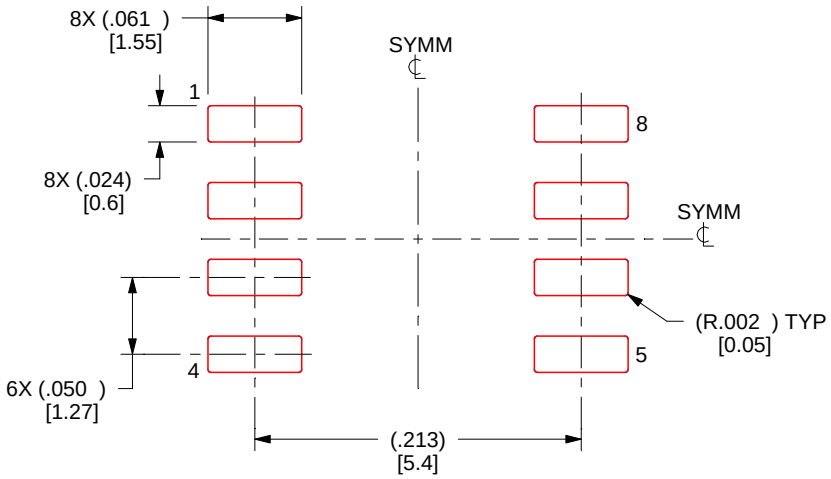
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

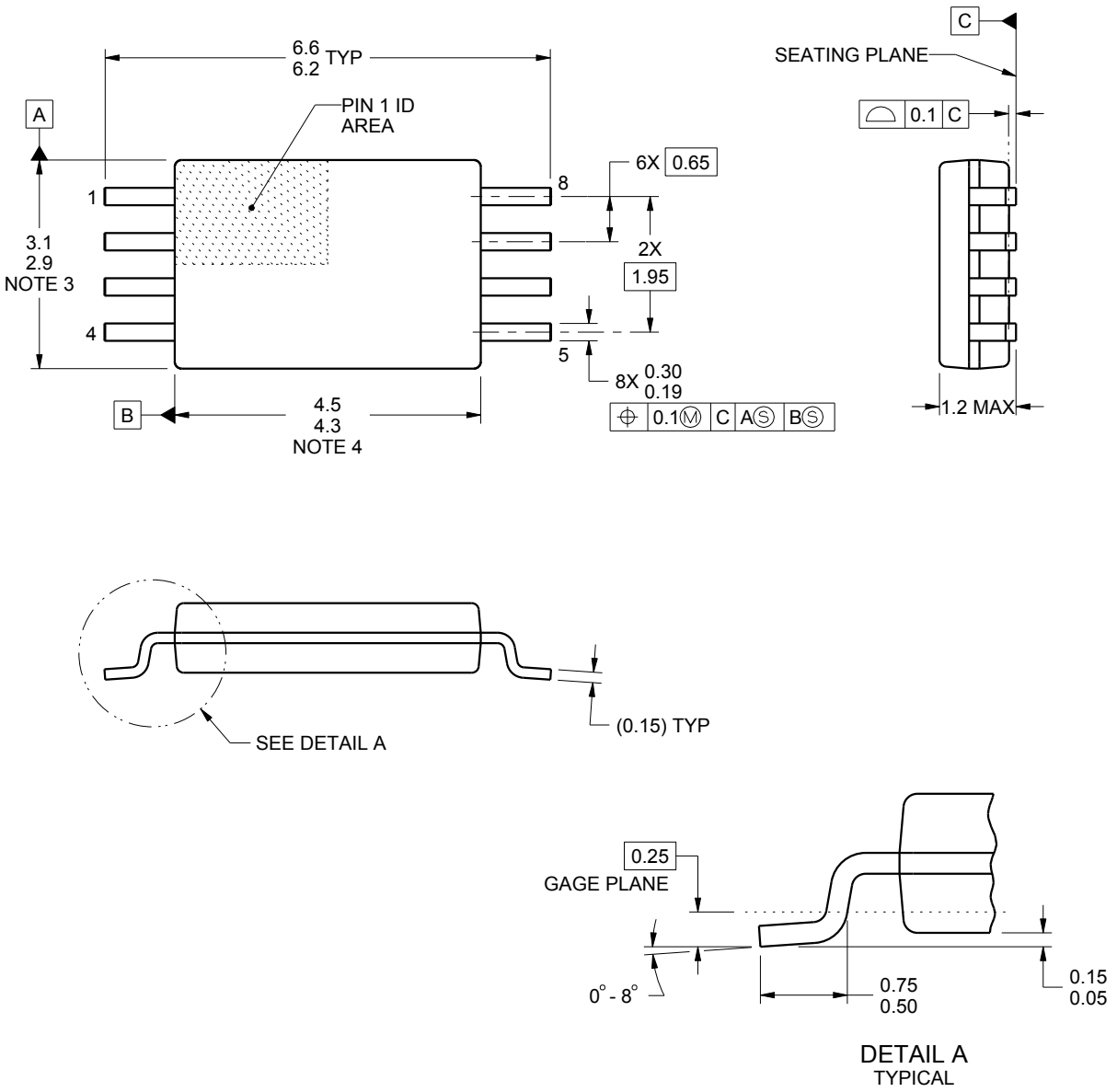
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

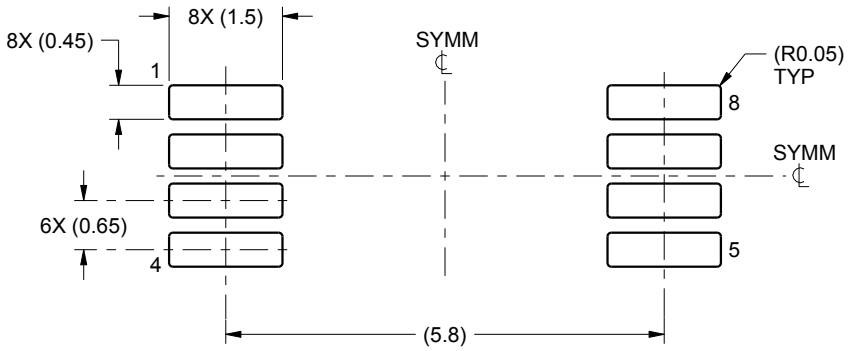
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

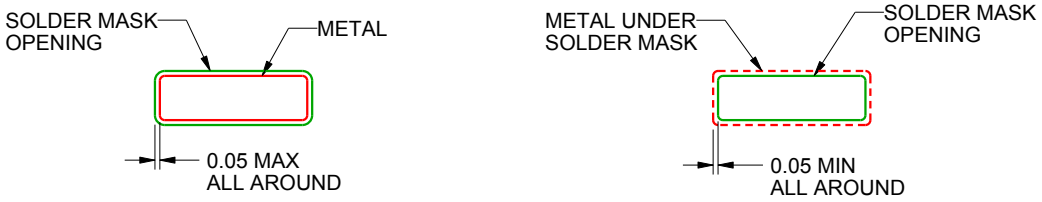


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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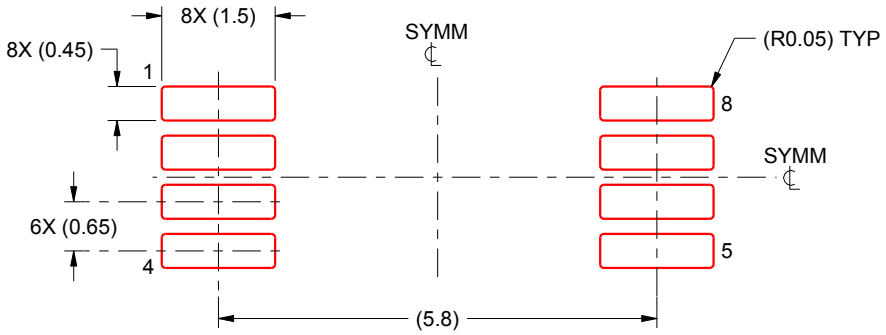
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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