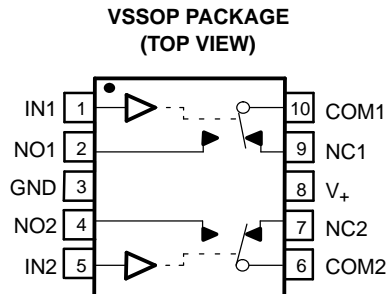


## FEATURES

- Specified Make-Before-Break Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

## APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



## DESCRIPTION

The TS5A23160 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

**FUNCTION TABLE**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TS5A23160**  
**0.9-Ω DUAL SPDT ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

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**SUMMARY OF CHARACTERISTICS<sup>(1)</sup>**

Configuration	Dual 2:1 Multiplexer/ Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance ( $r_{on}$ )	0.9 Ω
ON-state resistance match ( $\Delta r_{on}$ )	0.1 Ω
ON-state resistance flatness ( $r_{on(Flat)}$ )	0.15 Ω
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	2.5 ns/6 ns
Make-before-break time ( $t_{MKB}$ )	5.5 ns
Charge injection ( $Q_C$ )	1 pC
Bandwidth (BW)	95 MHz
OFF isolation ( $O_{ISO}$ )	–64 dB at 1 MHz
Crosstalk ( $X_{TALK}$ )	–64 dB at 1 MHz
Total harmonic distortion (THD)	0.004%
Leakage current ( $I_{NC(OFF)}$ )	±20 nA
Power-supply current ( $I_+$ )	0.1 μA
Package option	10-pin VSSOP

(1)  $V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	VSSOP – DGS (MSOP)	Tape and reel	TS5A23160DGSR	PREVIEW

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
V <sub>NC</sub> V <sub>NO</sub> V <sub>COM</sub>	Analog voltage range <sup>(3)(4)(5)</sup>	-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> < 0 or V <sub>NC</sub> , V <sub>NO</sub> , V <sub>COM</sub> > V <sub>+</sub>		mA
I <sub>NC</sub> I <sub>NO</sub> I <sub>COM</sub>	On-state switch current	-200	200	mA
	On-state peak switch current <sup>(6)</sup>	-400	400	
V <sub>I</sub>	Digital input voltage range <sup>(3)(4)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>I</sub> < 0		mA
I <sub>+</sub>	Continuous current through V+		100	mA
I <sub>GND</sub>	Continuous current through GND	-100	100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(7)</sup>		165	°C/W
T <sub>stg</sub>	Storage temperature range	-65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) All voltages are with respect to ground, unless otherwise specified.

(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(5) This value is limited to 5.5 V maximum.

(6) Pulse at 1-ms duration < 10% duty cycle

(7) The package thermal impedance is calculated in accordance with JESD 51-7.

**TS5A23160**  
**0.9-Ω DUAL SPDT ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

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**Electrical Characteristics for 5-V Supply<sup>(1)</sup>**

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	4.5 V		0.8	1.1	Ω
			Full					
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	4.5 V		0.7	0.9	Ω
			Full					
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	4.5 V		0.05	0.1	Ω
			Full					
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	4.5 V		0.15		Ω
			25°C					
			Full					
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = 4.5\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	5.5 V		-20	2	20
			Full					
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V		-1	1	μA
			Full					
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	5.5 V		-20	20	nA
			Full					
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V		-1	0.1	1
			Full					
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 1\text{ V}$ , $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 4.5\text{ V}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	5.5 V		-20	2	20
			Full					

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

### Electrical Characteristics for 5-V Supply (continued)

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		2.4		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	5.5 V	-2		2	nA
			Full		-1		1	μA
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	1	2.5	5.5	ns
			Full	4.5 V to 5.5 V	0.5		6.5	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	2	6	10	ns
			Full	4.5 V to 5.5 V	0.5		13.5	
Make-before break time	$t_{MKB}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	5 V		5.5		ns
			Full	4.5 V to 5.5 V	2		9.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	5 V		1		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 17</a>	25°C	5 V		18		pF
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	5 V		55		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	5 V		55		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 17</a>	25°C	5 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 20</a>	25°C	5 V		95		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See <a href="#">Figure 21</a>	25°C	5 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch ON, See <a href="#">Figure 22</a>	25°C	5 V		-64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	5 V		0.004		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V		10		nA
			Full			0.5		μA

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**TS5A23160**  
**0.9-Ω DUAL SPDT ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

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**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>**

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT			
<b>Analog Switch</b>											
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V			
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3 V		1.3	1.6	Ω			
			Full						2		
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3 V		1.2	1.5	Ω			
			Full						1.7		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2\text{ V}, 0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3 V		0.01	0.15	Ω			
			Full						0.15		
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3 V		0.2		Ω			
			25°C						Full	0.15	0.3
			Full								
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = 3\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 3\text{ V}$ , $V_{COM} = 1\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	3.6 V		-20	2	20			
			Full						-50	50	nA
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to } 0$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V		-1	0.2	1			
			Full						-15	15	μA
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 3\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	3.6 V		-20	2	20			
			Full						-20	20	nA
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 3.6\text{ V to } 0$ , $V_{COM} = 0 \text{ to } 3.6\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V		-1	0.2	1			
			Full						-15	15	μA
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 1\text{ V}$ , $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 3\text{ V}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	3.6 V		-20	2	20			
			Full						-20	20	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

### Electrical Characteristics for 3.3-V Supply (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		2		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	3.6 V	-2		2	nA
			Full		-20		20	
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	1.5	3.5	6.5	ns
			Full	3 V to 3.6 V	0.5		8	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	2.5	7	11.5	ns
			Full	3 V to 3.6 V	1		14.5	
Make-before break time	$t_{MKB}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	3.3 V		5.5		ns
			Full	3 V to 3.6 V	2		9.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	3.3 V		3		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 17</a>	25°C	3.3 V		18		pF
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	3.3 V		56		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	3.3 V		56		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 17</a>	25°C	3.3 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 20</a>	25°C	3.3 V		95		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See <a href="#">Figure 21</a>	25°C	3.3 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch ON, See <a href="#">Figure 22</a>	25°C	3.3 V		-64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	3.3 V		0.01		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V	10			nA
			Full		100			

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**0.9-Ω DUAL SPDT ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

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**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>**

$V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT			
<b>Analog Switch</b>											
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V			
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.3 V	1.8	2.5	Ω			
				Full					2.7		
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.8\text{ V}$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.3 V	1.5	2	Ω			
				Full					2.4		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.8\text{ V}$ , $0.8\text{ V}$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.3 V	0.15	0.2	Ω			
				Full					0.2		
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	2.3 V	0.6	1	Ω			
				25°C					2.7 V	0.6	1
				Full							
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$ , $V_{COM} = 2.3\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 2.3\text{ V}$ , $V_{COM} = 0.5\text{ V}$ ,	Switch OFF, See <a href="#">Figure 15</a>	25°C	2.7 V	-20	2	20			
				Full					-50	50	
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 2.7\text{ V}$ , $V_{COM} = 2.7\text{ V to } 0$ ,	Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V	-1	0.1	1			
				Full					-10	10	
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.5\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 2.3\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.7 V	-20	2	20			
				Full					-20	20	
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 2.7\text{ V to } 0$ , $V_{COM} = 0 \text{ to } 2.7\text{ V}$ ,	Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V	-1	0.1	1			
				Full					-10	10	
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0.5\text{ V}$ , $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 2.3\text{ V}$ ,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.7 V	-20	2	20			
				Full					-20	20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum



**Electrical Characteristics for 2.5-V Supply (continued)**
 $V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$		Full		1.8		5.5	V	
Input logic low	$V_{IL}$		Full		0		0.6	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	2.7 V	-2		2	nA	
			Full		-20		20		
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	2	4.5	8.5	ns
				Full	2.3 V to 2.7 V	1		10.5	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	3.5	8.5	13.5	ns
				Full	2.3 V to 2.7 V	1.5		16.5	
Make-before break time	$t_{MKB}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	2.5 V		6		ns
				Full	2.3 V to 2.7 V	8.5		10	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	2.5 V		4.5	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	2.5 V		18.5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		56.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		56.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 17</a>	25°C	2.5 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	2.5 V		100	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	2.5 V		-64	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	2.5 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	2.5 V		0.020	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V	10		nA	
				Full		50			

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**TS5A23160**  
**0.9-Ω DUAL SPDT ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER**

SCDS210A – AUGUST 2005 – REVISED APRIL 2006

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>**

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	5			Ω
			Full		30			
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	2			Ω
			Full		3.5			
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$ , $I_{COM} = -8\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	0.15			Ω
			Full		0.4			
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	5			Ω
			Full		4.5			
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = 1.65\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	1.95 V	-20	2	20	nA
			Full		-50	50		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 1.95\text{ V}$ , $V_{COM} = 1.95\text{ V to } 0$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V	-1	0.1	1	μA
			Full		-5	5		
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	1.95 V	-20	2	20	nA
			Full		-20	20		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = 0.3\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V	-1	0.1	1	μA
			Full		-5	5		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0.3\text{ V}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	1.95 V	-20	2	20	nA
			Full		-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 1.8-V Supply (continued)**

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		1.5		5.5	V
Input logic low	$V_{IL}$		Full		0		0.6	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	1.95 V	-2		2	nA
			Full		-20		20	
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	1.8 V	2.5	10	14.5	ns
			Full	1.65 V to 1.95 V	1		17	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	1.8 V	6.5	12.5	21.5	ns
			Full	1.65 V to 1.95 V	2		24	
Make-before break time	$t_{MKB}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	1.8 V		6.5		ns
			Full	1.65 V to 1.95 V	2.5		14	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	1.8 V		5.5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 17</a>	25°C	1.8 V		18.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	1.8 V		56.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	1.8 V		56.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 17</a>	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 20</a>	25°C	1.8 V		100		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See <a href="#">Figure 21</a>	25°C	1.8 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch ON, See <a href="#">Figure 22</a>	25°C	1.8 V		-64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	1.8 V		0.060		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V				nA
			Full				50	

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**TYPICAL PERFORMANCE**

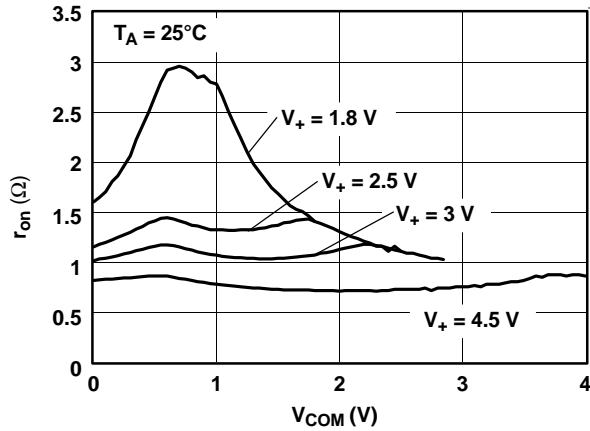


Figure 1.  $r_{on}$  vs  $V_{COM}$

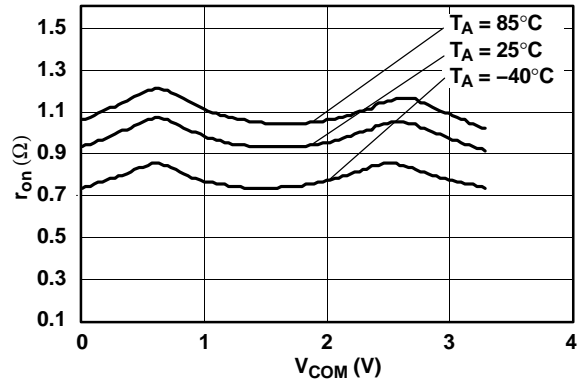


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3$  V)

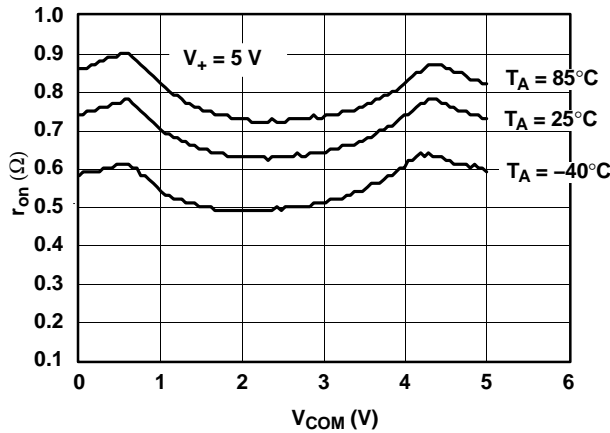


Figure 3.  $r_{on}$  vs  $V_{COM}$

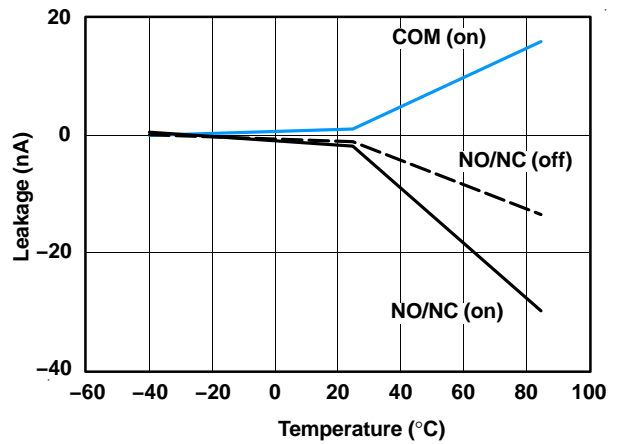


Figure 4. Leakage Current vs Temperature

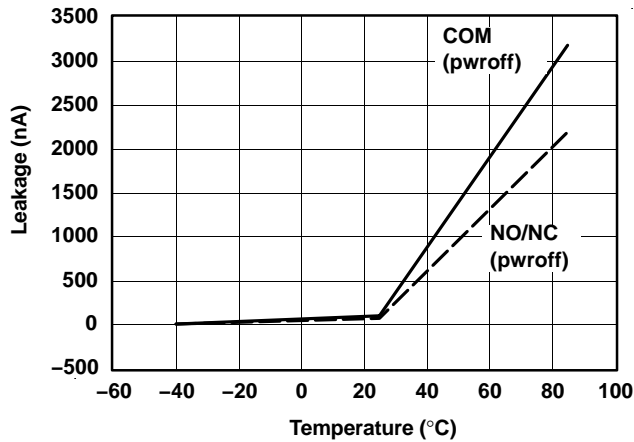


Figure 5. Leakage Current vs Temperature

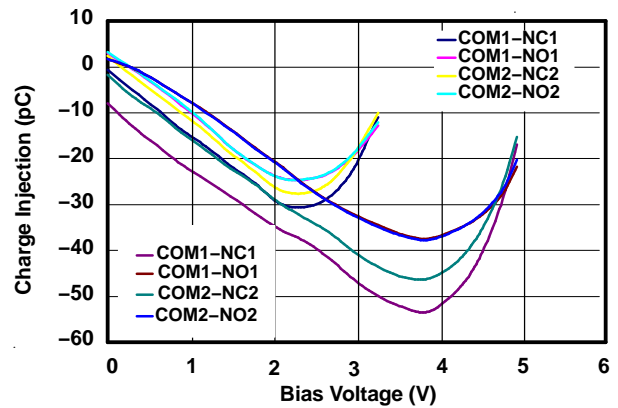


Figure 6. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

**TYPICAL PERFORMANCE (continued)**

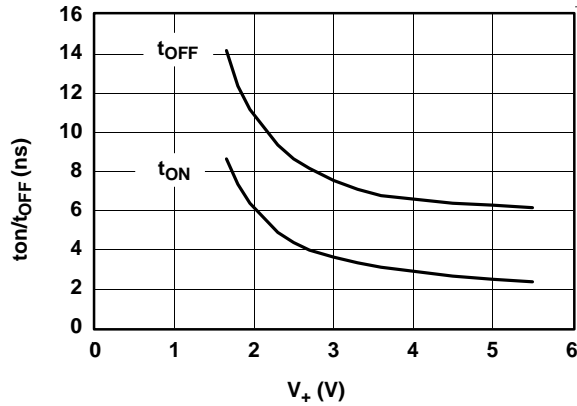


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

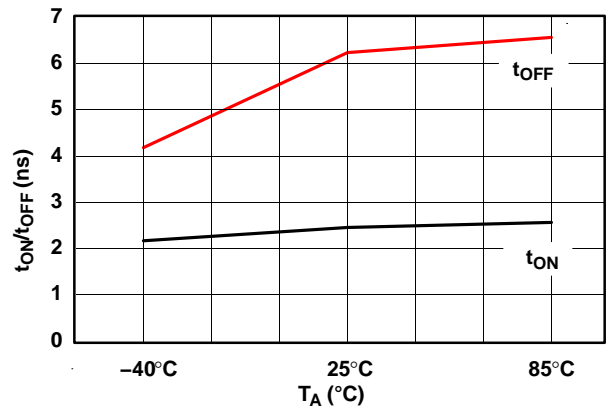


Figure 8.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5\text{ V}$ )

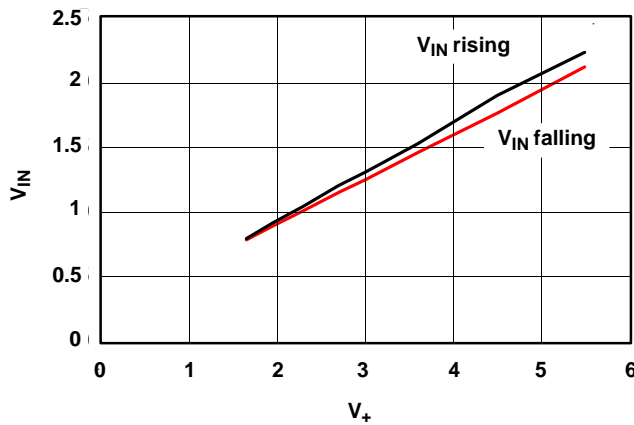


Figure 9. Logic Threshold vs  $V_+$

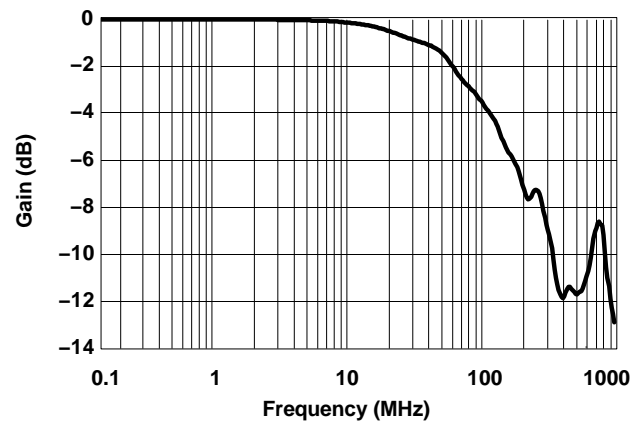


Figure 10. Bandwidth (Gain vs Frequency) ( $V_+ = 5\text{ V}$ )

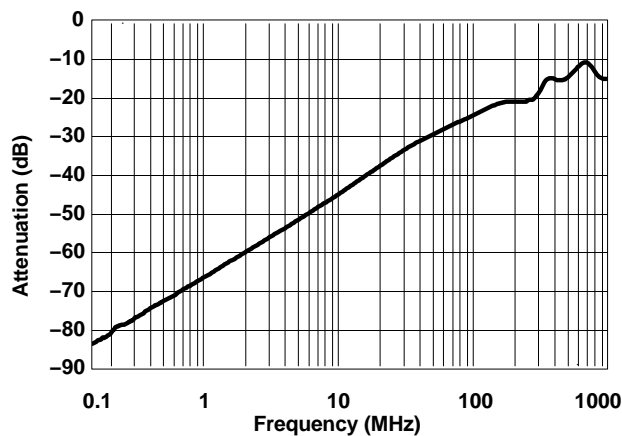


Figure 11. OFF Isolation vs Frequency

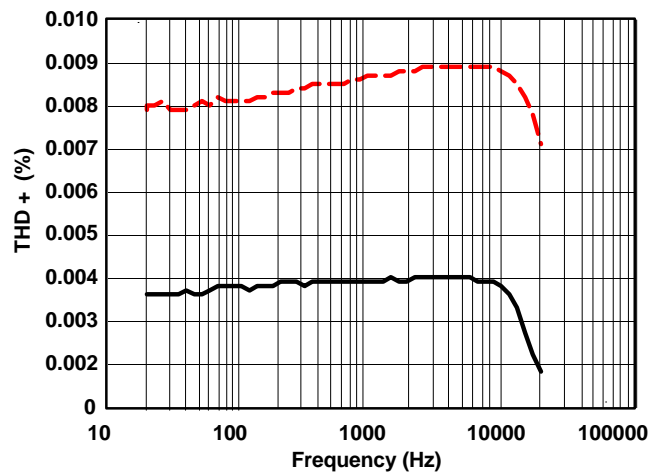
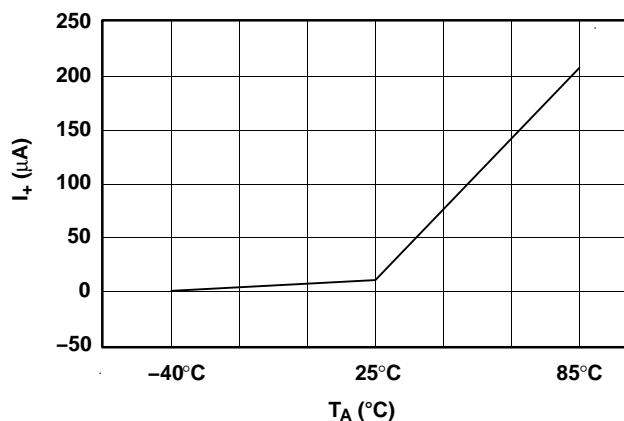


Figure 12. Total Harmonic Distortion vs Frequency ( $V_+ = 5\text{ V}$ )

**TYPICAL PERFORMANCE (continued)**



**Figure 13. Power-Supply Current vs Temperature (V<sub>+</sub> = 5 V)**

**PIN DESCRIPTION**

PIN	NAME	DESCRIPTION
1	IN1	Digital control to connect COM to NO or NC
2	NO1	Normally open
3	GND	Digital ground
4	NO2	Normally open
5	IN2	Digital control to connect COM to NO or NC
6	COM2	Common
7	NC2	Normally closed
8	V <sub>+</sub>	Power supply
9	NC1	Normally closed
10	COM1	Power supply

**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NC}$	Voltage at NC
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NC or COM and NO ports when the channel is ON
$r_{peak}$	Peak on-state resistance over a specified voltage range
$\Delta r_{on}$	Difference of $r_{on}$ between channels in a specific device
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
$t_{MBB}$	Make-before-break time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ . $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
$X_{TALK}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

PARAMETER MEASUREMENT INFORMATION

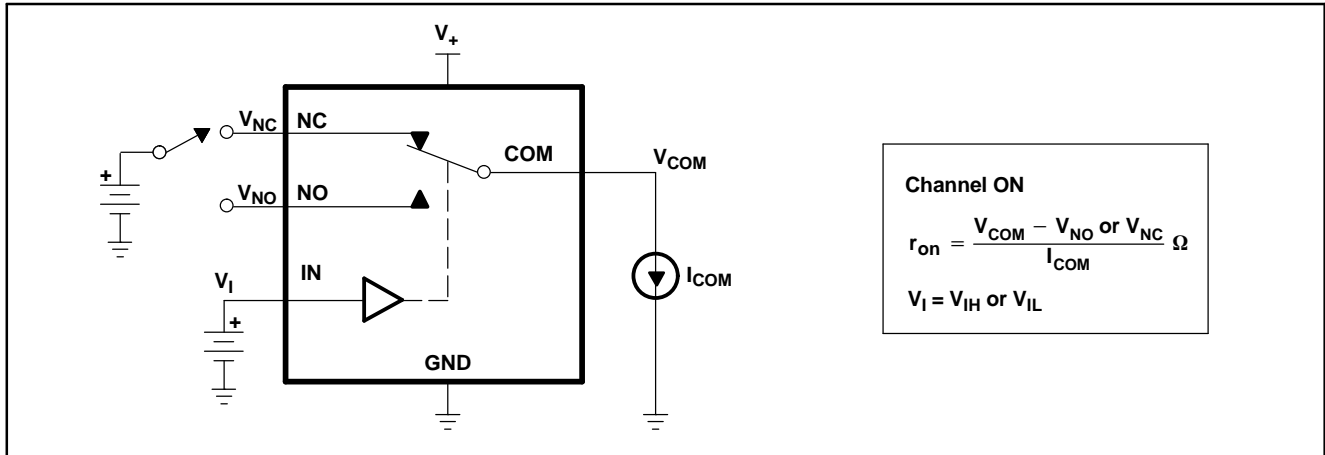


Figure 14. ON-State Resistance ( $r_{on}$ )

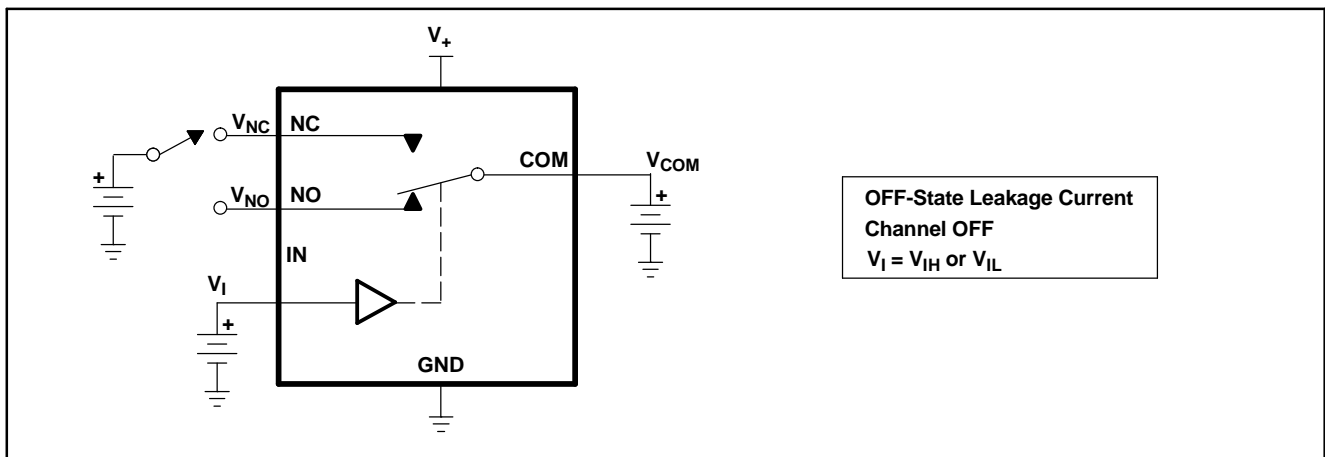


Figure 15. OFF-State Leakage Current ( $I_{NC(OFF)}$ ,  $I_{NC(PWROFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{NO(PWROFF)}$ ,  $I_{COM(OFF)}$ ,  $I_{COM(PWROFF)}$ )

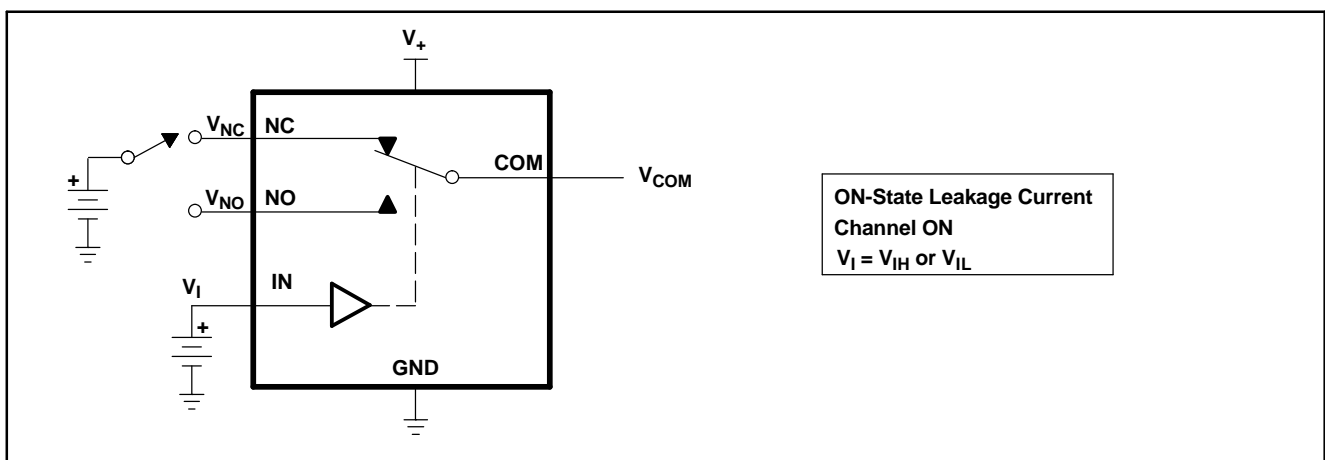
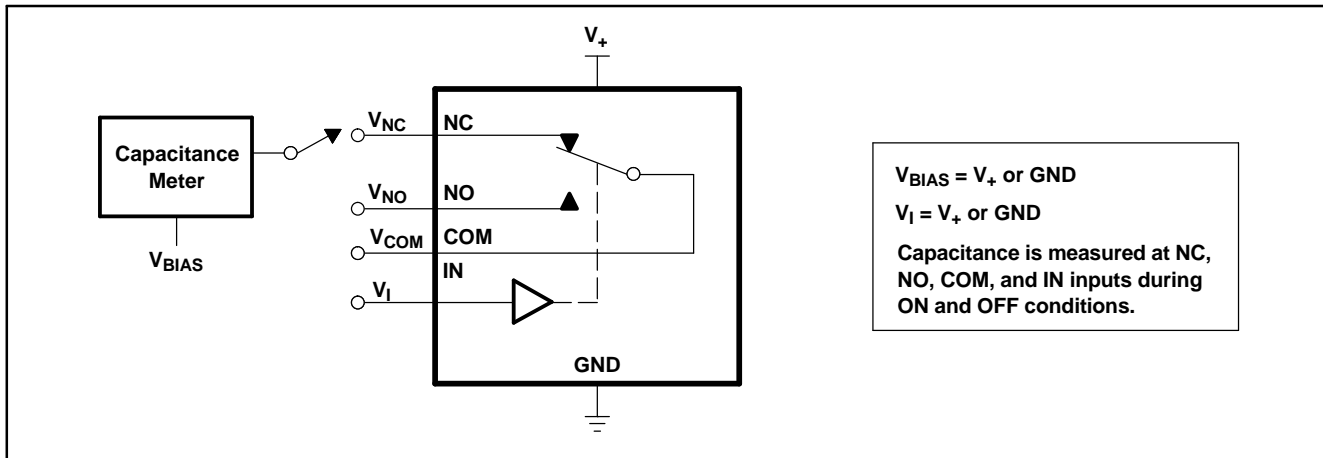


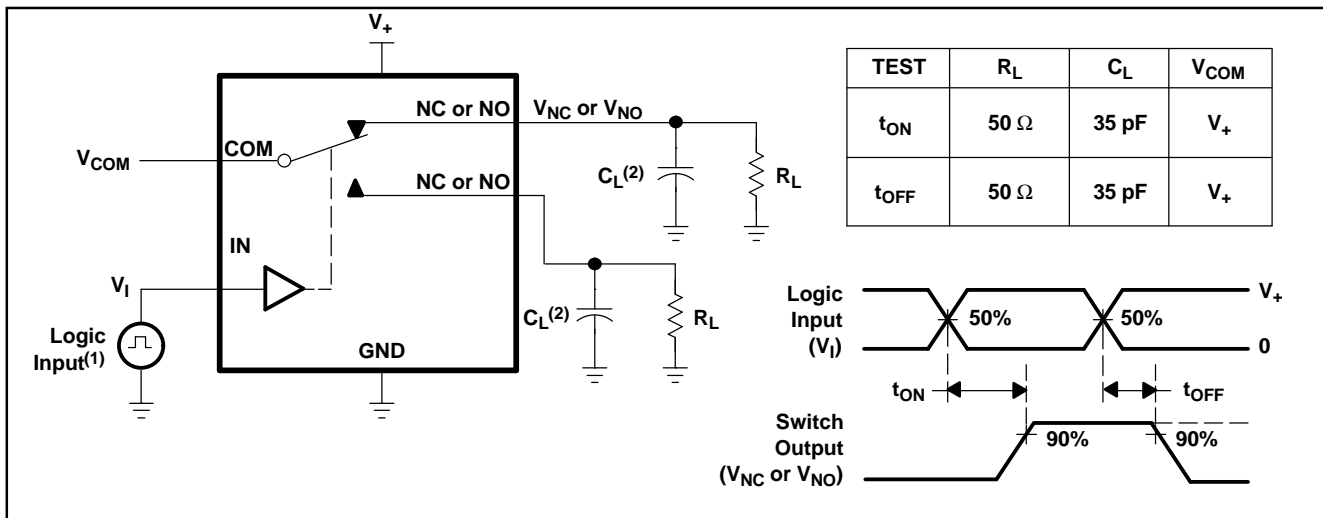
Figure 16. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )



**PARAMETER MEASUREMENT INFORMATION (continued)**



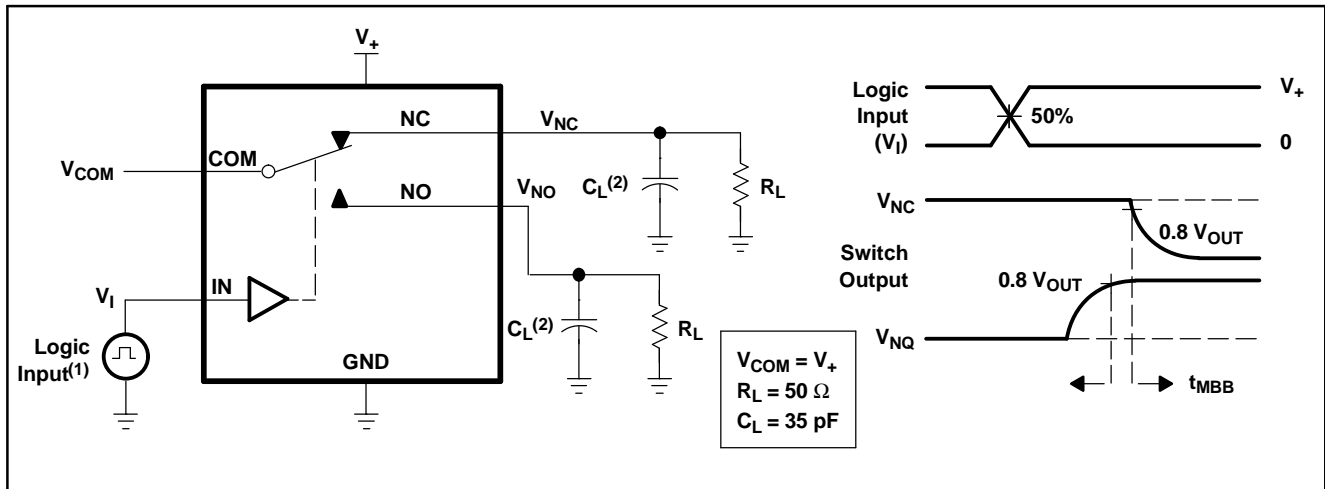
**Figure 17. Capacitance ( $C_I$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NO(OFF)}$ ,  $C_{NC(ON)}$ ,  $C_{NO(ON)}$ )**



- A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,
- B.  $C_L$  includes probe and jig capacitance.

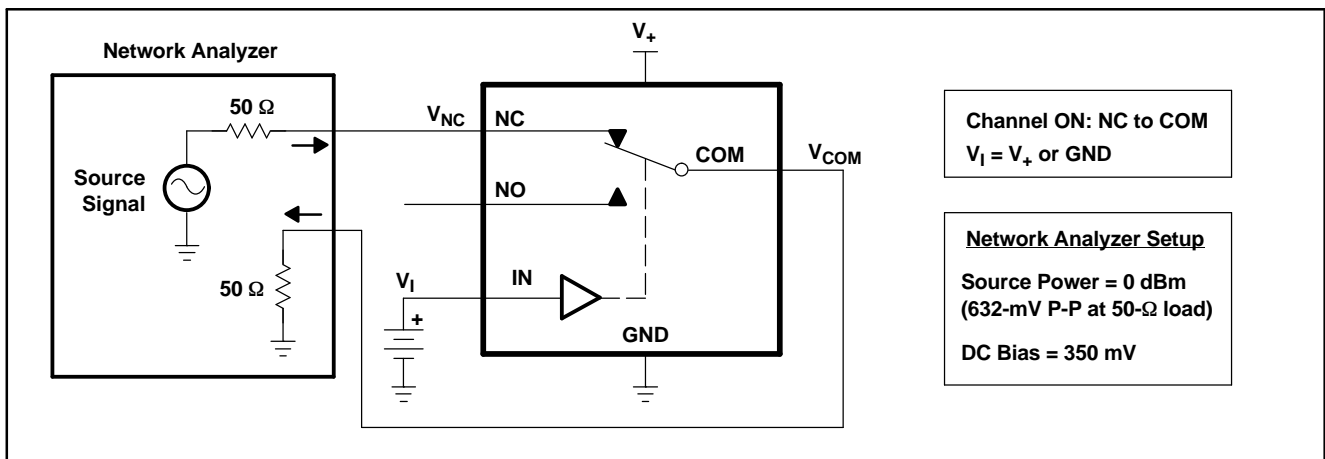
**Figure 18. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )**

**PARAMETER MEASUREMENT INFORMATION (continued)**



- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- B. C<sub>L</sub> includes probe and jig capacitance.

**Figure 19. Make-Before-Break Time (t<sub>MBB</sub>)**



**Figure 20. Bandwidth (BW)**

PARAMETER MEASUREMENT INFORMATION (continued)

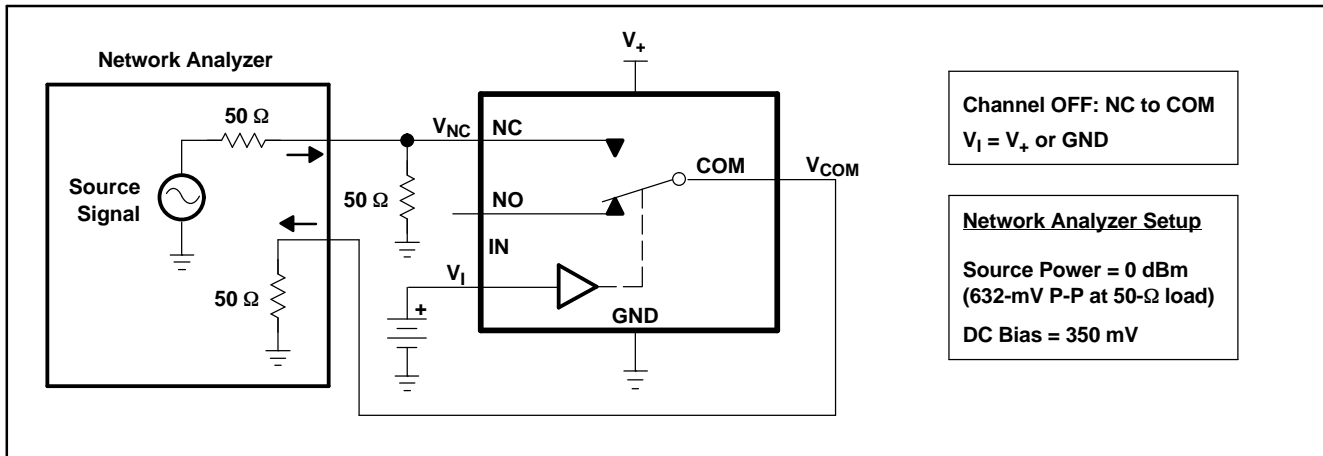
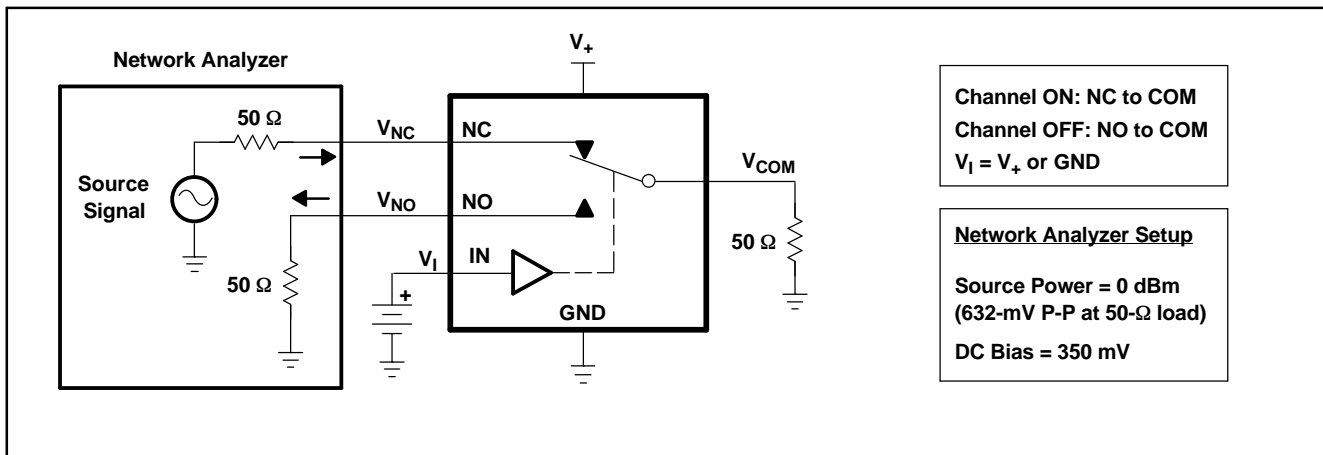


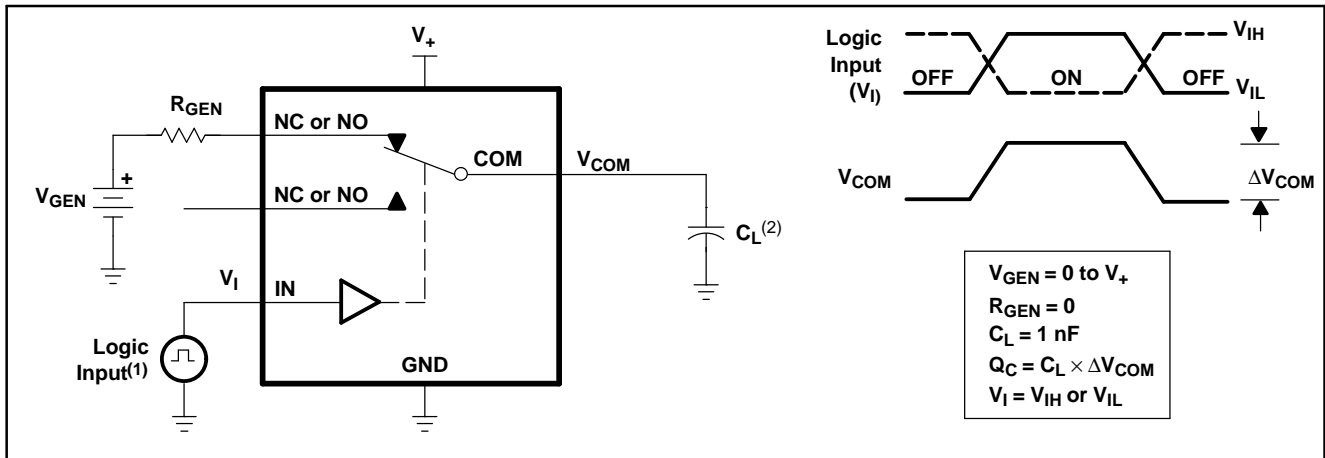
Figure 21. OFF Isolation ( $O_{ISO}$ )



- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- $C_L$  includes probe and jig capacitance.

Figure 22. Crosstalk ( $X_{TALK}$ )

PARAMETER MEASUREMENT INFORMATION (continued)



A.  $C_L$  includes probe and jig capacitance.

Figure 23. Charge Injection (QC)

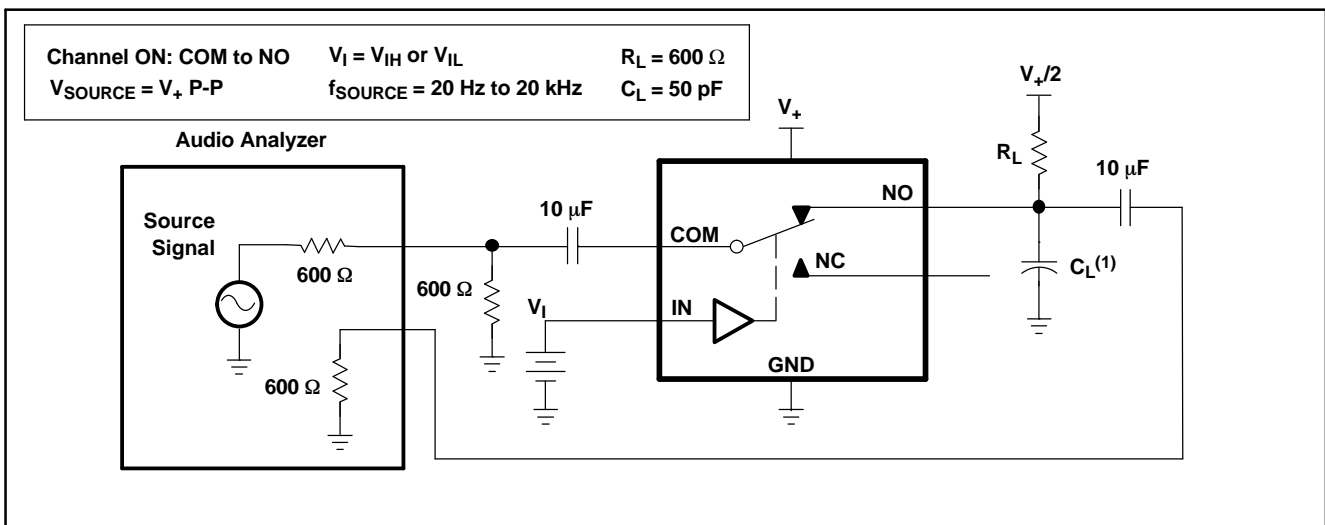


Figure 24. Total Harmonic Distortion (THD)

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23160DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JLR	Samples
TS5A23160DGST	LIFEBUY	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JLR	
TS5A23160DGSTG4	LIFEBUY	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JLR	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23160DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23160DGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23160DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A23160DGST	VSSOP	DGS	10	250	358.0	335.0	35.0



# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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