IEEE 1394b THREE-PORT CABLE TRANSCEIVER/ARBITER

FEATURES

- Fully Supports Provisions of IEEE 1394b-2002 at S100, S100B, S200, S200B, S400, and S400B Signaling Rates (B Signifies IEEE 1394b Signaling)
- Fully Supports Provisions of IEEE 1394a-2000 and 1394-1995 Standards for High-Performance Serial Bus
- Fully Interoperable With Firewire™, DTVLink, SB1394, DishWire, and i.LINK™ Implementation of IEEE Std 1394
- Provides Three Fully Backward- Compatible, (1394a-2000 Fully Compliant) Bilingual 1394b Cable Ports at 400 Megabits per Second (Mbps)
- Same Three Fully Backward-Compatible Ports Are 1394a-2000 Fully Compliant Cable Ports at 100/200/400 Mbps
- Full 1394a-2000 Support Includes:
  - Connection Debounce
  - Arbitrated Short Reset
  - Multispeed Concatenation
  - Arbitration Acceleration
  - Fly-By Concatenation
  - Port Disable/Suspend/Resume
  - Extended Resume Signaling for Compatibility With Legacy DV Devices
- Power-Down Features to Conserve Energy in Battery-Powered Applications
- Low-Power Automotive Sleep Mode Support
- Fully Compliant With Open Host Controller Interface (OHCI) Requirements
- Cable Power Presence Monitoring
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Control Bit, and 1394a-2000 Features
- Interface to Link-Layer Controller Supports Low-Cost Texas Instruments Bus-Holder Isolation
- Data Interface to Link-Layer Controller Terminal-Selectable From 1394a-2000 Mode (2/4/8 Parallel Bits at 49.152 MHz) or 1394b Mode (Eight Parallel Bits at 98.304 MHz)
- Interoperable With Link-Layer Controllers Using 3.3-V Supplies
- Interoperable With Other 1394 Physical Layers (PHYs) Using 1.8-V, 3.3-V, and 5-V Supplies
- Low-Cost 49.152-MHz Crystal Provides Transmit and Receive Data at 100/200/400 Mbps and Link-Layer Controller Clock at 49.152 MHz and 98.304 MHz
- Separate Bias (TPBIAS) for Each Port
- Low-Cost, High-Performance 80-Terminal TQFP (PFP) Thermally Enhanced Package
- Software Device Reset (SWR)
- Fail-Safe Circuitry Senses Sudden Loss of Power to the Device and Disables the Ports to Ensure That the TSB41BA3A Does Not Load the TPBIAS of Any Connected Device and Blocks Any Leakage From the Port Back to Power Plane.
- 1394a-2000-Compliant, Common-Mode Noise Filter on the Incoming Bias Detect Circuit to Filter Out Crosstalk Noise
- Cable/Transceiver Hardware Speed and Port Mode Are Selectable by Terminal States
- Supports Connection to CAT5 Cable Transceiver by Allowing Ports to be Forced to Beta-Only, 400-Mbps-Only, 200-Mbps-Only, or 100-Mbps-Only
- Supports Connection to S200 Plastic Optical Fiber Transceivers by Allowing Ports to be Forced to 1394b Beta-Only, S200-Mbps-Only, and S100-Mbps-Only
- Optical Signal Detect Input for All Ports in Beta Mode Enables Connection to Optical Transceivers
- Supports Use of 1394a Connectors by Allowing Ports 1 and 2 to Be Forced to 1394a-Only Mode

DESCRIPTION

The TSB41BA3A provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41BA3A interfaces with a link-layer controller (LLC), such as the TSB82AA2, TSB12LV21, TSB12LV26, TSB12LV32, TSB42AA4, TSB42AB4, TSB12LV01B, or TSB12LV01C. It can also be connected via cable port to an integrated 1394 Link + PHY layer such as the TSB43AB2.

The TSB41BA3A is powered by a single 3.3-V supply. The core voltage supply is supplied by an internal voltage regulator to the PLLVDD-CORE and DVDD-CORE terminals. To protect the phase-locked loop (PLL) from noise, the PLLVDD-CORE terminals must be separately decoupled from the DVDD-CORE terminals. The PLLVDD-CORE terminals are decoupled with 1-μF and smaller decoupling capacitors and the DVDD-CORE terminals are separately decoupled with 1-μF and smaller decoupling capacitors. The separation between DVDD-CORE and PLLVDD-CORE must be implemented by separate power supply rails or planes.

The TSB41BA3A can be powered by dual supplies, a 3.3-V supply for I/O and a core voltage supply. The core voltage supply is supplied to the PLLVDD-CORE and DVDD-CORE terminals to the requirements in the *recommended operating conditions* section of this data sheet. The PLLVDD-CORE terminals must be separated from the DVDD-CORE terminals, the PLLVDD-CORE terminals are decoupled with 1-μF and smaller decoupling capacitors and the DVDD-CORE terminals separately decoupled with 1-μF and smaller decoupling capacitors. The separation between DVDD-CORE and PLLVDD-CORE can be implemented by separate power supply rails, or by a single power supply rail, where the DVDD-CORE and PLLVDD-CORE are separated by a filter network to keep noise from the PLLVDD-CORE supply.

The TSB41BA3A requires an external 49.152-MHz crystal to generate a reference clock. The external clock drives an internal PLL, which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. A 49.152-MHz clock signal is supplied by the PHY to the associated LLC for synchronization of the two devices and is used for resynchronization of the received data when operating the PHY-link interface in compliance with the IEEE 1394a-2000 standard. A 98.304-MHz clock signal is supplied by the PHY to the associated LLC for synchronization of the two devices when operating the PHY-link interface in compliance with the IEEE 1394b-2002 standard. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

Data bits to be transmitted through the cable ports are received from the LLC on 2, 4, or 8 parallel paths (depending on the requested transmission speed and PHY-link interface mode of operation). They are latched internally, combined serially, encoded, and transmitted at 98.304, 122.78, 196.608, 245.76, 393.216, or 491.52 Mbps (referred to as S100, S100B, S200, S200B, S400, or S400B speed, respectively) as the outbound information stream.

The PHY-link interface can follow either the IEEE 1394a-2000 protocol or the IEEE 1394b-2002 protocol. When using a 1394a-2000 LLC such as the TSB12LV26, the BMODE terminal must be deasserted. The PHY-link interface then operates in accordance with the legacy 1394a-2000 standard. When using a 1394b LLC such as the TSB82AA2, the BMODE terminal must be asserted. The PHY-link interface then conforms to the 1394b-2002 standard.

The cable interface can follow either the IEEE 1394a-2000 protocol or the 1394b protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When any of the three ports is connected to a 1394a-2000-compliant device, the cable interface on that port operates in the 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to a 1394b-compliant node, the cable interface on that port operates per the 1394b-2002 standard at S100B, S200B, or S400B speed. The TSB41BA3A automatically determines the correct cable interface connection method for the bilingual ports.

NOTE:

The BMODE terminal does not select the cable interface mode of operation. The BMODE terminal selects the PHY-link interface mode of operation and affects the arbitration modes on the cable. When the BMODE terminal is deasserted, the PHY-link interface is placed in 1394a-2000 mode and BOSS arbitration is disabled. When the BMODE terminal is asserted, the PHY-link interface is placed in 1394b-2002 mode and BOSS arbitration is enabled.

During packet reception, the serial data bits are split into 2-, 4-, or 8-bit parallel streams (depending on the indicated receive speed and the PHY-link interface mode of operation), resynchronized to the local system clock, and sent to the associated LLC. The received data is also transmitted (repeated) on the other connected and active cable ports.

Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to a 1394a-2000-compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during 1394a-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to a 1394a-2000-compliant node, the TSB41BA3A provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB41BA3A are designed to work with external 112-Ω termination resistor networks in order to match the 110-Ω cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected ~56-Ω resistors. The midpoint of the pair of resistors that is connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 270 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

When the power supply of the TSB41BA3A is off while the twisted-pair cables are connected, the TSB41BA3A transmitter and receiver circuitry present a high-impedance signal to the cable that does not load the device at the other end of the cable.

When the TSB41BA3A is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the preferred method is for the port to be forced to the 1394a-only mode (data-strobe-only mode, DS), then the TPB+ and TPB– terminals can be tied together and then pulled to ground; or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS#_SD# terminal can be left unconnected.

If the port is left in bilingual (Bi) mode, then the TPB+ and TPB– terminals can be left unconnected or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS#_SD# terminal can be left unconnected.

If the port is left in a forced 1394b Beta-only (B1, B2, or B4) mode, then the TPB+ and TPB– terminals can be left unconnected or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS#_SD# terminal must be pulled to ground through a 1.2-kΩ or smaller resistor.

To operate a port as a 1394b bilingual port, the speed/mode selections terminals (S5_LKON, S4, S3, S2_PC0, S1_PC1, and S0_PC2) need to be pulled to VCC or ground through a 1-kΩ resistor. The port must be operated in the 1394b bilingual mode whenever a 1394b bilingual or a 1394b Beta-only connector is connected to the port. To operate the port as a 1394a-only port, the speed/mode selection terminals must be configured correctly to force 1394a-2000-only operation on that port. The only time the port must be forced to the data-strobe-only mode is if the port is connected to a 1394a connector (either 6-pin, which is recommended, or 4-pin). This mode is provided to ensure that 1394b signaling is never sent across a 1394a cable.

NOTE:

A bilingual port can only connect to a 1394b-only port that operates at S400b. It cannot establish a connection to a S200b or S100b port. A port that has been forced to S400b (B4) can connect to a 1394b-only port at S400b (B4) or S200b (B2) or S100b (B1). A port that has been forced to S200b can connect to a 1394b-only port at S200b or S100b. A port that has been forced to S100b can only connect to a 1394b-only port at S100b.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal must be connected to V_{DD} through a 1-kΩ resistor. The SE and SM terminals must be tied to ground through a 1-kΩ resistor.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. In some speed/mode selections the S2_PC0, S1_PC1, and S0_PC2 terminals indicate the default power–class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the TSB41BA3A, this bit can only be set by a write to the PHY register set. If a node is a contender for IRM or BM, then the node software must set this bit in the PHY register set.

The LPS (link power status) terminal works with the S5_LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used with the LCtrl bit to indicate the active/power status of the LLC. The LPS signal also resets, disables, and initializes the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

NOTE:

The TSB41BA3A does not have a cable-not-active (CNA) terminal. To achieve a similar function, the individual PHY ports can be set up to issue interrupts whenever the port changes state. If the LPS terminal is low, then this generates a link-on (LKON) output clock. See register bits PIE, PEI, and WDIE along with the individual interrupt bits.

The LPS input is considered inactive if it remains low for more than the LPS_RESET time (see the LPS terminal definition) and is considered active otherwise. When the TSB41BA3A detects that the LPS input is inactive, the PHY-LLC interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS_DISABLE time (see the LPS terminal definition), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The TSB41BA3A continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY initializes the interface and returns to normal operation. The PHY-LLC interface is also held in the disabled state during hardware reset. When the LPS terminal is returned to an active state after being sensed as having entered the LPS_DISABLE time, the TSB41BA3A issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY LLC now being accessible).

The PHY uses the S5_LKON terminal to notify the LLC to power up and become active. When activated, the output S5_LKON signal is a square wave. The PHY activates the S5_LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as previously described, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the S5_LKON output when the LLC becomes active (both LPS sensed as active and the LCtrl bit set to 1). The PHY also deasserts the S5_LKON output when a bus reset occurs, unless a PHY interrupt condition exists which would otherwise cause S5_LKON to be active. If the PHY is power-cycled and the power class is 0 through 4, then the PHY asserts S5_LKON for approximately 167 μs or until both the LPS is active and the LCtrl bit is 1.

NOTE:

This product is for high-volume applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB41BA3APFP	LIFEBUY	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TSB41BA3A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

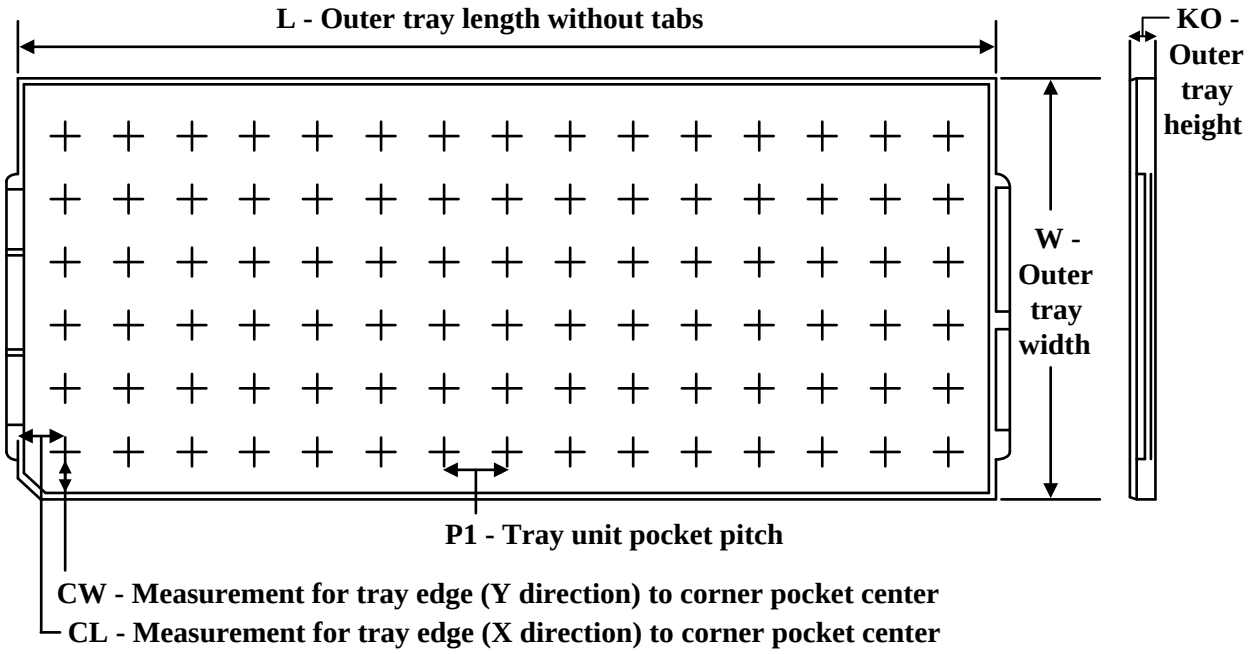
OTHER QUALIFIED VERSIONS OF TSB41BA3A :

- Enhanced Product : TSB41BA3A-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TRAY

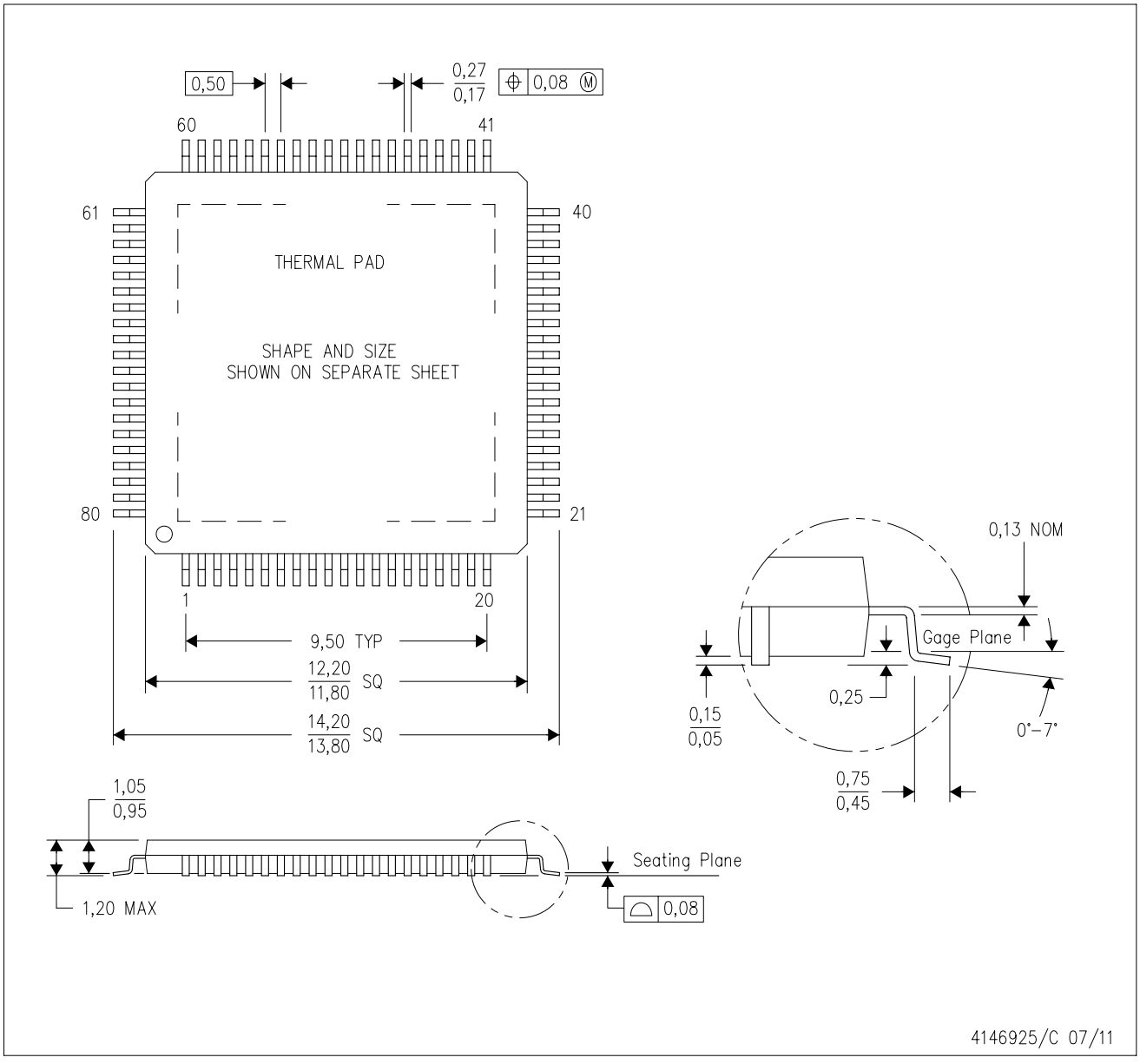


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSB41BA3APFP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

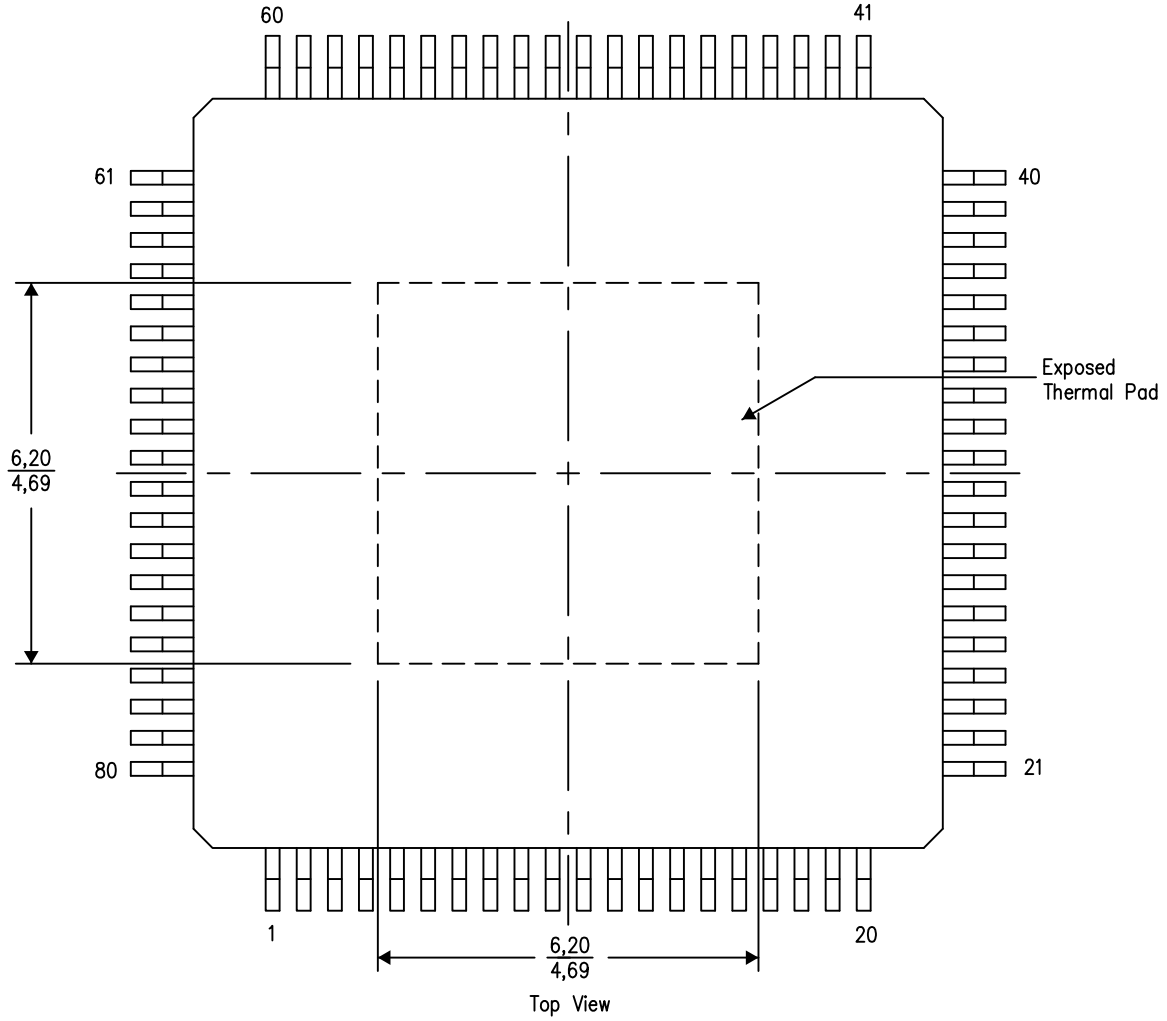
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



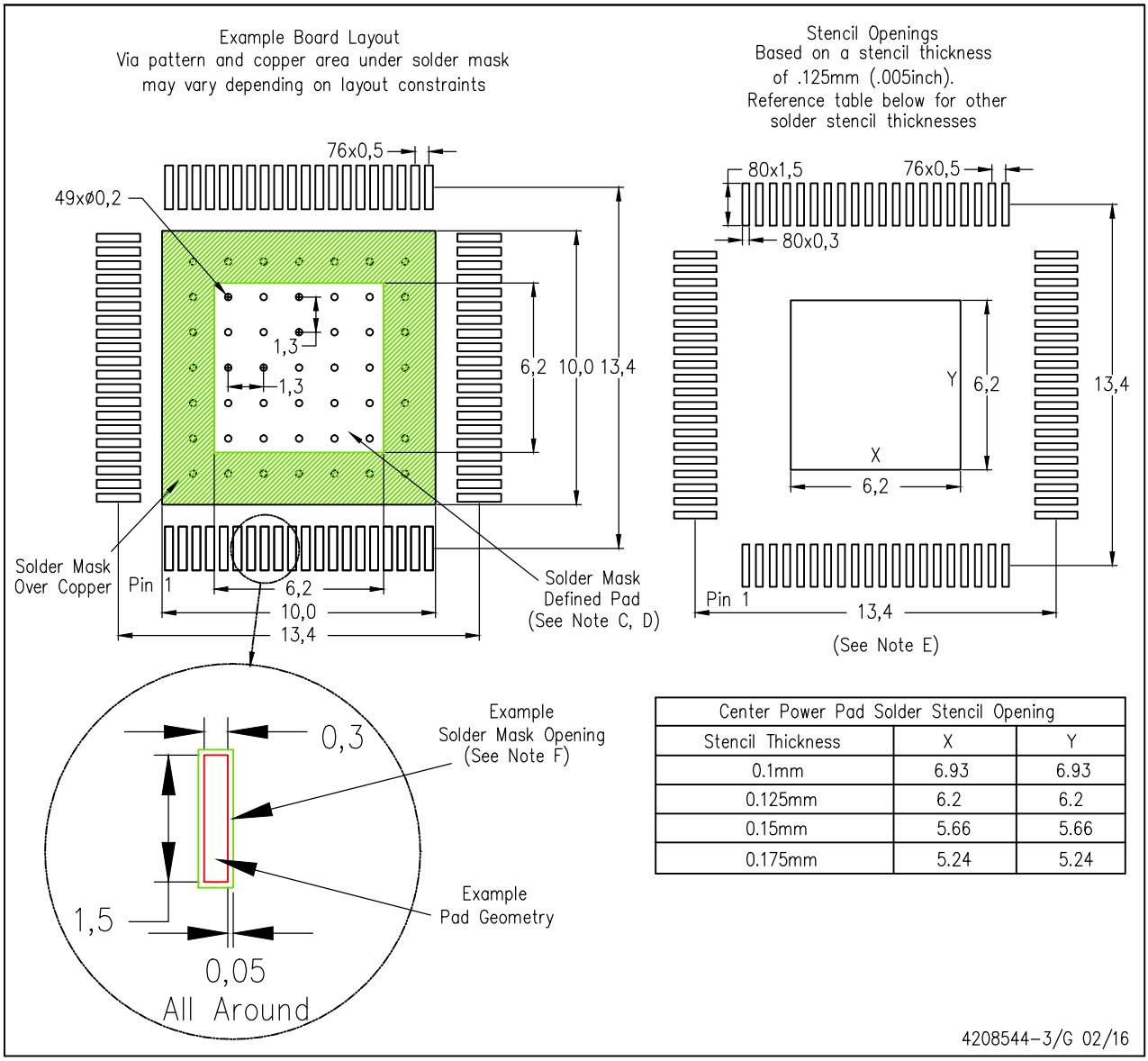
Exposed Thermal Pad Dimensions

4206327–3/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265