TSB83AA23 IEEE Std 1394b-2002
PHY and OHCI Link Device

Data Manual

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TEXAS INSTRUMENTS

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- **Provides Three Fully Backward-Compatible, (IEEE Std 1394a-2000 Fully Compliant) Bilingual IEEE Std 1394b-2002 Cable Ports at up to 800 Megabits per Second (Mbps)**
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1.2 Description

The TSB83AA23 is an integrated IEEE Std 1394b-2002 link-layer controller (LLC) design and physical layer (PHY) design combined in a single package to meet the demanding requirements of today's 1394 bus applications. The TSB83AA23 device is capable of exceptional 800-Mbps performance; thus, providing the throughput and bandwidth to move data efficiently and quickly between the PCI and 1394 buses. The TSB83AA23 device also provides outstanding ultralow power operation and intelligent power-management capabilities. The device provides the IEEE 1394 LLC function and PHY function and is compatible with 100-Mbps, 200-Mbps, 400-Mbps, and 800-Mbps serial-bus data rates.

The TSB83AA23 operates as the interface between 33-MHz/32-bit PCI local bus and an IEEE Std 1394a-2000 or IEEE Std 1394b-2002 serial-bus interface. It is capable of supporting serial data rates at 98.304, 196.608, 393.216, 491.52, or 786.432 Mbps (referred to as S100, S200, S400, S400B, or S800 speeds, respectively). When acting as a PCI bus master, the TSB83AA23 device is capable of multiple cache-line bursts of data, which can transfer at 132M bytes/s for 32-bit transfers after connecting to the memory controller.

Due to the high throughput potential of the TSB83AA23 device, it possible to encounter large PCI and legacy 1394 bus latencies, which can cause the 1394 data to be overrun. To overcome this potential problem, the TSB83AA23 implements deep transmit and receive FIFOs (see Section 1.1, *Features*, for FIFO size information) to buffer the 1394 data, thus, preventing possible problems due to bus latency. This also ensures that the device can transmit and receive sustained maximum-size isochronous or asynchronous data payloads at S800.

The TSB83AA23 LLC section implements other performance enhancements to improve overall performance of the device, such as a highly-tuned physical data path for enhanced SBP-2 performance, physical post writing buffers, multiple isochronous contexts, and advanced internal arbitration.

The TSB83AA23 LLC section also implements hardware enhancements to better support digital video (DV) and MPEG data stream reception and transmission. These enhancements are enabled through the isochronous receive digital video enhancements register at TI extension offset A80h (see Section 6.3.4, *Isochronous Receive Digital Video Enhancements Register*). These enhancements include automatic time-stamp insertion for transmitted DV and MPEG-formatted streams, and common isochronous packet (CIP) header stripping for received DV streams.

The CIP format is defined by the IEC 61883-1:1998 specification. The enhancements to the isochronous data contexts are implemented as hardware support for the synchronization time stamp for both DV and audio/video CIP formats. The TSB83AA23 device supports modification of the synchronization time-stamp field to ensure that the value inserted via software is not stale — that is, less than the current cycle timer when the packet is transmitted.

The TSB83AA23 performance and enhanced throughput make it an excellent choice for today's 1394 PC market; however, portable, mobile, and even desktop PC power-management schemes continue to require devices to use less and less power, and TI's 1394 product line has continued to raise the bar by providing the lowest-power 1394 devices in the industry. The TSB83AA23 device represents the next evolution of TI commitment to meet the challenge of power-sensitive applications. The TSB83AA23 device has ultralow operational power requirements and intelligent power-management capabilities that allow it to conserve power autonomously based on the device usage. The TSB83AA23 LLC section fully supports D0, D1, D2, and $D3_{hot/cold}$ power states, as specified in the *PC 2001 Design Guide* requirements and the *PCI Power Management Specification*. PME wake-event support is subject to operating-system support and implementation.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles as specified by the *PCI Local Bus Specification*, and provides plug-and-play (PnP) compatibility. Furthermore, the TSB83AA23 LLC section is fully compliant with the latest *PCI Local Bus Specification*, *PCI Bus Power Management Interface Specification*, IEEE Std 1394b-2002, IEEE Std 1394a-2000, and *1394 Open Host Controller Interface Specification*.

The TSB83AA23 PHY section provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The TSB83AA23 is powered by multiple voltage supplies, 3.3-V supplies for I/O and the LLC section, and a core voltage supply for the PHY section. The core voltage supply is supplied to the PLLVDD_CORE and DVDD_CORE terminals in accordance with the requirements in the recommended operating conditions. The PLLVDD_CORE terminals must be separated from the DVDD_CORE terminals, the PLLVDD_CORE terminals are decoupled with 1-μF and smaller decoupling capacitors, and the DVDD_CORE terminals separately decoupled with 1-μF and smaller decoupling capacitors. The separation between DVDD_CORE and PLLVDD_CORE can be implemented by separate power-supply rails, or by a single power-supply rail, where the DVDD_CORE and PLLVDD_CORE are separated by a filter network to keep noise from the PLLVDD_CORE supply. In addition, $\overline{\text{REG\_EN}}$ must be asserted low to enable the internal voltage regulator for the LLC section. If $\overline{\text{REG\_EN}}$ is not pulled low, the a 1.8-V power rail must be applied to the REG18 pins.

The TSB83AA23 requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbps (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

To ensure that the TSB83AA23 conforms to the IEEE Std 1394b-2002 standard, the BMODE terminal must be asserted.

NOTE

The BMODE terminal does not select the cable-interface mode of operation. The BMODE terminal selects the internal PHY section-LLC section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation.

The cable interface can follow either the IEEE Std 1394a-2000 protocol or the IEEE Std 1394b-2002 protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When any of the ports are connected to an IEEE Std 1394a-2000-compliant device, the cable interface on that port operates in the IEEE Std 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to an IEEE Std 1394b-2002-compliant node, the cable interface on that port operates per the IEEE Std 1394b-2002 standard at S400B or S800 speed. The TSB83AA23 automatically determines the correct cable interface connection method for the bilingual ports.

To operate a port as an IEEE Std 1394b-2002 bilingual port, the data-strobe-only terminal for the port (DS0 or DS1) must be pulled to ground through a 1-kΩ resistor. The port must be operated in the IEEE Std 1394b-2002 bilingual mode when an IEEE Std 1394b-2002 bilingual or an IEEE Std 1394b-2002 Beta-only connector is connected to the port. To operate the port as an IEEE Std 1394a-2000-only port, the data-strobe-only terminal (DS0 or DS1) must be pulled to 3.3-V V_{CC} through a 1-kΩ resistor. The only time the port must be forced to the data-strobe-only mode is if the port is connected to an IEEE Std 1394a-2000 connector (either 6 pin, which is recommended, or 4 pin). This mode is provided to ensure that IEEE Std 1394b-2002 signaling is never sent across an IEEE Std 1394a-2000 cable.

During packet reception, the serial data bits are split into 2-, 4-, or 8-bit parallel streams by the PHY section and sent to the link-layer controller (LLC) section. The received data is also transmitted (repeated) on the other connected and active cable ports.

Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to an IEEE Std 1394a-2000-compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during IEEE Std 1394a-2000-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to an IEEE Std 1394a-2000-compliant node, the TSB83AA23 PHY section provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY section contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB83AA23 PHY section are designed to work with external 112-Ω termination resistor networks to match the 110-Ω cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel RC network, with recommended values of 5 kΩ and 270 pF. The values of the external line-termination resistors are selected to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

When the power supply of the TSB83AA23 is off while the twisted-pair cables are connected, the TSB83AA23 transmitter and receiver circuitry present to the cable a high-impedance signal that does not load the device at the other end of the cable.

When the TSB83AA23 PHY section is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the port must be forced to the IEEE Std 1394a-2000-only mode (data-strobe-only mode), after which the TPB+ and TPB– terminals can be tied together and then pulled to ground; or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS terminal can be connected through a 1-μF capacitor to ground or left unconnected.

The TESTM, TESTW, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM and TESTW terminals must be connected to V_{DD} through a 1-kΩ resistor. The SE and SM terminals must be tied to ground through a 1-kΩ resistor.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the TSB83AA23, this bit can be set only by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.

The LPS (link power status) terminal of the PHY section works with the LKON terminal to manage the power usage in the node. The PHY_LPS signal from the LLC section is used with the LCtrl bit (see Section 1.3.5) to indicate the active/power status of the LLC section. The LPS signal also resets, disables, and initializes the PHY section-LLC section interface (the state of the PHY section-LLC section interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit). The LPS terminal of the PHY section must be connected to the PHY_LPS terminal of the LLC section during normal operation.

The LPS input is considered inactive if it remains low for more than the LPS_RESET time (see the LPS terminal definition) and is considered active otherwise. When the PHY section detects that the LPS input is inactive, the PHY section-LLC section interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS_DISABLE time (see the LPS terminal definition), the PHY section-LLC section interface is put into a low-power disabled state in which the PCLK output is also held inactive. The TSB83AA23 continues the necessary PHY repeater functions required for normal network operation, regardless of the state of the PHY section-LLC section interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY section initializes the interface and returns to normal operation. The PHY section-LLC section interface is also held in the disabled state during hardware reset. When the LPS terminal is returned to an active state after being sensed as having entered the LPS_DISABLE time, the TSB83AA23 issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY section and LLC section now being accessible).

The PHY section uses the LKON terminal to notify the LLC section to power up and become active. When activated, the output LKON signal is a square wave. The PHY section activates the LKON output when the LLC section is inactive and a wake-up event occurs. The LLC section is considered inactive when either the LPS input is inactive, as previously described, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY section deasserts the LKON output when the LLC section becomes active (both LPS sensed as active and the LCtrl bit set to 1). The PHY section also deasserts the LKON output when a bus reset occurs, unless a PHY interrupt condition exists, which would otherwise cause LKON to be active. If the TSB83AA23 is power cycled and the power class is 0 through 4, the PHY section asserts LKON for approximately 167 μs or until both the LPS is active and the LCtrl bit is 1.

1.3 Terminal Assignments

1.3.1 Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	PCI_AD17	PCI_AD18	PCI_AD21	PCI_AD22	PCI_AD23	PCI_AD24	PCI_AD27	PCI_AD28	PCI_AD30	PCI_PME	PCI_CLK	PC2	PCI_RST	PCI_INTA
13	PCI_AD16	PCI_AD19	PCI_AD20	PCI_IDSEL	PCI_C/BE3	PCI_AD25	PCI_AD26	PCI_AD29	PCI_AD31	PCI_REQ	PCI_GNT	PC1	SDA	TPA2+
12	PCI_FRAME	PCI_C/BE2	PINT	PHY_PINT	CNA	PD	TESTM	RESET	BMODE	TESTW (VREG_PD)	PC0	G_RST	SCL	TPA2-
11	PCI_DEVSEL	PCI_IRDY	LPS									MFUNC	REG_EN	TPB2+
10	PCI_STOP	PCI_TRDY	PHY_LPS		DVDD_3.3	DVDD_CORE	VCCP	REG18	GND	AVDD_3.3		TPBIAS2	GND	TPB2-
09	PCI_PERR	LKON/DS2	PHY_LINKON		VCC	GND	GND	GND	GND	AVDD_3.3		TPBIAS1	GND	TPA1+
08	PCI_SERR	LREQ	PHY_LREQ		VCC	GND	GND	GND	GND	VCC		TPBIAS0	GND	TPA1-
07	PCI_C/BE1	PCLK	PHY_PCLK		VCC	GND	GND	GND	GND	VCC		PHY_CTL0 -CTL0	GND	TPB1+
06	PCI_PAR	LCLK	PHY_LCLK		DVDD_3.3	GND	GND	GND	VCC	AVDD_3.3		PHY_CTL1 -CTL1	GND	TPB1-
05	PCI_AD15	PCI_AD14	PCI_C/BE0			DVDD_CORE	REG18	VCCP	VCC	AVDD_3.3		PHY_D0-D0	GND	TPA0+
04	PCI_AD12	PCI_AD13	PCI_ACK64									PHY_D1-D1	GND	TPA0-
03	PCI_AD11	PCI_AD6	PCI_AD5	PCI_AD4	PCI_REQ64	PLLVDD_CORE	PLLVDD_3.3	CPS	GND	GND	PHY_D7-D7	PHY_D2-D2	GND	TPB0+
02	PCI_AD10	PCI_AD7	PCI_AD2	PCI_AD3	AVDD_3.3	PLLGND	DS1	DS0	SE	GND	PHY_D6-D6	PHY_D3-D3	GND	TPB0-
01	PCI_AD9	PCI_AD8	PCI_AD1	PCI_AD0	R1	R0	RSVD (XO)	XI	SM	GND	PHY_D5-D5	PHY_D4-D4	GND	GND

1.3.2 Bottom View

	01	02	03	04	05	06	07	08	09	10	11	12	13	14
P	GND	TPB0-	TPB0+	TPA0-	TPA0+	TPB1-	TPB1+	TPA1-	TPA1+	TPB2-	TPB2+	TPA2-	TPA2+	PCI_INTA
N	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	REG_EN	SCL	SDA	PCI_RST
M	PHY_D4-D4	PHY_D3-D3	PHY_D2-D2	PHY_D1-D1	PHY_D0-D0	PHY_CTL1 -CTL1	PHY_CTL0 -CTL0	TPBIAS0	TPBIAS1	TPBIAS2	MFUNC	G_RST	PC1	PC2
L	PHY_D5-D5	PHY_D6-D6	PHY_D7-D7									PC0	PCI_GNT	PCI_CLK
K	GND	GND	GND		AVDD_3.3	AVDD_3.3	VCC	VCC	AVDD_3.3	AVDD_3.3		TESTW (VREG_PD)	PCI_REQ	PCI_PME
J	SM	SE	GND		VCC	VCC	GND	GND	GND	GND		BMODE	PCI_AD31	PCI_AD30
H	XI	DS0	CPS		VCCP	GND	GND	GND	GND	REG18		RESET	PCI_AD29	PCI_AD28
G	RSVD (XO)	DS1	PLLVDD_3.3		REG18	GND	GND	GND	GND	VCCP		TESTM	PCI_AD26	PCI_AD27
F	R0	PLLGND	PLLVDD_ CORE		DVDD_ CORE	GND	GND	GND	GND	DVDD_ CORE		PD	PCI_AD25	PCI_AD24
E	R1	AVDD_3.3	PCI_ REQ64			DVDD_3.3	VCC	VCC	VCC	DVDD_3.3		CNA	PCI_C/BE3	PCI_AD23
D	PCI_AD0	PCI_AD3	PCI_AD4									PHY_PINT	PCI_IDSEL	PCI_AD22
C	PCI_AD1	PCI_AD2	PCI_AD5	PCI_ACK64	PCI_C/BE0	PHY_LCLK	PHY_PCLK	PHY_LREQ	PHY_LINKON	PHY_LPS	LPS	PINT	PCI_AD20	PCI_AD21
B	PCI_AD8	PCI_AD7	PCI_AD6	PCI_AD13	PCI_AD14	LCLK	PCLK	LREQ	LKON/DS2	PCI_TRDY	PCI_IRDY	PCI_C/BE2	PCI_AD19	PCI_AD18
A	PCI_AD9	PCI_AD10	PCI_AD11	PCI_AD12	PCI_AD15	PCI_PAR	PCI_C/BE1	PCI_SERR	PCI_PERR	PCI_STOP	PCI_ DEVSEL	PCI_ FRAME	PCI_AD16	PCI_AD17

1.3.3 Signals Sorted by Terminal Number

Terminal Number	Signal Name	Terminal Number	Signal Name	Terminal Number	Signal Name	Terminal Number	Signal Name
A01	PCI_AD9	D01	PCI_AD0	H02	DS0	M02	PHY_D3-D3
A02	PCI_AD10	D02	PCI_AD3	H03	CPS	M03	PHY_D2-D2
A03	PCI_AD11	D03	PCI_AD4	H05	VCCP	M04	PHY_D1-D1
A04	PCI_AD12	D12	PHY_PINT	H06	GND	M05	PHY_D0-D0
A05	PCI_AD15	D13	PCI_IDSEL	H07	GND	M06	PHY_CTL1-CTL1
A06	PCI_PAR	D14	PCI_AD22	H08	GND	M07	PHY_CTL0-CTL0
A07	PCI_C/$\overline{BE1}$	E01	R1	H09	GND	M08	TPBIAS0
A08	$\overline{PCI\_SERR}$	E02	AVDD_3.3	H10	REG18	M09	TPBIAS1
A09	$\overline{PCI\_PERR}$	E03	$\overline{PCI\_REQ64}$	H12	$\overline{RESET}$	M10	TPBIAS2
A10	$\overline{PCI\_STOP}$	E06	DVDD_3.3	H13	PCI_AD29	M11	MFUNC
A11	$\overline{PCI\_DEVSEL}$	E07	VCC	H14	PCI_AD28	M12	$\overline{G\_RST}$
A12	$\overline{PCI\_FRAME}$	E08	VCC	J01	SM	M13	PC1
A13	PCI_AD16	E09	VCC	J02	SE	M14	PC2
A14	PCI_AD17	E10	DVDD_3.3	J03	GND	N01	GND
B01	PCI_AD8	E12	CNA	J05	VCC	N02	GND
B02	PCI_AD7	E13	PCI_C/$\overline{BE3}$	J06	VCC	N03	GND
B03	PCI_AD6	E14	PCI_AD23	J07	GND	N04	GND
B04	PCI_AD13	F01	R0	J08	GND	N05	GND
B05	PCI_AD14	F02	PLLGND	J09	GND	N06	GND
B06	LCLK	F03	PLLVDD_CORE	J10	GND	N07	GND
B07	PCLK	F05	DVDD_CORE	J12	BMODE	N08	GND
B08	LREQ	F06	GND	J13	PCI_AD31	N09	GND
B09	LKON/DS2	F07	GND	J14	PCI_AD30	N10	GND
B10	$\overline{PCI\_TRDY}$	F08	GND	K01	GND	N11	$\overline{REG\_EN}$
B11	$\overline{PCI\_IRDY}$	F09	GND	K02	GND	N12	SCL
B12	PCI_C/$\overline{BE2}$	F10	DVDD_CORE	K03	GND	N13	SDA
B13	PCI_AD19	F12	PD	K05	AVDD_3.3	N14	$\overline{PCI\_RST}$
B14	PCI_AD18	F13	PCI_AD25	K06	AVDD_3.3	P01	GND
C01	PCI_AD1	F14	PCI_AD24	K07	VCC	P02	TPB0–
C02	PCI_AD2	G01	RSVD (X0)	K08	VCC	P03	TPB0+
C03	PCI_AD5	G02	DS1	K09	AVDD_3.3	P04	TPA0–
C04	$\overline{PCI\_ACK64}$	G03	PLLVDD_3.3	K10	AVDD_3.3	P05	TPA0+
C05	PCI_C/$\overline{BE0}$	G05	REG18	K12	TESTW (VREG_PD)	P06	TPB1–
C06	PHY_LCLK	G06	GND	K13	$\overline{PCI\_REQ}$	P07	TPB1+
C07	PHY_PCLK	G07	GND	K14	$\overline{PCI\_PME}$	P08	TPA1–
C08	PHY_LREQ	G08	GND	L01	PHY_D5-D5	P09	TPA1+
C09	PHY_LINKON	G09	GND	L02	PHY_D6-D6	P10	TPB2–
C10	PHY_LPS	G10	VCCP	L03	PHY_D7-D7	P11	TPB2+
C11	LPS	G12	TESTM	L12	PC0	P12	TPA2–
C12	PINT	G13	PCI_AD26	L13	$\overline{PCI\_GNT}$	P13	TPA2+
C13	PCI_AD20	G14	PCI_AD27	L14	PCI_CLK	P14	$\overline{PCI\_INTA}$
C14	PCI_AD21	H01	XI	M01	PHY_D4-D4		

1.3.4 Signals Sorted by Name

Signal Name	Terminal Number	Signal Name	Terminal Number	Signal Name	Terminal Number	Signal Name	Terminal Number
AVDD_3.3	E02, K05, K06, K09, K10	N.C.	H11, J04, J11, K04, K11, L04, L05, L06, L07, L08 L09, L10, L11	PCI_AD29	H13	PHY_PINT	D12
				PCI_AD30	J14	PINT	C12
				PCI_AD31	J13	PLLGND	F02
BMODE	J12			PCI_C/$\overline{BE0}$	C05	PLLVDD_3.3	G03
CNA	E12			PCI_C/$\overline{BE1}$	A07	PLLVDD_ CORE	F03
CPS	H03			PCI_C/$\overline{BE2}$	B12	R0	F01
DS0	H02			PCI_C/$\overline{BE3}$	E13	R1	E01
DS1	G02	PC0	L12	PCI_CLK	L14	REG18	G05, H10
DVDD_3.3	E06, E10	PC1	M13	$\overline{PCI\_DEVSEL}$	A11	$\overline{REG\_EN}$	N11
DVDD_CORE	F05, F10	PC2	M14	$\overline{PCI\_FRAME}$	A12	$\overline{RESET}$	H12
$\overline{G\_RST}$	M12	$\overline{PCI\_ACK64}$	C04	$\overline{PCI\_GNT}$	L13	SCL	N12
GND	F06, F07, F08, F09, G06, G07, G08, G09, H06, H07, H08, H09, J03, J07, J08, J09, J10, K01, K02, K03, N01, N02, N03, N04, N05, N06, N07, N08, N09, N10, P01	PCI_AD0	D01	PCI_IDSEL	D13	SDA	N13
		PCI_AD1	C01	$\overline{PCI\_INTA}$	P14	SE	J02
		PCI_AD2	C02	$\overline{PCI\_IRDY}$	B11	SM	J01
		PCI_AD3	D02	PCI_PAR	A06	TESTM	G12
		PCI_AD4	D03	$\overline{PCI\_PERR}$	A09	TESTW (VREG_PD)	K12
		PCI_AD5	C03	$\overline{PCI\_PME}$	K14	TPA0–	P04
		PCI_AD6	B03	$\overline{PCI\_REQ}$	K13	TPA0+	P05
		PCI_AD7	B02	$\overline{PCI\_REQ64}$	E03	TPA1–	P08
		PCI_AD8	B01	$\overline{PCI\_RST}$	N14	TPA1+	P09
		PCI_AD9	A01	$\overline{PCI\_SERR}$	A08	TPA2–	P12
		PCI_AD10	A02	$\overline{PCI\_STOP}$	A10	TPA2+	P13
		PCI_AD11	A03	$\overline{PCI\_TRDY}$	B10	TPB0–	P02
		PCI_AD12	A04	PCLK	B07	TPB0+	P03
		PCI_AD13	B04	PD	F12	TPB1–	P06
		PCI_AD14	B05	PHY_CTL0-CTL0	M07	TPB1+	P07
		PCI_AD15	A05	PHY_CTL1-CTL1	M06	TPB2–	P10
LCKL	B06	PCI_AD16	A13	PHY_D0-D0	M05	TPB2+	P11
LKON/DS2	B09	PCI_AD17	A14	PHY_D1-D1	M04	TPBIAS0	M08
LPS	C11	PCI_AD18	B14	PHY_D2-D2	M03	TPBIAS1	M09
LREQ	B08	PC1_AD19	B13	PHY_D3-D3	M02	TPBIAS2	M10
MFUNC	M11	PCI_AD20	C13	PHY_D4-D4	M01	VCC	E07, E08, E09, J05, J06, K07, K08
N.C.	D04, D05, D06, D07, D08, D09, D10, D11, E04, E05, E11, F04, F11, G04, G11, H04,	PCI_AD21	C14	PHY_D5-D5	L01		
		PCI_AD22	D14	PHY_D6-D6	L02		
		PCI_AD23	E14	PHY_D7-D7	L03		
		PCI_AD24	F14	PHY_LCLK	C06	VCCP	G10, H05
		PCI_AD25	F13	PHY_LINKON	C09	XI	H01
		PCI_AD26	G13	PHY_LPS	C10	RSVD (XO)	G01
		PCI_AD27	G14	PHY_LREQ	C08		
		PCI_AD28	H14	PHY_PCLK	C07		

1.3.5 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Power Supply			
AVDD_3.3	E02, K05, K06, K09, K10		Analog circuit power. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1-µF and 0.001-µF. Lower-frequency 10-µF filtering capacitors also are recommended. These supply terminals are separated from the other power terminals internal to the device to provide noise isolation. The PLLVDD_3.3, AVDD_3.3, and DVDD_3.3 terminals must be tied together with a low-dc-impedance connection on the circuit board.
DVDD_CORE	F05, F10		Digital 1.95-V circuit power. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1-µF and 0.001-µF. An additional 1-µF capacitor is required for voltage regulation. These supply terminals are separated from the other power terminals internal to the device to provide noise isolation.
DVDD_3.3	E06, E10		Digital 3.3-V circuit power. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1-µF and 0.001-µF. Lower-frequency 10-µF filtering capacitors also are recommended. The DVDD_3.3 terminals must be tied together at a low-impedance point on the circuit board. These supply terminals are separated from the other power terminals internal to the device to provide noise isolation. The PLLVDD_3.3, AVDD_3.3, and DVDD_3.3 terminals must be tied together with a low-dc-impedance connection on the circuit board.
GND	F06, F07, F08, F09, G06, G07, G08, G09, H06, H07, H08, H09, J03, J07, J08, J09, J10, K01, K02, K03, N01, N02, N03, N04, N05, N06, N07, N08, N09, N10, P01		Ground. These terminals must be tied together to the low-impedance circuit-board ground plane.
PLLGND	F02		PLL circuit ground. These terminals must be tied together to the low-impedance circuit-board ground plane.
PLLVDD_CORE	F03		PLL 1.95-V circuit power. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1-µF and 0.001-µF. An additional 1-µF capacitor is required for voltage regulation, and the PLLVDD_CORE terminals must be separate from the DVDD_CORE terminals. These supply terminals are separated from the other power terminals internal to the device to provide noise isolation.
PLLVDD_3.3	G03		PLL 3.3-V circuit power. A combination of high-frequency decoupling capacitors near the terminal is suggested, such as paralleled 0.1-µF and 0.001-µF. Lower-frequency 10-µF filtering capacitors also are recommended. This supply terminal is separated from the other power terminals internal to the device to provide noise isolation. The DVDD_3.3 terminals must be tied together at a low-impedance point on the circuit board. The PLLVDD_3.3, AVDD_3.3, and DVDD_3.3 terminals must be tied together with a low-dc-impedance connection.
REG18	G05, H10		The REG18 terminals are connected to the internal 1.8-V LLC-section core voltage. They provide local bypass for the internal core voltage or to provide 1.8 V to the core externally if the internal regulator is disabled.
$\overline{\text{REG\_EN}}$	N11	I	Regulator enable. When this terminal is low, the internal 1.8-V regulator is enabled and generates the 1.8-V internal core voltage from the 3.3-V supply voltage. If it is disabled by pulling the terminal high through a 10-kΩ or smaller resistor, 1.8 V must be provided to the REG18 terminals for normal operation.
VCC	E07, E08, E09, J05, J06, K07, K08		3.3-V power supply. A parallel combination of high-frequency decoupling capacitors near each terminal is suggested, such as 0.1-µF and 0.001-µF. Lower-frequency 10-µF filtering capacitors also are recommended. They must be tied to a low-impedance point on the circuit board.
VCCP	G10, H05	I	PCI signaling clamp voltage power. PCI signals are clamped to this power rail per the *PCI Local Bus Specification*. In addition, if a 5-V ROM is used, the VCCP terminal must be connected to 5 V.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PHY Section-LLC Section Interface			
BMODE	J12	I	Beta-mode. This terminal determines the PHY section-LLC section interface connection protocol. When this terminal is a logic high (asserted), the PHY section-LLC section interface complies with the IEEE Std 1394b-2002 revision 1.33 Beta interface. When a logic low (deasserted), the PHY section-LLC section interface complies with the legacy IEEE Std 1394a-2000. This terminal must be pulled high with a 1-kΩ resistor during normal (Beta mode) operation.
PHY_CTL1-CTL1 PHY_CTL0-CTL0	M06 M07	I/O	Control I/Os. These bidirectional control bus signals indicate the phase of operation of the PHY section-LLC section interface. On a reset of the interface, this bus is driven by the PHY section. When driven by the PHY section, information on PHY_CTL0 and PHY_CTL1 is synchronous to PHY_PCLK. When driven by the LLC section, information on PHY_CTL0 and PHY_CTL1 is synchronous to PHY_LCLK. These terminals are connected internally in the TSB83AA23 and should be left unconnected on the board.
PHY_D7-D7 PHY_D6-D6 PHY_D5-D5 PHY_D4-D4 PHY_D3-D3 PHY_D2-D2 PHY_D1-D1 PHY_D0-D0	L03 L02 L01 M01 M02 M03 M04 M05	I/O	Data I/Os. These bidirectional data bus signals carry 1394 packet data, packet speed, and grant-type information between the PHY section and the LLC section. On a reset of the interface, this bus is driven by the PHY section. When driven by the PHY section, information on PHY_D7 through PHY_D0 is synchronous to PHY_PCLK. When driven by the LLC section, information on PHY_D7 through PHY_D0 is synchronous to PHY_LCLK. These terminals are connected internally in the TSB83AA23 and should be left unconnected on your board.
LCLK	B06	I	LLC-section clock. 98.304-MHz clock signal to synchronize data transfers from the link layer to the PHY when the PHY section-LLC section interface is in the IEEE Std 1394b-2002 mode. A bus holder is built into this terminal. This terminal must be connected to the PHY_LCLK output terminal of the LLC section.
PHY_LCLK	C06	O	LLC-section clock. PHY_LCLK is an output from the LLC section that is generated from the incoming PHY_PCLK signal. PHY_LCLK is frequency-locked to PHY_PCLK and synchronizes data and information generated by the LLC section. This terminal must be connected to the LCLK input terminal of the PHY section.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
LKON/DS2	B09	I/O	Link-on notification/Data-Strobe-only select. It is necessary to pull the terminal high through a 470-Ω or smaller resistor. This terminal also must be connected to the PHY_LINKON input terminal of the LLC section via a 1-kΩ series resistor. A bus holder is built into this terminal. At power up reset if DS2 is sampled, high port 2 operates in Data Strobe only mode. If DS2 is sampled low port 2 operates in bilingual mode. After hardware reset, this terminal is the link-on output, which notifies the LLC section or other power-up logic to power up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (eight PCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is in a high impedance state. The link-on output is activated if the LLC section is inactive (the LPS input inactive or the LCtrl bit cleared) and when any of the following occurs: a) The TSB83AA23 receives a link-on PHY packet addressed to this node. b) The PEI (port-event interrupt) register bit is 1. c) Any of the configuration-timeout interrupt (CTOI), cable-power-status interrupt (CPSI), or state-time-out interrupt (STOI) register bits are 1 and the resuming-port interrupt enable (RPIE) register bit also is 1. d) The PHY is power cycled and the power class is 0 through 4. Once activated, the link-on output is active until the LLC section becomes active (both the LPS input active and the LCtrl bit set). The PHY section also deasserts the link-on output when a bus reset occurs unless the link-on output is otherwise active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet) In the case of power cycling, the LKON signal must stop after 167 μs if the previous conditions have not been met. NOTE: If an interrupt condition exists, which otherwise causes the link-on output to be activated if the LLC section were inactive, the link-on output is activated when the LLC section subsequently becomes inactive. DS2 is the Data-strobe-only mode for port 2 1394a-2000-only programming terminal. On hardware reset, this terminal determines whether port 2 acts like an IEEE Std 1394b-2002 bilingual port (terminal at logic 0) or as an IEEE Std 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or smaller resistor (to enable IEEE Std 1394b-2002 bilingual mode) or high through a 10-kΩ or smaller resistor (to enable IEEE Std 1394a-2000-only mode). A bus holder is built into this terminal.
PHY_LINKON	C09	I/O	Link-on notification. PHY_LINKON is an input to the LLC section from the PHY section that is used to provide notification that a link-on packet has been received or an event, such as a port connection, has occurred. This input has meaning only when LPS is disabled. This includes the D0 (uninitialized), D2, and D3 power states. If PHY_LINKON becomes active in the D0 (uninitialized), D2, or D3 power state, the TSB83AA23 device sets bit 15 (PME_STS) in the power-management control and status register in the PCI configuration space at offset 48h (see Section 6.1.26, *Power Management Control and Status Register*). This terminal must be connected to the LKON/DS2 input/output terminal of the PHY section.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
LPS	C11	I	LLC-section power status. This terminal monitors the active/power status of the LLC section and controls the state of the PHY section-LLC section interface. This terminal must be connected to the PHY_LPS output of the LLC section, and must be pulled low with a 10-kΩ resistor during normal operation. The LPS input is considered inactive if it is sampled low by the PHY section for more than an LPS_RESET time (~2.6 μs), and is considered active otherwise (that is, asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 22 ns to be observed as high by the PHY section. When the PHY section detects that the LPS input is inactive, it places the PHY section-LLC section interface into a low-power reset state. In the reset state, the CTL (CTL0 and CTL1) and D (D0 to D7) outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than an LPS_DISABLE time (~26 μs), the PHY section-LLC section interface is put into a low-power disabled state in which the PCLK output also is held inactive. The PHY section-LLC section interface is placed into the disabled state on hardware reset. The LLC section state that is communicated in the self-ID packet is considered active only if both the LPS input is active and the LCtrl register bit is set to 1. The LLC-section state that is communicated in the self-ID packet is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0. This terminal must be connected to the PHY_LPS output of the LLC section, and must be pulled low with a 10-kΩ resistor during normal operation.
PHY_LPS	C10	O	LLC-section power status. PHY_LPS is an output from the LLC section that, when active, indicates that the LLC section is powered and capable of maintaining communications over the PHY section-LLC section interface. When this signal is inactive, it indicates that the LLC section is not powered or that the LLC section has not been initialized by software. This signal is active when bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) has been set by software according to the initialization as specified in the *1394 Open Host Controller Interface* specification. When active, the signal is nominally a 2-MHz pulse. This terminal must be connected to the LPS input of the PHY section.
LREQ	B08	I	LLC-section request. The LLC section uses this input to initiate a service request to the PHY section. This terminal must be connected to the PHY_LREQ output of the LLC section. A bus holder is built into this terminal
PHY_LREQ	C08	O	LLC-section request. PHY_LREQ is a serial output from the LLC section to the PHY section used to request packet transmissions, read and write PHY section registers, and to indicate the occurrence of certain link events that are relevant to the PHY section. Information encoded on PHY_LREQ is synchronous to PHY_LCLK. This terminal must be connected to the LREQ input of the PHY section.
PCLK	B07	O	PHY-section clock. Provides a 98.304-MHz clock signal, synchronized with data transfers, to the LLC when the PHY section-LLC section interface is operating in the IEEE Std 1394b-2002 mode (BMODE asserted). This terminal must be connected to the PHY_PCLK input of the LLC section.
PHY_PCLK	C07	I	PHY-section clock. PHY_PCLK is an input to the LLC section from the PHY section that, when active, provides a nominal 98.304-MHz clock with a 50/50 duty cycle or 40/60 duty cycle depending on port modes used). This terminal must be connected to the PCLK output of the PHY section.
PINT	C12	O	PHY-section interrupt. The PHY section uses this output to transfer status and interrupt information serially to the LLC section. This terminal must be connected to the PHY_PINT input of the LLC section. A bus holder is built into this terminal.
PHY_PINT	D12	I	PHY-section interrupt. PHY_PINT is a serial input to the LLC section from the PHY section that is used to transfer status, register, interrupt, and other information to the link. Information encoded on PHY_PINT is synchronous to PHY_PCLK. This terminal must be connected to the PINT output of the PHY section.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PHY Section Cable Interface			
CNA	E12	O	Cable not active. This terminal is asserted high when there are no ports receiving incoming bias voltage. When any port receives bias, this terminal goes low.
CPS	H03	I	Cable power status. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This transition from cable power sensed to cable power not sensed can be used to generate an interrupt.
DS0	H02	I	Data-strobe-only mode for port 0. IEEE Std 1394a-2000-only port-0-enable programming terminal. On hardware reset, this terminal allows the user to select whether port 0 acts like an IEEE Std 1394b-2002 bilingual port (terminal at logic 0) or as an IEEE Std 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or smaller resistor (to enable IEEE Std 1394b-2002 bilingual mode) or high through a 10-kΩ or smaller resistor (to enable IEEE Std 1394a-2000-only mode). A bus holder is built into this terminal.
DS1	G02	I	Data-strobe-only mode for port 1. IEEE Std 1394a-2000-only port-1-enable programming terminal. On hardware reset, this terminal allows the user to select whether port 1 acts like an IEEE Std 1394b-2002 bilingual port (terminal at logic 0) or as an IEEE Std 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or smaller resistor (to enable IEEE Std 1394b-2002 bilingual mode) or high through a 10-kΩ or smaller resistor (to enable IEEE Std 1394a-2000-only mode). A bus holder is built into this terminal.
PC0 PC1 PC2	L12 M13 M14	I	Power class programming. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high through a 1-kΩ or smaller resistor or by tying directly to ground through a 1-kΩ or smaller resistor. Bus holders are built into these terminals.
TPA0– TPA0+ TPB0– TPB0+	P04 P05 P02 P03	I/O	Port 0 twisted-pair differential signal. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA1– TPA1+ TPB1– TPB1+	P08 P09 P06 P07	I/O	Port 1 twisted-pair differential signal. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA2– TPA2+ TPB2– TPB2+	P12 P13 P10 P11	I/O	Port 2 twisted-pair differential signal. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector.
TPBIAS0 TPBIAS1 TPBIAS2	M08 M09 M10	O	Twisted-pair bias output. This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection in IEEE Std 1394a-2000 mode. Each of these terminals, except for an unused port, must be decoupled with a 1-µF capacitor to ground. For the unused port, this terminal can be left unconnected.
Reset, Clock, and Miscellaneous Terminals			
$\overline{\text{G\_RST}}$	M12	I	Global power reset. This reset brings all of the TSB83AA23 internal LLC-section registers to their default states, including those registers not reset by $\overline{\text{PCI\_RST}}$. When $\overline{\text{G\_RST}}$ is asserted, the LLC section is completely nonfunctional. Additionally, $\overline{\text{G\_RST}}$ must be asserted a minimum of 2 ms after both 3.3 V and 1.8 V are valid at the device. When implementing wake capabilities from the 1394 host controller, it is necessary to implement two resets to the TSB83AA23 device. $\overline{\text{G\_RST}}$ is designed to be a one-time power-on reset, and $\overline{\text{PCI\_RST}}$ must be connected to the PCI bus $\overline{\text{RST}}$.
MFUNC	M11	I/O	Multifunction. MFUNC is a multifunction terminal whose function is selected via the multifunction select register: **Bits 2–0** — **Function** 000 — General-purpose input/output (GPIO) 001 — CYCLEIN 010 — CYCLEOUT 011 — $\overline{\text{PCI\_CLKRUN}}$ 100–111 — Reserved

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{PCI\_RST}}$	N14	I	PCI reset. When this bus reset is asserted, the TSB83AA23 device places all LLC-section output buffers in a high-impedance state and resets all LLC-section internal registers except device power-management context and vendor-specific bits initialized by host power-on software. When $\overline{\text{PCI\_RST}}$ is asserted, the LLC section is completely nonfunctional. This terminal must be connected to PCI bus $\overline{\text{RST}}$.
PD	F12	I	Power down. A high on this terminal turns off all internal circuitry, except the cable-active monitor circuits that control the CNA output. Asserting PD high also activates an internal pulldown on the $\overline{\text{RESET}}$ terminal to force a reset of the internal control logic.
$\overline{\text{RESET}}$	H12	I	Logic reset. Asserting this terminal low resets the internal logic. An internal pullup resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation (see *Power-Up Reset*, Section 4.2). The $\overline{\text{RESET}}$ terminal also incorporates an internal pulldown which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and also can be driven by an open-drain type driver.
R0 R1	F01 E01		Current-setting resistor. These terminals are connected to a precision external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1% is required to meet IEEE Std 1394-1995 output voltage limits.
SCL	N12	I/O	Serial clock. This terminal provides the SCL serial clock signaling. ROM is implemented: Connect terminal 3 to the SCL terminal on the ROM; the 2.7-kΩ resistor pulls this signal to the ROM V_{CC}. (SDA is implemented as open drain.) ROM is not implemented. Connect terminal 3 to ground with a 220-Ω resistor.
SDA	N13	I/O	Serial data. This terminal provides the SDA serial data signaling. This terminal is sampled at $\overline{\text{G\_RST}}$ to determine if a serial ROM is implemented; thus if no ROM is implemented, then this terminal must be connected to ground. ROM is implemented: Connect terminal 4 to the SDA terminal on the ROM; the 2.7-kΩ resistor pulls this signal to the ROM V_{CC}. (SDA is implemented as open drain.) ROM is not implemented. Connect terminal 4 to ground with a 220-Ω resistor.
SE	J02	I	Test control. This input is used in the manufacturing test of the TSB83AA23. For normal use, this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
SM	J01	I	Test control. This input is used in the manufacturing test of the TSB83AA23. For normal use, this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
TESTM	G12	I	Test control. This input is used in the manufacturing test of the TSB83AA23. For normal use, this terminal must be pulled high through a 1-kΩ resistor to V_{DD}.
TESTW (VREG_PD)	K12	I	Test control. This input is used in the manufacturing test of the TSB83AA23. For normal use, this terminal must be pulled high through a 1-kΩ resistor to V_{DD}.
XI	H01	I	Oscillator input. This terminal connects to a 98.304-MHz low-jitter external oscillator. XI is a 1.8-V CMOS input. Oscillator jitter must be 5-ps RMS or better. If only 3.3-V oscillators can be acquired, great care must be taken to not introduce significant jitter by the means used to level shift from 3.3 V to 1.8 V. If a resistor divider is used, a high-current oscillator and low-value resistors must be used to minimize RC time constants.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
32-Bit PCI Bus Interface			
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0	J13 J14 H13 H14 G14 G13 F13 F14 E14 D14 C14 C13 B13 B14 A14 A13 A05 B05 B04 A04 A03 A02 A01 B01 B02 B03 C03 D03 D02 C02 C01 D01	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data on the PCI interface. During the address phase of a PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
PCI_C/$\overline{\text{BE0}}$ PCI_C/$\overline{\text{BE1}}$ PCI_C/$\overline{\text{BE2}}$ PCI_C/$\overline{\text{BE3}}$	C05 A07 B12 E13	I/O	PCI bus commands and byte enables. The command and byte enable signals are multiplexed on the same PCI terminals. During the address phase of a bus cycle, PCI_C/$\overline{\text{BE3}}$–PCI_C/$\overline{\text{BE0}}$ define the bus command. During the data phase, this 4-bit bus is used as a byte enable.
PCI_CLK	L14	I	PCI bus clock. Provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCI_CLK.
$\overline{\text{PCI\_DEVSEL}}$	A11	I/O	PCI device select. The TSB83AA23 device asserts this signal to claim a PCI cycle as the target device. As a PCI initiator, the TSB83AA23 device monitors this signal until a target responds. If no target responds before time-out occurs, the TSB83AA23 device terminates the cycle with an initiator abort.
$\overline{\text{PCI\_FRAME}}$	A12	I/O	PCI cycle frame. This signal is driven by the initiator of a PCI bus cycle. $\overline{\text{PCI\_FRAME}}$ is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When $\overline{\text{PCI\_FRAME}}$ is deasserted, the PCI bus transaction is in the final data phase.
$\overline{\text{PCI\_GNT}}$	L13	I	PCI bus grant. This signal is driven by the PCI bus arbiter to grant the TSB83AA23 device access to the PCI bus after the current data transaction has completed. This signal may or may not follow a PCI bus request, depending on the PCI bus parking algorithm.
PCI_IDSEL	D13	I	PCI initialization device select. PCI_IDSEL selects the TSB83AA23 device during configuration space accesses. PCI_IDSEL can be connected to one of the upper 24 PCI address lines on the PCI bus.
$\overline{\text{PCI\_INTA}}$	P14	O	PCI interrupt. This output indicates interrupts from the TSB83AA23 device to the host. This terminal is implemented as open drain.
$\overline{\text{PCI\_IRDY}}$	B11	I/O	PCI initiator ready. $\overline{\text{PCI\_IRDY}}$ indicates the ability of the PCI bus initiator to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCI_CLK where both $\overline{\text{PCI\_IRDY}}$ and $\overline{\text{PCI\_TRDY}}$ are asserted.
PCI_PAR	A06	I/O	PCI parity. In all PCI bus read and write cycles, the TSB83AA23 device calculates even parity across the PCI_AD31–PCI_AD0 and PCI_C/$\overline{\text{BE0}}$–PCI_C/$\overline{\text{BE3}}$ buses. As an initiator during PCI cycles, the TSB83AA23 device outputs this parity indicator with a one-PCI_CLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator parity indicator; a miscompare can result in a parity error assertion ($\overline{\text{PCI\_PERR}}$).

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PCI_PERR	A09	I/O	PCI parity error indicator. This signal is driven by a PCI device to indicate that calculated parity does not match PCI_PAR and/or PCI_PAR64 when PERR_ENB (bit 6) is set to 1 in the command register at offset 04h in the PCI configuration space (see Section 6.1.3, *Command Register*).
PCI_PME	K14	O	This terminal indicates wake events to the host. It is an open-drain signal that is asserted when PME_STS is asserted and bit 8 (PME_ENB) in the PCI power management control and status register at offset 48h in the PCI configuration space (see Section 6.1.26, *Power Management Control and Status Register*) has been set. Bit 15 (PME_STS) in the PCI power management control and status register is set due to any unmasked interrupt in the D0 (active) or D1 power state, and on a PHY_LINKON indication in the D2, D3, or D0 (uninitialized) power state.
PCI_REQ	K13	O	PCI bus request. Asserted by the TSB83AA23 device to request access to the bus as an initiator. The host arbiter asserts PCI_GNT when the TSB83AA23 device has been granted access to the bus.
PCI_SERR	A08	O	PCI system error. When SERR_ENB (bit 8) in the command register at offset 04h in the PCI configuration space (see Section 6.1.3, *Command Register*) is set to 1, the output is pulsed, indicating an address parity error has occurred. The TSB83AA23 device need not be the target of the PCI cycle to assert this signal. This terminal is implemented as open drain.
PCI_STOP	A10	I/O	PCI cycle stop. This signal is driven by a PCI target to request the initiator to stop the current PCI bus transaction. This signal is used for target disconnects, and is commonly asserted by target devices that do not support burst data transfers.
PCI_TRDY	B10	I/O	PCI target ready. PCI_TRDY indicates the ability of the PCI bus target to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCI_CLK where both PCI_IRDY and PCI_TRDY are asserted.
PCI_ACK64	C04	I	PCI bus 64-bit transfer acknowledge. This terminal should be pulled high to V_{DD} through a 4.7-kΩ resistor.
PCI_REQ64	E03	I	PCI bus request for 64-bit transfer. This terminal should be pulled high to V_{DD} through a 4.7-kΩ resistor.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings(1)

over operating temperature ranges (unless otherwise noted)

			MIN	MAX	UNIT
V_{SUP}	Supply voltage range (3.3-V supplies)(2)	AVDD_3.3, DVDD_3.3, PLLVDD_3.3, VCC	–0.3	3.6	V
V_{CCP}	Supply voltage range		–0.5	5.5	V
V_I	Input voltage range(2)		–0.5	V_{SUP} + 0.5	V
V_I	Input voltage range for PCI		–0.5	V_{CCP} + 0.5	mA
V_O	Output voltage range at any output		–0.5	V_{SUP} + 0.5	mA
T_A	Operating free-air temperature range		0	70	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground.

2.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM(1)	MAX	UNIT
V_{SUP}	Supply voltage, 3.3-V	Source power node	3	3.3	3.6	V
		Nonsource power node	3(2)	3.3	3.6	
V_{DD}	Supply voltage, core		1.85	1.95	2.05	V
V_{CCP}	PCI I/O clamping voltage	3.3-V operation	3	3.3	3.6	V
		5-V operation	4.5	5	5.5	
V_{IH}	High-level input voltage	LREQ, CTL0, CTL1, D0–D7, LCLK	2.6		3.6	V
		LKON, PC0, PC1, PC2, PD, BMODE	0.7 V_{SUP}			
		$\overline{\text{RESET}}$	0.6 V_{SUP}			
		PCI interface, 3.3 V(3)	0.475 V_{CCP}		V_{CCP}	
		PCI interface, 5 V(3)	2		V_{CCP}	
		PHY_PINT, PHY_CTL0, PHY_CTL1, PHY_D0–PHY_D7, PHY_PCLK(3)	2		3.6	
V_{IL}	Low-level input voltage	LREQ, CTL0, CTL1, D0–D7, LCLK			1.2	V
		LKON, PC0, PC1, PC2, PD, BMODE			0.2 V_{SUP}	
		$\overline{\text{RESET}}$			0.3 V_{SUP}	
		PCI interface, 3.3 V(3)	0		0.325 V_{CCP}	
		PCI interface, 5 V(3)	0		0.8	
		PHY_PINT, PHY_CTL0, PHY_CTL1, PHY_D0–PHY_D7, PHY_PCLK(3)	0		0.8	
$I_{OL/OH}$	Output current	CTL0, CTL1, D0–D7, CNA, LKON, PINT, PCLK	–4		4	mA
I_O	Output current	TPBIAS outputs	–5.6		1.3	mA
T_J	Maximum junction temperature (see $R_{\theta JA}$ values listed in thermal characteristics table)	$R_{\theta JA}$ = 63.9°C/W, PHY section, T_A = 70°C			102.6	°C
		$R_{\theta JA}$ = 51.6°C/W, LLC section, T_A = 70°C			96.5	

(1) All nominal values are at V_{DD} = 3.3 V and T_A = 25°C.
(2) For a node that does not source power; see Section 4.2.2.2 in IEEE Std 1394a-2000.
(3) Applies to external inputs and bidirectional buffers without hysteresis

Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM(1)	MAX	UNIT
T_A	Operating ambient temperature			0	25	70	°C
V_{ID}	1394b differential input voltage	Cable inputs, during data reception		200		800	mV
	1394a differential input voltage	Cable inputs	During data reception	118		260	
			During arbitration	168		265	
V_{IC}	1394a common-mode input voltage	TPB cable inputs	Source power node	0.4706		2.515	V
			Nonsource power node	0.4706		2.015(2)	
t_{pu}	Power-up reset time	$\overline{\text{RESET}}$ input		2(4)			ms
V_I	PCI input voltage	PCI interface, 3.3 V		0		V_{CCP}	V
V_O	PCI output voltage(5)	PCI interface, 3.3 V		0		V_{CCP}	V
t_t	Input transition time (t_r and t_f)	PCI interface		0		6	ns
	1394a receive input jitter	TPA, TPB cable inputs	S100 operation			±1.08	ns
			S200 operation			±0.5	
			S400 operation			±0.315	
	1394a receive input skew	Between TPA and TPB cable inputs	S100 operation			±0.8	ns
			S200 operation			±0.55	
			S400 operation			±0.5	

(4) Time after valid clock received at PHY XI input terminal
(5) Applies to external output buffers

2.3 Electrical Characteristics, PHY Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	1394a differential output voltage	56 Ω, See Figure 2-1	172		265	mV
	1394b differential output voltage			700		
I_{DIFF}	Driver difference current (TPA+, TPA–, TPB+, TPB–)	Drivers enabled, Speed signaling off	–1.05 (1)		1.05 (1)	mA
I_{SP200}	Common-mode speed signaling current (TPB+, TPB–)	S200 speed signaling enabled	–4.84 (2)		–2.53 (2)	mA
I_{SP400}	Common-mode speed signaling current (TPB+, TPB–)	S400 speed signaling enabled	–12.4 (2)		–8.1 (2)	mA
V_{OFF}	Off-state differential voltage	Drivers disabled, See Figure 2-1			20	mV
V_{CM}	1394b common-mode voltage			1.5		V

(1) Limits are defined as the algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
(2) Limits are defined as the absolute limit of each of TPB+ and TPB– driver currents.

2.4 Electrical Characteristics, PHY Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30		30	mV
$V_{TH–CB}$	Cable bias detect threshold, TPBx cable inputs	Drivers disabled	0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
$V_{TH–}$	Negative arbitration comparator threshold voltage	Drivers disabled	–168		–89	mV
$V_{TH–SP200}$	Speed signal threshold	TPBIAS–TPA common-mode voltage, Drivers disabled	49		131	mV
$V_{TH–SP400}$			314		396	

2.5 Electrical Characteristics, General

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	3.3 V_{DD} (1)			91	120	mA
		Core V_{DD} (1)			68	75	
V_{TH}	Power status threshold, CPS input (2)		400-kΩ resistor (2)	4.7		7.5	V
V_{OH}	High-level output voltage	CTL0, CTL1, D0–D7, CNA, LKON, PCLK outputs	V_{DD} = 3 V to 3.6 V, I_{OH} = –4 mA	2.8			
		PHY_CTL0, PHY_CTL1, PHY_D0–PHY_D7, PHY_LINKON, PHY_LCLK, PHY_LPS	I_{OH} = –4 mA	2.8			
			I_{OH} = –8 mA	V_{CC} – 0.6			
		PCI interface	I_{OH} = –0.5 mA	0.9 V_{CC}			
			I_{OH} = –2 mA	2.4			
V_{OL}	Low-level output voltage	CTL0, CTL1, D0–D7, CNA, LKON, PCLK outputs	I_{OL} = 4 mA			0.4	V
		PHY_CTL0, PHY_CTL1, PHY_D0–PHY_D7, PHY_LINKON, PHY_LCLK, PHY_LPS	I_{OL} = 8 mA			0.5	
		PCI interface	I_{OL} = 1.5 mA			0.1 V_{CC}	
			I_{OL} = 6 mA			0.55	
		$\overline{PCI\_PME}$	I_{OL} = 4 mA			0.5	
I_{BH+}	Positive peak bus holder current (D0–D7, CTL0–CTL1, LREQ)		V_{DD} = 3.6 V, V_I = 0 V to V_{DD}	0.05		1	mA
$I_{BH–}$	Negative peak bus holder current (D0–D7, CTL0–CTL1, LREQ)		V_{DD} = 3.6 V, V_I = 0 V to V_{DD}	–1		–0.05	mA
I_{OZ}	Off-state output current	CTL0, CTL1, D0–D7, LKON I/Os	V_O = V_{DD} or 0 V			±5	µA
		LLC portion outputs	V_O = V_{DD} or 0 V			±20	
I_{IRST}	Pullup current ($\overline{RESET}$ input)		V_I = 1.5 V or 0 V	–90		–20	µA
V_O	TPBIAS output voltage		At rated I_O current	1.665		2.015	V

(1) Repeat max packet (one port receiving maximum-size isochronous packet—8192 bytes, sent on every isochronous interval, S800, data value of 0xCCCC CCCC; three ports repeating; all ports with beta-mode connection), $V_{DD3.3}$ = 3.3 V, V_{DDCORE} = 1.95 V, T_A = 25°C
(2) Measured at cable power side of resistor

2.6 Thermal Characteristics

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	PHY section: Two-signal, two-plane JEDEC board	63.9	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		39.3	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance	LLC section: Two-signal, two-plane JEDEC board	51.6	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		27.1	°C/W

2.7 Switching Characteristics for PHY Portion

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	TP differential rise time, transmit	10% to 90% at 1394 connector	0.5	1.2	ns
t_f	TP differential fall time, transmit	90% to 10% at 1394 connector	0.5	1.2	ns
t_{su}	Setup time, CTL0, CTL1, D1–D7, LREQ until PCLK—1394a-2000	50% to 50%, See Figure 2-2	2.5		ns
t_h	Hold time, CTL0, CTL1, D1–D7, LREQ after PCLK—1394a-2000	50% to 50%, See Figure 2-2	0		ns
t_{su}	Setup time, CTL0, CTL1, D1–D7, LREQ until LCLK—1394b	50% to 50%, See Figure 2-2	2.5		ns
t_h	Hold time, CTL0, CTL1, D1–D7, LREQ after LCLK—1394b	50% to 50%, See Figure 2-2	1		ns
t_d	Delay time, PCLK until CTL0, CTL1, D1–D7, PINT	50% to 50%, See Figure 2-3	0.5	7	ns

2.8 Switching Characteristics for PCI Interface

PARAMETER		MIN	MAX	UNIT
t_{su}	Setup time before PCI_CLK	7		ns
t_h	Hold time after PCI_CLK	0		ns
t_{val}	Delay time, PCI_CLK to data valid	2		ns

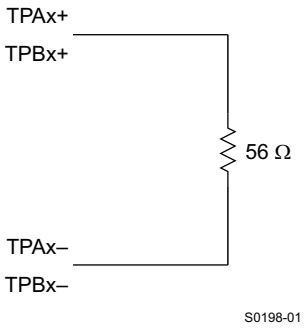


Figure 2-1. Test Load Diagram

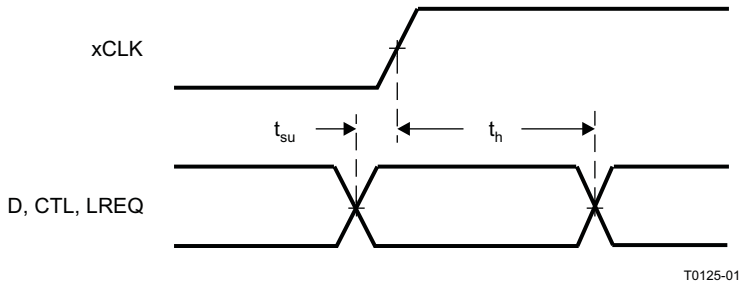


Figure 2-2. Setup and Hold Time Waveforms for Dx, CTLx, and LREQ Inputs

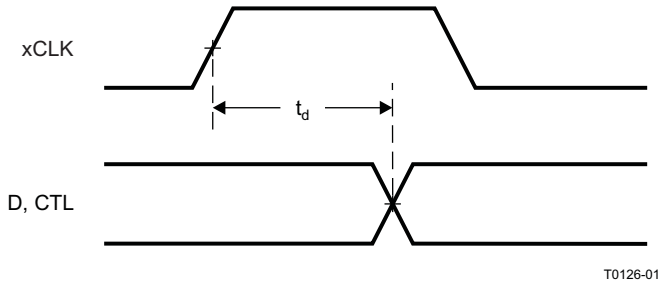


Figure 2-3. Dx and CTLx Output Delay Relative to xCLK Waveforms

3 PHY Section Register Configuration

There are 16 accessible PHY section registers in the TSB83AA23. The configuration of the registers at addresses 0h–7h (the base registers) is fixed, while the configuration of the registers at addresses 8h–Fh (the paged registers) is dependent on which of 8 pages, numbered 0h–7h, is currently selected. The selected page is set in base register 7h. While this register set is compatible with IEEE Std 1394a-2000 register sets, some fields have been redefined and this register set contains additional fields

Table 3-1 shows the configuration of the base registers, and Table 3-2 gives the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2–6 are reserved.

Table 3-1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Num_Ports (0011b)				
0011	PHY_Speed (111b)			Rsvd	Delay (0000b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	WDIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Max Legacy SPD			BLINK	Bridge		Rsvd	
0111	Page_Select			Rsvd	Port_Select			

Table 3-2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical_ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical ID is invalid after a bus reset until the self-ID has completed, as indicated by an unsolicited register 0 status transfer from the PHY section to the LLC section.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial-bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable-power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the TSB83AA23 to attempt to become root after the next bus reset. The RHB is reset to 0 by a hardware reset and is unaffected by a bus reset. If two nodes on a single bus have their root-holdoff bit set, the result is not defined. To prevent two nodes from having their root-holdoff bit set, this bit must only be written using a PHY configuration packet.

Table 3-2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
IBR	1	Rd/Wr	Initiate bus reset. This bit instructs the TSB83AA23 to initiate a long (166-µs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is reset to 0 after a hardware reset or a bus reset. Care must be exercised when writing to this bit to not change the other bits in this register. It is recommended that, when possible, a bus reset be initiated using the ISBR bit and not the IBR bit.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets, without an intervening write to the gap count register (either by a write to the PHY section register or by a PHY_CONFIG packet). It is strongly recommended that this field only be changed using PHY configuration packets.
Extended	3	Rd	Extended register definition. For the TSB83AA23, this field is 111b, indicating that the extended register set is implemented.
Num_Ports	5	Rd	Number of ports. This field indicates the number of ports implemented in the TSB83AA23. For the TSB83AA23 this field is 3.
PHY_Speed	3	Rd	PHY section speed capability. This field is no longer used. For the TSB83AA23, this field is 111b. Speeds for IEEE Std 1394b-2002 PHYs must be checked on a port-by-port basis.
Delay	4	Rd	PHY repeater data delay. This field indicates the worst-case repeater data delay of the PHY section, expressed as 144+(delay × 20) ns. For the TSB83AA23, this field is 2h. This value is the repeater delay for the S400B case, which is slower than the S800B or 1394a cases. Because the IEEE 1394B-2002 Std PHY register set has only a single field for the delay parameter, the slowest value is used. If a network uses only S800B or 1394a connections, a delay value of 00h may be used. The worst-case PHY repeater delay is 197 ns for S400B and 127 ns for S800B cable speeds (trained, raw bit speed).
LCtrl	1	Rd/Wr	Link-active status control. This bit controls the indicated active status of the LLC section reported in the self-ID packet. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC bit in the node self-ID packet is set active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software controllable means to indicate the LLC self-ID active status in lieu of using the LPS input terminal. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus reset. NOTE: The state of the PHY section-LLC section interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY section-LLC section interface is operational as determined by the LPS input being active, received packets and status information continue to be presented on the interface, and any requests indicated on the LREQ input are processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to 0 on hardware reset. After hardware reset, this bit can be set only via a software register write. This bit is unaffected by a bus reset.
Jitter	3	Rd	PHY section repeater jitter. This field indicates the worst-case difference between the fastest and slowest repeater data delay, expressed as (jitter+1) × 20 ns. For the TSB83AA23, this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the PC0–PC2 input terminals on a hardware reset, and is unaffected by a bus reset. See *Power Class Descriptions*, Table 4-1.
WDIE	1	Rd/Wr	Watchdog interrupt enable. This bit, if set to 1, enables the port event interrupt (PIE) bit to be set when resume operations begin on any port, or when any of the CTOI, CPSI, or STOI interrupt bits are set and the PHY section-LLC section interface is nonoperational. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the TSB83AA23 to initiate a short (1.3-µs) arbitrated bus reset at the next opportunity. This bit is reset to 0 by a bus reset. It is recommended that short bus reset is the only reset type initiated by software. IEC 61883-6 requires that a node initiate short bus resets to minimize any disturbance to an audio stream. NOTE: Legacy IEEE Std 1394-1995-compliant PHYs are not capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.

Table 3-2. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start, and might indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the CTOI and WDIE bits are both set and the LLC is or becomes inactive, the PHY section activates the LKON output to notify the LLC section to service the interrupt. NOTE: If the network is configured in a loop, then only those nodes that are part of the loop generate a configuration-time-out interrupt. Instead, all other nodes time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus reset. This bit is set only when the bus topology includes IEEE Std 1394a-2000 nodes; otherwise, IEEE Std 1394b-2002 loop healing prevents loops from being formed in the topology.
CPSI	1	Rd/Wr	Cable-power-status interrupt. This bit is set to 1 when the CPS input transitions from high to low, indicating that cable power might be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit. If the CPSI and WDIE bits are both set and the LLC section is or becomes inactive, the PHY section activates the LKON output to notify the LLC section to service the interrupt.
STOI	1	Rd/Wr	State-time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus-reset to occur). This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit. If the STOI and WDIE bits are both set and the LLC is or becomes inactive, the PHY section activates the LKON output to notify the LLC section to service the interrupt.
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (WDIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the TSB83AA23 to perform the various arbitration acceleration enhancements defined in IEEE Std 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in IEEE Std 1394b-2002 mode.
EMC	1	Rd/Wr	Enable multispeed concatenated packets. This bit enables the TSB83AA23 to transmit concatenated packets of differing speeds in accordance with the protocols defined in IEEE Std 1394a-2000. This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in IEEE Std 1394b-2002 mode.
Max Legacy SPD	3	Rd	Maximum legacy path speed. This field holds the maximum speed capability of any legacy node (IEEE Std 1394a-2000 or 1394-1995-compliant) as indicated in the self-ID packets received during bus initialization. Encoding is the same as for the PHY_SPEED field (but limited to S400 maximum).
BLINK	1	Rd	Beta-mode link. This bit indicates that a Beta-mode-capable LLC section is attached to the PHY section. This bit is set by the BMODE input terminal on the TSB83AA23 and should be set to 1.
Bridge	2	Rd/Wr	Bridge. This field controls the value of the bridge (brdg) field in the self-ID packet. The power reset value is 0. Details for when to set these bits are specified in the IEEE 1394.1 bridging specification.
Page_Select	3	Rd/Wr	Page Select. This field selects the register page to use when accessing register addresses 8–15. This field is reset to 0 by a hardware reset and is unaffected by bus reset.
Port_Select	4	Rd/Wr	Port Select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus reset.

The port-status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. Table 3-3 shows the configuration of the port-status page registers, and Table 3-4 gives the corresponding field descriptions. If the selected port is not implemented, all registers in the port-status page are read as 0.

Table 3-3. Page-0 (Port-Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Astat		BStat		Ch	Con	RxOK	Dis
1001	Negotiated_speed			PIE	Fault	Standby_fault	Disscrm	B_Only
1010	DC_connected	Max_port_speed (011b)			LPP	Cable_speed		

Table 3-3. Page-0 (Port-Status) Register Configuration (continued)

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1011	Connection_unreliable	Reserved			Beta_mode	Reserved		
1100	Port_error							
1101	Reserved					Loop_disable	In_standby	Hard_disable
1110	Reserved							
1111	Reserved							

Table 3-4. Page-0 (Port-Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Astat	2	Rd	TPA line state. This field indicates the instantaneous TPA line state of the selected port, encoded as: **Code** **Arbitration Value** 11 Z 10 1 01 0 00 Invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the AStat field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but this does not necessarily mean that the port is active. For IEEE Std 1394b-2002-coupled connections, the Con bit is set when a port detects connection tones from the peer PHY and operating-speed negotiation is completed.
RxOK	1	Rd	Receive OK. In IEEE Std 1394a-2000 mode, this bit indicates the reception of a debounced TPBias signal. In Beta_mode, this bit indicates the reception of a continuous electrically valid signal. NOTE: RxOK is set to false during the time that only connection tones are detected in Beta mode.
Dis	1	Rd/Wr	Port disabled control. If this bit is 1, the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset. When this bit is set, the port cannot become active; however, the port still tones, but does not establish an active connection.
Negotiated_speed	3	Rd	Negotiated speed. Indicates the maximum speed negotiated between this port and its immediately connected port. The encoding is as for Max_port_speed. It is set on connection when in Beta_mode, or to a value established during self-ID when in IEEE Std 1394a-2000 mode.
PIE	1	Rd/Wr	Port event interrupt enable. When this bit is 1, a port event on the selected port sets the port event interrupt (PEI) bit and notifies the link. This bit is reset to 0 by a hardware reset and is unaffected by bus reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
Standby_fault	1	Rd/Wr	Standby fault. This bit is set to 1 if an error is detected during a standby operation and cleared on exit from the standby state. A write of 1 to this bit or receipt of the appropriate remote command packet clears it to 0. When this bit is cleared, standby errors are cleared.
Disscrm	1	Rd/Wr	Disable scrambler. If this bit is set to 1, the data sent during packet transmission is not scrambled.
B_Only	1	Rd	Beta-mode operation only. For the TSB83AA23, this bit is set to 0 for all ports.

Table 3-4. Page-0 (Port-Status) Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
DC_connected	1	Rd	If this bit is set to 1, the port has detected a dc connection to the peer port by means of an IEEE Std 1394a-2000-style connect-detect circuit.
Max_port_speed	3	Rd/Wr	Maximum port speed. The maximum speed at which a port is allowed to operate in Beta mode. The encoding is: 000 = S100 001 = S200 010 = S400 011 = S800 100 = S1600 101 = S3200 110 = Reserved 111 = Reserved An attempt to write to the register with a value greater than the hardware capability of the port results in the value for the maximum speed of which the port is capable being stored in the register. The port uses this register only when a new connection is established in the Beta mode. The power reset value is the maximum speed capable of the port. Software can modify this value to force a port to train at a lower than maximum, but no lower than minimum speed.
LPP (Local_plug_present)	1	Rd	Local plug present. This flag is set permanently to 1.
Cable_speed	3	Rd	Cable speed. This variable is set to the value for the maximum speed that the port is capable of. The encoding is the same as for Max_port_speed.
Connection_unreliable	1	Rd/Wr	Connection unreliable. If this bit is set to 1, a Beta-mode speed negotiation has failed or synchronization has failed. A write of 1 to this field resets the value to 0.
Beta_mode	1	Rd	Operating in Beta mode. If this bit is 1, the port is operating in Beta mode; it is equal to 0 otherwise (that is, when operating in IEEE Std 1394a-2000 mode, or when disconnected). If Con is 1, RxOK is 1, and Beta_mode is 0, the port is active and operating in the IEEE Std 1394a-2000 mode.
Port_error	8	Rd/Wr	Port error. Incremented when the port receives an invalid codeword, unless the value is already 255. Cleared when read (including being read by means of a remote access packet). Intended for use by a single bus-wide diagnostic program.
Loop_disable	1	Rd	Loop disable. This bit is set to 1 if the port has been placed in the loop-disable state as part of the loop-free build process (the PHYs at either end of the connection are active, but if the connection itself were activated, a loop would exist). Cleared on bus reset and on disconnection.
In_standby	1	Rd	In standby. This bit is set to 1 if the port is in standby power-management state.
Hard_disable	1	Rd/Wr	Hard disable. No effect unless the port is disabled. If this bit is set to 1, the port does not maintain connectivity status on an ac connection when disabled. The values of the Con and RxOK bits are forced to 0. This flag can be used to force renegotiation of the speed of a connection. It also can be used to place the device into a lower-power state because when hard disabled, a port no longer *tones* to maintain IEEE Std 1394b-2002 ac-connectivity status.

The vendor identification page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. Table 3-5 shows the configuration of the vendor identification page, and Table 3-6 shows the corresponding field descriptions.

Table 3-5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 3-6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB83AA23, this field is 02h, indicating compliance with the IEEE Std 1394b-2002 specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB83AA23, this field is 08 0028h (TI) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the TSB83AA23, this field is 83_13_06h.

The vendor-dependent page provides access to the special control features of the TSB83AA23, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. Table 3-7 shows the configuration of the vendor-dependent page, and Table 3-8 shows the corresponding field descriptions.

Table 3-7. Page 7 (Vendor-Dependent) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Reserved							
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	SWR	Reserved for test						
1111	Reserved for test							

Table 3-8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
SWR	1	Rd/Wr	Software hard reset. Writing a 1 to this bit forces a hard reset of the PHY section (same effect as momentarily asserting the $\overline{\text{RESET}}$ terminal low). This bit is always read as a 0.

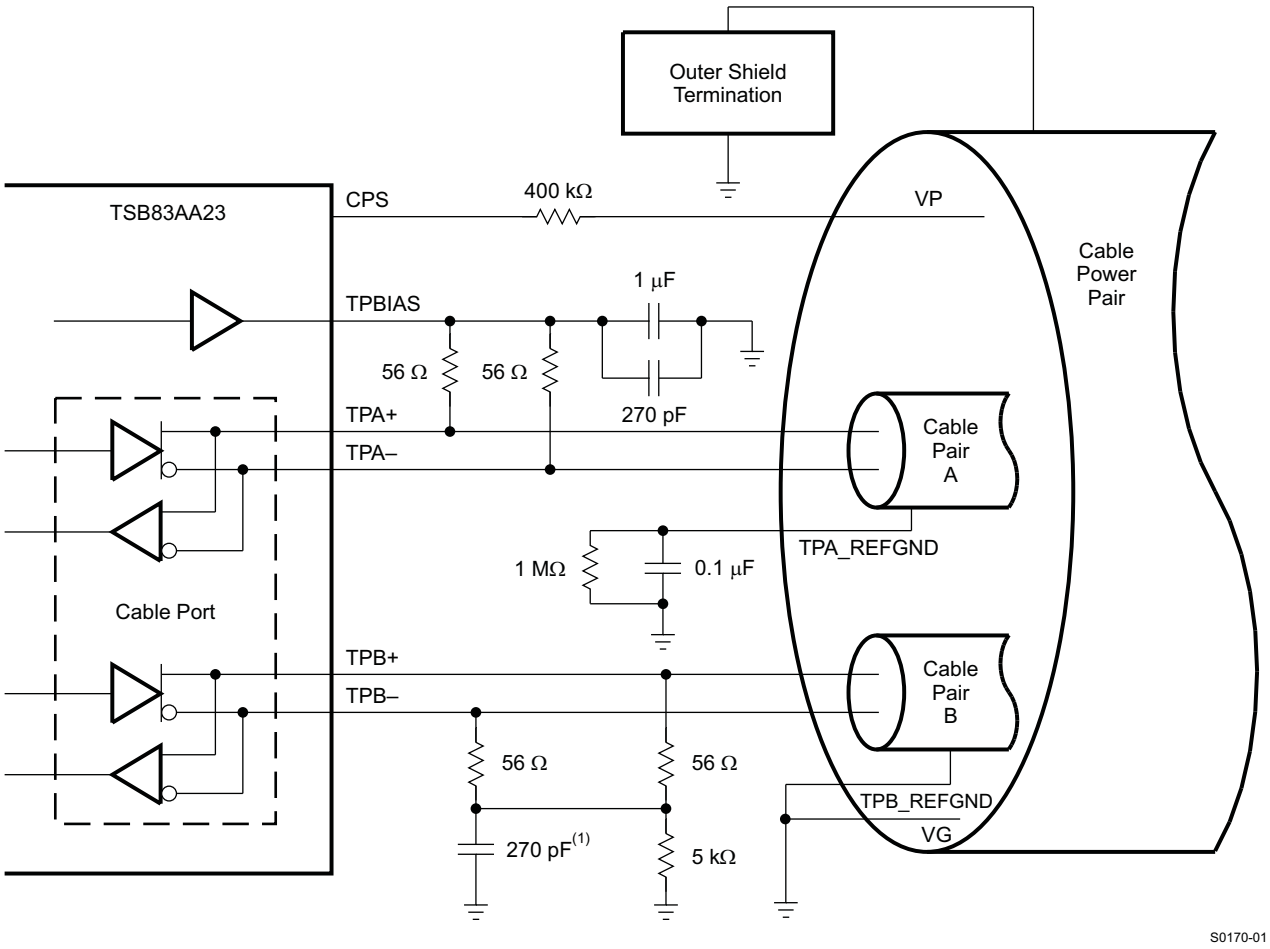
4 PHY Section Application Information

4.1 Power-Class Programming

The PC0–PC2 terminals are programmed to set the default value of the power class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Descriptions of the various power classes are given in Table 4-1. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 4-1. Power Class Descriptions

PC[0:2]	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self powered and provides a minimum of 15 W to the bus.
010	Node is self powered and provides a minimum of 30 W to the bus.
011	Node is self powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W; no additional power is needed to enable the link. The node also may provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Reserved for future standardization
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.



NOTE: IEEE Std 1394-1995 calls for a 250-pF capacitor, which is a nonstandard component value. A 270-pF capacitor is recommended.

Figure 4-1. Typical Twisted Pair IEEE Std 1394a-2000 Cable Connections

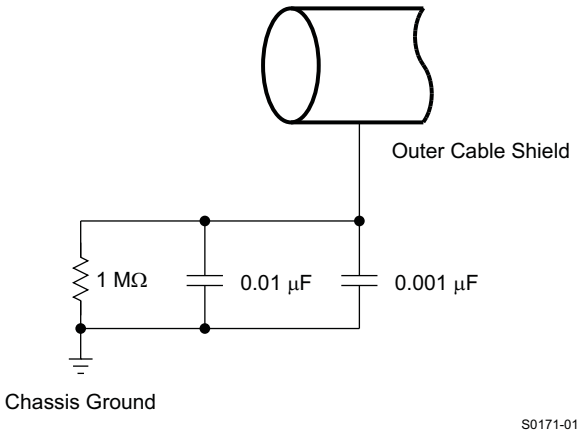


Figure 4-2. Typical DC-Isolated Outer Shield Termination

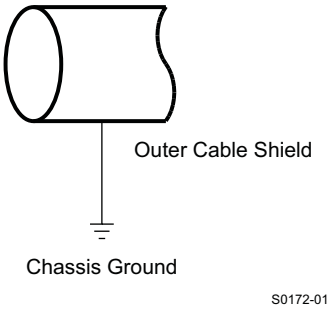


Figure 4-3. Non-DC-Isolated Outer Shield Termination

4.2 Power-Up Reset

To ensure proper operation of the TSB83AA23 PHY section, the $\overline{\text{RESET}}$ terminal must be asserted low for a minimum of 2 ms from the time that DVDD, AVDD, and PLLVDD power reaches the minimum required supply voltage and the input clock is valid. If a fundamental-mode crystal is used rather than an oscillator, the start-up time parameter may be set to zero. When using a passive capacitor on the $\overline{\text{RESET}}$ terminal to generate a power-on-reset signal, the minimum reset time is assured if the value of the capacitor satisfies the following equation (the value must be no smaller than approximately 0.1 µF):

C_{min} = (0.0077 T) + 0.085 + (external_oscillator_start-up_time 0.05)

Where:

C_{min} = Minimum capacitance on the $\overline{\text{RESET}}$ terminal in µF

T = V_{DD} ramp time, 10%–90% (in ms)

external_oscillator_start-up_time = Time from power applied to the external oscillator until the oscillator outputs a valid clock in ms

4.3 Crystal Oscillator Selection

The TSB83AA23 is designed to use an external 98.304-MHz crystal oscillator connected to the XI terminal to provide the reference clock. This clock, in turn, drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S800 media data rates.

A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE Std 1394. Adjacent PHYs may, therefore, have a difference of up to 200 ppm from each other in their internal clocks, and PHYs must be able to compensate for this difference over the maximum packet length. Larger clock variations can cause resynchronization overflows or underflows, resulting in corrupted packet data.

For the TSB83AA23, the PCLK output can be used to measure the frequency accuracy and stability of the internal oscillator and PLL from which it is derived. The frequency of the PCLK output must be within ±100 ppm of the nominal frequency of 98.304 MHz.

The following are some typical specifications for an oscillator used with the TSB83AA23, to achieve the required frequency accuracy and stability:

- RMS jitter of 5 ps or less
- RMS phase-noise jitter of 1 ps or less over the range 12 kHz to 20 MHz or higher
- Frequency tolerance at 25°C: Total frequency variation for the complete circuit is ±100 ppm. A device with ±30-ppm or ±50-ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A device with ±30-ppm or ±50-ppm frequency stability is recommended for adequate margin.

NOTE

The total frequency variation must be kept below ±100 ppm from nominal, with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made, as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80-ppm possible variation due to the oscillator alone. Aging also contributes to the frequency variation.

It is strongly recommended that part of the verification process for the design is to measure the frequency of the PCLK output of the PHY section. This should be done using a frequency counter with an accuracy of 6 digits or better.

4.4 Bus Reset

It is recommended that when the user has a choice, the user should initiate a bus reset by writing to the initiate-short-bus-reset (ISBR) bit (bit 1 PHY register 0101b). Care must be taken not to change the value of any of the other writeable bits in this register when the ISBR bit is written to.

In the TSB83AA23, the initiate-bus-reset (IBR) bit can be set to 1 to initiate a bus reset and initialization sequence; however, it is recommended to use the ISBR bit instead. The IBR bit is located in PHY register 1 along with the root-holdoff bit (RHB) and gap count. As required by the IEEE Std 1394b-2002 Supplement, this configuration maintains compatibility with older TI PHY designs that were based on either the suggested register set defined in Annex J of IEEE Std 1394-1995 or the IEEE Std 1394a-2000 Supplement. Therefore, when the IBR bit is written, the RHB and gap count are also necessarily written.

It is recommended that the RHB and gap count only be updated by PHY configuration packets. The TSB83AA23 is IEEE Std 1394a-2000 and IEEE Std 1394b-2002 compliant and, therefore, both the reception and transmission of PHY configuration packets cause the RHB and gap count to be loaded, unlike older IEEE Std 1394-1995-compliant PHYs that decode only received PHY configuration packets.

The gap count is set to the maximum value of 63 after two consecutive bus resets without an intervening write to the gap count, either by a write to PHY register 1 or by a PHY configuration packet. This mechanism allows a PHY configuration packet to be transmitted and then a bus reset initiated to verify that all nodes on the bus have updated their RHBs and gap counts, without having the gap count set back to 63 by the bus reset. The subsequent connection of a new node to the bus, which initiates a bus reset, then causes the gap count of each node to be set to 63. Note, however, that if a subsequent bus reset is instead initiated by a write to register 1 to set the IBR bit, all other nodes on the bus have their gap counts set to 63, while this node's gap count remains set to the value just loaded by the write to PHY register 1.

Therefore, to maintain consistent gap counts throughout the bus, the following rules apply to the use of the IBR bit, RHB, and gap count in PHY register 1:

- Following the transmission of a PHY configuration packet, a bus reset must be initiated to verify that all nodes have correctly updated their RHBs and gap counts, and to ensure that a subsequent new connection to the bus causes the gap count to be set to 63 on all nodes in the bus. If this bus reset is initiated by setting the IBR bit to 1, the RHB and gap count register also must be loaded with the correct values consistent with the just-transmitted PHY configuration packet. In the TSB83AA23, the RHB and gap count have been updated to their correct values on the transmission of the PHY configuration packet, so these values can first be read from register 1 and then rewritten.
- Other than to initiate the bus reset that must follow the transmission of a PHY configuration packet, when the IBR bit is set to 1 to initiate a bus reset, the gap count also must be set to 63 to be consistent with other nodes on the bus, and the RHB must be maintained with its current value.
- The PHY register 1 must not be written to except to set the IBR bit. The RHB and gap count must not be written without also setting the IBR bit to 1.
- To avoid these problems all bus resets initiated by software must be initiated by writing the ISBR bit (bit 1 PHY register 0101b). Care must be taken to not change the value of any of the other writeable bits in this register when the ISBR bit is written to. Also, the only means to change the gap count of

any node must be by means of the PHY configuration packet, which changes all nodes to the same gap count.

5 Principles of Operation (IEEE Std 1394b-2002 Interface)

The following paragraphs describe the operation of the PHY section-LLC section interface. This interface is formally specified in IEEE Std 1394b-2002.

The interface to the LLC section consists of the PCLK, LCLK, CTL0–CTL1, D0–D7, LREQ, PINT, LPS, and LKON terminals on the TSB83AA23, as shown in Figure 5-1. The interface to the PHY section consists of PHY_PCLK, PHY_LCLK, PHY_CTL0–PHY_CTL1, PHY_D0–PHY_D7, PHY_LREQ, PHY_LPS, PHY_LINKON, PHY_PINT as shown in Figure 5-1.

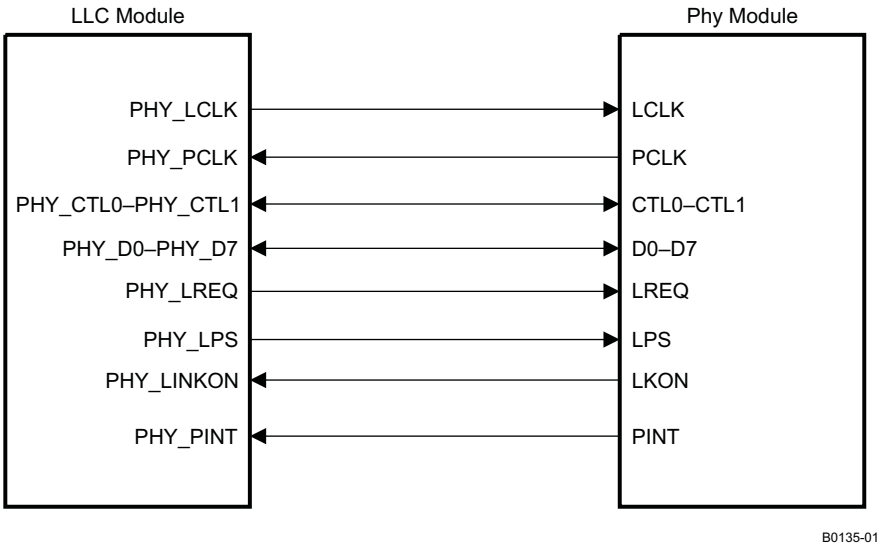


Figure 5-1. PHY Section-LLC Section Interface

The LCLK/PHY_LCLK terminals provide a clock signal to the PHY section. The LLC section derives this clock from the PCLK/PHY_PCLK signal and is phase locked to the PCLK/PHY_PCLK signal. All LLC-section to PHY-section transfers are synchronous to LCLK/PHY_LCLK.

The PCLK/PHY_PCLK terminals provide a 98.304-MHz interface system clock. All control, data, and PHY-section interrupt signals are synchronized to the rising edge of PCLK/PHY_PCLK.

The PHY_CTL0-CTL0 and PHY_CTL1-CTL1 terminals form a bidirectional control bus that controls the flow of information and data.

The D0–D7/PHY_D0–PHY_D7 terminals form a bidirectional data bus that transfers status information, control information, or packet data between the sections. The TSB83AA23 supports S400B and S800 data transfers over the D0–D7/PHY_D0–PHY_D7 data bus. In S400B and S800 operation, all Dn terminals are used.

The LREQ/PHY_LREQ terminals are controlled by the LLC section to send serial service requests to the PHY section, to request access to the serial bus for packet transmission, read or write PHY section registers, or control arbitration acceleration. All data on LREQ/PHY_LREQ is synchronous to LCLK/PHY_LCLK.

The LPS/PHY_LPS and LKON/PHT_LINKON terminals are used for power management. The LPS terminal indicates the power status of the LLC section, and can be used to reset the PHY section-LLC section interface or to disable PCLK. The LKON terminal sends a wake-up notification to the LLC section and indicates an interrupt to the LLC section when either LPS is inactive or the PHY register L bit is 0.

The PINT/PHY_PINT terminals are used by the PHY section for the serial transfer of status, interrupt, and other information to the LLC section.

The PHY section normally controls the PHY_CTL0-CTL0–PHY_CTL1-CTL1 and D0–D7/PHY_D0–PHY_D7 bidirectional buses. The LLC section is allowed to drive these buses only after the LLC section has been granted permission to do so by the PHY section.

There are four operations that can occur on the PHY section-LLC section interface: link service request, status transfer, data transmit, and data receive.

- The LLC section issues a service request to read or write a PHY section register or to request the PHY section to gain control of the serial bus to transmit a packet.
- The PHY section can initiate a status transfer either autonomously or in response to a register read request from the LLC section.
- The PHY section initiates a receive operation when a packet is received from the serial bus.
- The PHY section initiates a transmit operation after winning control of the serial bus following a bus request by the LLC section. The transmit operation is initiated when the PHY section grants control of the interface to the LLC section.

Table 5-1 and Table 5-2 show the encoding of the CTL0–CTL1 bus.

Table 5-1. CTL Encoding When PHY Section Has Control of the Bus

PHY_CTL 0-CTL0	PHY_CTL 1-CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY section to the LLC section.
1	0	Receive	An incoming packet is being sent from the PHY section to the LLC section.
1	1	Grant	The LLC section has been given control of the bus to send an outgoing packet.

Table 5-2. CTL Encoding When LLC Section Has Control of the Bus

PHY_CTL 0-CTL0	PHY_CTL 1-CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC section releases the bus (transmission has been completed).
0	1	Transmit	An outgoing packet is being sent from the LLC section to the PHY section.
1	0	Reserved	Reserved
1	1	Hold/more information	The LLC section is holding the bus while data is being prepared for transmission, or the LLC section is sending a request to arbitrate for access to the bus, or the LLC section is identifying the end of a subaction gap to the PHY section.

5.1 LLC Section Service Request

To request access to the bus, to read or write a PHY section register, or to send a link notification to PHY section, the LLC section sends a serial bit stream on the LREQ/PHY_LREQ terminal (see Figure 5-2).

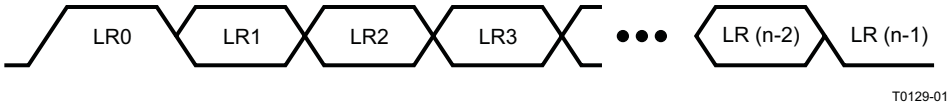


Figure 5-2. LREQ/PHY_LREQ Request Stream

The length of the stream varies depending on the type of request as shown in Table 5-3.

Table 5-3. Request Stream Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	11
Read register request	10
Write register request	18
LLC section notification request	6
PHY section-LLC section interface reset request	6

Regardless of the type of request, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. The 2nd through 5th bits of the request stream indicate the type of the request. In the descriptions below, bit 0 is the most significant and is transmitted first in the request bit stream. The LREQ/PHY_LREQ terminals are normally low.

Table 5-4 shows the encoding for the request type.

Table 5-4. Request-Type Encoding

LR[1:4]	NAME	DESCRIPTION
0000	Reserved	Reserved
0001	Immed_Req	Immediate request. On detection of idle, the PHY section arbitrates for the bus.
0010	Next_Even	Next even request. The PHY section arbitrates for the bus to send an asynchronous packet in the even fairness interval phase.
0011	Next_Odd	Next odd request. The PHY section arbitrates for the bus to send an asynchronous packet in the odd fairness interval phase.
0100	Current	Current request. The PHY section arbitrates for the bus to send an asynchronous packet in the current fairness interval.
0101	Reserved	Reserved
0110	Isoch_Req_Even	Isochronous even request. The PHY section arbitrates for the bus to send an isochronous packet in the even isochronous period.
0111	Isoch_Req_Odd	Isochronous odd request. The PHY section arbitrates for the bus to send an isochronous packet in the odd isochronous period.
1000	Cyc_Start_Req	Cycle-start request. The PHY section arbitrates for the bus to send a cycle-start packet.
1001	Reserved	Reserved
1010	Reg_Read	Register read request. The PHY section returns the specified register contents through a status transfer.
1011	Reg_Write	Register write request. Write to the specified register in the PHY section.
1100	Isoch_Phase_Even	Isochronous phase-even notification. The LLC section reports to the PHY section that: 1) A cycle-start packet has been received. 2) The LLC section has set the isochronous phase to even.
1101	Isoch_Phase_Odd	Isochronous phase-odd notification. The LLC section reports to the PHY section that: 1) A cycle-start packet has been received. 2) The LLC section has set the isochronous phase to odd.
1110	Cycle_Start_Due	Cycle-start-due notification. The LLC section reports to the PHY section that a cycle-start packet is due for reception.
1111	Reserved	Reserved

For a bus request, the length of the LREQ/PHY_LREQ bit stream is 11 bits (see Table 5-5).

Table 5-5. Bus Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	Indicates the type of bus request (see Table 5-4).
5	Request format	Indicates the packet format to be used for packet transmission (see Table 5-6).
6–9	Request speed	Indicates the speed at which the link sends the data to the PHY section. See Table 5-7 for the encoding of this field.
10	Stop bit	Indicates the end of the transfer (always 0). If bit 6 is 0, this bit may be omitted.

Table 5-6 shows the 1-bit request format field used in bus requests.

Table 5-6. Bus-Request Format Encoding

LR5	DATA RATE
0	LLC section does not request either Beta or legacy packet format for bus transmission.
1	LLC section requests Beta packet format for bus transmission.

Table 5-7 shows the 4-bit request speed field used in bus requests.

Table 5-7. Bus-Request Speed Encoding

LR[6:9]	DATA RATE
0000	S100
0001	Reserved
0010	S200
0011	Reserved
0100	S400
0101	Reserved
0110	S800
All Others	Invalid

NOTE

The TSB83AA23 PHY section accepts a bus request with an invalid speed code and processes the bus request normally. However, during packet transmission for such a request, the TSB83AA23 PHY section ignores any data presented by the LLC section and transmits a null packet.

For a read register request, the length of the LREQ/PHY_LREQ bit stream is 10 bits (see Table 5-8).

Table 5-8. Read Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	1010 indicates this is a read register request.
5–8	Address	Identifies the address of the PHY section register to be read
9	Stop bit	Indicates the end of the transfer (always 0)

For a write register request, the length of the LREQ/PHY_LREQ bit stream is 18 bits (see Table 5-9).

Table 5-9. Write Register Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	1011 indicates this is a write register request.
5–8	Address	Identifies the address of the PHY section register to be written
9–16	Data	Gives the data that is to be written to the specified register address
17	Stop bit	Indicates the end of the transfer (always 0)

For a link notification request, the length of the LREQ/PHY_LREQ bit stream is 6 bits (see Table 5-10).

Table 5-10. Link Notification Request

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–4	Request type	1100, 1101, or 1110 indicates this is a link notification request.
5	Stop bit	Indicates the end of the transfer (always 0)

For fair or priority access, the LLC section sends a bus request at least one clock after the PHY section-LLC section interface becomes idle. The PHY section queues all bus requests and can queue one request of each type. If the LLC section issues a different request of the same type, the new request overwrites any nonserviced request of that type. Note, on the receipt (CTL terminals are asserted to the receive state, 10b) of a packet, queued requests are not cleared by the PHY section.

The cycle master node uses a cycle-start request (Cyc_Start_Req) to send a cycle-start message. After receiving or transmitting a cycle-start message, the LLC section can issue an isochronous bus request (IsoReq). The PHY section clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the LLC section must issue an immediate bus request (Immed_Req) during the reception of the packet addressed to it. This is required to minimize the idle gap between the end of the received packet and the start of the transmitted acknowledge packet. As soon as the received packet ends, the PHY section immediately grants control of the bus to the LLC section. The LLC section sends an acknowledgment to the sender unless the header CRC of the received packet is corrupted. In this case, the LLC section does not transmit an acknowledge, but instead cancels the transmit operation and immediately releases the interface ; the LLC section must not use this grant to send another type of packet. After the interface is released the LLC section can proceed with another request.

For write register requests, the PHY section loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY section returns the contents of the addressed register to the LLC section at the next opportunity through a PHY status transfer. A write or read register request can be made at any time, including while a bus request is pending. Once a read register request is made, the PHY section ignores further read register requests until the register contents are successfully transferred to the LLC section. A bus reset does not clear a pending read register request.

5.2 Status Transfer

A status transfer is initiated by the PHY section when there is status information to be transferred to the LLC section. Two types of status transfers can occur: bus status transfer and PHY status transfer. Bus status transfers send the following status information: bus-reset indications, subaction and arbitration reset gap indications, cycle-start indications, and PHY section interface-reset indications. PHY status transfers send the following information: PHY section interrupt indications, unsolicited and solicited PHY section register data, bus initialization indications, and PHY section-LLC section interface-error indications. The PHY section uses a different mechanism to send the bus status transfer and the PHY status transfer.

Bus status transfers use the PHY_CTL0-CTL0–PHY_CTL1-CTL1 and D0–D7/PHY_D0–D7 terminals to transfer status information. Bus status transfers can occur during idle periods on the PHY section-LLC section interface or during packet reception. When the status transfer occurs, a single PCLK/PHY_PCLK cycle of status information is sent to the LLC section. The information is sent such that each individual Dn terminal conveys a different bus status transfer event. During any bus status transfer, only one status bit is set. If the PHY section-LLC section interface is inactive, the status information is not sent. When a bus reset on the serial bus occurs, the PHY section sends a bus reset indication (via the CTLn and Dn terminals), cancels all packet transfer requests, sets asynchronous and isochronous phases to even, forwards self-ID packets to the link, and sends an unsolicited PHY section register 0 status transfer (via the PINT terminal) to the LLC. In the case of a PHY section interface reset operation, the PHY section-LLC section interface is reset on the following PCLK/PHY_PCLK cycle.

Table 5-11 shows the definition of the bits during the bus status transfer and Figure 5-3 shows the timing.

Table 5-11. Status Bits

STATUS BIT	DESCRIPTION
D0	Bus reset
D1	Arbitration reset gap—odd
D2	Arbitration reset gap—even
D3	Cycle start—odd
D4	Cycle start—even
D5	Subaction gap
D6	PHY section interface reset
D7	Reserved

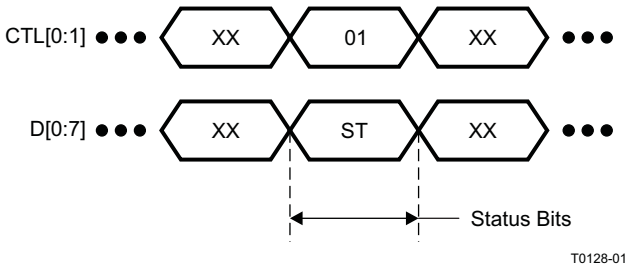
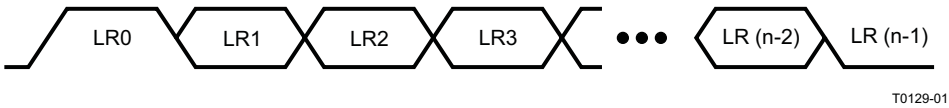


Figure 5-3. Bus Status Transfer

PHY status transfers use the PINT/PHY_PINT terminals to send status information serially to the LLC section (see Figure 5-4). PHY status transfers (see Table 5-12) can occur at any time during normal operation. The PHY section uses the PHY_INTERRUPT PHY status transfer when required to interrupt the LLC section due to a configuration timeout, a cable power failure, a port interrupt, or an arbitration timeout. When transferring PHY register contents, the PHY section uses either the solicited or the unsolicited register read status transfer. The unsolicited register 0 contents are passed to the LLC only during initialization of the serial bus. After any PHY section-LLC section interface initialization, the PHY section sends a PHY status transfer indicating whether or not a bus reset occurred during the inactive period of the PHY section-LLC section interface. If the PHY section receives an illegal request from the LLC section, the PHY section issues an INTERFACE_ERROR PHY status transfer.



NOTE: Each cell represents one clock sample time, and n is the number of bits in the request stream.

Figure 5-4. PINT (PHY Section Interrupt) Stream

Table 5-12. PHY Status Transfer Encoding

PI[1:3]	NAME	DESCRIPTION	NUMBER OF BITS
000	NOP	No status indication	5
001	PHY_INTERRUPT	Interrupt indication: configuration timeout, cable power failure, port event interrupt, or arbitration state machine timeout	5
010	PHY_REGISTER_SOL	Solicited PHY section register read	17
011	PHY_REGISTER_UNSOL	Unsolicited PHY section register read	17
100	PH_RESTORE_NO_RESET	PHY section-LLC section interface initialized; no bus resets occurred	5
101	PH_RESTORE_RESET	PHY section-LLC section interface initialized; a bus reset occurred	5
110	INTERFACE_ERROR	PHY section received illegal request	5
111	Reserved	Reserved	Reserved

Most PHY status transfers are 5 bits long. The transfer consists of a start bit (always 1), followed by a request type (see Table 5-12), and lastly followed by a stop bit (always 0). The only exception is when the transfer of register contents occurs. Solicited and unsolicited PHY register read transfers are 17 bits long and include the additional information of the register address and the data contents of the register (see Table 5-13).

Table 5-13. Register Read (Solicited and Unsolicited) PHY Status Transfer Encoding

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	010 or a 011 indicates a solicited or unsolicited register contents transfer.
4–7	Address	Identifies the address of the PHY section register whose contents are being transferred
8–15	Data	The contents of the register addressed in bits 4 through 7
16	Stop bit	Indicates the end of the transfer (always 0)

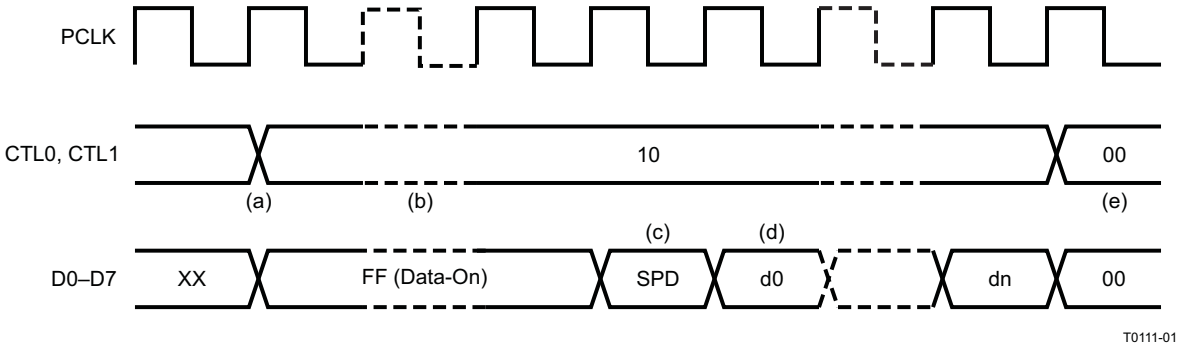
5.3 Receive

When the PHY section detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL/PHY_CTL terminals and a logic 1 on each of the D/PHY_D terminals (data-on indication). The PHY section indicates the start of a packet by placing the speed code (encoded as shown in Table 5-14) on the D/PHY_D terminals, followed by packet data. The PHY section holds the CTL/PHY_CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY section indicates the end of packet data by asserting idle on the CTL/PHY_CTL terminals. All received packets are transferred to the LLC section. The speed code is part of the PHY section-LLC section protocol and is not included in the calculation of CRC or any other data protection mechanisms.

The PHY section can optionally send status information to the LLC section at any time during the data-on indication. Only bus status transfer information can be sent during a data-on indication. The PHY section holds the CTL/PHY_CTL terminals in the status state for one PCLK cycle and modifies the D/PHY_D terminals to the correct status state. The status transfer during the data-on indication does not need to be preceded or followed by a data-on indication.

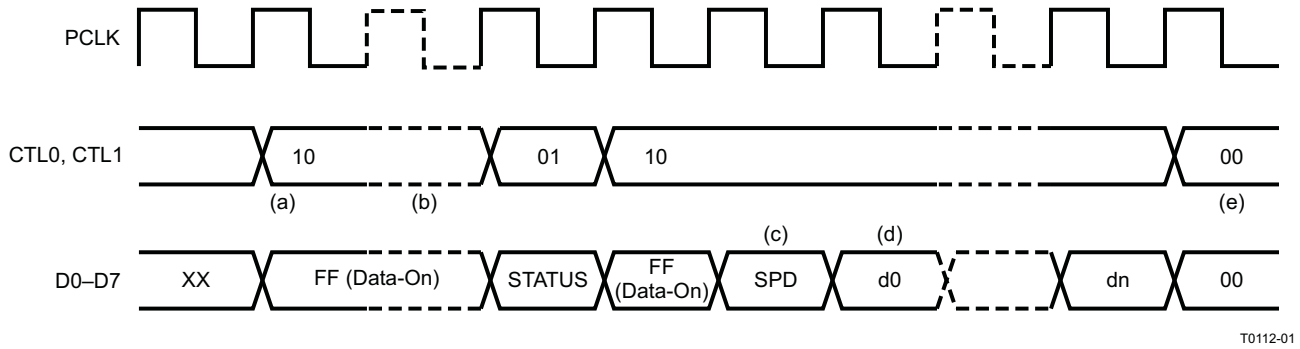
The PHY section can receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted when the packet speed exceeds the capability of the receiving PHY section, or when the LLC section immediately releases the bus without transmitting any data. In this case, the PHY section asserts receive on the CTL/PHY_CTL terminals with the data-on indication (all 1s) on the D/PHY_D terminals, followed by idle on the CTL/PHY_CTL terminals, without any speed code or data being transferred. In all cases, in normal operation, the TSB83AA23 PHY section sends at least one data-on indication before sending the speed code or terminating the receive operation.

The TSB83AA23 PHY section also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the LLC. This packet is transferred to the LLC section just as any other received self-ID packet.



NOTE: SPD = speed code (see Table 5-14), d0–dn = packet data

Figure 5-5. Normal Packet Reception



NOTE: SPD = speed code (see Table 5-14), d0–dn = packet data, STATUS = status bits (see Table 5-11)

Figure 5-6. Normal Packet Reception With Optional Bus Status Transfer

The sequence of events for a normal packet reception is:

1. Receive operation initiated. The PHY section indicates a receive operation by asserting receive on the CTL/PHY_CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status-transfer operation that is in progress so that the CTL/PHY_CTL lines can change from status to receive without an intervening idle.
2. Data-on indication. The PHY section may assert the data-on indication code on the D/PHY_D lines for one or more cycles preceding the speed code. The PHY section may optionally send a bus status transfer during the data-on indication for one PCLK cycle. During this cycle, the PHY section asserts status (01b) on the CTL/PHY_CTL lines while sending status information on the D/PHY_D lines.
3. Speed code. The PHY section indicates the speed of the received packet by asserting a speed code on the D/PHY_D lines for one cycle immediately preceding packet data. The LLC section decodes the speed code on the first receive cycle for which the D/PHY_D lines are not the data-on code. If the speed code is invalid or indicates a speed higher than that which the LLC section is capable of handling, the link must ignore the subsequent data.
4. Receive data. Following the data-on indication (if any) and the speed code, the PHY section asserts packet data on the D/PHY_D lines with receive on the CTL/PHY_CTL lines for the remainder of the receive operation.
5. Receive operation terminated. The PHY section terminates the receive operation by asserting idle on the CTL/PHY_CTL lines. The PHY section asserts at least one idle cycle following a receive operation.

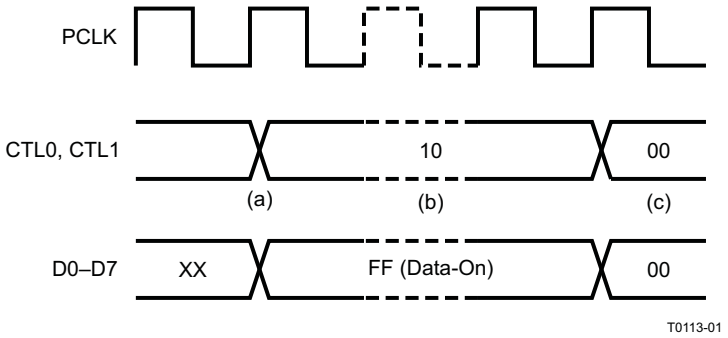


Figure 5-7. Null Packet Reception

The sequence of events for a null packet reception is:

1. Receive operation initiated. The PHY section indicates a receive operation by asserting receive on the CTL/PHY_CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL/PHY_CTL lines can change from status to receive without an intervening idle.
2. Data-on indication. The PHY section asserts the data-on indication code on the D/PHY_D lines for one or more cycles.
3. Receive operation terminated. The PHY section terminates the receive operation by asserting idle on the CTL/PHY_CTL lines. The PHY section asserts at least one idle cycle following a receive operation.

Table 5-14. Receive Speed Codes and Format(1) (2)

D0–D7	DATA RATE AND FORMAT
0000 0000	S100 legacy
0000 0001	S100 beta
0000 0100	S200 legacy
0000 0101	S200 beta
0000 1000	S400 legacy
0000 1001	S400 beta
0000 1101	S800 beta
1111 1111	Data-on indication
All Others	Reserved

(1) Y = Output as 1 by PHY section, ignored by LLC section
(2) X = Output as 0 by PHY section, ignored by LLC section

5.4 Transmit

When the LLC section issues a bus request through the LREQ terminal, the PHY section arbitrates to gain control of the bus. If the PHY section wins arbitration for the serial bus, the PHY section-LLC section interface bus is granted to the LLC section by asserting the grant state (11b) on the CTL/PHY_CTL terminals and the grant type on the D/PHY_D terminals for one PCLK cycle, followed by idle for one clock cycle. The LLC section then takes control of the bus by asserting either idle (00b), hold (11b), or transmit (01b) on the CTL/PHY_CTL terminals. If the PHY does not detect a hold or transmit state within eight PCLK cycles, the PHY section takes control of the PHY section-LLC section interface. The hold state is used by the LLC section to retain control of the bus while it prepares data for transmission. The LLC section can assert hold for zero or more clock cycles (that is, the LLC section need not assert hold before transmit). During the hold state, the LLC section is expected to drive the D/PHY_D lines to 0. The PHY section asserts data-prefix on the serial bus during this time.

When the LLC section is ready to send data, the LLC section asserts transmit on the CTL/PHY_CTL terminals, as well as sending the first bits of packet data on the D/PHY_D lines. The transmit state is held on the CTL/PHY_CTL terminals until the last bits of data have been sent. The LLC section then asserts either hold or idle on the CTL/PHY_CTL terminals for one clock cycle. If hold is asserted, the hold is immediately followed by one clock cycle of idle. The LLC section then releases the PHY section-LLC section interface by putting the CTL/PHY_CTL and D/PHY_D terminals in a high-impedance state. The PHY section then regains control of the PHY section-LLC section interface.

The hold state asserted at the end of packet transmission allows the LLC section to make an additional link request for packet transmission and/or to notify the PHY section that the packet marks the end of a subaction. The link requests allowed after packet transmission are listed in Table 5-15 (The link request types allowed during this period are a subset of all of the allowed types of link requests—see Table 5-4). The associated speed codes and packet format are listed in Table 5-16 and Table 5-17, respectively. If the LLC section requests to send an additional packet, the PHY does not necessarily have to grant the request. If the LLC section is notifying the PHY section of the end of a subaction, the LLC section sets D4 during the hold state at the end of packet transmission.

Table 5-15. Link-Request-Type Encoding During Packet Transmission

D[1:3]	REQUEST TYPE
000	No request
001	Isoch_Req_Odd
010	Isoch_Req_Even
011	Current
100	Next_Even
101	Next_Odd
110	Cyc_Start_Req
111	Reserved

Table 5-16. Link-Request Speed-Code Encoding During Packet Transmission

D[5:6]	DATA RATE
00	S100
01	S200
10	S400
11	S800

Table 5-17. Link-Request Format Encoding During Packet Transmission

D0	FORMAT
0	LLC section does not request either Beta or legacy packet format for bus transmission
1	LLC section requests Beta packet format for bus transmission

Table 5-18. Subaction End-Notification Encoding During Packet Transmission

D4	DESCRIPTION
0	Transmitted packet does not represent end of a subaction
1	Transmitted packet marks the end of a subaction

The PHY section indicates to the LLC section during the GRANT cycle which type of grant is being issued. This indication includes the grant type, as well as the grant speed. The LLC section uses the bus grant for transmitting the granted packet type. The LLC section transmits a granted packet type only if its request type matches the granted speed and the granted format.

Table 5-19. Format Type During Grant Cycle

D0 VALUE DURING GRANT CYCLE	FORMAT
0	Unspecified
1	Beta format

Table 5-20. Grant Type Values During Grant Cycle

D[1:3] VALUE DURING GRANT CYCLE	REQUEST TYPE
000	Reserved
001	Reserved
010	Isochronous grant
011	Reserved
100	Reserved
101	Asynchronous grant
110	Cycle-start grant
111	Immediate grant

Table 5-21. Speed Type Values During Grant Cycle

D[5:6] VALUE DURING GRANT CYCLE	SPEED TYPE
00	S100
01	S200
10	S400
11	S800

6 TSB83AA23 Link Layer Controller Programming Model

This section describes the internal PCI configuration registers used to program the TSB83AA23 device. All registers are detailed in the same format—a brief description for each register, followed by the register offset and a bit table describing the reset state for each register.

A bit description table, typically included when the register contains bits of more than one type or purpose, indicates bit field names; field access tags, which appear in the *Type* column; and a detailed field description. Table 6-1 describes the field access tags.

Table 6-1. Bit Field Access Tag Descriptions

ACCESS TAG	NAME	MEANING
R	Read	Field can be read by software.
W	Write	Field can be written by software to any value.
S	Set	Field can be set (value changed to 1) by a write of 1. Writes of 0 have no effect.
C	Clear	Field can be cleared (value changed to 0) by a write of 1. Writes of 0 have no effect.
U	Update	Field can be autonomously updated by the TSB83AA23 device.

6.1 PCI Configuration Registers

The TSB83AA23 device is a single-function PCI device. The configuration header is compliant with the PCI Local Bus Specification as a standard header. Table 6-2 shows the PCI configuration header that includes both the predefined portion of the configuration space and the user-definable registers.

Table 6-2. PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class code			Revision ID	08h
Built-in self-test	Header type	Latency timer	Cache line size	0Ch
OHCI base address				10h
TI extension base address				14h
CardBus CIS base address				18h
Reserved				1Ch–27h
CardBus CIS pointer				28h
Subsystem ID		Subsystem vendor ID		2Ch
Reserved				30h
Reserved			Power management capabilities pointer	34h
Reserved				38h
Maximum latency	Minimum grant	Interrupt pin	Interrupt line	3Ch
OHCI control				40h
Power management capabilities		Next-item pointer	Capability ID	44h
Power management data	Power management extension	Power management control and status		48h
Reserved				4Ch–E4h
Multifunction select				E8h
Reserved				ECh
Miscellaneous configuration				F0h
LLC section enhancement control				F4h
Subsystem access				F8h
GPIO control register				FCh

6.1.1 Vendor ID Register

The vendor ID register contains a value allocated by the PCI SIG and identifies the manufacturer of the PCI device. The vendor ID assigned to TI is 104Ch.

Type: Read only
Offset: 00h
Default: 104Ch

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

6.1.2 Device ID Register

The device ID register contains a value assigned to the TSB83AA23 device by TI. The device identification for the TSB83AA23 device is 8025h.

Type: Read only
Offset: 02h
Default: 8025h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

6.1.3 Command Register

The command register provides control over the TSB83AA23 interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*, as given in the following bit descriptions. See Table 6-3 for a description of the register contents.

Type: Read/write, read only
Offset: 04h
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-3. Command Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–11	RSVD	R	Reserved. Bits 15–11 return 0s when read.
10	INT_DISABLE	R/W	INTx disable. When set to 1, this bit disables the function from asserting interrupts on the INTx signals. 0 = INTx assertion is enabled (default). 1 = INTx assertion is disabled. This bit has been defined as part of the *PCI Local Bus Specification* (Revision 2.3).
9	FBB_ENB	R	Fast back-to-back enable. The TSB83AA23 device does not generate fast back-to-back transactions; therefore, bit 9 returns 0 when read.
8	SERR_ENB	R/W	$\overline{\text{PCI\_SERR}}$ enable. When bit 8 is set to 1, the TSB83AA23 $\overline{\text{PCI\_SERR}}$ driver is enabled. $\overline{\text{PCI\_SERR}}$ can be asserted after detecting an address parity error on the PCI bus.
7	STEP_ENB	R	Address/data stepping control. The TSB83AA23 device does not support address/data stepping; therefore, bit 7 is hardwired to 0.
6	PERR_ENB	R/W	Parity error enable. When bit 6 is set to 1, the TSB83AA23 device is enabled to drive $\overline{\text{PCI\_PERR}}$ response to parity errors through the $\overline{\text{PCI\_PERR}}$ signal.
5	VGA_ENB	R	VGA palette snoop enable. The TSB83AA23 device does not feature VGA palette snooping; therefore, bit 5 returns 0 when read.
4	MWI_ENB	R/W	Memory write and invalidate enable. When bit 4 is set to 1, the TSB83AA23 device is enabled to generate MWI PCI bus commands. If this bit is cleared, then the TSB83AA23 device generates memory write commands instead.
3	SPECIAL	R	Special cycle enable. The TSB83AA23 function does not respond to special cycle transactions; therefore, bit 3 returns 0 when read.
2	MASTER_ENB	R/W	Bus master enable. When bit 2 is set to 1, the TSB83AA23 device is enabled to initiate cycles on the PCI bus.
1	MEMORY_ENB	R/W	Memory response enable. Setting bit 1 to 1 enables the TSB83AA23 device to respond to memory cycles on the PCI bus. This bit must be set to access OHCI registers.
0	IO_ENB	R	I/O space enable. The TSB83AA23 device does not implement any I/O-mapped functionality; therefore, bit 0 returns 0 when read.

6.1.4 Status Register

The status register provides status over the TSB83AA23 interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*. See Table 6-4 for a description of the register contents.

Type: Read/clear/update, read only
Offset: 06h
Default: 0210h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	0	0	0	0	1	0.	0	0	0

Table 6-4. Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. Bit 15 is set to 1 when either an address parity or data parity error is detected.
14	SYS_ERR	RCU	Signaled system error. Bit 14 is set to 1 when $\overline{\text{PCI\_SERR}}$ is enabled and the TSB83AA23 device has signaled a system error to the host.
13	MABORT	RCU	Received master abort. Bit 13 is set to 1 when a cycle initiated by the TSB83AA23 device on the PCI bus is terminated by a master abort.
12	TABORT_REC	RCU	Received target abort. Bit 12 is set to 1 when a cycle initiated by the TSB83AA23 device on the PCI bus is terminated by a target abort.
11	TABORT_SIG	RCU	Signaled target abort. Bit 11 is set to 1 by the TSB83AA23 device when it terminates a transaction on the PCI bus with a target abort.
10–9	PCI_SPEED	R	DEVSEL timing. Bits 10 and 9 encode the timing of $\overline{\text{PCI\_DEVSEL}}$ and are hardwired to 01b, indicating that the TSB83AA23 device asserts this signal at a medium speed on nonconfiguration cycle accesses.
8	DATAPAR	RCU	Data parity error detected. Bit 8 is set to 1 when the following conditions have been met: a. $\overline{\text{PCI\_PERR}}$ was asserted by any PCI device including the TSB83AA23 device. b. The TSB83AA23 device was the bus master during the data parity error c. Bit 6 (PERR_ENB) in the command register at offset 04h in the PCI configuration space (see Section 6.1.3) is set to 1.
7	FBB_CAP	R	Fast back-to-back capable. The TSB83AA23 device cannot accept fast back-to-back transactions; therefore, bit 7 is hardwired to 0.
6	UDF	R	User-definable features (UDF) supported. The TSB83AA23 device does not support the UDF; therefore, bit 6 is hardwired to 0.
5	66MHZ	R	66-MHz capable. The TSB83AA23 device operates at a maximum PCI_CLK frequency of 33 MHz; therefore, bit 5 is hardwired to 0.
4	CAPLIST	R	Capabilities list. Bit 4 returns 1 when read, indicating that capabilities additional to standard PCI are implemented. The linked list of PCI power-management capabilities is implemented in this function.
3	INT_STATUS	RU	Interrupt status. This bit reflects the interrupt status of the function. Only when bit 10 (INT_DISABLE) in the command register (PCI offset 04h, see Section 1.4) is a 0 and this bit is a 1, is the function's INTx signal asserted. Setting the INT_DISABLE bit to a 1 has no effect on the state of this bit. This bit has been defined as part of the *PCI Local Bus Specification* (Revision 2.3).
2–0	RSVD	R	Reserved. Bits 2–0 return 0s when read.

6.1.5 Revision ID Register

The revision ID register contains the TI chip revision. See Table 6-5 for a description of the register contents.

Type: Read only
Offset: 08h
Default: 01h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	1

Table 6-5. Revision ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	CHIPREV	R	Silicon revision. This field returns 01h when read, indicating the silicon revision of the TSB83AA23 device.

6.1.6 Class Code Register

The class code register categorizes the TSB83AA23 device as a serial bus controller (0Ch) controlling an IEEE 1394 bus (00h), with an OHCI programming model (10h). See Table 6-6 for a description of the register contents.

Type: Read only
Offset: 09h
Default: 0C00 10h

Bit	23	22	21	20	19	18	17	16
Default	0	0	0	0	1	1	0	0

Bit	15	14	13	12	11	10	9	8
Default	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	0	0

Table 6-6. Class Code Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
23–16	BASECLASS	R	Base class. This field returns 0Ch when read, which broadly classifies the function as a serial bus controller.
15–8	SUBCLASS	R	Subclass. This field returns 00h when read, which specifically classifies the function as controlling an IEEE 1394 serial bus.
7–0	PGMIF	R	Programming interface. This field returns 10h when read, which indicates that the programming model is compliant with the *1394 Open Host Controller Interface Specification*.

6.1.7 Cache Line Size Register

The cache line size register is programmed by the host BIOS to indicate the system cache line size associated with the TSB83AA23 device. See Table 6-7 for a description of the register contents.

Type: Read/write
Offset: 0Ch
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-7. Cache Line Size Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	CACHELINE_SZ	R/W	Cache line size. This value is used by the TSB83AA23 device during memory write-and-invalidate, memory read-line, and memory read-multiple transactions.

6.1.8 Latency Timer Register

The latency timer register is programmed by host BIOS to indicate the latency timer associated with the TSB83AA23 device. See Table 6-8 for a description of the register contents.

Type: Read/write
Offset: 0Dh
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-8. Latency Timer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	LATENCY_TIMER	R/W	PCI latency timer. The value in this register specifies the latency timer for the TSB83AA23 device, in units of PCI clock cycles. When the TSB83AA23 device is a PCI bus initiator and asserts $\overline{\text{PCI\_FRAME}}$, the latency timer begins counting from zero. If the latency timer expires before the TSB83AA23 transaction has terminated, then the TSB83AA23 device terminates the transaction when its $\overline{\text{PCI\_GNT}}$ is deasserted.

6.1.9 Header Type Register

The header type register indicates the TSB83AA23 PCI header type. See Table 6-9 for a description of the register contents.

Type: Read only
Offset: 0Eh
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-9. Header Type Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	HEADER_TYPE	R	PCI header type. The TSB83AA23 device includes the standard PCI header, which is communicated by returning 00h when this field is read.

6.1.10 Built-In Self-Test (BIST) Register

The built-in self-test (BIST) register indicates the TSB83AA23 PCI header type, and indicates no built-in self test. See Table 6-10 for a description of the register contents.

Type: Read only
Offset: 0Fh
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-10. Built-In Self-Test (BIST) Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	BIST	R	Built-in self-test. The TSB83AA23 device does not include a BIST; therefore, this field returns 00h when read.

6.1.11 OHCI Base Address Register

The OHCI base address register is programmed with a base address referencing the memory-mapped OHCI control. When BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the OHCI registers. See Table 6-11 for a description of the register contents.

Type: Read/write, read only
Offset: 10h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-11. OHCI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	OHCIREG_PTR	R/W	OHCI register pointer. This field specifies the upper 21 bits of the 32-bit OHCI base address register.
10–4	OHCI_SZ	R	OHCI register size. This field returns 0s when read, indicating that the OHCI registers require a 2K-byte region of memory.
3	OHCI_PF	R	OHCI register prefetch. Bit 3 returns 0 when read, indicating that the OHCI registers are nonprefetchable.
2–1	OHCI_MEMTYPE	R	OHCI memory type. This field returns 0s when read, indicating that the OHCI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	OHCI_MEM	R	OHCI memory indicator. Bit 0 returns 0 when read, indicating that the OHCI registers are mapped into system memory space.

6.1.12 TI Extension Base Address Register

The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. When BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the TI registers. See Table 6-12 for a description of the register contents.

Type: Read/write, read only
Offset: 14h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-12. TI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	TIREG_PTR	R/W	TI register pointer. This field specifies the upper 21 bits of the 32-bit TI base address register.
10–4	TI_SZ	R	TI register size. This field returns 0s when read, indicating that the TI registers require a 2K-byte region of memory.
3	TI_PF	R	TI register prefetch. Bit 3 returns 0 when read, indicating that the TI registers are nonprefetchable.
2–1	TI_MEMTYPE	R	TI memory type. This field returns 0s when read, indicating that the TI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	TI_MEM	R	TI memory indicator. Bit 0 returns 0 when read, indicating that the TI registers are mapped into system memory space.

6.1.13 CardBus CIS Base Address Register

The TSB83AA23 device can be configured to support CardBus registers via bit 6 (CARDBUS) in the PCI miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 6.1.30). If CARDBUS is low (default), then this 32-bit register returns 0s when read. If CARDBUS is high, this register is to be programmed with a base address referencing the memory-mapped card information structure (CIS). This register must be programmed with a nonzero value before the CIS can be accessed. See Table 6-13 for a description of the register contents.

Type: Read/write, read only
Offset: 18h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-13. CardBus CIS Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	CIS_BASE	R/W	CIS base address. This field specifies the upper 21 bits of the 32-bit CIS base address. If CARDBUS is sampled high on a $\overline{\text{G\_RST}}$, this field is read only, returning 0s when read.
10–4	CIS_SZ	R	CIS address space size. This field returns 0s when read, indicating that the CIS space requires a 2K-byte region of memory.
3	CIS_PF	R	CIS prefetch. Bit 3 returns 0 when read, indicating that the CIS is nonprefetchable. Furthermore, the CIS is a byte-accessible address space, and either a double word or 16-bit word access yields indeterminate results.
2–1	CIS_MEMTYPE	R	CIS memory type. This field returns 0s when read, indicating that the CardBus CIS base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	CIS_MEM	R	CIS memory indicator. This bit returns 0 when read, indicating that the CIS is mapped into system memory space.

6.1.14 CardBus CIS Pointer Register

The TSB83AA23 device can be configured to support CardBus registers via bit 6 (CARDBUS) in the PCI miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 6.1.30). If CARDBUS is low (default), then this register is read-only returning 0s when read. If CARDBUS is high, then this register contains the pointer to the CardBus card information structure (CIS). See Table 6-14 for a description of the register contents.

Type: Read only
Offset: 28h
Default: 0000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X

Table 6-14. CardBus CIS Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–28	ROM_IMAGE	R	Because the CIS is not implemented as a ROM image, this field returns 0s when read.
27–3	CIS_OFFSET	R	This field indicates the offset into the CIS address space where the CIS begins, and bits 7–3 are loaded from the serial EEPROM field CIS_Offset (7–3). This implementation allows the TSB83AA23 device to produce serial EEPROM addresses equal to the lower PCI address byte to acquire data from the serial EEPROM.
2–0	CIS_INDICATOR	R	This field indicates the address space where the CIS resides and returns 011b if bit 6 (CARDBUS) in the PCI miscellaneous configuration register is high, then 011b indicates that CardBus CIS base address register at offset 18h in the PCI configuration header contains the CIS base address. If CARDBUS is low, this field returns 000b when read.

6.1.15 Subsystem Vendor ID Register

The subsystem vendor ID register is used for system and option card identification purposes. This register can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the PCI configuration space (see Section 6.1.32). See Table 6-15 for a description of the register contents.

Type: Read/update
Offset: 2Ch
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-15. Subsystem Vendor ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–0	OHCI_SSVID	RU	Subsystem vendor ID. This field indicates the subsystem vendor ID.

6.1.16 Subsystem ID Register

The subsystem ID register is used for system and option card identification purposes. This register can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the PCI configuration space (see Section 6.1.32). See Table 6-16 for a description of the register contents.

Type: Read/update
Offset: 2Eh
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-16. Subsystem ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–0	OHCI_SSID	RU	Subsystem device ID. This field indicates the subsystem device ID.

6.1.17 Power Management Capabilities Pointer Register

The power management capabilities pointer register provides a pointer into the PCI configuration header where the power-management register block resides. The TSB83AA23 configuration header double words at offsets 44h and 48h provide the power-management registers. This register is read only and returns 44h when read.

Type: Read only
Offset: 34h
Default: 44h

Bit	7	6	5	4	3	2	1	0
Default	0	1	0	0	0	1	0	0

6.1.18 Interrupt Line Register

The interrupt line register communicates interrupt line routing information. See Table 6-17 for a description of the register contents.

Type: Read/write
Offset: 3Ch
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-17. Interrupt Line Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	INTR_LINE	R/W	Interrupt line. This field is programmed by the system and indicates to software that interrupt line the TSB83AA23 $\overline{\text{PCI\_INTA}}$ is connected to.

6.1.19 Interrupt Pin Register

The interrupt pin register communicates interrupt line routing information. See Table 6-18 for a description of the register contents.

Type: Read only
Offset: 3Dh
Default: 01h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	1

Table 6-18. Interrupt Line and Pin Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	INTR_PIN	R	Interrupt pin. Returns 01h when read, indicating that the TSB83AA23 PCI function signals interrupts on the $\overline{\text{PCI\_INTA}}$ terminal.

6.1.20 Minimum Grant Register

The minimum grant register communicates to the system the desired setting of the latency timer register at offset 0Dh in the PCI configuration space (see Section 6.1.8). If a serial EEPROM is detected, the contents of this register are loaded through the serial EEPROM interface after a $\overline{\text{PCI\_RST}}$. If no serial EEPROM is detected, this register returns a default value that corresponds to MIN_GNT = 2. See Table 6-19 for a description of the register contents.

Type: Read/update
Offset: 3Eh
Default: 02h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	0

Table 6-19. Minimum Grant Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	MIN_GNT	RU	Minimum grant. The contents of this field can be used by host BIOS to assign a latency timer register value to the TSB83AA23 device. The default for this field indicates that the TSB83AA23 device might need to sustain burst transfers for nearly 64 μs and, thus, request a large value be programmed in the TSB83AA23 latency timer register at offset 0Dh in the PCI configuration space (see Section 6.1.8, *Latency Timer Register*).

6.1.21 Maximum Latency Register

The maximum latency register communicates to the system the desired setting of the latency timer and class cache line size register at offset 0Dh in the PCI configuration space (see Section 6.1.8). If a serial EEPROM is detected, the contents of this register are loaded through the serial EEPROM interface after a $\overline{\text{PCI\_RST}}$. If no serial EEPROM is detected, this register returns a default value that corresponds to MAX_LAT = 4. See Table 6-20 for a description of the register contents.

Type: Read/update
Offset: 3Fh
Default: 04h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	0	0

Table 6-20. Maximum Latency Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	MAX_LAT	RU	Maximum latency. The contents of this field can be used by host BIOS to assign an arbitration priority level to the TSB83AA23 device. The default for this field indicates that the TSB83AA23 device might need to access the PCI bus as often as every 0.25 μs; thus, an extremely high priority level is requested. The contents of this field also can be loaded through the serial EEPROM.

6.1.22 OHCI Control Register

The OHCI control register is defined by the *1394 Open Host Controller Interface Specification* and provides a bit for big endian PCI support. See Table 6-21 for a description of the register contents.

Type: Read/write, read only
Offset: 40h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-21. OHCI Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–1	RSVD	R	Reserved. Bits 31–1 return 0s when read.
0	GLOBAL_SWAP	R/W	When bit 0 is set to 1, all quadlets read from and written to the PCI interface are byte swapped (big endian). This bit is loaded from serial EEPROM and must be cleared to 0 for normal operation.

6.1.23 Capability ID Register

The capability ID register identifies the linked-list capability item. See Table 6-22 for a description of the register contents.

Type: Read only
Offset: 44h
Default: 01h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	1

Table 6-22. Capability ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	CAPABILITY_ID	R	Capability identification. This field returns 01h when read, which is the unique ID assigned by the PCI SIG for PCI power-management capability.

6.1.24 Next-Item Pointer Register

The next-item pointer register provides a pointer to the next capability item. See Table 6-23 for a description of the register contents.

Type: Read only
Offset: 45h
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-23. Next-Item Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	NEXT_ITEM	R	Next-item pointer. The TSB83AA23 device supports only one additional capability that is communicated to the system through the extended capabilities list; therefore, this field returns 00h when read.

6.1.25 Power Management Capabilities Register

The power management capabilities register indicates the capabilities of the TSB83AA23 device related to PCI power management. See Table 6-24 for a description of the register contents.

Type: Read/update, read only
Offset: 46h
Default: 7E02h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0

Table 6-24. Power Management Capabilities Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_D3COLD	RU	$\overline{\text{PCI\_PME}}$ support from D3cold. This bit can be set to 1 or cleared to 0 via bit 15 (PME_D3COLD) in the miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 6.1.30, *Miscellaneous Configuration Register*). The miscellaneous configuration register is loaded from ROM. When this bit is set to 1, it indicates that the TSB83AA23 device is capable of generating a $\overline{\text{PCI\_PME}}$ wake event from $D3_{cold}$. This bit state is dependent on the TSB83AA23 V_{AUX} implementation and can be configured by using bit 15 (PME_D3COLD) in the miscellaneous configuration register (see Section 6.1.30).
14–11	PME_SUPPORT	R	$\overline{\text{PCI\_PME}}$ support. This 4-bit field indicates the power states from which the TSB83AA23 device can assert $\overline{\text{PCI\_PME}}$. This field returns a value of 1111b, indicating that $\overline{\text{PCI\_PME}}$ can be asserted from the $D3_{hot}$, D2, D1, and D0 power states. Bit 14 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the $D3_{hot}$ state. Bit 13 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the D2 state. Bit 12 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the D1 state. Bit 11 contains the value 1 to indicate that the $\overline{\text{PCI\_PME}}$ signal can be asserted from the D0 state.
10	D2_SUPPORT	R	D2 support. Bit 10 is hardwired to 1, indicating that the TSB83AA23 device supports the D2 power state.
9	D1_SUPPORT	R	D1 support. Bit 9 is hardwired to 1, indicating that the TSB83AA23 device supports the D1 power state.
8–6	AUX_CURRENT	R	Auxiliary current. This 3-bit field reports the 3.3-V_{AUX} auxiliary current requirements. When bit 15 (PME_D3COLD) is cleared, this field returns 000b; otherwise, it returns 001b. 000b = Self powered 001b = 55 mA (3.3-V_{AUX} maximum current required)
5	DSI	R	Device-specific initialization. Bit 5 returns 0 when read, indicating that the TSB83AA23 device does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Bit 4 returns 0 when read.
3	PME_CLK	R	PME clock. Bit 3 returns 0 when read, indicating that no host bus clock is required for the TSB83AA23 device to generate $\overline{\text{PCI\_PME}}$.
2–0	PM_VERSION	R	Power-management version. This field returns 010b when read, indicating that the TSB83AA23 device is compatible with the registers described in the *PCI Bus Power Management Interface Specification* (Revision 1.1).

6.1.26 Power Management Control and Status Register

The power management control and status register implements the control and status of the PCI power management function. This register is not affected by the internally generated reset caused by the transition from the $D3_{hot}$ to D0 state. See Table 6-25 for a description of the register contents.

Type: Read/clear, read/write, read only
Offset: 48h
Default: 0000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-25. Power Management Control and Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_STS	RC	Bit 15 is set to 1 when the TSB83AA23 device normally asserts the PME signal, independent of the state of bit 8 (PME_ENB). This bit is cleared by a write back of 1, which also clears the $\overline{\text{PCI\_PME}}$ signal driven by the TSB83AA23 device. Writing a 0 to this bit has no effect.
14–9	RSVD	R	Reserved. Bits 14–9 return 0s when read.

Table 6-25. Power Management Control and Status Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
8	PME_ENB	R/W	When bit 8 is set to 1, PME assertion is enabled. When bit 8 is cleared, PME assertion is disabled. This bit defaults to 0 if the function does not support PME generation from $D3_{cold}$. If the function supports PME from $D3_{cold}$, this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Functions that do not support PME generation from any D-state (that is, bits 15–11 in the power management capabilities register at offset 46h in the PCI configuration space (see Section 6.1.30, *Power Management Capabilities Register*) equal 00000b), may hardwire this bit to be read-only, always returning a 0 when read by system software.
7–2	RSVD	R	Reserved. Bits 7–2 return 0s when read.
1–0	PWR_STATE	R/W	Power state. This 2-bit field is used to set the TSB83AA23 device power state and is encoded as follows: 00 = Current power state is D0. 01 = Current power state is D1. 10 = Current power state is D2. 11 = Current power state is D3.

6.1.27 Power Management Extension Register

The power management extension register provides extended power-management features not applicable to the TSB83AA23 device; thus, it is read-only and returns 0s when read. See Table 6-26 for a description of the register contents.

Type: Read only
Offset: 4Ah
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-26. Power Management Extension Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	RSVD	R	Reserved. Bits 7–0 return 0s when read.

6.1.28 Power Management Data Register

The power management data register provides extended power-management features not applicable to the TSB83AA23 device; thus, it is read-only and returns 0s when read. See Table 6-26 for a description of the register contents.

Type: Read only
Offset: 4Bh
Default: 00h

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 6-27. Power Management Data Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
7–0	RSVD	R	Reserved. Bits 7–0 return 0s when read.

6.1.29 Multifunction Select Register

The multifunction select register provides a method. See Table 6-28 for a description of the register contents.

Type: Read/write/update, read only
Offset: E8h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-28. Multifunction Select Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7	RSVD	R	Reserved. This read-only bit is for internal use only.
6–4	RSVD	R	Reserved. Bits 6–4 return 0s when read.
3–0	MFUNC_SEL	R/W/U	Power state. This 4-bit field is used to set the TSB83AA23 device power state and is encoded as follows: 0000 = General-purpose input/output 0001 = CYCLEIN 0010 = CYCLEOUT 0011 = $\overline{\text{PCI\_CLKRUN}}$ 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved

6.1.30 Miscellaneous Configuration Register

The miscellaneous configuration register provides miscellaneous PCI-related configuration. See Table 6-29 for a description of the register contents.

Type: Read/write, read only
Offset: F0h
Default: 0000 0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 6-29. Miscellaneous Configuration Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	PME_D3COLD	R/W	$\overline{\text{PCI\_PME}}$ support from $D3_{cold}$. This bit programs bit 15 (PME_D3COLD) in the power management capabilities register at offset 46h in the PCI configuration space (see Section 6.1.30, *Power Management Capabilities Register*).
14–11	RSVD	R	Reserved. Bits 14–11 return 0s when read.
10	Ignore_ IntMask.masterInt Enable_for_pme	R/W	Ignore_IntMask.masterIntEnable_for_pme generation. When set to 1, this bit causes PME generation behavior to be changed. Also, when set to 1, this bit causes bit 26 of the OHCI vendor ID register at OHCI offset 40h (see Section 6.2.15, *OHCI Vendor ID Register*) to read 1; otherwise, bit 26 reads 0. 0 = PME behavior generated from unmasked interrupt bits and bit 31 (masterIntEnable) in the interrupt mask register at OHCI offset 88h (see Section 6.2.22, *Interrupt Mask Register*) (default) 1 = PME behavior does not depend on the value of bit 31 (masterIntEnable).
9–8	MR_ENHANCE	R/W	This field selects the read command behavior of the PCI master. 00 = Memory read line (default) 01 = Memory read 10 = Memory read multiple 11 = Reserved
7	RSVD	R	Reserved. Bit 7 returns 0 when read.
6	CARDBUS	R/W	CardBus. When bit 6 is set to 1, CardBus register support is enabled, that is, the CardBus base register and CardBus CIS pointer are valid. Bit 6 is only set if a serial EEPROM is present and contains a valid CIS. If bit 6 is set to 1, a valid CIS must be implemented in the EEPROM at an offset pointed to in EEPROM word 0x14, bits 7–3.
5	RSVD	R	Reserved. Bit 5 returns 0 when read.
4	DIS_TGT_ABT	R/W	Bit 4 defaults to 1, disabling the target abort behavior when accesses are made to PHY clock domain registers while no clock is present. Bit 4 can be set to 0 to provide OHCI-Lynx™-compatible target abort signaling. When this bit is set to 1, it enables the no-target-abort mode, in which the TSB83AA23 device returns indeterminate data instead of signaling target abort. The TSB83AA23 LLC is divided into the PCI_CLK and SCLK domains. If software tries to access registers in the link that are not active because SCLK is disabled, a target abort is issued by the link. On some systems, this can cause a problem resulting in a fatal system error. Enabling this bit allows the link to respond to these types of requests by returning FFh. It is recommended that this bit be set to 1.
3	RSVD	R	Reserved. Bit 3 returns 0 when read.
2	DISABLE_ SCLKGATE	R/W	When bit 2 is set to 1, the internal SCLK runs identically with the chip input. This is a test feature only and must be cleared to 0 (all applications).
1	DISABLE_PCIGATE	R/W	When bit 1 is set to 1, the internal PCI clock runs identically with the chip input. This is a test feature only and must be cleared to 0 (all applications).
0	KEEP_PCLK	R/W	When bit 0 is set to 1, the PCI clock always is kept running through the $\overline{\text{PCI\_CLKRUN}}$ protocol. When this bit is cleared, the PCI clock can be stopped using $\overline{\text{PCI\_CLKRUN}}$.

6.1.31 LLC Section Enhancement Control Register

The LLC section enhancement control register implements TI proprietary bits that are initialized by software or by a serial EEPROM, if present. After these bits are set to 1, their functionality is enabled only if bit 22 (aPhyEnhanceEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1. See Table 6-30 for a description of the register contents.

Type: Read/write, read only
Offset: F4h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-30. LLC Section Enhancement Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	DisableATPipelining	R/W	Disable AT pipelining. When bit 15 is set to 1, out-of-order AT pipelining is disabled.
14	EnableDraft	R/W	Enable OHCI 1.2 draft features. When bit 14 is set to 1, it enables some features beyond the OHCI 1.1 specification. Specifically, this enables HCControl.LPS to be cleared by writing a 1 to the HCControlClear.LPS bit and enables the link to set bit 9 in the xferStatus field of AR and IR ContextControl registers.
13–12	atx_thresh	R/W	This field sets the initial AT threshold value, which is used until the AT FIFO is under run. When the TSB83AA23 device retries the packet, it uses a 2K-byte threshold resulting in a store-and-forward operation. 00 = 4K-byte threshold, resulting in a store-and-forward operation (default) 01 = 1.7K-byte threshold 10 = 1K-byte threshold 11 = 512-byte threshold These bits fine-tune the asynchronous transmit threshold. Changing this value can increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, then the remaining data must be received before the AT FIFO is emptied; otherwise, an under run condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation—that is, wait until it has the complete packet in the FIFO before retransmitting it on the second attempt, to ensure delivery. An AT threshold of 4K results in store-and-forward operation, which means that asynchronous data is not transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 4K results in only complete packets being transmitted. This device always uses store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 6.2.3, *Asynchronous Transmit Retries Register*) is cleared.
11–10	RSVD	R	Reserved. Bits 11–10 return 0s when read.
9	enab_aud_ts	R/W	Enable audio/music CIP timestamp enhancement. When bit 9 is set to 1, the enhancement is enabled for audio/music CIP transmit streams (FMT = 10h).
8	enab_dv_ts	R/W	Enable DV CIP timestamp enhancement. When bit 8 is set to 1, the enhancement is enabled for DV CIP transmit streams (FMT = 00h).
7	enab_unfair	R/W	Enable asynchronous priority requests. OHCI-Lynx compatible. Setting bit 7 to 1 enables the LLC section to respond to requests with priority arbitration. It is recommended that this bit be set to 1.
6	RSVD	R	Bit 6 is not assigned in the TSB83AA23 follow-on products because this location, which is loaded by the serial EEPROM from the enhancements field, corresponds to bit 23 (programPhyEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*).
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2	enab_insert_idle	R/W	Enable insert idle. OHCI-Lynx compatible. When the PHY section has control of the PHY_CTL0–PHY_CTL1 control lines and PHY_DATA0–PHY_DATA7 data lines and the link requests control, the PHY section drives 11b on the PHY_CTL0–PHY_CTL1 lines. The LLC section can then start driving these lines immediately. Setting bit 2 to 1 inserts an idle state, so the link waits one clock cycle before it starts driving the lines (turnaround time).
1	enab_accel	R/W	Enable acceleration enhancements. OHCI-Lynx compatible. When bit 1 is set to 1, the PHY section is notified that the LLC section supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that bit 1 be set to 1.
0	RSVD	R	Reserved. Bit 0 returns 0 when read.

6.1.32 Subsystem Access Register

During a write to the subsystem access register, the value written updates the subsystem identification register. The system ID value written to this register also can be read back from this register. See Table 6-31 for a description of the register contents.

Type: Read/write
Offset: F8h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-31. Subsystem Access Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	SUBDEV_ID	R/W	Subsystem device ID alias. This field indicates the subsystem device ID.
15–0	SUBVEN_ID	R/W	Subsystem vendor ID alias. This field indicates the subsystem vendor ID.

6.1.33 GPIO Control Register

The GPIO control register has the control and status bits for the GPIO2 and GPIO3 ports. See Table 6-32 for a description of the register contents.

Type: Read/write/update, read/write, read only
Offset: FCh
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-32. GPIO Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	RSVD	R	Reserved. Bits 31–24 return 0s when read.
23	INT_EN	R/W	When bit 23 is set to 1, a TSB83AA23 general-purpose interrupt event occurs on a level change of the GPIO input. This event can generate an interrupt, with mask and event status reported through the interrupt mask register at OHCI offset 88h/8Ch (see Section 6.2.22, *Interrupt Mask Register*) and the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*).
22	RSVD	R	Reserved. Bit 22 returns 0 when read.
21	GPIO_INV	R/W	GPIO polarity invert. When bit 21 is set to 1, the polarity of GPIO is inverted.
20	GPIO_ENB	R/W	GPIO enable control. When bit 20 is set to 1, the output is enabled. Otherwise, the output is high impedance.
19–17	RSVD	R	Reserved. Bits 19–17 return 0s when read.
16	GPIO_DATA	RWU	GPIO data. Reads from bit 16 return the logical value of the input to GPIO. Writes to this bit update the value to drive to GPIO when the output is enabled.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

6.2 OHCI Registers

The OHCI registers defined by the *1394 Open Host Controller Interface Specification* are memory mapped into a 2K-byte region of memory pointed to by the OHCI base address register at offset 10h in PCI configuration space (see Section 6.1.11, *OHCI Base Address Register*). These registers are the primary interface for controlling the TSB83AA23 IEEE 1394 link function.

This section provides the register interface and bit descriptions. Several set/clear register pairs in this programming model are implemented to solve various issues with typical read-modify-write control registers. There are two addresses for a set/clear register, RegisterSet and RegisterClear. See Table 6-33 for a register listing. A 1 bit written to RegisterSet causes the corresponding bit in the set/clear register to be set to 1; a 0 bit leaves the corresponding bit unaffected. A 1 bit written to RegisterClear causes the corresponding bit in the set/clear register to be cleared; a 0 bit leaves the corresponding bit in the set/clear register unaffected.

Typically, a read from either RegisterSet or RegisterClear returns the contents of the set or clear register, respectively. However, sometimes reading the RegisterClear provides a masked version of the set or clear register. The interrupt event register is an example of this behavior.

Table 6-33. OHCI Register Map

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
—	OHCI version	Version	00h
	GUID ROM	GUID_ROM	04h
	Asynchronous transmit retries	ATRetries	08h
	CSR data	CSRData	0Ch
	CSR compare data	CSRCompareData	10h
	CSR control	CSRControl	14h
	Configuration ROM header	ConfigROMhdr	18h
	Bus identification	BusID	1Ch
	Bus options	BusOptions	20h
	GUID high	GUIDHi	24h
	GUID low	GUIDLo	28h
	Reserved	—	2Ch–30h
	Configuration ROM mapping	ConfigROMmap	34h
	Posted write address low	PostedWriteAddressLo	38h
	Posted write address high	PostedWriteAddressHi	3Ch
	OHCI vendor ID	VendorID	40h
	Reserved	—	44h–4Ch
	Host controller control	HCControlSet	50h
		HCControlClr	54h
	Reserved	—	58h–5Ch
Self-ID	Reserved	—	60h
	Self-ID buffer pointer	SelfIDBuffer	64h
	Self-ID count	SelfIDCount	68h
	Reserved	—	6Ch

Table 6-33. OHCI Register Map (continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
—	Isochronous receive channel mask high	IRChannelMaskHiSet	70h
		IRChannelMaskHiClear	74h
	Isochronous receive channel mask low	IRChannelMaskLoSet	78h
		IRChannelMaskLoClear	7Ch
	Interrupt event	IntEventSet	80h
		IntEventClear	84h
	Interrupt mask	IntMaskSet	88h
		IntMaskClear	8Ch
	Isochronous transmit interrupt event	IsoXmitIntEventSet	90h
		IsoXmitIntEventClear	94h
	Isochronous transmit interrupt mask	IsoXmitIntMaskSet	98h
		IsoXmitIntMaskClear	9Ch
—	Isochronous receive interrupt event	IsoRecvIntEventSet	A0h
		IsoRecvIntEventClear	A4h
	Isochronous receive interrupt mask	IsoRecvIntMaskSet	A8h
		IsoRecvIntMaskClear	ACh
	Initial bandwidth available	IntBandwidthAvailable	B0h
	Initial channels available high	IntChannelHiAvailable	B4h
	Initial channels available low	IntChannelLoAvailable	B8h
	Reserved	—	BCh–D8h
	Fairness control	FairnessControl	DCh
	LLC section control	LinkControlSet	E0h
		LinkControlClear	E4h
	Node identification	NodeID	E8h
	PHY layer control	PhyControl	ECh
	Isochronous cycle timer	Isocyctimer	F0h
	Reserved	—	F4h–FCh
	Asynchronous request filter high	AsyncRequestFilterHiSet	100h
		AsyncRequestFilterHiClear	104h
	Asynchronous request filter low	AsyncRequestFilterLoSet	108h
		AsyncRequestFilterloClear	10Ch
	Physical request filter high	PhysicalRequestFilterHiSet	110h
		PhysicalRequestFilterHiClear	114h
	Physical request filter low	PhysicalRequestFilterLoSet	118h
		PhysicalRequestFilterloClear	11Ch
	Physical upper bound	PhysicalUpperBound	120h
	Reserved	—	124h–17Ch
Asynchronous Request Transmit [ATRQ]	Asynchronous context control	ContextControlSet	180h
		ContextControlClear	184h
	Reserved	—	188h
	Asynchronous context command pointer	CommandPtr	18Ch
	Reserved	—	190h–19Ch
Asynchronous Response Transmit [ATRS]	Asynchronous context control	ContextControlSet	1A0h
		ContextControlClear	1A4h
	Reserved	—	1A8h
	Asynchronous context command pointer	CommandPtr	1ACh
	Reserved	—	1B0h–1BCh

Table 6-33. OHCI Register Map (continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Asynchronous Request Receive [ARRQ]	Asynchronous context control	ContextControlSet	1C0h
		ContextControlClear	1C4h
	Reserved	—	1C8h
	Asynchronous context command pointer	CommandPtr	1CCh
	Reserved	—	1D0h–1DCh
Asynchronous Response Receive [ARRS]	Asynchronous context control	ContextControlSet	1E0h
		ContextControlClear	1E4h
	Reserved	—	1E8h
	Asynchronous context command pointer	CommandPtr	1ECh
	Reserved	—	1F0h–1FCh
Isochronous Transmit Context n n = 0, 1, 2, 3, …, 7	Isochronous transmit context control	ContextControlSet	200h + 16*n
		ContextControlClear	204h + 16*n
	Reserved	—	208h + 16*n
	Isochronous transmit context command pointer	CommandPtr	20Ch + 16*n
	Reserved	—	280h–3FCh
Isochronous Receive Context n n = 0, 1, 2, 3	Isochronous receive context control	ContextControlSet	400h + 32*n
		ContextControlClear	404h + 32*n
	Reserved	—	408h + 32*n
	Isochronous receive context command pointer	CommandPtr	40Ch + 32*n
	Isochronous receive context match	ContextMatch	410h + 32*n

6.2.1 OHCI Version Register

The OHCI version register indicates the OHCI version support and whether or not the serial EEPROM is present. See Table 6-34 for a description of the register contents.

Type: Read only
Offset: 00h
Default: 0X01 0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 6-34. OHCI Version Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	RSVD	R	Reserved. Bits 31–25 return 0s when read.
24	GUID_ROM	R	The TSB83AA23 device sets bit 24 to 1 if the serial EEPROM is detected. If the serial EEPROM is present, the Bus_Info_Block is automatically loaded on system (hardware) reset.
23–16	version	R	Major version of the OHCI. The TSB83AA23 device is compliant with the *1394 Open Host Controller Interface Specification* (Revision 1.1); thus, this field reads 01h.
15–8	RSVD	R	Reserved. Bits 15–8 return 0s when read.
7–0	revision	R	Minor version of the OHCI. The TSB83AA23 device is compliant with the *1394 Open Host Controller Interface Specification* (Revision 1.1); thus, this field reads 10h.

6.2.2 GUID ROM Register

The GUID ROM register accesses the serial EEPROM and is applicable only if bit 24 (GUID_ROM) in the OHCI version register at OHCI offset 00h (see Section 6.2.1, *OHCI Version Register*) is set to 1. See Table 6-35 for a description of the register contents.

Type: Read/set/update, read/update, read only
Offset: 04h
Default: 00XX 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-35. GUID ROM Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	addrReset	RSU	Software sets bit 31 to 1 to reset the GUID ROM address to 0. When the TSB83AA23 device completes the reset, it clears this bit. The TSB83AA23 device does not automatically fill bits 23–16 (rdData field) with the 0^{th} byte.
30–26	RSVD	R	Reserved. Bits 30–26 return 0s when read.
25	rdStart	RSU	A read of the currently addressed byte is started when bit 25 is set to 1. This bit is automatically cleared when the TSB83AA23 device completes the read of the currently addressed GUID ROM byte.
24	RSVD	R	Reserved. Bit 24 returns 0 when read.
23–16	rdData	RU	This field represents the data read from the GUID ROM.
15–8	RSVD	R	Reserved. Bits 15–8 return 0s when read.
7–0	miniROM	R	Mini ROM. The TSB83AA23 device uses bits 7–0 to indicate the first byte location of the mini-ROM image in the GUID ROM. A value of 00h in this field indicates that no mini ROM is implemented.

6.2.3 *Asynchronous Transmit Retries Register*

The asynchronous transmit retries register indicates the number of times the TSB83AA23 device attempts a retry for asynchronous DMA request transmit and for asynchronous physical and DMA response transmit. See Table 6-36 for a description of the register contents.

Type: Read/write, read only
Offset: 08h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-36. Asynchronous Transmit Retries Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–29	secondLimit	R	The second limit field returns 0s when read, because outbound dual-phase retry is not implemented.
28–16	cycleLimit	R	The cycle limit field returns 0s when read, because outbound dual-phase retry is not implemented.
15–12	RSVD	R	Reserved. Bits 15–12 return 0s when read.
11–8	maxPhysRespRetries	R/W	This field tells the physical response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.
7–4	maxATRespRetries	R/W	This field tells the asynchronous transmit response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.
3–0	maxATReqRetries	R/W	This field tells the asynchronous transmit DMA request unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.

6.2.4 CSR Data Register

The CSR data register accesses the bus management CSR registers from the host through compare-swap operations. This register contains the data to be stored in a CSR if the compare is successful.

Type: Read only
Offset: 0Ch
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

6.2.5 CSR Compare Data Register

The CSR compare register accesses the bus management CSR registers from the host through compare-swap operations. This register contains the data to be compared with the existing value of the CSR resource.

Type: Read only
Offset: 10h
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

6.2.6 CSR Control Register

The CSR control register accesses the bus management CSR registers from the host through compare-swap operations. This register controls the compare-swap operation and selects the CSR resource. See Table 6-37 for a description of the register contents.

Type: Read/write, read/update, read only
Offset: 14h
Default: 8000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X

Table 6-37. CSR Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	csrDone	RU	Bit 31 is set to 1 by the TSB83AA23 device when a compare-swap operation is complete. It is cleared when this register is written.
30–2	RSVD	R	Reserved. Bits 30–2 return 0s when read.
1–0	csrSel	R/W	This field selects the CSR resource as follows: 00 = BUS_MANAGER_ID 01 = BANDWIDTH_AVAILABLE 10 = CHANNELS_AVAILABLE_HI 11 = CHANNELS_AVAILABLE_LO

6.2.7 Configuration ROM Header Register

The configuration ROM header register externally maps to the first quadlet of the 1394 configuration ROM, offset FFFF F000 0400h. See Table 6-38 for a description of the register contents.

Type: Read/write
Offset: 18h
Default: 0000 XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-38. Configuration ROM Header Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	info_length	R/W	IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
23–16	crc_length	R/W	IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
15–0	rom_crc_value	R/W	IEEE 1394 bus-management field. Must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1. The reset value is undefined if no serial EEPROM is present. If a serial EEPROM is present, then this field is loaded from the serial EEPROM.

6.2.8 Bus Identification Register

The bus identification register externally maps to the first quadlet in the Bus_Info_Block and contains the constant 3133 3934h, which is the ASCII value of 1394.

Type: Read only
Offset: 1Ch
Default: 3133 3934h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	0

6.2.9 Bus Options Register

The bus options register externally maps to the second quadlet of the Bus_Info_Block. See Table 6-39 for a description of the register contents.

Type: Read/write, read only
Offset: 20h
Default: X0XX B0X2h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	0	0	0	0	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	1	0	1	1	0	0	0	0	X	X	0	0	0	0	1	0

Table 6-39. Bus Options Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	irmc	R/W	Isochronous resource-manager capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
30	cmc	R/W	Cycle master capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
29	isc	R/W	Isochronous support capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
28	bmc	R/W	Bus manager capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
27	pmc	R/W	Power-management capable. IEEE 1394 bus-management field. When bit 27 is set to 1, this indicates that the node is power-management capable. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
26–24	RSVD	R	Reserved. Bits 26–24 return 0s when read.
23–16	cyc_clk_acc	R/W	Cycle master clock accuracy, in parts per million. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1.
15–12	max_rec	R/W	Maximum request. IEEE 1394 bus-management field. Hardware initializes this field to indicate the maximum number of bytes in a block request packet that is supported by the implementation. This value, max_rec_bytes must be 512 or greater, and is calculated by 2^(max_rec + 1). Software can change this field; however, this field must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1. A received block-write request packet with a length greater than max_rec_bytes can generate an ack_type_error. This field is not affected by a software reset, and defaults to a value indicating 4096 bytes on a system (hardware) reset.
11–8	RSVD	R	Reserved. Bits 11–8 return 0s when read.
7–6	g	R/W	Generation counter. This field is incremented if any portion of the configuration ROM has been incremented since the prior bus reset.
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2–0	Lnk_spd	R	Link speed. This field returns 011, indicating that the link speeds of 100 Mbps, 200 Mbps, 400 Mbps and 800 Mbps are supported.

6.2.10 GUID High Register

The GUID high register represents the upper quadlet in a 64-bit global unique ID (GUID), which maps to the third quadlet in the Bus_Info_Block. This register contains node_vendor_ID and chip_ID_hi fields. This register initializes to 0s on a system (hardware) reset, which is an illegal GUID value. If a serial EEPROM is detected, the contents of this register are loaded through the serial EEPROM interface after a GRST#. At that point, the contents of this register cannot be changed. If no serial EEPROM is detected, the contents of this register are loaded by the BIOS. At that point, the contents of this register cannot be changed. All bits in this register are reset by GRST# only.

Type: Read only
Offset: 24h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2.11 GUID Low Register

The GUID low register represents the lower quadlet in a 64-bit global unique ID (GUID), which maps to chip_ID_lo in the Bus_Info_Block. This register initializes to 0s on a system (hardware) reset and behaves identically to the GUID high register at OHCI offset 24h (see Section 6.2.10, *GUID High Register*).

Type: Read only
Offset: 28h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2.12 Configuration ROM Mapping Register

The configuration ROM mapping register contains the start address within system memory that maps to the start address of 1394 configuration ROM for this node. See Table 6-40 for a description of the register contents.

Type: Read/write, read only
Offset: 34h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-40. Configuration ROM Mapping Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–10	configROMaddr	R/W	If a quadlet read request to 1394 offset FFFF F000 0400h through offset FFFF F000 07FFh is received, the low-order 10 bits of the offset are added to this register to determine the host memory address of the read request.
9–0	RSVD	R	Reserved. Bits 9–0 return 0s when read.

6.2.13 Posted Write Address Low Register

The posted write address low register communicates error information if a write request is posted and an error occurs while writing the posted data packet. See Table 6-41 for a description of the register contents.

Type: Read/update
Offset: 38h
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-41. Posted Write Address Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	offsetLo	RU	The lower 32 bits of the 1394 destination offset of the write request that failed

6.2.14 Posted Write Address High Register

The posted write address high register communicates error information if a write request is posted and an error occurs while writing the posted data packet. See Table 6-42 for a description of the register contents.

Type: Read/update
Offset: 3Ch
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-42. Posted Write Address High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	sourceID	RU	This field is the 10-bit bus number (bits 31–22) and 6-bit node number (bits 21–16) of the node that issued the write request that failed.
15–0	offsetHi	RU	The upper 16 bits of the 1394 destination offset of the write request that failed

6.2.15 OHCI Vendor ID Register

The OHCI vendor ID register provides the company ID of an organization that specifies any vendor-unique registers or features. The TSB83AA23 device implements several unique features with regards to OHCI. Therefore, bits 23–0 are programmed with Texas Instruments OUI, 08 0028h. See Table 6-43 for a description of the register contents.

Type: Read/update, read only
Offset: 40h
Default: 0X08 0028h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	X	X	0	0	0	0	0	1	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Table 6-43. Vendor ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–27	RSVD	R	Reserved. Bits 31–27 return 0s when read.
26	PME_Enhance	RU	Bit 26 is conditionally set based on the value of bit 10 (Ignore IntMask.masterIntEnable_for_pme) in the miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 6.1.30, *Miscellaneous Configuration Register*). If bit 10 is set to 1, bit 26 is set to 1 to indicate that the device supports the generation of PME regardless of the status of bit 31 (masterIntEnable) in the interrupt mask register at OHCI offset 88h (see Section 6.2.22, *Interrupt Mask Register*). If bit 10 is not set, bit 26 returns 0.
25	OHCI12_draft	RU	OHCI 1.2 draft features. Bit 25 is conditionally set based on the value of bit 14 (EnableDraft) in the link enhancement control register at offset F4h in the PCI configuration space (see Section 6.1.31, *LLC Section Enhancement Control Register*). If bit 14 is set to 1, bit 25 is set to 1 to indicate that the device supports some features that have been defined in the OHCI 1.2 specification draft. If bit 14 is not set, bit 25 returns 0.
24	Iso_enhancements	R	Isochronous enhancements. Bit 24 is set to 1 indicating that it supports the isochronous enhancements defined in Sections 1.4 and 1.5.
23–0	vendorCompanyID	R	Vendor company organizational unique ID. This field returns Texas Instruments OUI, 08 0028h, indicating that the device supports unique features defined by TI.

6.2.16 Host Controller Control Register

The host controller control set/clear register pair provides flags for controlling the TSB83AA23 device. See Table 6-44 for a description of the register contents.

Type: Read/set/clear/update, read/set/update, read/set/clear, read/clear, read only
Offset: 50h Set register
54h Clear register
Default: X00X 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	X	0	0	0	0	0	0	0	0	0	0	0	X	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-44. Host Controller Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	BIBimageValid	RSU	When bit 31 is set to 1, the TSB83AA23 physical response unit is enabled to respond to block read requests to host configuration ROM and to the mechanism for automatically updating configuration ROM. Software creates a valid image of the bus_info_block in host configuration ROM before setting this bit. When this bit is cleared, the TSB83AA23 device returns ack_type_error on block read requests to host configuration ROM. Also, when this bit is cleared and a 1394 bus reset occurs, the configuration ROM mapping register at OHCI offset 34h (see Section 6.2.12, *Configuration ROM Mapping Register*), configuration ROM header register at OHCI offset 18h (see Section 6.2.7, *Configuration ROM Header Register*), and bus options register at OHCI offset 20h (see Section 6.2.9, *Bus Options Register*) are not updated. Software can set this bit only when bit 17 (linkEnable) is 0. Once bit 31 is set to 1, it can be cleared by a system (hardware) reset, a software reset, or if a fetch error occurs when the TSB83AA23 device loads bus_info_block registers from host memory.
30	noByteSwapData	RSC	Bit 30 controls whether physical accesses to locations outside the TSB83AA23 device itself, as well as any other DMA data accesses, are byte swapped.

Table 6-44. Host Controller Control Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
29	ack_Tardy_enable	RSC	Bit 29 controls the acknowledgment of ack_tardy. When bit 29 is set to 1, ack_tardy can be returned as an acknowledgment to configuration ROM accesses from 1394 to the TSB83AA23 device, including accesses to the bus_info_block. The TSB83AA23 device returns ack_tardy to all other asynchronous packets addressed to the TSB83AA23 node. When the TSB83AA23 device sends ack_tardy, bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) is set to 1 to indicate the attempted asynchronous access. Software ensures that bit 27 (ack_tardy) in the interrupt event register is 0. Software also unmasks wake-up interrupt events such as bit 19 (Phy) and bit 27 (ack_tardy) in the interrupt event register before placing the device into D1. Software does not set this bit if the TSB83AA23 node is the 1394 bus manager.
28–24	RSVD	R	Reserved. Bits 28–24 return 0s when read.
23	programPhyEnable	RC	Bit 23 informs upper-level software that lower-level software has consistently configured the IEEE Std 1394a-2000 enhancements in the LLC and PHY sections. When this bit is 1, generic software such as the OHCI driver is responsible for configuring IEEE Std 1394a-2000 enhancements in the PHY section and bit 22 (aPhyEnhanceEnable) in the TSB83AA23 device. When this bit is 0, the generic software cannot modify the IEEE Std 1394a-2000 enhancements in the TSB83AA23 and cannot interpret the setting of bit 22 (aPhyEnhanceEnable). This bit is initialized from the serial EEPROM.
22	aPhyEnhanceEnable	RSC	When bits 23 (programPhyEnable) and 17 (linkEnable) are 1, the OHCI driver can set bit 22 to 1 to use all IEEE Std 1394a-2000 enhancements. When bit 23 (programPhyEnable) is cleared to 0, the software does not change PHY section enhancements or this bit.
21–20	RSVD	R	Reserved. Bits 21–20 return 0s when read.
19	LPS	RSC	Bit 19 controls the link power status. Software must set this bit to 1 to permit LLC section-PHY section communication. A 0 prevents LLC section-PHY section communication. The OHCI-link is divided into two clock domains (PCI_CLK and PHY_SCLK). If software tries to access any register in the PHY_SCLK domain while the PHY_SCLK is disabled, a target abort is issued by the link. This problem can be avoided by setting bit 4 (DIS_TGT_ABT) in the miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 6.1.30, *Miscellaneous Configuration Register*). This allows the link to respond to these types of request by returning all Fs (hex). OHCI registers at offsets DCh–F0h and 100h–11Ch are in the PHY_SCLK domain. After setting LPS, software must wait approximately 10 ms before attempting to access any of the OHCI registers. This gives the PHY_SCLK time to stabilize.
18	postedWriteEnable	RSC	Bit 18 enables (1) or disables (0) posted writes. Software changes this bit only when bit 17 (linkEnable) is 0.
17	linkEnable	RSC	Bit 17 is cleared to 0 by either a system (hardware) or software reset. Software must set this bit to 1 when the system is ready to begin operation and then force a bus reset. This bit is necessary to keep other nodes from sending transactions before the local system is ready. When this bit is cleared, the TSB83AA23 device is logically and immediately disconnected from the 1394 bus, no packets are received or processed, nor are packets transmitted.
16	SoftReset	RSCU	When bit 16 is set to 1, all TSB83AA23 states are reset, all FIFOs are flushed, and all OHCI registers are set to their system (hardware) reset values, unless otherwise specified. PCI registers are not affected by this bit. This bit remains set to 1 while the software reset is in progress and reverts back to 0 when the reset has completed.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

6.2.17 Self-ID Buffer Pointer Register

The self-ID buffer pointer register points to the 2K-byte-aligned base address of the buffer in host memory where the self-ID packets are stored during bus initialization. Bits 31–11 are read/write accessible. Bits 10–0 are reserved, and return 0s when read.

Type: Read/write, read only
Offset: 64h
Default: XXXX XX00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

6.2.18 Self-ID Count Register

The self-ID count register keeps a count of the number of times the bus self-D process has occurred, flags self-ID packet errors, and keeps a count of the self-ID data in the self-ID buffer. See Table 6-45 for a description of the register contents.

Type: Read/update, read only
Offset: 68h
Default: X0XX 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-45. Self-ID Count Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	selfIDError	RU	When bit 31 is set to 1, an error was detected during the most recent self-ID packet reception. The contents of the self-ID buffer are undefined. This bit is cleared after a self-ID reception in which no errors are detected. Aan error can be a hardware error or a host bus write error.
30–24	RSVD	R	Reserved. Bits 30–24 return 0s when read.
23–16	selfIDGeneration	RU	The value in this field increments each time a bus reset is detected. This field rolls over to 0 after reaching 255.
15–11	RSVD	R	Reserved. Bits 15–11 return 0s when read.
10–2	selfIDSize	RU	This field indicates the number of quadlets that have been written into the self-ID buffer for the current bits 23–16 (selfIDGeneration field). This includes the header quadlet and the self-ID data. This field is cleared to 0s when the self-ID reception begins.
1–0	RSVD	R	Reserved. Bits 1–0 return 0s when read.

6.2.19 Isochronous Receive Channel Mask High Register

The isochronous receive channel mask high set/clear register enables packet receives from the upper 32 isochronous data channels. A read from either the set register or clear register returns the content of the isochronous receive channel mask high register. See Table 6-46 for a description of the register contents.

Type: Read/set/clear
Offset: 70h Set register
74h Clear register
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-46. Isochronous Receive Channel Mask High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel63	RSC	When bit 31 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 63 (bit number + 32).
30	isoChannel62	RSC	When bit 30 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 62 (bit number + 32).
29–2	isoChannel*n*	RSC	Bits 29 through 2 (isoChannel*n*, where *n* = 61, 60, 59, ..., 34) follow the same pattern and bits 31 and 30.
1	isoChannel33	RSC	When bit 1 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 33 (bit number + 32).
0	isoChannel32	RSC	When bit 0 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 32 (bit number + 32).

6.2.20 Isochronous Receive Channel Mask Low Register

The isochronous receive channel mask low set/clear register enables packet receives from the lower 32 isochronous data channels. See Table 6-47 for a description of the register contents.

Type: Read/set/clear
Offset: 78h Set register
7Ch Clear register
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-47. Isochronous Receive Channel Mask Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel31	RSC	When bit 31 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 31.
30	isoChannel30	RSC	When bit 30 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 30.
29–2	isoChannel*n*	RSC	Bits 29 through 2 (isoChannel*n*, where *n* = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	isoChannel1	RSC	When bit 1 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 1.
0	isoChannel0	RSC	When bit 0 is set to 1, the TSB83AA23 device is enabled to receive from isochronous channel number 0.

6.2.21 Interrupt Event Register

The interrupt event set/clear register reflects the state of the various TSB83AA23 interrupt sources. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register.

This register is fully compliant with *1394 Open Host Controller Interface Specification*, and the TSB83AA23 device adds a vendor-specific interrupt function to bit 30. When the interrupt event register is read, the return value is the bit-wise AND function of the interrupt event and interrupt mask registers. See Table 6-48 for a description of the register contents

Type: Read/set/clear/update, read/set/clear, read/update, read only
Offset: 80h Set register
84h Clear register [returns the content of the interrupt event register bit-wise ANDed with the interrupt mask register when read]
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 6-48. Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	RSVD	R	Reserved. Bit 31 returns 0 when read.
30	vendorSpecific	RSC	This vendor-specific interrupt event is reported when either of the general-purpose interrupts is asserted. The general-purpose interrupts are enabled by setting the corresponding bits INT_3EN and INT_2EN (bits 31 and 23, respectively) to 1 in the GPIO control register at offset FCh in the PCI configuration space (see Section 6.1.33, *GPIO Control Register*).
29	SoftInterrupt	RSC	Software interrupt. Bit 29 is used by software to generate a TSB83AA23 interrupt for its own use.
28	RSVD	R	Reserved. Bit 28 returns 0 when read.
27	ack_Tardy	RSCU	Bit 27 is set to 1 when bit 29 (ack_Tardy_enable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*) is set to 1 and any of the following conditions occurs: a. Data is present in the receive FIFO that is to be delivered to the host. b. The physical response unit is busy processing requests or sending responses. c. The TSB83AA23 device sent an ack_tardy acknowledgment.
26	PhyRegRcvd	RSCU	The bit is set to 1 when the TSB83AA23 device has received a PHY section register data byte, which can be read from bits 23–16 in the PHY section control register at OHCI offset ECh (see Section 6.2.33, *Phy Layer Control Register*).
25	cycleTooLong	RSCU	If bit 21 (cycleMaster) in the link control register at OHCI offset E0h/E4h (see Section 6.2.31, *LLC Section Control Register*) is set to 1, then this indicates that over 125 µs has elapsed between the start of sending a cycle-start packet and the end of a subaction gap. Bit 21 (cycleMaster) in the LLC section control register is cleared by this event.
24	unrecoverableError	RSCU	This event occurs when the TSB83AA23 device encounters any error that forces it to stop operations on any or all of its subunits, for example, when a DMA context sets its dead bit to 1. While bit 24 is set to 1, all normal interrupts for the context(s) that caused this interrupt are blocked from being set to 1.
23	cycleInconsistent	RSCU	A cycle start was received that had values for cycleSeconds and cycleCount fields that are different from the values in bits 31–25 (cycleSeconds field) and bits 24–12 (cycleCount field) in the isochronous cycle timer register at OHCI offset F0h (see Section 6.2.34, *Isochronous Cycle Timer Register*).
22	cycleLost	RSCU	A lost cycle is indicated when no cycle_start packet is sent or received between two successive cycleSynch events. A lost cycle can be predicted when a cycle_start packet does not immediately follow the first subaction gap after the cycleSynch event or if an arbitration reset gap is detected after a cycleSynch event without an intervening cycle start. Bit 22 can be set either when a lost cycle occurs or when logic predicts that one will occur.
21	cycle64Seconds	RSCU	A 1 indicates that the 7^{th} bit of the cycle second counter has changed.
20	cycleSynch	RSCU	Indicates that a new isochronous cycle has started. Bit 20 is set to 1 when the low-order bit of the cycle count toggles.
19	Phy	RSCU	Indicates that the PHY section requests an interrupt through a status transfer.
18	regAccessFail	RSCU	Indicates that an LLC section register access has failed due to a missing SCLK clock signal from the PHY section. When a register access fails, bit 18 is set to 1 before the next register access.
17	busReset	RSCU	A 1 indicates that the PHY section has entered bus-reset mode.
16	selfIDcomplete	RSCU	A self-ID packet stream has been received. It is generated at the end of the bus initialization process. Bit 16 is turned off simultaneously when bit 17 (busReset) is turned on.
15	selfIDcomplete2	RSCU	Secondary indication of the end of a self-ID packet stream. Bit 15 is set to 1 by the TSB83AA23 device when it sets bit 16 (selfIDcomplete), and retains its state, independent of bit 17 (busReset).
14–10	RSVD	R	Reserved. Bits 14–10 return 0s when read.
9	lockRespErr	RSCU	Indicates that the TSB83AA23 device sent a lock response for a lock request to a serial bus register, but did not receive an ack_complete.
8	postedWriteErr	RSCU	Indicates that a host bus error occurred while the TSB83AA23 device was trying to write a 1394 write request, which had already been given an ack_complete, into system memory.
7	isochRx	RU	Isochronous receive DMA interrupt. Indicates that one or more isochronous receive contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous receive interrupt event register at OHCI offset A0h/A4h (see Section 6.2.26, *Isochronous Receive Interrupt Event Register*) and isochronous receive interrupt mask register at OHCI offset A8h/ACh (see Section 6.2.24, *Isochronous Receive Interrupt Mask Register*). The isochronous receive interrupt event register indicates which contexts have been interrupted.

Table 6-48. Interrupt Event Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
6	isochTx	RU	Isochronous transmit DMA interrupt. Indicates that one or more isochronous transmit contexts have generated an interrupt. This is not a latched event, it is the logical OR of all bits in the isochronous transmit interrupt event register at OHCI offset 90h/94h (see Section 6.2.23, *Isochronous Transmit Interrupt Event Register*) and isochronous transmit interrupt mask register at OHCI offset 98h/9Ch (see Section 6.2.24, *Isochronous Transmit Interrupt Mask Register*). The isochronous transmit interrupt event register indicates which contexts have been interrupted.
5	RSPkt	RSCU	A 1 indicates that a packet was sent to an asynchronous receive response context buffer and the descriptor's xferStatus and resCount fields have been updated.
4	RQPkt	RSCU	A 1 indicates that a packet was sent to an asynchronous receive request context buffer and the descriptor's xferStatus and resCount fields have been updated.
3	ARRS	RSCU	Asynchronous receive response DMA interrupt. Bit 3 is conditionally set to 1 on completion of an ARRS DMA context command descriptor.
2	ARRQ	RSCU	Asynchronous receive request DMA interrupt. Bit 2 is conditionally set to 1 on completion of an ARRQ DMA context command descriptor.
1	respTxComplete	RSCU	Asynchronous response transmit DMA interrupt. Bit 1 is conditionally set to 1 on completion of an ATRS DMA command.
0	reqTxComplete	RSCU	Asynchronous request transmit DMA interrupt. Bit 0 is conditionally set to 1 on completion of an ATRQ DMA command.

6.2.22 Interrupt Mask Register

The interrupt mask set/clear register enables the various TSB83AA23 interrupt sources. Reads from either the set register or the clear register always return the contents of the interrupt mask register. In all cases except bit 31 (masterIntEnable) and bit 30 (VendorSpecific), the enables for each interrupt event align with the interrupt event register bits detailed in Table 6-48.

This register is fully compliant with *1394 Open Host Controller Interface Specification*, and the TSB83AA23 device adds a vendor-specific interrupt function to bit 30. See Table 6-49 for a description of the register contents.

Type: Read/set/clear/update, read/set/clear, read only
Offset: 88h Set register
8Ch Clear register
Default: XXXX 0XXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 6-49. Interrupt Mask Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	masterIntEnable	RSCU	Master interrupt enable. If bit 31 is set to 1, the external interrupts are generated in accordance with the interrupt mask register. If bit 31 is cleared, the external interrupts are not generated, regardless of the interrupt mask register settings.
30	VendorSpecific	RSC	When this bit and bit 30 (vendorSpecific) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this vendor-specific interrupt mask enables interrupt generation.
29	SoftInterrupt	RSC	When this bit and bit 29 (SoftInterrupt) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this soft-interrupt mask enables interrupt generation.
28	RSVD	R	Reserved. Bit 28 returns 0 when read.
27	ack_tardy	RSC	When this bit and bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this acknowledge-tardy interrupt mask enables interrupt generation.
26	PhyRegRcvd	RSC	When this bit and bit 26 (PhyRegRcvd) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this PHY-register interrupt mask enables interrupt generation.
25	cycleTooLong	RSC	When this bit and bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this cycle-too-long interrupt mask enables interrupt generation.
24	unrecoverableError	RSC	When this bit and bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this unrecoverable-error interrupt mask enables interrupt generation.
23	cycleInconsistent	RSC	When this bit and bit 23 (cycleInconsistent) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this inconsistent-cycle interrupt mask enables interrupt generation.
22	cycleLost	RSC	When this bit and bit 22 (cycleLost) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this lost-cycle interrupt mask enables interrupt generation.
21	cycle64Seconds	RSC	When this bit and bit 21 (cycle64Seconds) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this 64-second-cycle interrupt mask enables interrupt generation.
20	cycleSynch	RSC	When this bit and bit 20 (cycleSynch) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this isochronous-cycle interrupt mask enables interrupt generation.
19	Phy	RSC	When this bit and bit 19 (Phy) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this PHY-status-transfer interrupt mask enables interrupt generation.
18	regAccessFail	RSC	When this bit and bit 18 (regAccessFail) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this register-access-failed interrupt mask enables interrupt generation.
17	busReset	RSC	When this bit and bit 17 (busReset) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this bus-reset interrupt mask enables interrupt generation.
16	selfIDcomplete	RSC	When this bit and bit 16 (selfIDcomplete) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this self-ID-complete interrupt mask enables interrupt generation.
15	selfIDcomplete2	RSC	When this bit and bit 15 (selfIDcomplete2) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this second-self-ID-complete interrupt mask enables interrupt generation.
14–10	RSVD	R	Reserved. Bits 14–10 return 0s when read.
9	lockRespErr	RSC	When this bit and bit 9 (lockRespErr) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this lock-response-error interrupt mask enables interrupt generation.
8	postedWriteErr	RSC	When this bit and bit 8 (postedWriteErr) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this posted-write-error interrupt mask enables interrupt generation.
7	isochRx	RSC	When this bit and bit 7 (isochRx) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this isochronous-receive-DMA interrupt mask enables interrupt generation.

Table 6-49. Interrupt Mask Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
6	isochTx	RSC	When this bit and bit 6 (isochTx) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this isochronous-transmit-DMA interrupt mask enables interrupt generation.
5	RSPkt	RSC	When this bit and bit 5 (RSPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this receive-response-packet interrupt mask enables interrupt generation.
4	RQPkt	RSC	When this bit and bit 4 (RQPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this receive-request-packet interrupt mask enables interrupt generation.
3	ARRS	RSC	When this bit and bit 3 (ARRS) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this asynchronous-receive-response-DMA interrupt mask enables interrupt generation.
2	ARRQ	RSC	When this bit and bit 2 (ARRQ) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this asynchronous-receive-request-DMA interrupt mask enables interrupt generation.
1	respTxComplete	RSC	When this bit and bit 1 (respTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this response-transmit-complete interrupt mask enables interrupt generation.
0	reqTxComplete	RSC	When this bit and bit 0 (reqTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) are set to 1, this request-transmit-complete interrupt mask enables interrupt generation.

6.2.23 Isochronous Transmit Interrupt Event Register

The isochronous transmit interrupt event set/clear register reflects the interrupt state of the isochronous transmit contexts. An interrupt is generated on behalf of an isochronous transmit context if an OUTPUT_LAST* command completes and its interrupt bits are set to 1. On determining that the isochTx (bit 6) interrupt has occurred in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*), software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal, or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register. See Table 6-50 for a description of the register contents.

Type: Read/set/clear, read only
Offset: 90h Set register
94h Clear register (returns the contents of the isochronous transmit interrupt event register bit-wise ANDed with the isochronous transmit interrupt mask register when read)
Default: 0000 00XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Table 6-50. Isochronous Transmit Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7	isoXmit7	RSC	Isochronous transmit channel 7 caused the interrupt event register bit 6 (isochTx) interrupt.
6	isoXmit6	RSC	Isochronous transmit channel 6 caused the interrupt event register bit 6 (isochTx) interrupt.
5	isoXmit5	RSC	Isochronous transmit channel 5 caused the interrupt event register bit 6 (isochTx) interrupt.
4	isoXmit4	RSC	Isochronous transmit channel 4 caused the interrupt event register bit 6 (isochTx) interrupt.
3	isoXmit3	RSC	Isochronous transmit channel 3 caused the interrupt event register bit 6 (isochTx) interrupt.
2	isoXmit2	RSC	Isochronous transmit channel 2 caused the interrupt event register bit 6 (isochTx) interrupt.
1	isoXmit1	RSC	Isochronous transmit channel 1 caused the interrupt event register bit 6 (isochTx) interrupt.
0	isoXmit0	RSC	Isochronous transmit channel 0 caused the interrupt event register bit 6 (isochTx) interrupt.

6.2.24 Isochronous Transmit Interrupt Mask Register

The isochronous transmit interrupt mask set/clear register enables the isochTx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous transmit interrupt mask register. In all cases, the enables for each interrupt event align with the event register bits detailed in Table 6-50.

Type: Read/set/clear, read only
Offset: 98h Set register
9Ch Clear register
Default: 0000 00XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

6.2.25 Isochronous Receive Interrupt Event Register

The isochronous receive interrupt event set/clear register reflects the interrupt state of the isochronous receive contexts. An interrupt is generated on behalf of an isochronous receive context if an INPUT_* command completes and its interrupt bits are set to 1. On determining that the isochRx (bit 7) interrupt in the interrupt event register at OHCI offset 80h/84h (see Table 6-50, *Interrupt Event Register*) has occurred, software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal, or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register. See Table 6-51 for a description of the register contents.

Type: Read/set/clear, read only
Offset: A0h Set register
A4h Clear register (returns the contents of isochronous receive interrupt event register bit-wise ANDed with the isochronous receive mask register when read)
Default: 0000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Table 6-51. Isochronous Receive Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	RSVD	R	Reserved. Bits 31–4 return 0s when read.
3	isoRecv3	RSC	Isochronous receive channel 3 caused the interrupt event register bit 7 (isochRx) interrupt.
2	isoRecv2	RSC	Isochronous receive channel 2 caused the interrupt event register bit 7 (isochRx) interrupt.
1	isoRecv1	RSC	Isochronous receive channel 1 caused the interrupt event register bit 7 (isochRx) interrupt.
0	isoRecv0	RSC	Isochronous receive channel 0 caused the interrupt event register bit 7 (isochRx) interrupt.

6.2.26 Isochronous Receive Interrupt Mask Register

The isochronous receive interrupt mask set/clear register enables the isochRx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous receive interrupt mask register. In all cases, the enables for each interrupt event align with the isochronous receive interrupt event register bits detailed in Table 6-51.

Type: Read/set/clear, read only
Offset: A8h Set register
ACh Clear register
Default: 0000 000Xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

6.2.27 Initial Bandwidth Available Register

The initial bandwidth available register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 6-52 for a description of the register contents.

Type: Read/write, read only
Offset: B0h
Default: 0000 1333h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1

Table 6-52. Initial Bandwidth Available Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–13	RSVD	R	Reserved. Bits 31–13 return 0s when read.
12–0	InitBWAvailable	R/W	This field is reset to 1333h on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the BANDWIDTH_AVAILABLE CSR register on a $\overline{\text{G\_RST}}$, $\overline{\text{PCI\_RST}}$, or 1394 bus reset.

6.2.28 Initial Channels Available High Register

The initial channels available high register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 6-53 for a description of the register contents.

Type: Read/write
Offset: B4h
Default: FFFF FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 6-53. Initial Channels Available High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	InitChanAvailHi	R/W	This field is reset to FFFF FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_HI CSR register on a $\overline{\text{G\_RST}}$, $\overline{\text{PCI\_RST}}$, or 1394 bus reset.

6.2.29 Initial Channels Available Low Register

The initial channels available low register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 6-54 for a description of the register contents.

Type: Read/write
Offset: B8h
Default: FFFF FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 6-54. Initial Channels Available High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	InitChanAvailLo	R/W	This field is reset to FFFF FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_LO CSR register on a $\overline{\text{G\_RST}}$, $\overline{\text{PCI\_RST}}$, or 1394 bus reset.

6.2.30 Fairness Control Register

The fairness control register provides a mechanism by which software can direct the host controller to transmit multiple asynchronous requests during a fairness interval. See Table 6-55 for a description of the register contents.

Type: Read/write, read only
Offset: DCh
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-55. Fairness Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7–0	pri_req	R/W	This field specifies the maximum number of priority arbitration requests for asynchronous request packets that the link is permitted to make of the PHY section during a fairness interval.

6.2.31 LLC Section Control Register

The LLC section control set/clear register provides the control flags that enable and configure the link core protocol portions of the TSB83AA23 device. It contains controls for the receiver and cycle timer. See Table 6-56 for a description of the register contents.

Type: Read/set/clear/update, read/set/clear, read/set, read only
Offset: A8h Set register
ACh Clear register
Default: 00X0 0X00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	X	X	X	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0

Table 6-56. LLC Section Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–23	RSVD	R	Reserved. Bits 31–23 return 0s when read.
22	cycleSource	RSC	When bit 22 is set to 1, the cycle timer uses an external source (CYCLEIN) to determine when to roll over the cycle timer. When this bit is cleared, the cycle timer rolls over when the timer reaches 3072 cycles of the 24.576-MHz clock (125 µs).
21	cycleMaster	RSCU	When bit 21 is set to 1 and the PHY section has notified the LLC section that PHY section is root, the TSB83AA23 device generates a cycle-start packet every time the cycle timer rolls over, based on the setting of bit 22 (cycleSource). When bit 21 is cleared, the OHCI-Lynx accepts received cycle-start packets to maintain synchronization with the node which is sending them. Bit 21 is automatically cleared when bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) is set to 1. Bit 21 cannot be set to 1 until bit 25 (cycleTooLong) is cleared.
20	CycleTimerEnable	RSC	When bit 20 is set to 1, the cycle timer offset counts cycles of the 24.576-MHz clock and rolls over at the appropriate time, based on the settings of the above bits. When this bit is cleared, the cycle timer offset does not count.
19–11	RSVD	R	Reserved. Bits 19–11 return 0s when read.
10	RcvPhyPkt	RSC	When bit 10 is set to 1, the receiver accepts incoming PHY packets into the AR request context if the AR request context is enabled. This bit does not control receipt of self-ID packets.
9	RcvSelfID	RSC	When bit 9 is set to 1, the receiver accepts incoming self-ID packets. Before setting this bit to 1, software must ensure that the self-ID buffer pointer register contains a valid address.
8–7	RSVD	R	Reserved. Bits 8–7 return 0s when read.
6	tag1SyncFilterLock	RS	When this bit is set to 1, bit 6 (tag1SyncFilter) in the isochronous receive context match register (see Section 6.2.46, *Isochronous Receive Context Match Register*) is set to 1 for all isochronous receive contexts. When this bit is cleared, bit 6 (tag1SyncFilter) in the isochronous receive context match register has read/write access. This bit is cleared when $\overline{\text{G\_RST}}$ is asserted.
5–0	RSVD	R	Reserved. Bits 5D/PHY_D0 return 0s when read.

6.2.32 Node Identification Register

The node identification register contains the address of the node on which the OHCI-Lynx chip resides, and indicates the valid node number status. The 16-bit combination of the busNumber field (bits 15–6) and the NodeNumber field (bits 5–0) is referred to as the node ID. See Table 6-57 for a description of the register contents.

Type: Read/write/update, read/update, read only
Offset: E8h
Default: 00X0 0X00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0

Table 6-57. Node Identification Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	IDValid	RU	Bit 31 indicates whether or not the TSB83AA23 device has a valid node number. It is cleared when a 1394 bus reset is detected, and set to 1 when the TSB83AA23 device receives a new node number from its PHY section.
30	root	RU	Bit 30 is set to 1 during the bus reset process if the attached PHY section is root.
29–28	RSVD	R	Reserved. Bits 29–28 return 0s when read.
27	CPS	RU	Bit 27 is set to 1 if the PHY section is reporting that cable power status is OK.
26–16	RSVD	R	Reserved. Bits 26–16 return 0s when read.
15–6	BusNumber	RWU	This field identifies the specific 1394 bus the TSB83AA23 device belongs to when multiple IEEE Std 1394-compatible buses are connected via a bridge.
5–0	NodeNumber	RU	This field is the physical node number established by the PHY section during self-identification. It is automatically set to the value received from the PHY section after the self-identification phase. If the PHY section sets the NodeNumber to 63, then software must not set bit 15 (run) in the asynchronous context control register (see Section 6.2.40, *Asynchronous Context Control Register*) for either of the AT DMA contexts.

6.2.33 PHY Layer Control Register

The PHY layer control register reads from or writes to a PHY section register. See Table 6-58 for a description of the register contents.

Type: Read/write/update, read/write, read/update, read only
Offset: ECh
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-58. PHY Layer Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	rdDone	RU	Bit 31 is cleared to 0 by the TSB83AA23 device when either bit 15 (rdReg) or bit 14 (wrReg) is set to 1. This bit is set to 1 when a register transfer is received from the PHY section.
30–28	RSVD	R	Reserved. Bits 30–28 return 0s when read.
27–24	rdAddr	RU	This field is the address of the register most recently received from the PHY section.
23–16	rdData	RU	This field is the contents of a PHY section register that has been read.
15	rdReg	RWU	Bit 15 is set to 1 by software to initiate a read request to a PHY section register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1 simultaneously.
14	wrReg	RWU	Bit 14 is set to 1 by software to initiate a write request to a PHY section register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1 simultaneously.
13–12	RSVD	R	Reserved. Bits 13–12 return 0s when read.

Table 6-58. PHY Layer Control Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
11–8	regAddr	R/W	This field is the address of the PHY section register to be written or read.
7–0	wrData	R/W	This field is the data to be written to a PHY section register and is ignored for reads.

6.2.34 Isochronous Cycle Timer Register

The isochronous cycle timer register indicates the current cycle number and offset. When the TSB83AA23 device is cycle master, this register is transmitted with the cycle-start message. When the TSB83AA23 device is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle-start message is not received, the fields can continue incrementing on their own (if programmed) to maintain a local time reference. See Table 6-59 for a description of the register contents.

Type: Read/write/update
Offset: F0h
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-59. Isochronous Cycle Timer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	cycleSeconds	RWU	This field counts seconds [rollovers from bits 24–12 (cycleCount field)] modulo 128.
24–12	cycleCount	RWU	This field counts cycles [rollovers from bits 11–0 (cycleOffset field)] modulo 8000.
11–0	cycleOffset	RWU	This field counts 24.576-MHz clocks modulo 3072, that is, 125 µs. If an external 8-kHz clock configuration is being used, this field must be cleared to 0s at each tick of the external clock.

6.2.35 Asynchronous Request Filter High Register

The asynchronous request filter high set/clear register enables asynchronous receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for either the physical request context or the ARRQ context, the source node ID is examined. If the bit corresponding to the node ID is not set to 1 in this register, the packet is not acknowledged and the request is not queued. The node ID comparison is done if the source node is on the same bus as the TSB83AA23 device. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1. None of the bits in this register can be accessed while a bus reset interrupt is pending in the interrupt event register (see Section 6.2.21, *Interrupt Event Register*). See Table 6-60 for a description of the register contents.

Type: Read/set/clear
Offset: 100h Set register
104h Clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-60. Asynchronous Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqAllBuses	RSC	If bit 31 is set to 1, all asynchronous requests received by the TSB83AA23 device from nonlocal bus nodes are accepted.
30	asynReqResource62	RSC	If bit 30 is set to 1 for local bus node number 62 (bit number + 32), asynchronous requests received by the TSB83AA23 device from that node are accepted.
29	asynReqResource61	RSC	If bit 29 is set to 1 for local bus node number 61 (bit number + 32), asynchronous requests received by the TSB83AA23 device from that node are accepted.
28–2	asynReqResource*n*	RSC	Bits 28 through 2 (asynReqResource*n*, where *n* = 61, 60, 59, ..., 34) follow the same pattern as bits 30 and 29.
1	asynReqResource33	RSC	If bit 1 is set to 1 for local bus node number 33 (bit number + 32), asynchronous requests received by the TSB83AA23 device from that node are accepted.
0	asynReqResource32	RSC	If bit 0 is set to 1 for local bus node number 32 (bit number + 32), asynchronous requests received by the TSB83AA23 device from that node are accepted.

6.2.36 Asynchronous Request Filter Low Register

The asynchronous request filter low set/clear register enables asynchronous receive requests on a per-node basis, and handles the lower node IDs. Other than filtering different node IDs, this register behaves identically to the asynchronous request filter high register for all bits except bit 31. None of the bits in this register can be accessed while a bus reset interrupt is pending in the interrupt event register (see Section 6.2.21, *Interrupt Event Register*). See Table 6-61 for a description of the register contents.

Type: Read/set/clear
Offset: 108h Set register
10Ch Clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-61. Asynchronous Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqResource31	RSC	If bit 31 is set to 1 for local bus node number 31, asynchronous requests received by the TSB83AA23 device from that node are accepted.
30	asynReqResource30	RSC	If bit 30 is set to 1 for local bus node number 30, asynchronous requests received by the TSB83AA23 device from that node are accepted.
29–2	asynReqResource*n*	RSC	Bits 29 through 2 (asynReqResource*n*, where *n* = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	asynReqResource1	RSC	If bit 1 is set to 1 for local bus node number 1, asynchronous requests received by the TSB83AA23 device from that node are accepted.
0	asynReqResource0	RSC	If bit 0 is set to 1 for local bus node number 0, asynchronous requests received by the TSB83AA23 device from that node are accepted.

6.2.37 Physical Request Filter High Register

The physical request filter high set/clear register enables physical receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for the physical request context and the node ID has been compared against the ARRQ registers, the comparison is done again with this register. If the bit corresponding to the node ID is not set to 1 in this register, the request is handled by the ARRQ context instead of the physical request context. The node ID comparison is done if the source node is on the same bus as the TSB83AA23 device. Nonlocal-bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1. See Table 6-62 for a description of the register contents.

Type: Read/set/clear
Offset: 110h Set register
114h Clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-62. Physical Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	PhysReqAllBusses	RSC	If bit 31 is set to 1, all physical requests received by the TSB83AA23 device from nonlocal-bus nodes are accepted. Bit 31 is not cleared by a $\overline{\text{PCI\_RST}}$.
30	PhysReqResource62	RSC	If bit 30 is set to 1 for local bus node number 62 (bit number + 32), physical requests received by the TSB83AA23 device from that node are handled through the physical request context.
29	PhysReqResource61	RSC	If bit 29 is set to 1 for local bus node number 61 (bit number + 32), physical requests received by the TSB83AA23 device from that node are handled through the physical request context.
28–2	PhysReqResource*n*	RSC	Bits 28 through 2 (PhysReqResource*n*, where *n* = 60, 59, 58, ..., 34) follow the same pattern as bits 30 and 29.
1	PhysReqResource33	RSC	If bit 1 is set to 1 for local bus node number 33 (bit number + 32), physical requests received by the TSB83AA23 device from that node are handled through the physical request context.
0	PhysReqResource32	RSC	If bit 0 is set to 1 for local bus node number 32 (bit number + 32), physical requests received by the TSB83AA23 device from that node are handled through the physical request context.

6.2.38 Physical Request Filter Low Register

The physical request filter low set/clear register enables physical receive requests on a per-node basis and handles the lower node IDs. When a packet is destined for the physical request context and the node ID has been compared against the asynchronous request filter registers, the node ID comparison is done again with this register. If the bit corresponding to the node ID is not set to 1 in this register, the request is handled by the asynchronous request context instead of the physical request context. See Table 6-63 for a description of the register contents.

Type: Read/set/clear
Offset: 118h Set register
11Ch Clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-63. Physical Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	PhysReqResource31	RSC	If bit 31 is set to 1 for local bus node number 31, physical requests received by the TSB83AA23 device from that node are handled through the physical request context.
30	PhysReqResource30	RSC	If bit 30 is set to 1 for local bus node number 30, physical requests received by the TSB83AA23 device from that node are handled through the physical request context.
29–2	PhysReqResourcen	RSC	Bits 29 through 2 (PhysReqResourcen, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	PhysReqResource1	RSC	If bit 1 is set to 1 for local bus node number 1, physical requests received by the TSB83AA23 device from that node are handled through the physical request context.
0	PhysReqResource0	RSC	If bit 0 is set to 1 for local bus node number 0, physical requests received by the TSB83AA23 device from that node are handled through the physical request context.

6.2.39 Physical Upper Bound Register (Optional Register)

The physical upper bound register is an optional register and is not implemented. This register returns all 0s when read.

Type: Read only
Offset: 120h
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2.40 Asynchronous Context Control Register

The asynchronous context control set/clear register controls the state and indicates status of the DMA context. See Table 6-64 for a description of the register contents.

Type: Read/set/clear/update, read/set/update, read/update, read only
Offset:
180h Set register [ATRQ]
184h Clear register [ATRQ]
1A0h Set register [ATRS]
1A4h Clear register [ATRS]
1C0h Set register [ARRQ]
1C4h Clear register [ARRQ]
1E0h Set register [ARRS]
1E4h Clear register [ARRS]
Default: 0000 X0XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 6-64. Asynchronous Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	run	RSCU	Bit 15 is set to 1 by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB83AA23 device changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets bit 12 to 1 to cause the TSB83AA23 device to continue or resume descriptor processing. The TSB83AA23 device clears this bit on every descriptor fetch.
11	dead	RU	The TSB83AA23 device sets bit 11 when it encounters a fatal error, and clears the bit when software clears bit 15 (run). Asynchronous contexts supporting out-of-order pipelining provide unique contextControl.dead functionality. See Section 7.7 in the *1394 Open Host Controller Interface Specification* (Revision 1.1) for more information.
10	active	RU	The TSB83AA23 device sets bit 10 to 1 when it is processing descriptors.
9	betaFrame	RU	Bit 9 is set to 1 when the PHY indicates that the received packet is sent in Beta format. A response to a request sent using Beta format also uses Beta format.
8	RSVD	R	Reserved. Bit 8 returns 0 when read.
7–5	spd	RU	This field indicates the speed at which a packet was received or transmitted and only contains meaningful information for receive contexts. This field is encoded as: 000 = 100 Mbps

Table 6-64. Asynchronous Context Control Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
			001 = 200 Mbps 010 = 400 Mbps 011 = 800 Mbps All other values are reserved.
4–0	eventcode	RU	This field holds the acknowledge sent by the link core for this packet or holds an internally generated error code if the packet was not transferred successfully.

6.2.41 Asynchronous Context Command Pointer Register

The asynchronous context command pointer register contains a pointer to the address of the first descriptor block that the TSB83AA23 device accesses when software enables the context by setting bit 15 (run) of the asynchronous context control register (see Section 6.2.40, *Asynchronous Context Control Register*) to 1. See Table 6-65 for a description of the register contents.

Type: Read/write/update
Offset: 18Ch ATRQ
1ACh ATRS
1CCh ARRQ
1ECh ARRS
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 6-65. Asynchronous Context Command Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	descriptorAddress	RWU	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block.
3–0	Z	RWU	Indicates the number of contiguous descriptors at the address pointed to by the descriptor address. If Z is 0, it indicates that the descriptorAddress field (bits 31–4) is not valid.

6.2.42 Isochronous Transmit Context Control Register

The isochronous transmit context control set/clear register controls options, state, and status for the isochronous transmit DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7). See Table 6-66 for a description of the register contents.

Type: Read/set/clear/update, read/set/clear, read/update, read only
Offset: 200h + (16 × n) Set register
204h + (16 × n) Clear register
Default: XXXX X0XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 6-66. Isochronous Transmit Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	cycleMatchEnable	RSCU	When bit 31 is set to 1, processing occurs such that the packet described by the context first descriptor block is transmitted in the cycle whose number is specified in the cycleMatch field (bits 30–16). The cycleMatch field (bits 30–16) must match the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycle-start packet that is sent or received immediately before isochronous transmission begins. Because the isochronous transmit DMA controller can work ahead, the processing of the first descriptor block might begin slightly in advance of the actual cycle in which the first packet is transmitted. The effects of this bit, however, are impacted by the values of other bits in this register and are explained in the *1394 Open Host Controller Interface Specification*. Once the context has become active, hardware clears this bit.
30–16	cycleMatch	RSC	This field contains a 15-bit value, corresponding to the low-order 2 bits of the isochronous cycle timer register at OHCI offset F0h (see Section 6.2.34, *Isochronous Cycle Timer Register*) cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12). If bit 31 (cycleMatchEnable) is set to 1, this isochronous transmit DMA context becomes enabled for transmits when the low-order two bits of the isochronous cycle timer register cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
15	run	RSC	Bit 15 is set to 1 by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB83AA23 device changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets bit 12 to 1 to cause the TSB83AA23 device to continue or resume descriptor processing. The TSB83AA23 device clears this bit on every descriptor fetch.
11(1)	dead	RU	The TSB83AA23 device sets bit 11 to 1 when it encounters a fatal error, and clears the bit when software clears bit 15 (run) to 0.
10	active	RU	The TSB83AA23 device sets bit 10 to 1 when it is processing descriptors.
9–5	RSVD	R	Reserved. Bits 9–5 return 0s when read.
4–0(1)	event code	RU	Following an OUTPUT_LAST* command, the error code is indicated in this field. Possible values are: ack_complete, evt_descriptor_read, evt_data_read, and evt_unknown.

(1) On an overflow for each running context, the isochronous transmit DMA supports up to seven cycle skips when the following are true:
- Bit 11 (dead) in either the isochronous transmit or receive context control register is set to 1.
- Bits 4–0 (eventcode field) in either the isochronous transmit or receive context control register is set to evt_timeout.
- Bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) is set to 1.

6.2.43 Isochronous Transmit Context Command Pointer Register

The isochronous transmit context command pointer register contains a pointer to the address of the first descriptor block that the TSB83AA23 device accesses when software enables an isochronous transmit context by setting bit 15 (run) in the isochronous transmit context control register (see Section 6.2.42, *Isochronous Transmit Context Control Register*) to 1. The isochronous transmit DMA context command pointer can be read when a context is active. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7).

Type: Read only
Offset: 20Ch + (16 n)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

6.2.44 Isochronous Receive Context Control Register

The isochronous receive context control set/clear register controls options, state, and status for the isochronous receive DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 6-67 for a description of the register contents.

Type: Read/set/clear/update, read/set/clear, read/update, read only
Offset: 400h + (32 n) Set register
404h + (32 n) Clear register
Default: XX00 X0XXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 6-67. Isochronous Receive Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	bufferFill	RSC	When bit 31 is set to 1, received packets are placed back to back to completely fill each receive buffer. When this bit is cleared, each received packet is placed in a single buffer. If bit 28 (multiChanMode) is set to 1, this bit also must be set to 1. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
30	isochHeader	RSC	When bit 30 is set to 1, received isochronous packets include the complete 4-byte isochronous packet header seen by the link layer. The end of the packet is marked with xferStatus in the first doublet, and a 16-bit timeStamp indicating the time of the most recently received (or sent) cycleStart packet. When this bit is cleared, the packet header is stripped from received isochronous packets. The packet header, if received, immediately precedes the packet payload. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
29	cycleMatchEnable		RSCU When bit 29 is set to 1 and the 13-bit cycleMatch field (bits 24–12) in the isochronous receive context match register (see Section 6.2.46, *Isochronous Receive Context Match Register*) matches the 13-bit cycleCount field in the cycleStart packet, the context begins running. The effects of this bit, however, are impacted by the values of other bits in this register. Once the context has become active, hardware clears this bit. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
28	multiChanMode	RSC	When bit 28 is set to 1, the corresponding isochronous receive DMA context receives packets for all isochronous channels enabled in the isochronous receive channel mask high register at OHCI offset 70h/74h (see Section 6.2.19, *Isochronous Receive Channel Mask High Register*) and isochronous receive channel mask low register at OHCI offset 78h/7Ch (see Section 6.2.20). The isochronous channel number specified in the isochronous receive context match register (see Section 6.2.46, *Isochronous Receive Context Match Register*) is ignored. When this bit is cleared, the isochronous receive DMA context receives packets for the single channel specified in the isochronous receive context match register (see Section 6.2.46, *Isochronous Receive Context Match Register*). Only one isochronous receive DMA context can use the isochronous receive channel mask registers (see Section 6.2.19, *Isochronous Receive Channel Mask High Register*, and Section 6.2.20, *Isochronous Receive Channel Mask Low Register*). If more than one isochronous receive context control register has this bit set, the results are undefined. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
27	dualBufferMode	RSC	When bit 27 is set to 1, receive packets are separated into first and second payload and streamed independently to the firstBuffer series and secondBuffer series as described in Section 10.2.3 in the 1394 Open Host Controller Interface Specification. Also, when bit 27 is set to 1, both bits 28 (multiChanMode) and 31 (bufferFill) are cleared to 0. The value of this bit does not change when either bit 10 (active) or bit 15 (run) is set to 1.
26–16	RSVD	R	Reserved. Bits 26–16 return 0s when read.
15	run	RSCU	Bit 15 is set to 1 by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB83AA23 device changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14 and 13 return 0s when read.
12	wake	RSU	Software sets bit 12 to 1 to cause the TSB83AA23 device to continue or resume descriptor processing. The TSB83AA23 device clears this bit on every descriptor fetch.
11(1)	dead	RU	The TSB83AA23 device sets bit 11 to 1 when it encounters a fatal error, and clears the bit when software clears bit 15 (run).
10	active	RU	The TSB83AA23 device sets bit 10 to 1 when it is processing descriptors.
9	betaFrame	RU	Bit 9 is set to 1 when the PHY section indicates that the received packet is sent in Beta format. A response to a request sent using Beta format also uses Beta format.
8	RSVD	R	Reserved. Bit 8 returns 0 when read.
7–5	spd	RU	This field indicates the speed at which the packet was received. 000 = 100 Mbps 001 = 200 Mbps 010 = 400 Mbps 011 = 800 Mbps

(1) On an overflow for each running context, the isochronous transmit DMA supports up to seven cycle skips when the following are true:

- Bit 11 (dead) in either the isochronous transmit or receive context control register is set to 1.
- Bits 4–0 (eventcode field) in either the isochronous transmit or receive context control register is set to evt_timeout.
- Bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 6.2.21, *Interrupt Event Register*) is set to 1.

Table 6-67. Isochronous Receive Context Control Register Description (continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
			All other values are reserved.
4–0[1]	event code	RU	For bufferFill mode, possible values are ack_complete, evt_descriptor_read, evt_data_write, and evt_unknown. Packets with data errors (either dataLength mismatches or dataCRC errors) and packets for which a FIFO overrun occurred are backed out. For packet-per-buffer mode, possible values are ack_complete, ack_data_error, evt_long_packet, evt_overrun, evt_descriptor_read, evt_data_write, and evt_unknown.

6.2.45 Isochronous Receive Context Command Pointer Register

The isochronous receive context command pointer register contains a pointer to the address of the first descriptor block that the TSB83AA23 device accesses when software enables an isochronous receive context by setting bit 15 (run) in the isochronous receive context control register (see Section 6.2.44) to 1. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3).

Type: Read only
Offset: 40Ch + (32 n)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

6.2.46 Isochronous Receive Context Match Register

The isochronous receive context match register starts an isochronous receive context running on a specified cycle number, filters incoming isochronous packets based on tag values, and waits for packets with a specified sync value. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 6-68 for a description of the register contents.

Type: Read/write, read only
Offset: 410Ch + (32 n)
Default: XXXX XXXXh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X

Table 6-68. Isochronous Receive Context Match Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	tag3	R/W	If bit 31 is set to 1, this context matches on isochronous receive packets with a tag field of 11b.
30	tag2	R/W	If bit 30 is set to 1, this context matches on isochronous receive packets with a tag field of 10b.
29	tag1	R/W	If bit 29 is set to 1, this context matches on isochronous receive packets with a tag field of 01b.
28	tag0	R/W	If bit 28 is set to 1, this context matches on isochronous receive packets with a tag field of 00b.
27	RSVD	R	Reserved. Bit 27 returns 0 when read.
26–12	cycleMatch	R/W	Contains a 15-bit value, corresponding to the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycleStart packet. If bit 29 (cycleMatchEnable) in the isochronous receive context control register (see Section 6.2.44, *Isochronous Receive Context Control Register*) is set to 1, this context is enabled for receives when thelow-order two bits of the bus isochronous cycle timer register at OHCI offset F0h (see Section 6.2.34, *Isochronous Cycle Timer Register*) cycleSeconds field (bits 31–25) and cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
11–8	sync	R/W	This 4-bit field is compared to the sync field of each isochronous packet for this channel when the command descriptor w field is set to 11b.
7	RSVD	R	Reserved. Bit 7 returns 0 when read.
6	tag1SyncFilter	R/W	If bit 6 and bit 29 (tag1) are set to 1, packets with tag 01b are accepted into the context if the two most significant bits of the packet sync field are 00b. Packets with tag values other than 01b are filtered according to bit 28 (tag0), bit 30 (tag2), and bit 31 (tag3), without any additional restrictions. If this bit is cleared, then this context matches on isochronous receive packets as specified in bits 28–31 (tag0–tag3), with no additional restrictions.
5–0	channelNumber	R/W	This 6-bit field indicates the isochronous channel number for which this isochronous receive DMA context accepts packets.

6.3 TI Extension Registers

The TI extension base address register provides a method of accessing memory-mapped TI extension registers. The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. See Section 6.1.12, *TI Extension Base Address Register*, for register bit field details. See Table 6-69 for the TI extension register listing.

Table 6-69. TI Extension Register Map

REGISTER NAME	OFFSET
Reserved	00h–A7Fh
Isochronous receive DV set enhancement	A80h
Isochronous receive DV enhancement clear	A84h
LLC section enhancement control set	A88h
LLC section enhancement control clear	A8Ch
Isochronous transmit context-0 timestamp offset	A90h
Isochronous transmit context-1 timestamp offset	A94h
Isochronous transmit context-2 timestamp offset	A98h
Isochronous transmit context-3 timestamp offset	A9Ch
Isochronous transmit context-4 timestamp offset	AA0h
Isochronous transmit context-5 timestamp offset	AA4h
Isochronous transmit context-6 timestamp offset	AA8h
Isochronous transmit context-7 timestamp offset	AA8h

6.3.1 DV Timestamp Enhancements

The DV timestamp enhancements are enabled by bit 8 (enab_dv_ts) in the LLC section enhancement control register located at PCI offset F4h and are aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

The DV and MPEG transmit enhancements are enabled separately by bits in the LLC section enhancement control register located in PCI configuration space at PCI offset F4h. The link enhancement control register is also aliased as a set/clear register in TI extension space at offset A88h (set) and A8Ch (clear).

Bit 8 (enab_dv_ts) of the LLC section enhancement control register enables DV timestamp support. When enabled, the link calculates a timestamp based on the cycle timer and the timestamp offset register and substitutes it in the SYT field of the CIP once per DV frame.

Bit 10 (enab_mpeg_ts) of the link enhancement control register enables MPEG timestamp support. Two MPEG time stamp modes are supported. The default mode calculates an initial delta that is added to the calculated timestamp in addition to a user-defined offset. The initial offset is calculated as the difference in the intended transmit cycle count and the cycle count field of the timestamp in the first TSP of the MPEG2 stream. The use of the initial delta can be controlled by bit 31 (DisableInitialOffset) in the timestamp offset register (see Section 6.3.6, *Timestamp Offset Register*).

6.3.2 MPEG2 Timestamp Procedure

The MPEG2 timestamp enhancements are enabled by bit 10 (enab_mpeg_ts) in the link enhancement control register located at PCI offset F4h and aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

When bit 10 (enab_mpeg_ts) is set to 1, the hardware applies the timestamp enhancements to isochronous transmit packets that have the tag field equal to 01b in the isochronous packet header and a FMT field equal to 10h.

6.3.3 Isochronous Receive Digital Video Enhancements

The DV frame synchronization and branch enhancement provides a mechanism in buffer-fill mode to synchronize 1394 DV data, which is received in the correct order to DV frame-sized data buffers described by several INPUT_MORE descriptors (see *1394 Open Host Controller Interface Specification*, Revision 1.1). This is accomplished by waiting for the start-of-frame packet in a DV stream before transferring the received isochronous stream into the memory buffer described by the INPUT_MORE descriptors. This can improve the DV capture application performance by reducing the amount of processing overhead required to strip the CIP header and copy the received packets into frame-sized buffers.

The start of a DV frame is represented in the 1394 packet as a 16-bit pattern of 1FX7h (first byte 1Fh and second byte X7h) received as the first two bytes of the third quadlet in a DV isochronous packet. The TSB12LV23 OHCI-Lynx used a field match of 1F07h to synchronize the frame. However, this does not accommodate all camcorder cases. To accommodate these models, the TSB83AA23 uses the pattern 1FX7h.

6.3.4 Isochronous Receive Digital Video Enhancements Register

The isochronous receive digital video enhancements register enables the DV enhancements in the TSB83AA23 device. The bits in this register can only be modified when both the active (bit 10) and run (bit 15) bits of the corresponding context control register are 0. See Table 6-70 for a description of the register contents.

Type: Read/set/clear, read only
Offset: A80h Set register
A84h Clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-70. Isochronous Receive Digital Video Enhancements Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–14	RSVD	R	Reserved. Bits 31–14 return 0s when read.
13	DV_Branch3	RSC	When bit 13 is set to 1, the isochronous receive context 3 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is interpreted only when bit 12 (CIP_Strip3) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
12	CIP_Strip3	RSC	When bit 12 is set to 1, the isochronous receive context 3 strips the first two quadlets of payload. This bit is interpreted only when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
11–10	RSVD	R	Reserved. Bits 11 and 10 return 0s when read.
9	DV_Branch2	RSC	When bit 9 is set to 1, the isochronous receive context 2 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is interpreted only when bit 8 (CIP_Strip2) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
8	CIP_Strip2	RSC	When bit 8 is set to 1, the isochronous receive context 2 strips the first two quadlets of payload. This bit is interpreted only when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
7–6	RSVD	R	Reserved. Bits 7 and 6 return 0s when read.
5	DV_Branch1	RSC	When bit 5 is set to 1, the isochronous receive context 1 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is interpreted only when bit 4 (CIP_Strip1) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
4	CIP_Strip1	RSC	When bit 4 is set to 1, the isochronous receive context 1 strips the first two quadlets of payload. This bit is interpreted only when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
3–2	RSVD	R	Reserved. Bits 3 and 2 return 0s when read.
1	DV_Branch0	RSC	When bit 1 is set to 1, the isochronous receive context 0 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is interpreted only when bit 0 (CIP_Strip0) is 1 and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.
0	CIP_Strip0	RSC	When bit 0 is set to 1, the isochronous receive context 0 strips the first two quadlets of payload. This bit is interpreted only when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 6.2.44, *Isochronous Receive Context Control Register*) is 0.

6.3.5 *Link Enhancement Register*

This register is a memory-mapped set/clear register that is an alias of the LLC section enhancement control register at PCI offset F4h. These bits can be initialized by software. Some of the bits also can be initialized by a serial EEPROM, if one is present, as noted in the following bit descriptions. If the bits are to be initialized by software, the bits must be initialized prior to setting bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*). See Table 6-71 for a description of the register contents.

Type: Read/set/clear, read/write, read only
Offset: A88h Set register
A8Ch Clear register
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-71. Link Enhancement Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	dis_at_pipeline	RSC	Disable AT pipelining. When bit 15 is set to 1, out-of-order AT pipelining is disabled.
14	RSVD	R	Reserved
13–12	atx_thresh	RSC	This field sets the initial AT threshold value, which is used until the AT FIFO is under run. When the TSB83AA23 device retries the packet, it uses a 2-Kbyte threshold, resulting in a store-and-forward operation. 00 = 4K-byte threshold, resulting in a store-and-forward operation (default) 01 = 1.7K-byte threshold 10 = 1K-byte threshold 11 = 512-byte threshold These bits fine tune the asynchronous transmit threshold. For most applications, the 1.7K-byte threshold is optimal. Changing this value might increase or decrease the 1394 latency, depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, the remaining data must be received before the AT FIFO is emptied; otherwise, an under run condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation, that is, wait until it has the complete packet in the FIFO before retransmitting it on the second attempt, to ensure delivery. An AT threshold of 4K results in store-and-forward operation, which means that asynchronous data is not transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 4K results in only complete packets being transmitted. This device always uses store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 6.2.3, *Asynchronous Transmit Retries Register*) is cleared.
11–10	RSVD	R	Reserved. Bits 11–10 returns 0 when read.
9	enab_aud_ts	R/W	Enable audio/music CIP timestamp enhancement. When bit 9 is set to 1, the enhancement is enabled for audio/music CIP transmit streams (FMT = 10h).
8	enab_dv_ts	RSC	Enable DV CIP timestamp enhancement. When bit 8 is set to 1, the enhancement is enabled for DV CIP transmit streams (FMT = 00h).
7	enab_unfair	RSC	Enable asynchronous priority requests. OHCI-Lynx compatible. Setting bit 7 to 1 enables the LLC section to respond to requests with priority arbitration. It is recommended that this bit be set to 1.
6	RSVD	R	This bit is not assigned in the TSB83AA23 follow-on products, because this bit location loaded by the serial EEPROM from the enhancements field corresponds to bit 23 (programPhyEnable) in the host controller control register at OHCI offset 50h/54h (see Section 6.2.16, *Host Controller Control Register*).
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2	enab_insert_idle	RSC	Enable insert idle. OHCI-Lynx compatible. When the PHY section has control of the PHY_CTL0–PHY_CTL1 internal control lines and PHY_DATA0–PHY_DATA7 internal data lines and the LLC section requests control, the PHY section drives 11b on the PHY_CTL0–PHY_CTL1 internal lines. The LLC section can then start driving these lines immediately. Setting bit 2 to 1 inserts an idle state, so the link waits one clock cycle before it starts driving the lines (turnaround time).
1	enab_accel	RSC	Enable acceleration enhancements. OHCI-Lynx compatible. When bit 1 is set to 1, the PHY section is notified that the link supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1.
0	RSVD	R	Reserved. Bit 0 returns 0 when read.

6.3.6 Timestamp Offset Register

The value of this register is added as an offset to the cycle timer value when using the MPEG, DV, and CIP enhancements. A timestamp offset register is implemented per isochronous transmit context. The n value following the offset indicates the context number (n = 0, 1, 2, 3, …, 7). These registers are programmed by software as appropriate. See Table 6-72 for a description of the register contents.

Type: Read/write, read only
Offset: A90h + (4 n)
Default: 0000 0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-72. Timestamp Offset Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	DisableInitialOffset	R/W	Bit 31 disables the use of the initial timestamp offset when the MPEG2 enhancements are enabled. A value of 0 indicates the use of the initial offset, a value of 1 indicates that the initial offset must not be applied to the calculated timestamp. This bit has no meaning for the DV timestamp enhancements.
30–25	RSVD	R	Reserved. Bits 30–25 return 0s when read.
24–12	CycleCount	R/W	This field adds an offset to the cycle count field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle count field is incremented modulo 8000; therefore, values in this field must be limited between 0 and 7999.
11–0	CycleOffset	R/W	This field adds an offset to the cycle offset field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle offset field is incremented modulo 3072; therefore, values in this field must be limited between 0 and 3071.

7 General-Purpose Input/Output (GPIO) Interface

The GPIO interface consists of one GPIO port available via the MFUNC terminal by configuring the multifunction configuration register (PCI offset E8h). GPIO powers up as a general-purpose input and is programmable via the GPIO control register. Figure 7-1 shows the logic diagram for GPIO implementation.

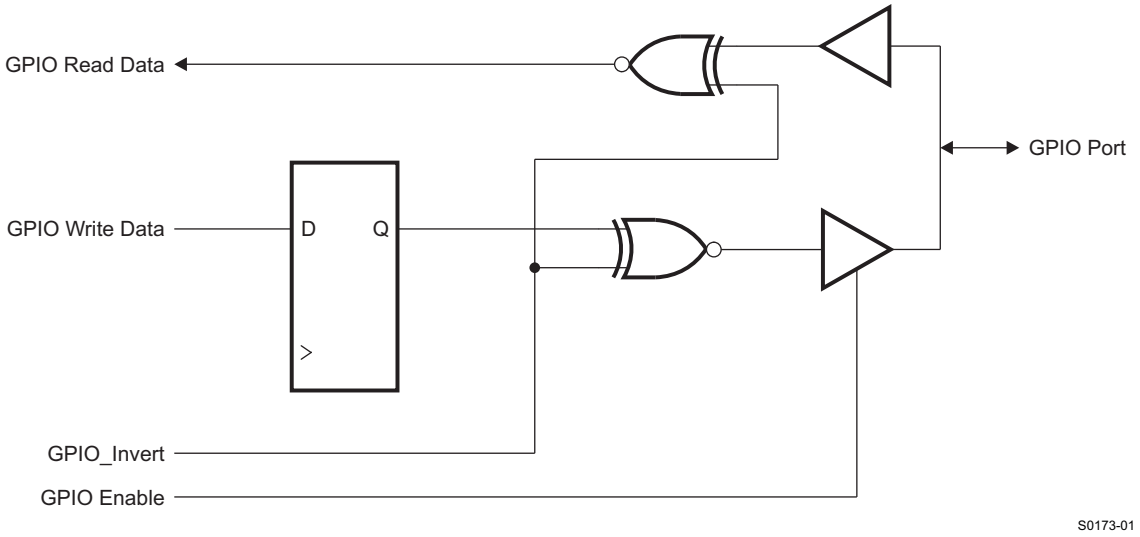


Figure 7-1. GPIO Logic Diagram

8 Serial EEPROM Interface

The TSB83AA23 device provides a serial bus interface to initialize the 1394 global unique ID register and a few PCI configuration registers through a serial EEPROM. The TSB83AA23 device communicates with the serial EEPROM via the two-wire serial interface.

After power up, the serial interface initializes the locations listed in Table 8-1. While the TSB83AA23 device accesses the serial EEPROM, all incoming PCI slave accesses are terminated with retry status. Table 8-1 shows the serial EEPROM memory map required for initializing the TSB83AA23 registers.

NOTE

If a ROM is implemented in the design, it must be programmed. An unprogrammed ROM defaults to all 1s, which could adversely impact device operation.

Table 8-1. Serial EEPROM Map

BYTE ADDRESS	BYTE DESCRIPTION							
00	PCI maximum latency (PCI offset 3Eh)				PCI minimum grant (PCI offset 3Fh)			
01	PCI subsystem vendor ID alias (least significant byte) (PCI offset F8h)							
02	PCI subsystem vendor ID alias (most significant byte) (PCI offset F9h)							
03	PCI subsystem ID alias (least significant byte) (PCI offset FAh)							
04	PCI subsystem ID alias (most significant byte) (PCI offset FBh)							
05	[7] Link_enhancementControl. enab_unfair (PCI offset F4h, bit 7)	[6] HCControl. ProgramPhy Enable (OHCI offset 50h, bit 23)	[5–3] RSVD			[2] Link_enhancement Control.enab_ insert_idle (PCI offset F4h, bit 2)	[1] Link_enhancement Control.enab_acce l (PCI offset F4h, bit 1)	[0] RSVD
06	[7–6] RSVD		[5] (1) MiniROM enable (OHCI offset 04h, bit 5)		[4–0] RSVD			
07	1394 GUID high (byte 0, least significant) (OHCI offset 24h)							
08	1394 GUID high (byte 1) (OHCI offset 25h)							
09	1394 GUID high (byte 2) (OHCI offset 26h)							
0A	1394 GUID high (byte 3, most significant) (OHCI offset 27h)							
0B	1394 GUID low (byte 0, least significant) (OHCI offset 28h)							
0C	1394 GUID low (byte 1) (OHCI offset 29h)							
0D	1394 GUID low (byte 2) (OHCI offset 30h)							
0E	1394 GUID low (byte 3, most significant) (OHCI offset 31h)							
0F	Checksum							
10	[15] Link Enhancement.dis_at_ pipeline (PCI offset F4h, bit 15)	[14] Enab_draft (PCI offset F4h, bit 14)	[13–12] Link Enhancement.atx_ thresh (PCI offset F4h, bits 13–12)		[11–8] RSVD			
11	[7] RSVD	[6] MiscConfig. cardbus (PCI offset F0h, bit 6)	[5] RSVD	[4] MiscConfig.dis_ tgt_abt (PCI offset F0h, bit 4	[3] RSVD	[2] MiscConfig.disable _sclkgate (PCI offset F0h, bit 2)	[1] MiscConfig.disable _pcigate (PCI offset F0h, bit 1)	[0] MiscConfig.keep _pclk (PCI offset F0h, bit 0)
12	[15] MiscConfig.PME_D3c old (PCI offset F0h, bit 15)	[14—11] RSVD				[10] ignore_IntEvent. MasterIntEnable_ for_pme (PCI offset F0h, bit 10)	[9–8] MR_Enhance (PCI offset F0h, bits 9–8)	
13	[7–4] BusOptions.Max_Rec (OHCI offset 20h, bits 15–12)				[3–0] RSVD			
14	[7–3] CIS offset (PCI offset 28h, bits 7–3)					[2–0] RSVD		
15–16	[7–0] RSVD							
17	[7–3] RSVD					[2–0] MultifunctionSelect.MFunc_Sel (PCI offset E8h, bits 2–0)		
18–1F	RSVD							

(1) If bit 5 at EEPROM byte offset 06h is set, then the MiniROM is enabled and the starting address is 20h.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB83AA23ZAY	LIFEBUY	NFBGA	ZAY	167	160	RoHS & Non-Green	SNAGCU	Level-3-260C-168 HR	0 to 70	TSB83AA23	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

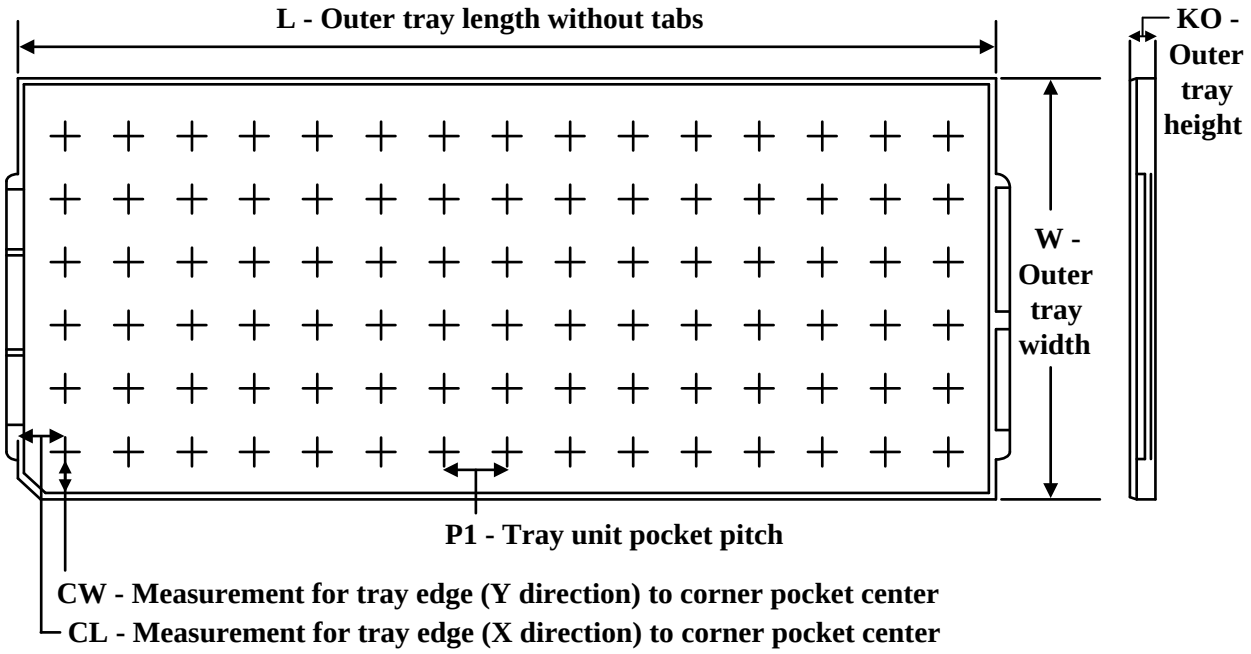
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

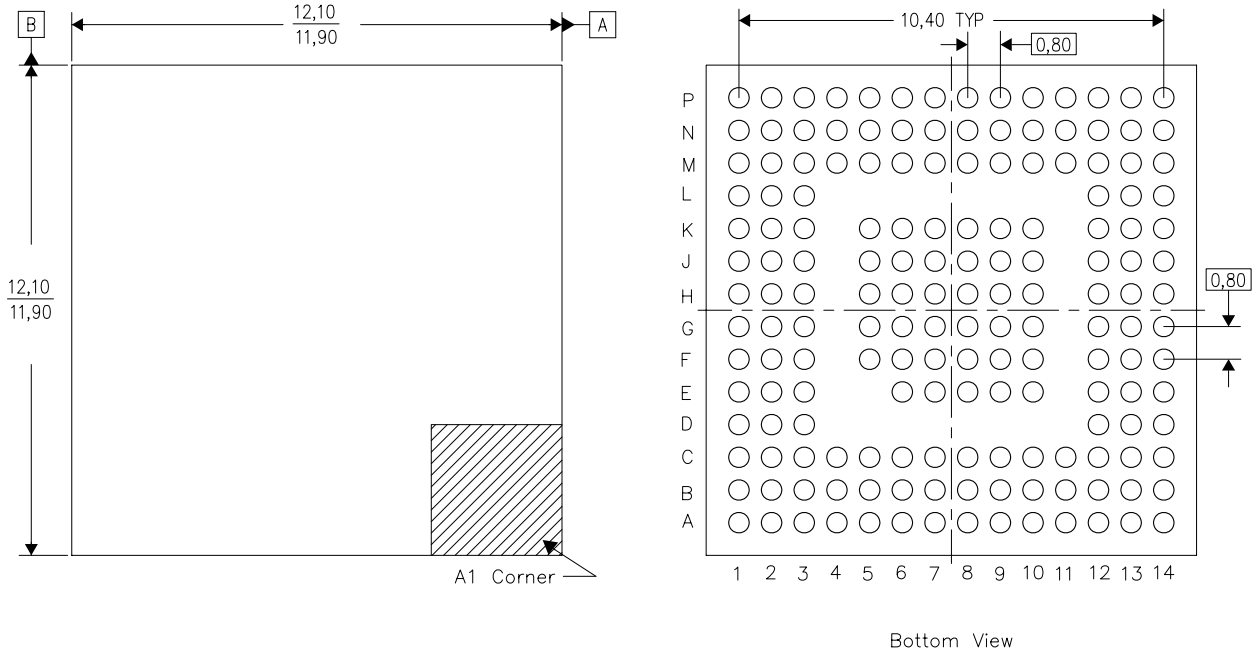


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSB83AA23ZAY	ZAY	NFBGA	167	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65

ZAY (S–PBGA–N167) PLASTIC BALL GRID ARRAY



4208324–2/C 09/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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