

# CSD19535KCS 100V N-Channel NexFET™ Power MOSFET

## 1 Features

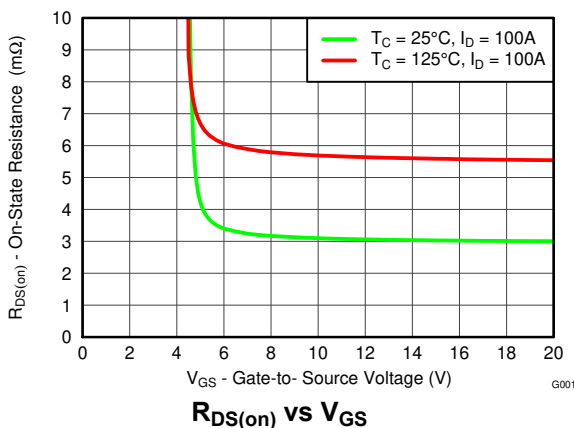
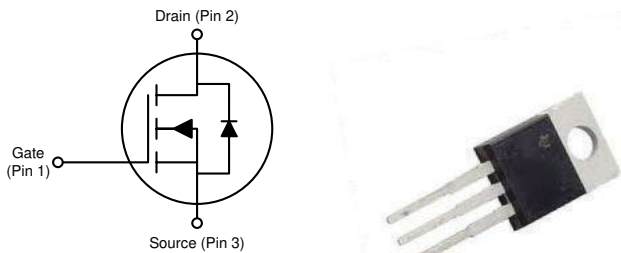
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- TO-220 plastic package

## 2 Applications

- Secondary side synchronous rectifier
- Motor control

## 3 Description

This 100V, 3.1m $\Omega$ , TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	100		V
$Q_g$	Gate Charge Total (10V)	78		nC
$Q_{gd}$	Gate Charge Gate to Drain	13		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{V}$	3.4	m $\Omega$
		$V_{GS} = 10\text{V}$	3.1	m $\Omega$
$V_{GS(th)}$	Threshold Voltage	2.7		V

## Ordering Information

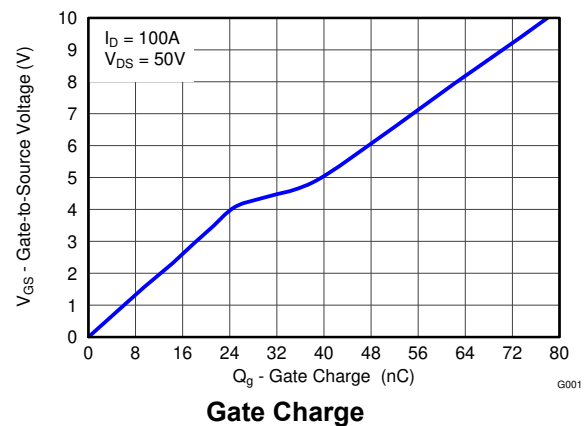
Device	Package <sup>(1)</sup>	Media	Qty	Ship
CSD19535KCS	TO-220 Plastic Package	Tube	50	Tube

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package limited)	150	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	187	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	133	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	400	A
$P_D$	Power Dissipation	300	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 95\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	451	mJ

- (1) Max  $R_{\theta JC} = 0.5^\circ\text{C/W}$ , pulse duration  $\leq 100\mu\text{s}$ , duty cycle  $\leq 1\%$



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## 4 Specifications

### 4.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-Source Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 80V			1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 20V			100	nA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.2	2.7	3.4	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = 6V, I <sub>D</sub> = 100A	3.4		4.4	mΩ
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 100A	3.1		3.6	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 100A	274			S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 50V, f = 1MHz		6100	7930	pF
C <sub>oss</sub>	Output Capacitance			1160	1500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			29	38	pF
R <sub>G</sub>	Series Gate Resistance	V <sub>DS</sub> = 50V, I <sub>D</sub> = 100A		1.4	2.8	Ω
Q <sub>g</sub>	Gate Charge Total (10V)			78	101	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain			13		nC
Q <sub>gs</sub>	Gate Charge Gate to Source			25		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			16		nC
Q <sub>oss</sub>	Output Charge	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V		196		nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 10V, I <sub>DS</sub> = 100A, R <sub>G</sub> = 0Ω		32		ns
t <sub>r</sub>	Rise Time			15		ns
t <sub>d(off)</sub>	Turn Off Delay Time			60		ns
t <sub>f</sub>	Fall Time			5		ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = 100A, V <sub>GS</sub> = 0V		0.9	1.1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = 50V, I <sub>F</sub> = 100A, di/dt = 300A/μs		421		nC
t <sub>rr</sub>	Reverse Recovery Time			89		ns

### 4.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-Case Thermal Resistance			0.5	°C/W
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance			62	

### 4.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

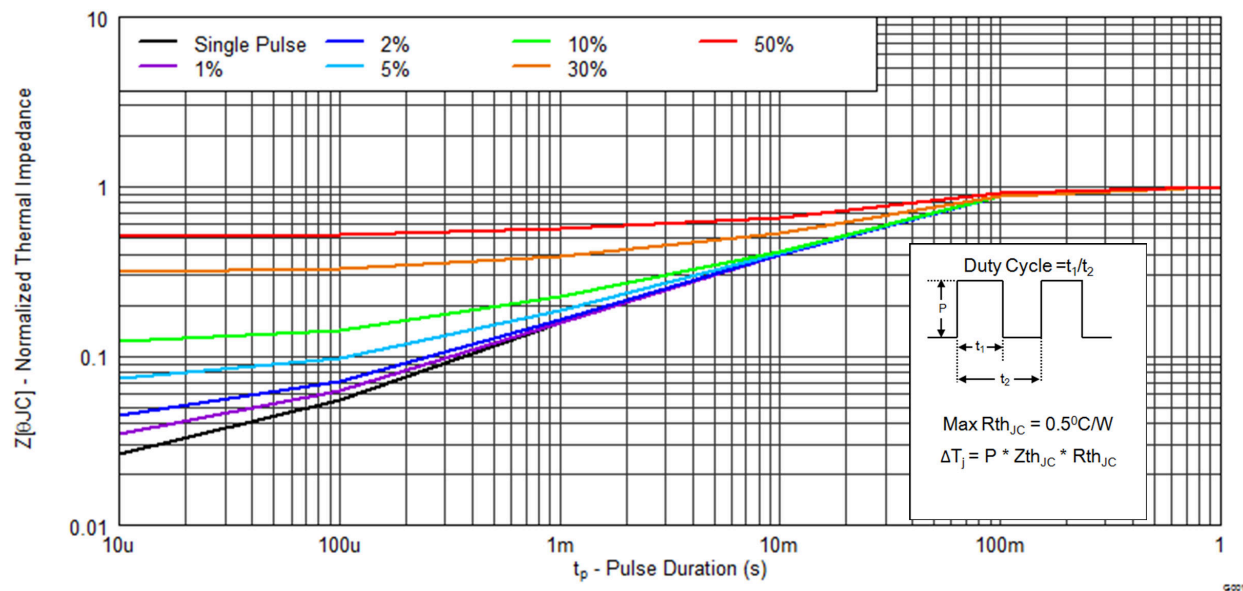


Figure 4-1. Transient Thermal Impedance

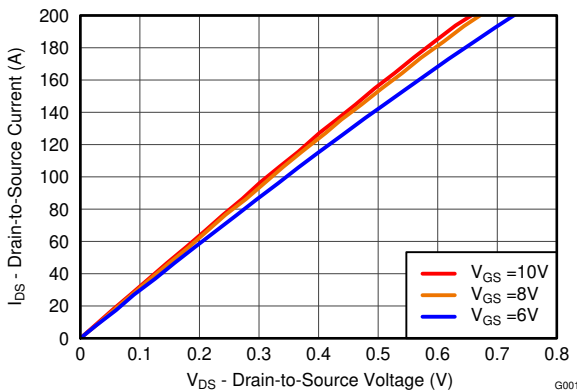


Figure 4-2. Saturation Characteristics

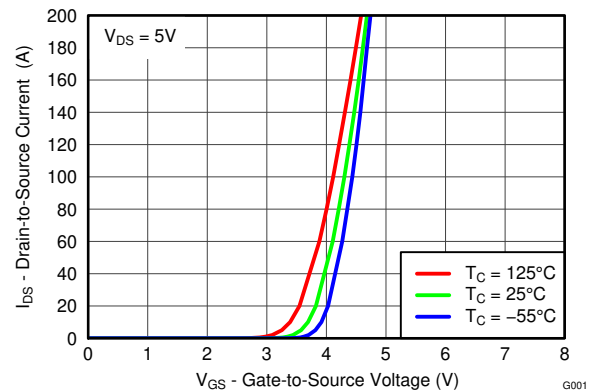
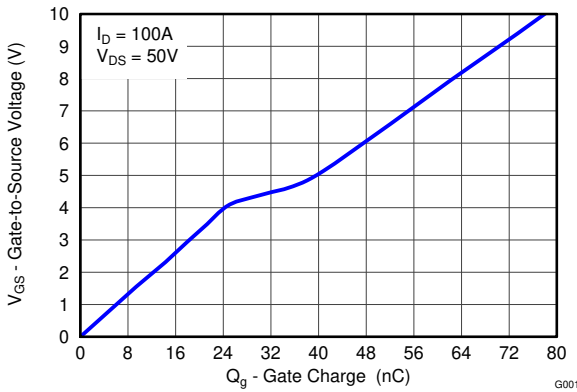


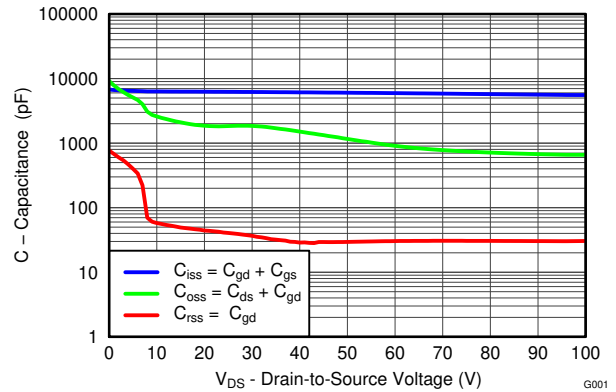
Figure 4-3. Transfer Characteristics

### 4.3 Typical MOSFET Characteristics (continued)

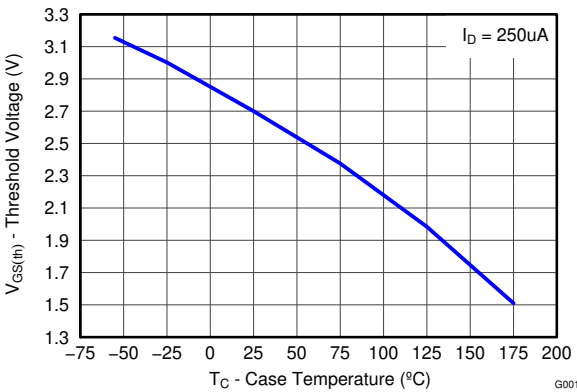
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



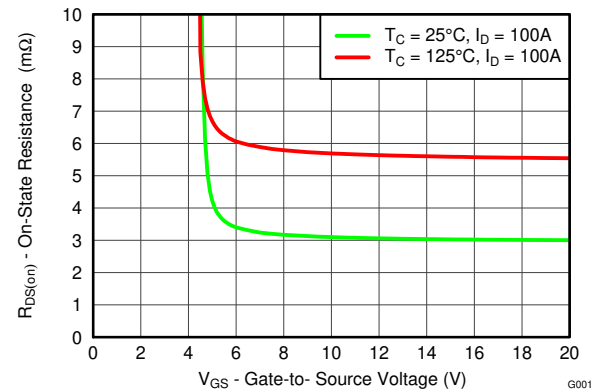
**Figure 4-4. Gate Charge**



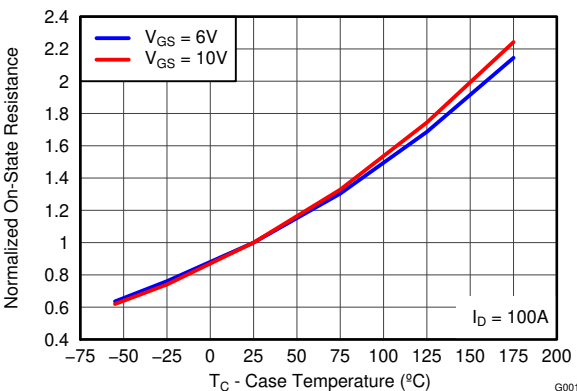
**Figure 4-5. Capacitance**



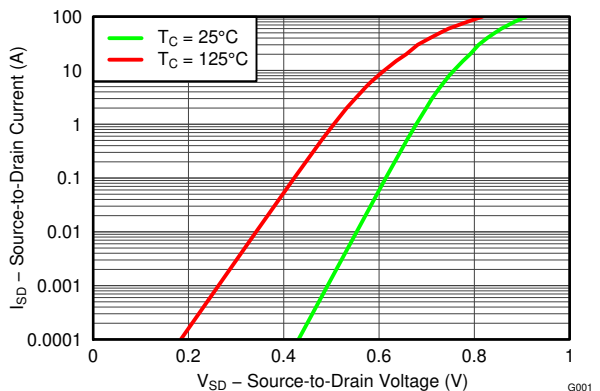
**Figure 4-6. Threshold Voltage vs Temperature**



**Figure 4-7. On-State Resistance vs Gate-to-Source Voltage**



**Figure 4-8. Normalized On-State Resistance vs Temperature**



**Figure 4-9. Typical Diode Forward Voltage**

### 4.3 Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

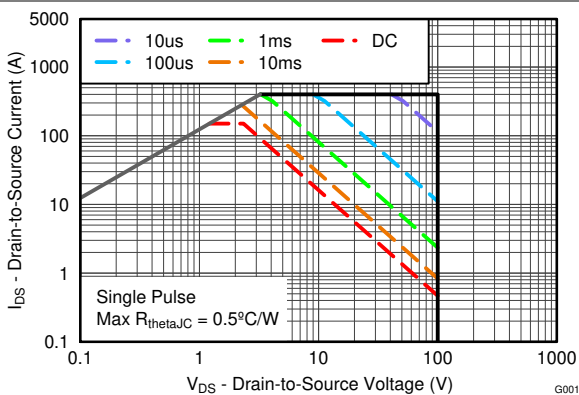


Figure 4-10. Maximum Safe Operating Area

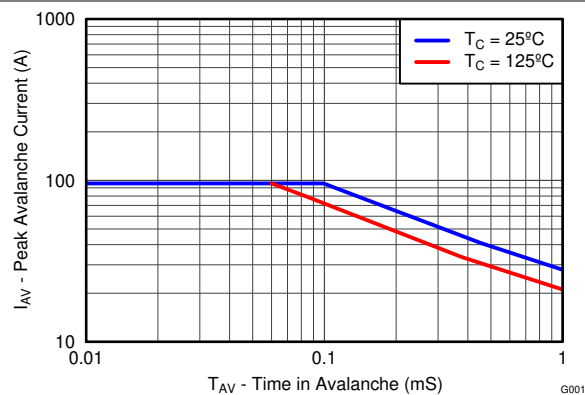


Figure 4-11. Single Pulse Unclamped Inductive Switching

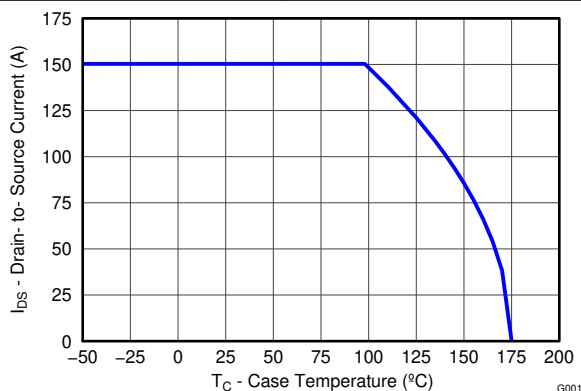


Figure 4-12. Maximum Drain Current vs Temperature

## 5 Device and Documentation Support

### 5.1 Third-Party Products Disclaimer

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### 5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (October 2014) to Revision C (May 2024) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... **1**

### Changes from Revision A (February 2014) to Revision B (October 2014) Page

- Updated Pulsed Drain Current conditions ..... **1**
- Updated the SOA in [Figure 4-10](#) ..... **4**

### Changes from Revision \* (January 2014) to Revision A (February 2014) Page

- Increased Pulsed Drain Current to 400A..... **1**
- Updated SOA Curve ..... **4**

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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