



DMOS

250mA Low-Dropout Regulator

FEATURES

- **NEW DMOS TOPOLOGY:**
Ultra Low Dropout Voltage:
150mV typ at 250mA
Output Capacitor *not* Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE:** 28μVrms
- **HIGH ACCURACY:** ±1.5% max
- **HIGH EFFICIENCY:**
 $I_{GND} = 600\mu A$ at $I_{OUT} = 250mA$
Not Enabled: $I_{GND} = 0.01\mu A$
- **2.5V, 2.8V, 2.85V, 3.0V, 3.3V, AND 5.0V
ADJUSTABLE OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON
REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**
SOT23-5, SOT223-5, and SO-8

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

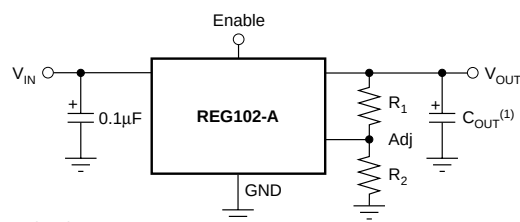
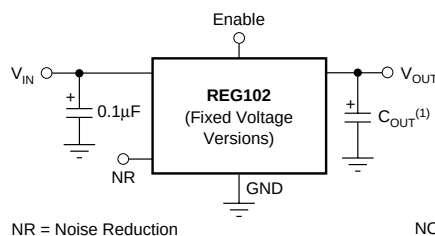
DESCRIPTION

The REG102 is a family of low-noise, low-dropout linear regulators with low ground pin current. The new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 150mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1μF.

Typical ground pin current is only 600μA (at $I_{OUT} = 250mA$) and drops to 10nA when not enabled. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG102 has very low output noise (typically 28μVrms for $V_{OUT} = 3.3V$ with $C_{NR} = 0.01\mu F$), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG102 is well protected—internal circuitry provides a current limit that protects the load from damage; furthermore, thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG102 is available in SOT23-5, SOT223-5, and SO-8 packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Input Voltage, V_{IN}	–0.3V to 12V
Enable Input Voltage, V_{EN}	–0.3V to V_{IN}
Feedback Voltage, V_{FB}	–0.3V to 6.0V
NR Pin Voltage, V_{NR}	–0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (T_J)	–55°C to +125°C
Storage Temperature Range (T_A)	–65°C to +150°C
Lead Temperature (soldering, 3s)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

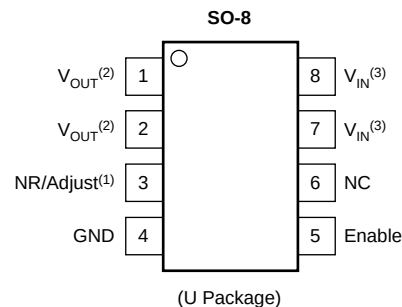
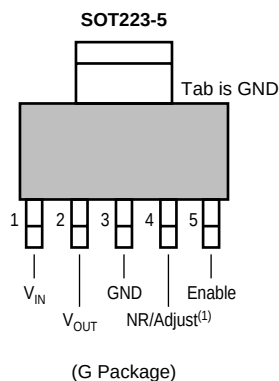
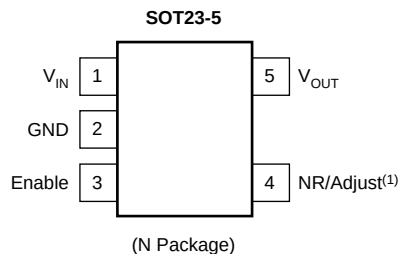
PRODUCT	$V_{OUT}^{(2)}$
REG102xx-yyy/z	XX is package designator. YYYY is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). ZZZ is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

PIN CONFIGURATIONS

Top View



NOTES: (1) For REG102A-A: voltage setting resistor pin.
 All other models: noise reduction capacitor pin.
 (2) Both pin 1 and pin 2 must be connected.
 (3) Both pin 7 and pin 8 must be connected.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

At $T_J = +25^{\circ}\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$ ($V_{OUT} = 2.5\text{V}$ for REG102-A), $V_{ENABLE} = 1.8\text{V}$, $I_{OUT} = 5\text{mA}$, $C_{NR} = 0.01\mu\text{F}$, and $C_{OUT} = 0.1\mu\text{F}^{(1)}$, unless otherwise noted.

PARAMETER	CONDITION	REG102NA REG102GA REG102UA			UNITS
		MIN	TYP	MAX	
OUTPUT VOLTAGE					
Output Voltage Range	V_{OUT}		2.5		V
REG102-2.5			2.8		V
REG102-2.8			2.85		V
REG102-3.0			3.0		V
REG102-3.3			3.3		V
REG102-5			5		V
REG102-A		2.5		5.5	V
Reference Voltage	V_{REF}		1.26		V
Adjust Pin Current	I_{ADJ}		0.2	1	μA
Accuracy			± 0.5	± 1.5	%
Over Temperature				± 2.3	%
vs Temperature	dV_{OUT}/dT		50		ppm/ $^{\circ}\text{C}$
vs Line and Load			± 0.8	± 2.0	%
Over Temperature				± 2.8	%
DC DROPOUT VOLTAGE⁽²⁾	V_{DROP}				
For all models			4	10	mV
Over Temperature			150	220	mV
				270	mV
VOLTAGE NOISE	V_n				
$f = 10\text{Hz}$ to 100kHz					
Without C_{NR} (all models)					μVrms
With C_{NR} (all fixed voltage models)					μVrms
			$23\mu\text{Vrms/V} \cdot V_{OUT}$		
			$7\mu\text{Vrms/V} \cdot V_{OUT}$		
OUTPUT CURRENT					
Current Limit ⁽³⁾	I_{CL}	340	400	470	mA
Over Temperature		300		490	mA
Short-Circuit Current Limit	I_{SC}		150		mA
RIPPLE REJECTION					
$f = 120\text{Hz}$			65		dB
ENABLE CONTROL					
V_{ENABLE} High (output enabled)	V_{ENABLE}	1.8		V_{IN}	V
V_{ENABLE} Low (output disabled)		-0.2		0.5	V
I_{ENABLE} High (output enabled)	I_{ENABLE}		1	100	nA
I_{ENABLE} Low (output disabled)			2	100	nA
Output Disable Time			50		μs
Output Enable Softstart Time			1.5		ms
THERMAL SHUTDOWN					
Junction Temperature					
Shutdown			160		$^{\circ}\text{C}$
Reset from Shutdown			140		$^{\circ}\text{C}$
GROUND PIN CURRENT					
Ground Pin Current	I_{GND}		400	500	μA
			600	800	μA
Enable Pin Low			0.01	0.2	μA
INPUT VOLTAGE	V_{IN}				
Operating Input Voltage Range ⁽⁵⁾		1.8		10	V
Specified Input Voltage Range		$V_{OUT} + 0.4$		10	V
Over Temperature		$V_{OUT} + 0.6$		10	V
TEMPERATURE RANGE					
Specified Range	T_J	-40		+85	$^{\circ}\text{C}$
Operating Range	T_J	-55		+125	$^{\circ}\text{C}$
Storage Range	T_A	-65		+150	$^{\circ}\text{C}$
Thermal Resistance					
SOT23-5 Surface-Mount	θ_{JA}		200		$^{\circ}\text{C/W}$
SO-8 Surface-Mount	θ_{JA}		150		$^{\circ}\text{C/W}$
SOT223-5 Surface-Mount	θ_{JC}		15		$^{\circ}\text{C/W}$
	θ_{JA}		See Figure 8		$^{\circ}\text{C/W}$

NOTES: (1) The REG102 does not require a minimum output capacitor for stability, however, transient response can be improved with proper capacitor selection.

(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at $V_{IN} = V_{OUT} + 1\text{V}$ at fixed load.

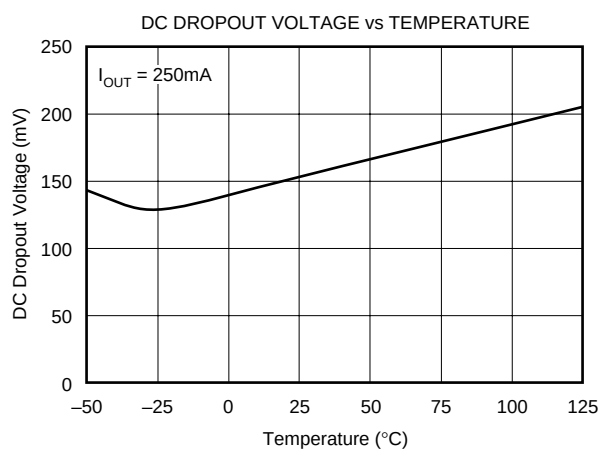
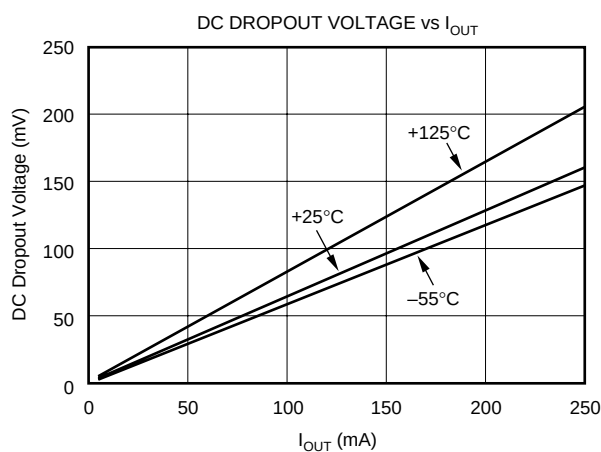
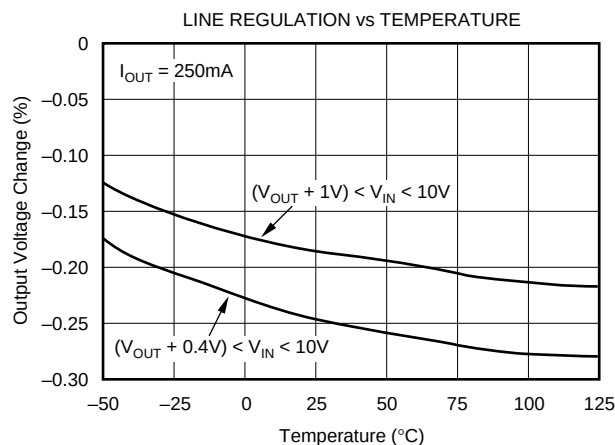
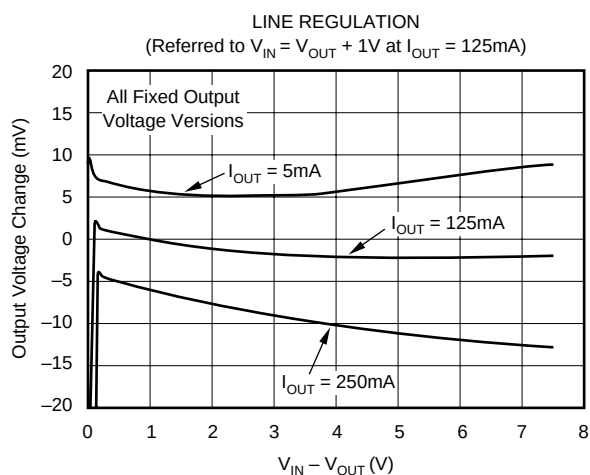
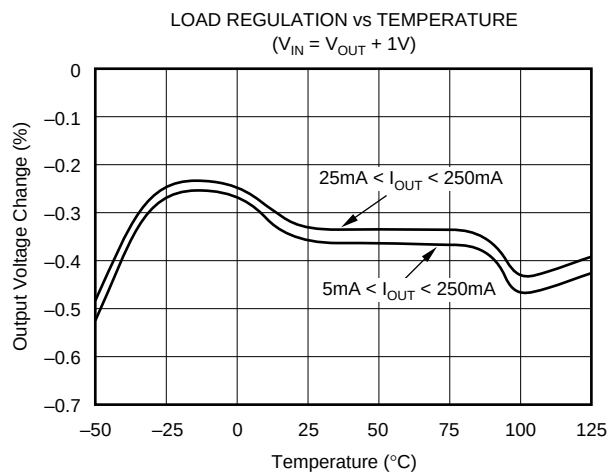
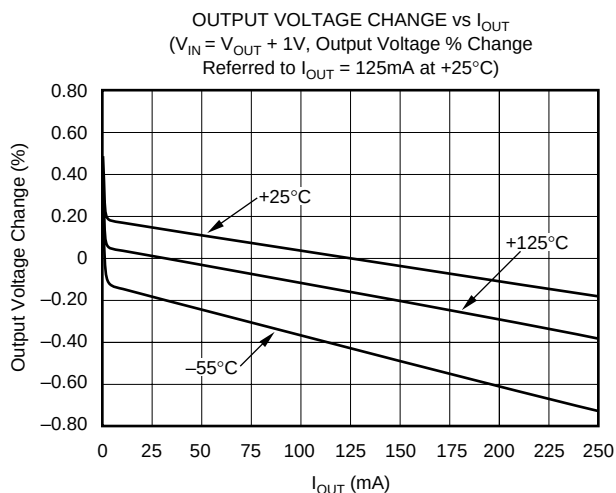
(3) Current limit is the output current that produces a 10% change in output voltage from $V_{IN} = V_{OUT} + 1\text{V}$ and $I_{OUT} = 5\text{mA}$.

(4) For $V_{ENABLE} > 6.5\text{V}$, see typical characteristic I_{ENABLE} vs V_{ENABLE} .

(5) The REG102 no longer regulates when $V_{IN} < V_{OUT} + V_{DROP(MAX)}$. In dropout, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at $T_J = +25^{\circ}\text{C}$.

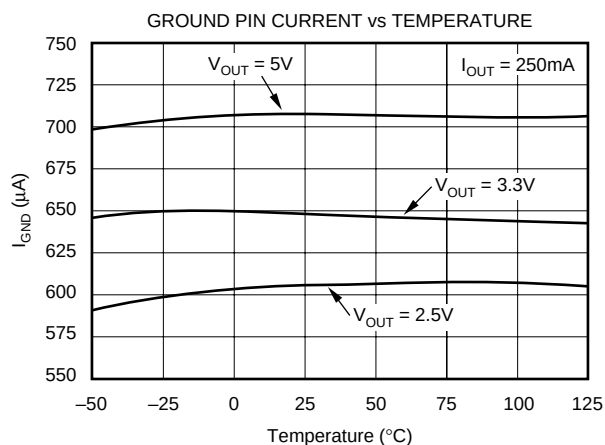
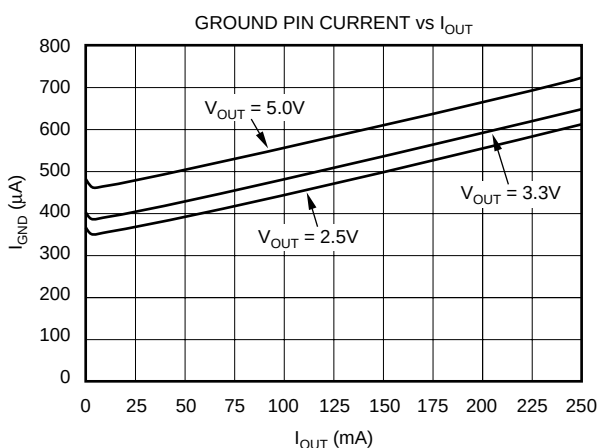
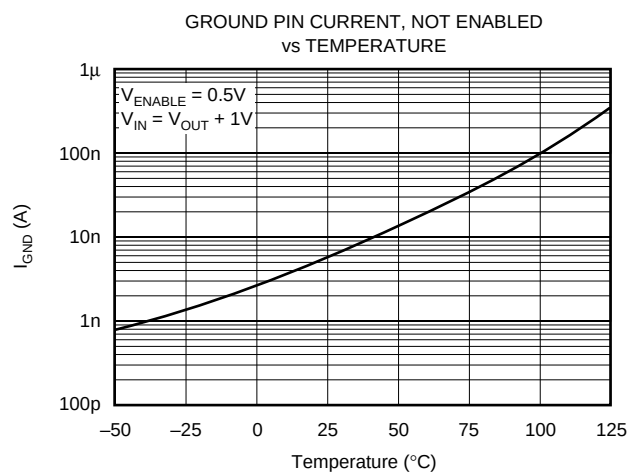
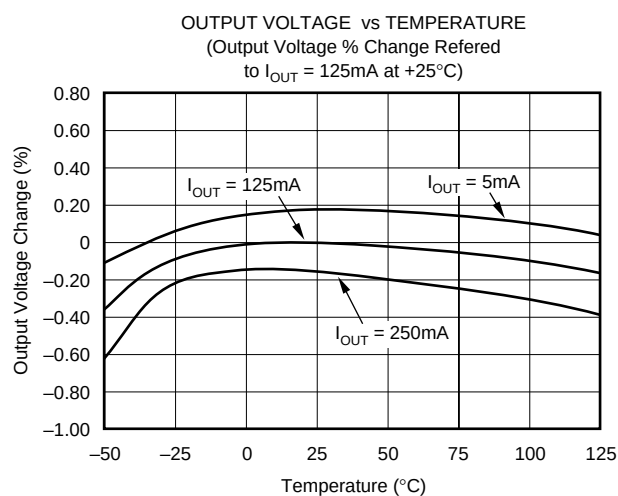
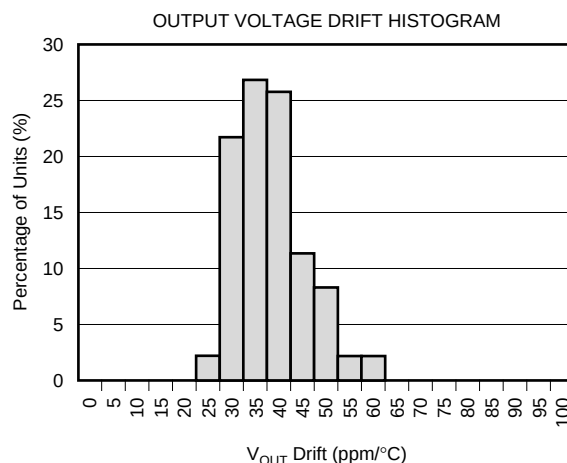
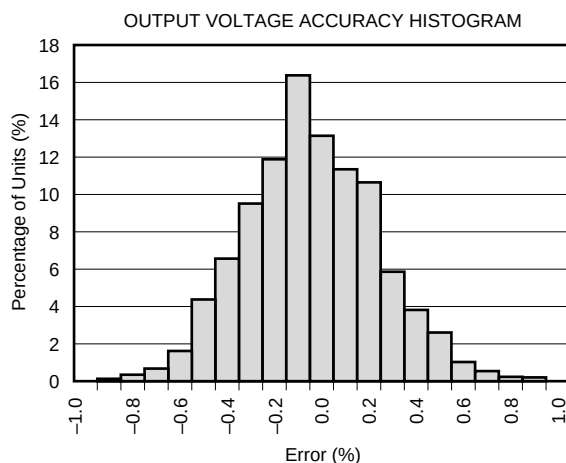
TYPICAL CHARACTERISTICS

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



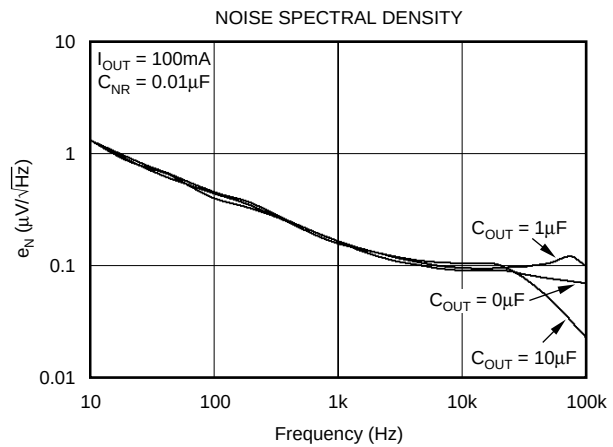
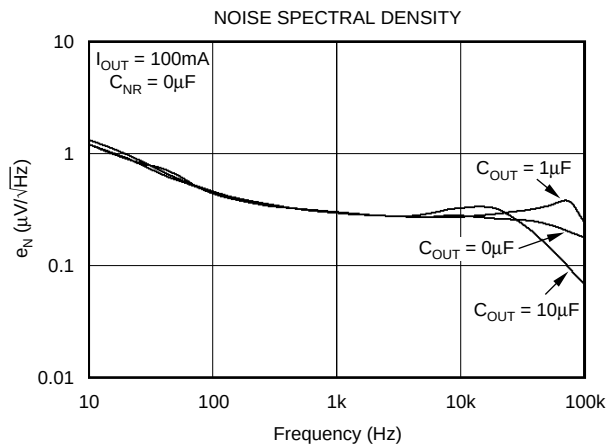
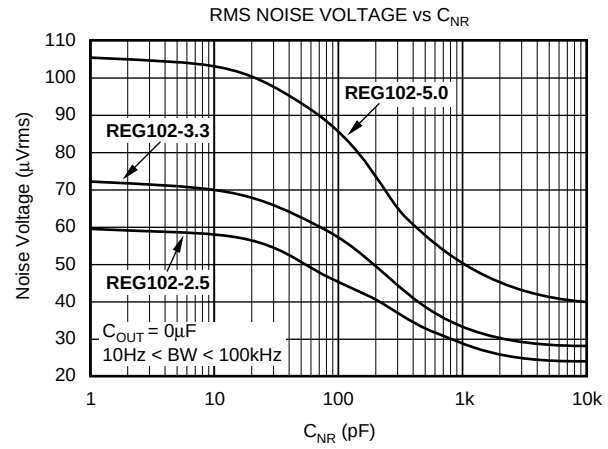
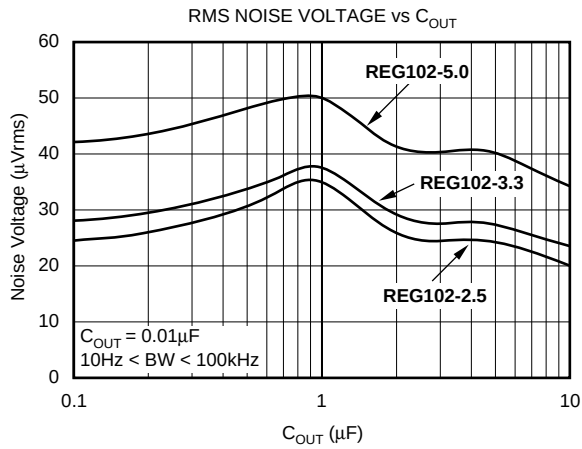
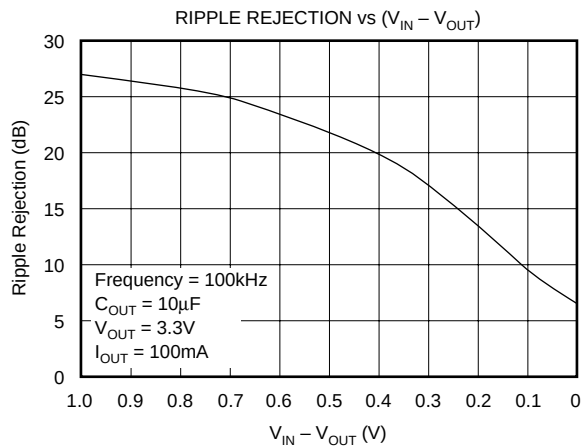
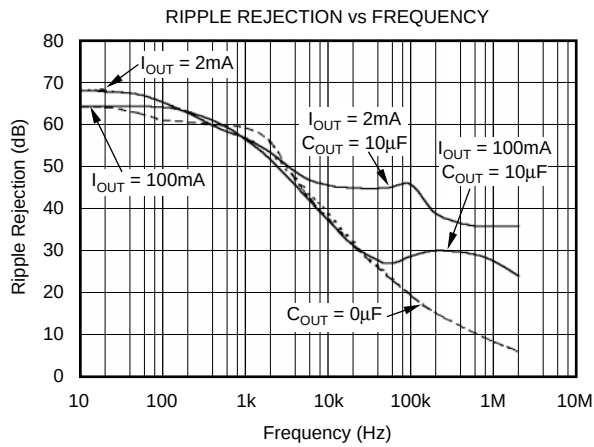
TYPICAL CHARACTERISTICS (Cont.)

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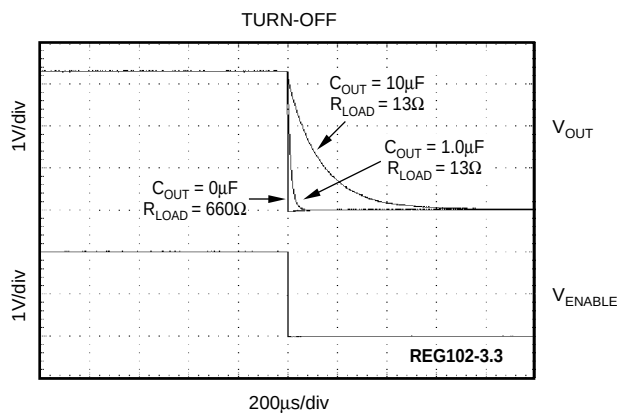
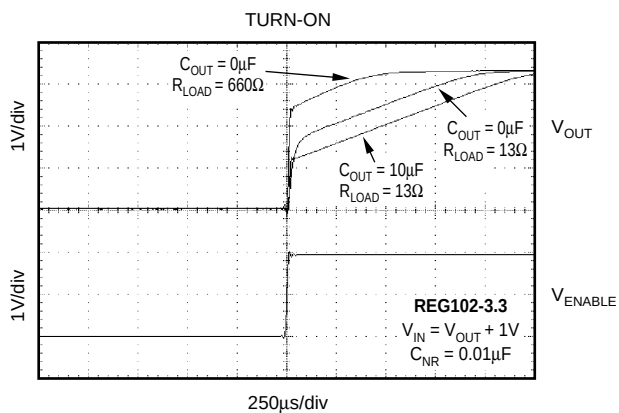
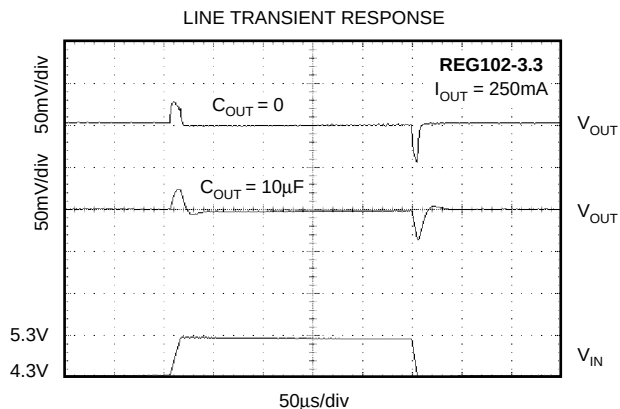
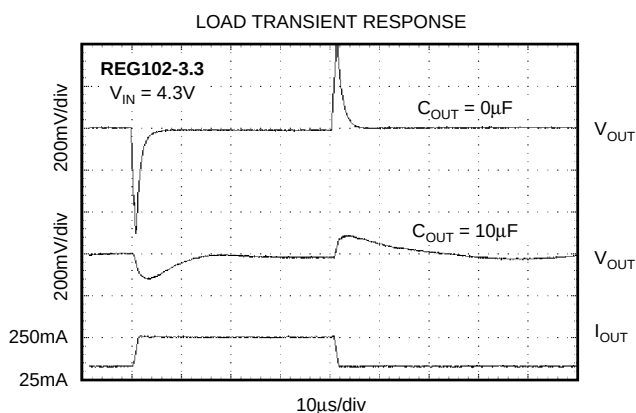
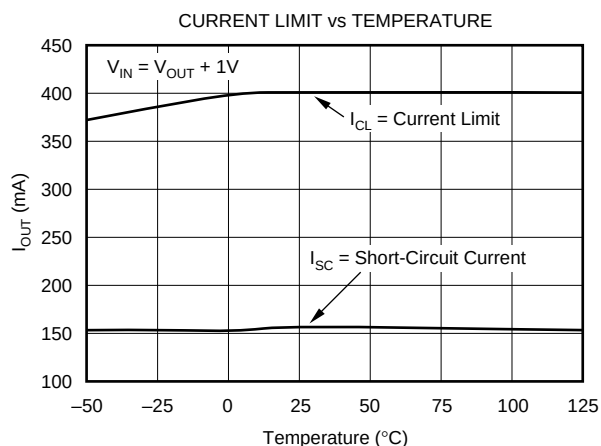
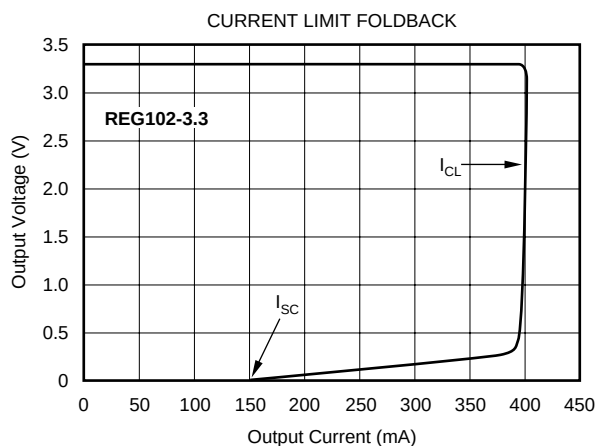
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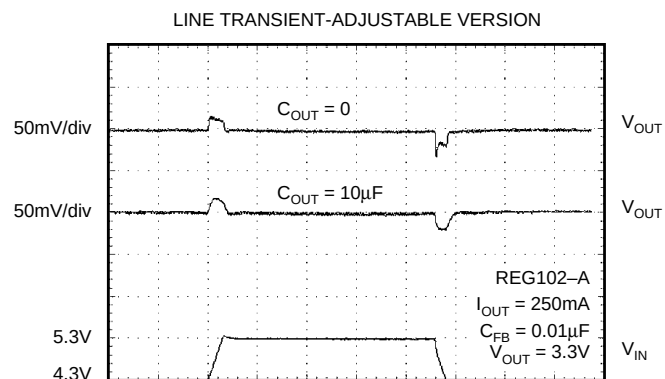
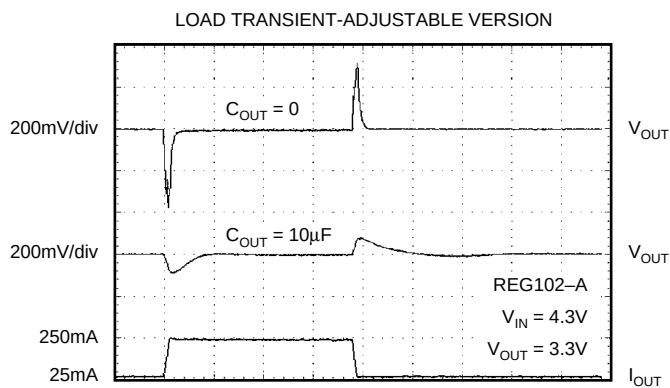
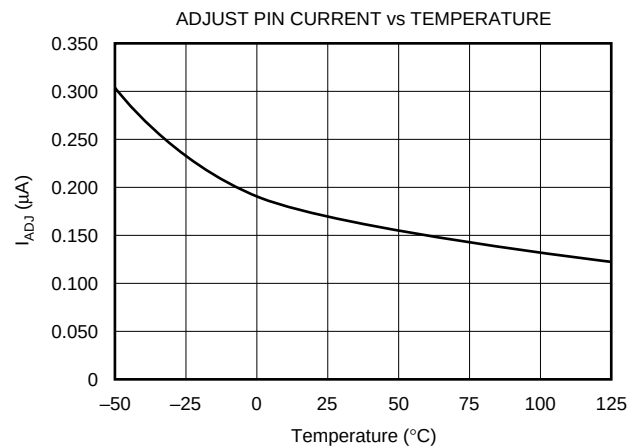
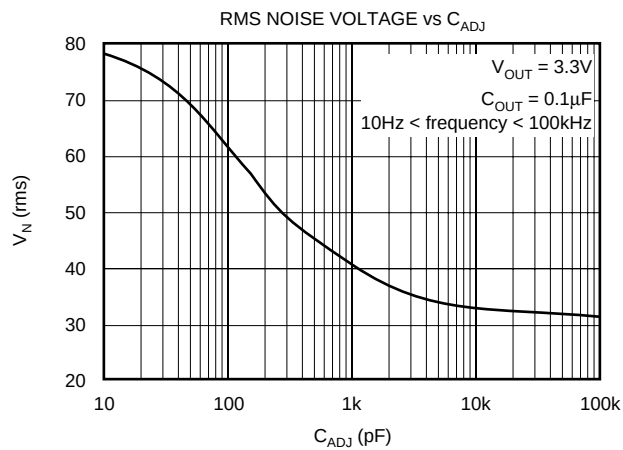
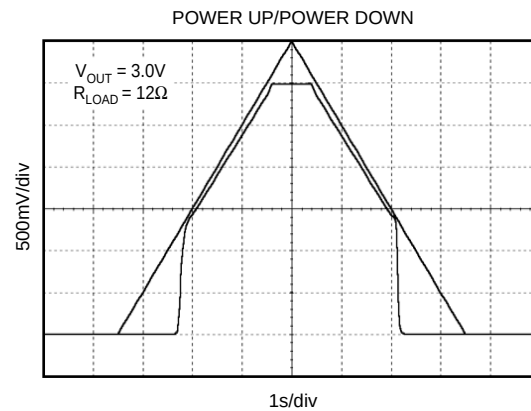
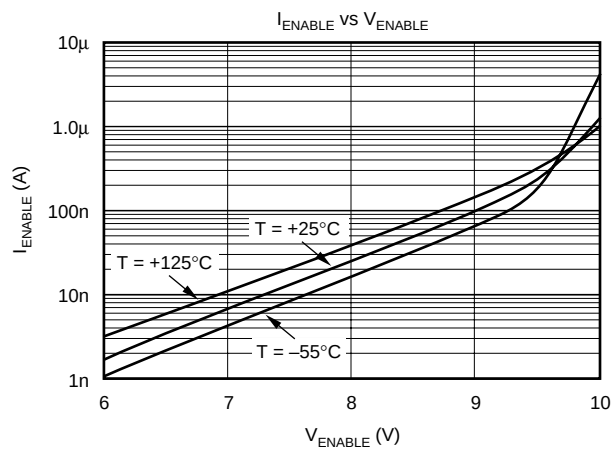
TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



BASIC OPERATION

The REG102 series of LDO (low dropout) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version as well. The REG102 belongs to a family of new generation LDO regulators that use a DMOS pass transistor to achieve ultra low-dropout performance and freedom from output capacitor constraints. Ground pin current remains under 1mA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG102 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10 μ F or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by adding a 1k Ω to 2k Ω load resistor, using capacitance values smaller than 10 μ F, or keeping the effective series resistance greater than 0.05 Ω including the capacitor ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is a good standard analog design practice to connect a 0.1 μ F low ESR capacitor across the input supply voltage. This is recommended to counteract reactive input sources and improve ripple rejection by reducing input voltage ripple.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG102A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

INTERNAL CURRENT LIMIT

The REG102 internal current limit has a typical value of 400mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 150mA, which helps to protect

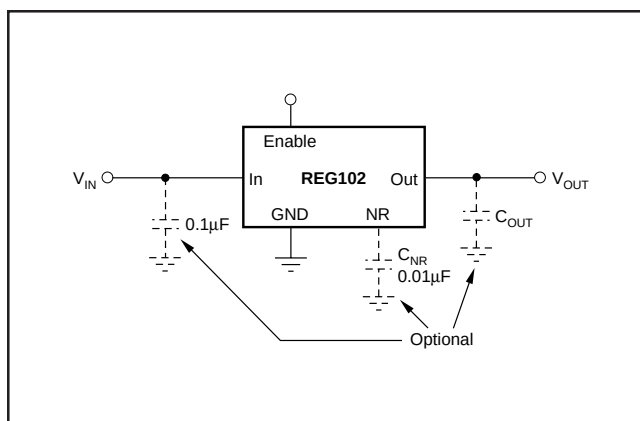


FIGURE 1. Fixed Voltage Nominal Circuit for the REG102.

the regulator from damage under all load conditions. A characteristic of V_{OUT} versus I_{OUT} is given in Figure 3 and in the Typical Characteristics section.

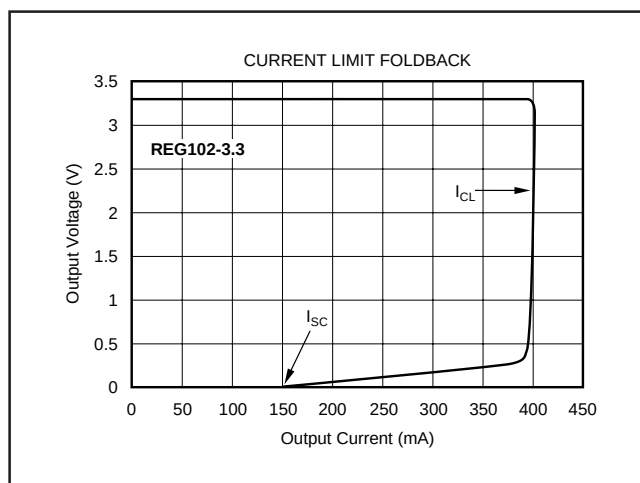


FIGURE 3. Foldback Current Limit of the REG102-3.3 at 25°C.

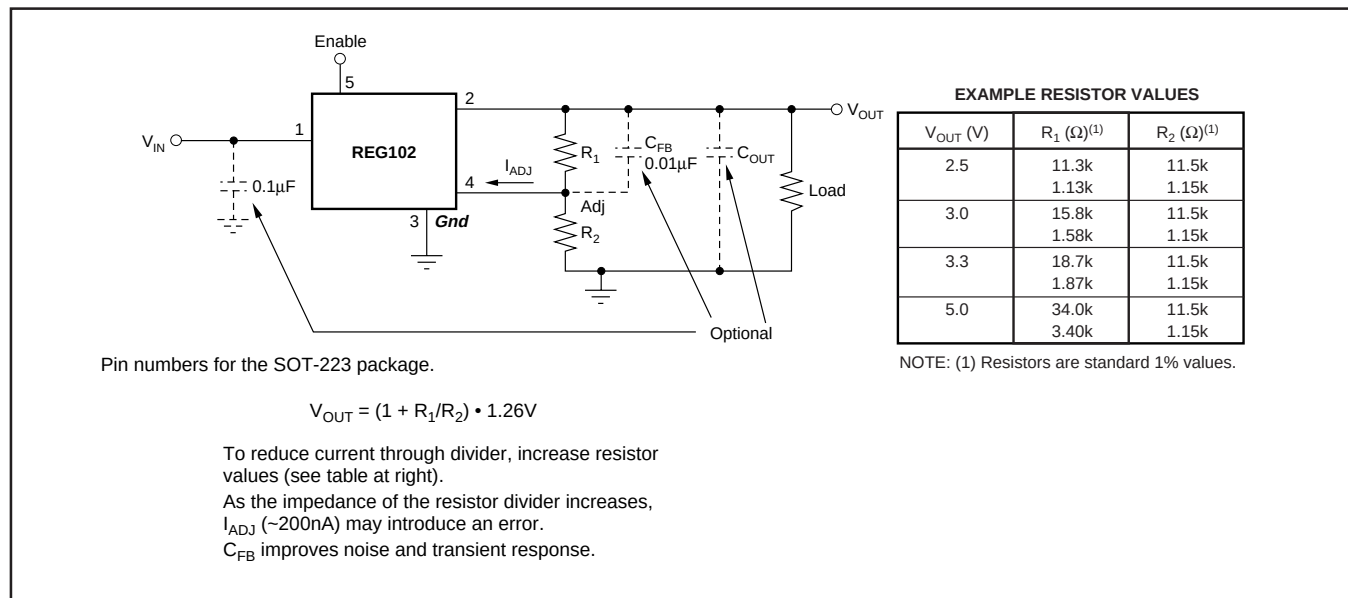


FIGURE 2. Adjustable Voltage Circuit for the REG102A.

ENABLE

The Enable pin is active high and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When not used, the Enable pin can be connected to V_{IN} . When a pull-up resistor is used, and operation below 1.8V is required, use pull-up resistor values below 50k Ω .

OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the REG102 and generates approximately 29 μ Vrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu\text{Vrms} \frac{R_1 + R_2}{R_2} = 29\mu\text{Vrms} \cdot \frac{V_{OUT}}{V_{REF}} \quad (1)$$

As the value of V_{REF} is 1.26V, this relationship reduces to:

$$V_N = 23 \frac{\mu\text{Vrms}}{\text{V}} \cdot V_{OUT} \quad (2)$$

Connecting a capacitor, C_{NR} , from the Noise Reduction (NR) pin to ground forms a low-pass filter for the voltage reference. Adding C_{NR} (as shown in Figure 4) forms a low-pass filter for the voltage reference. For $C_{NR} = 10\text{nF}$, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for $V_{OUT} = 3.3\text{V}$. This noise reduction effect is shown in Figure 5 and as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

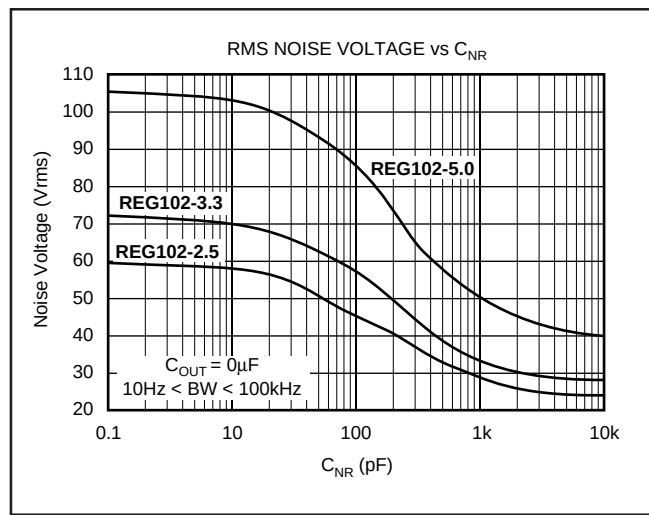


FIGURE 5. Output Noise versus Noise Reduction Capacitor.

Noise can be further reduced by carefully choosing an output capacitor, C_{OUT} . Best overall noise performance is achieved with very low ($< 0.22\mu\text{F}$) or very high ($> 2.2\mu\text{F}$) values of C_{OUT} (see the *RMS Noise Voltage vs C_{OUT}* typical characteristic).

The REG102 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN} . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of I_{OUT} and C_{OUT} .

The REG102 adjustable version does not have the noise-reduction pin available; however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB} , connected from the output to the adjust pin can reduce both the output noise and the peak error from a load transient (see the typical characteristics for output noise performance).

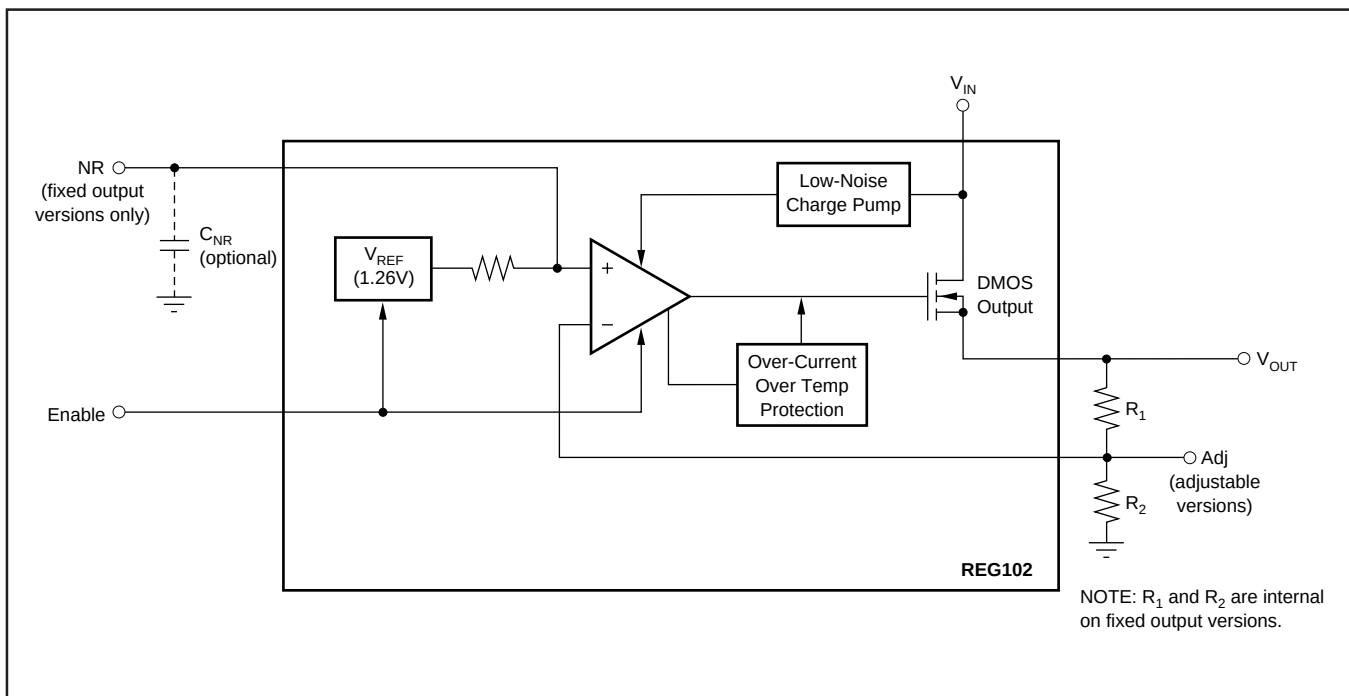


FIGURE 4. Block Diagram.

DROPOUT VOLTAGE

The REG102 uses an N-channel DMOS as the pass element. When $(V_{IN} - V_{OUT})$ is less than the drop-out voltage (V_{DROP}), the DMOS pass device behaves like a resistor; therefore, for low values of $(V_{IN} - V_{OUT})$, the regulator input-to-output resistance is the $R_{DS(ON)}$ of the DMOS pass element (typically 600m Ω). For static (DC) loads, the REG102 typically maintains regulation down to a $(V_{IN} - V_{OUT})$ voltage drop of 150mV at full rated output current. In Figure 6, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent dropout under DC load conditions.

For large step changes in load current, the REG102 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient drop-out region is shown as the top line in Figure 6 and values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

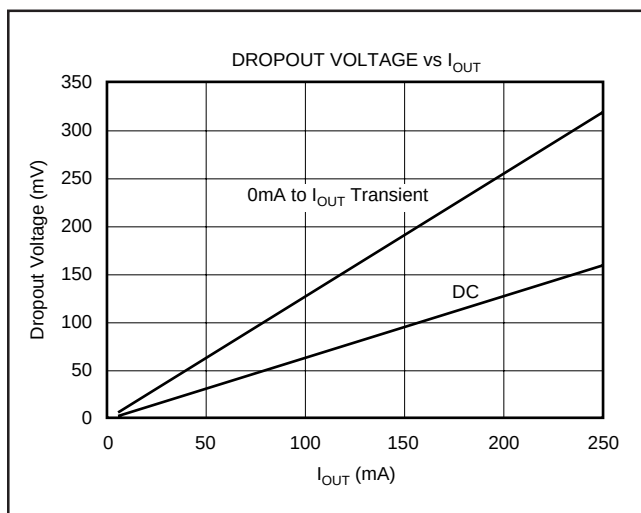


FIGURE 6. Transient and DC Dropout.

In the transient dropout region between DC and Transient, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available headroom V_{IN} to V_{OUT} voltage drop. Under worst-

case conditions (full-scale load change with $(V_{IN} - V_{OUT})$ voltage drop close to DC dropout levels), the REG102 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG102 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 0.47 μ F) from the output pin to ground can improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin can also improve the transient response.

THERMAL PROTECTION

Power dissipated within the REG102 can cause the junction temperature to rise. The REG102 has thermal shutdown circuitry that protects the regulator from damage which disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, but can have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG102 is designed to protect against overload conditions and is not intended to replace proper heat sinking. Continuously running the REG102 into thermal shutdown will degrade reliability.

POWER DISSIPATION

The REG102 is available in three different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Although it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several simplified configurations are shown in Figure 7. In all cases, the PCB copper area is bare copper (free of solder resist mask), not solder plated, and are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

Power dissipation depends on input voltage, load conditions, and duty cycle and is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (3)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

REGULATOR MOUNTING

The tab of the SOT-223 package is electrically connected to ground. For best thermal performance, this tab must be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation, as shown in Figure 8.

Although the tab of the SOT-223 is electrical ground, it is not intended to carry current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG102 devices are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the Texas Instruments web site (www.ti.com).

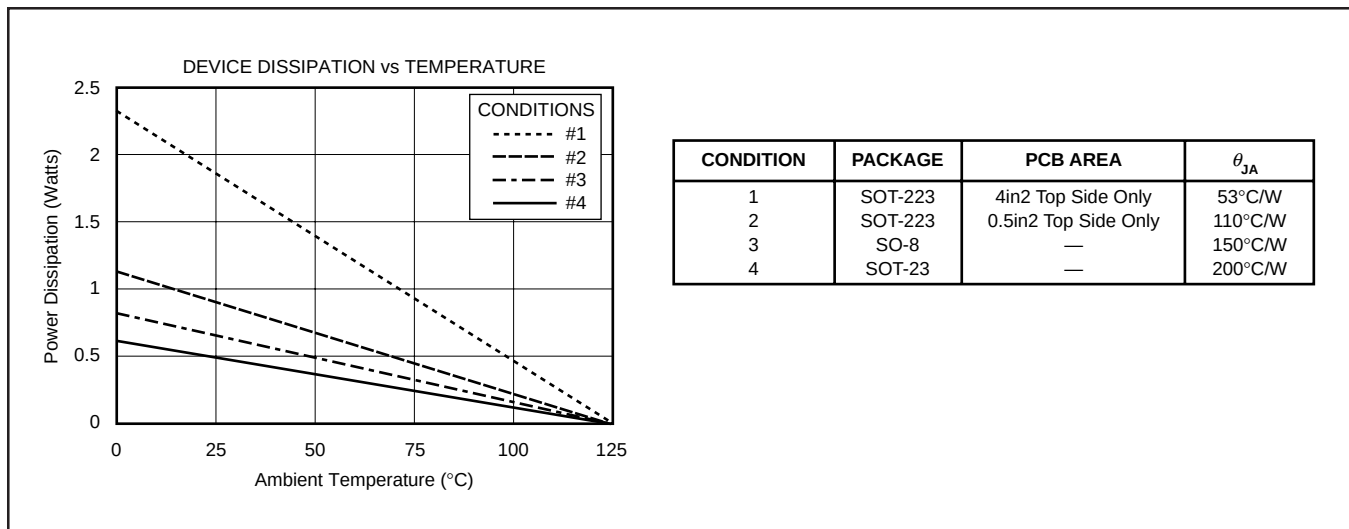


FIGURE 7. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

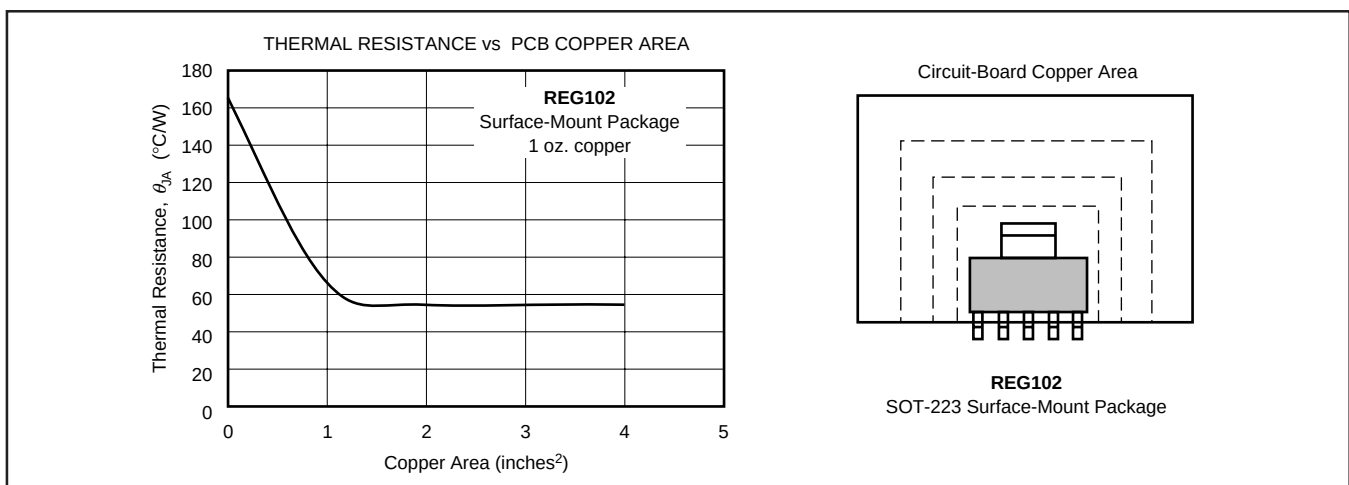


FIGURE 8. Thermal Resistance versus PCB Area for the Five-Lead SOT-223.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG102GA-2.5	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R102G25	
REG102GA-2.85	LIFEBUY	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R102285	
REG102GA-3	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R102G30	Samples
REG102GA-3.3	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R102G33	Samples
REG102GA-3.3/2K5	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R102G33	Samples
REG102GA-3.3G4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R102G33	Samples
REG102GA-5	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R102G50	Samples
REG102GA-A	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R102GA	Samples
REG102GA-A/2K5	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R102GA	Samples
REG102GA-AG4	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		R102GA	Samples
REG102NA-2.5/250	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2D	
REG102NA-2.5/250G4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2D	
REG102NA-2.8/250	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2E	
REG102NA-2.85/250	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2N	
REG102NA-2.85/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2N	Samples
REG102NA-3.3/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2C	Samples
REG102NA-3.3/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2C	Samples
REG102NA-3/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2G	Samples
REG102NA-3/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2G	Samples
REG102NA-3/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2G	Samples
REG102NA-5/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2B	Samples
REG102NA-5/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG102NA-5/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO2B	Samples
REG102NA-A/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2A	Samples
REG102NA-A/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2A	Samples
REG102NA-A/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		RO2A	Samples
REG102UA-2.5	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REG 102U25	
REG102UA-3	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 102U30	Samples
REG102UA-3.3	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 102U33	Samples
REG102UA-3.3/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 102U33	Samples
REG102UA-5	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 102U50	Samples
REG102UA-5/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 102U50	Samples
REG102UA-5G4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 102U50	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

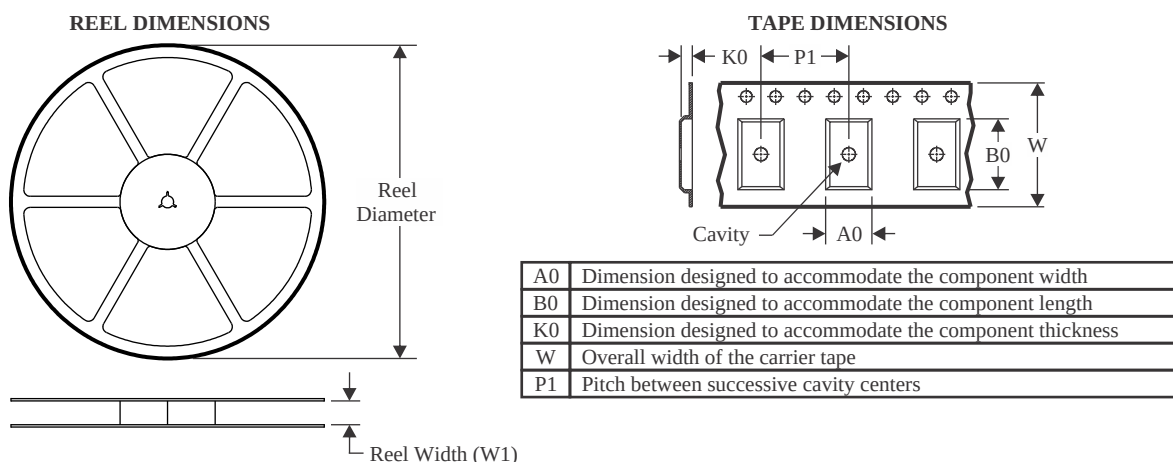
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

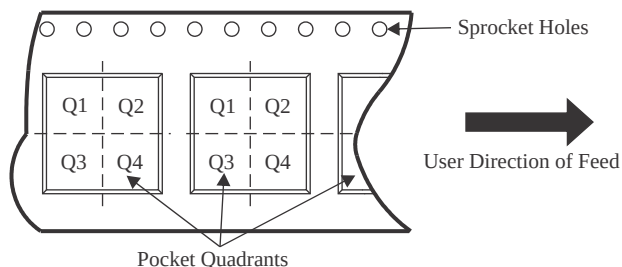
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

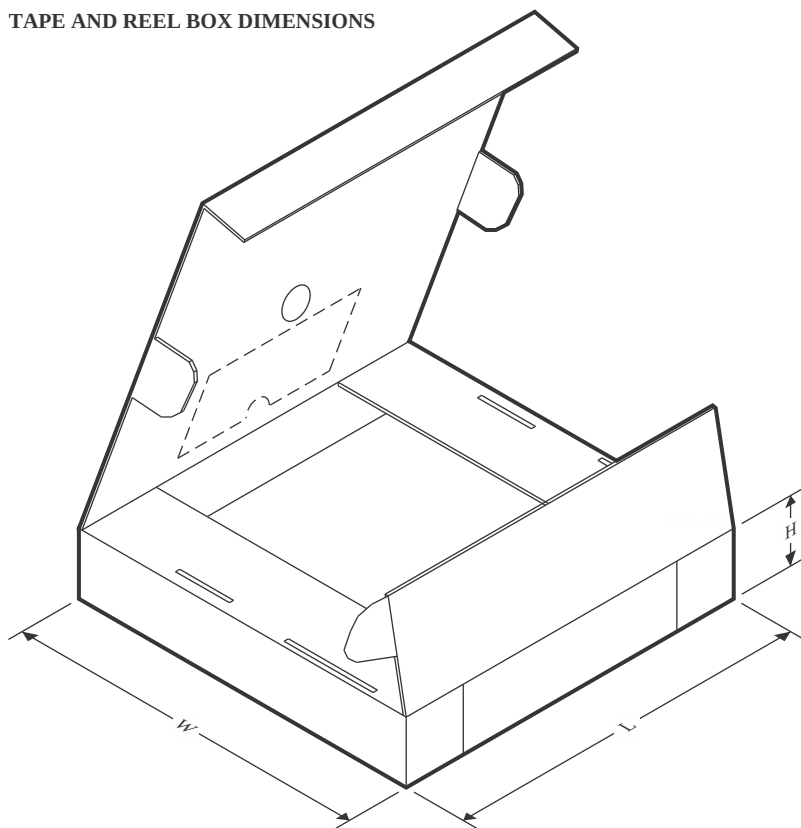


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG102GA-3.3/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG102GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG102NA-2.5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-2.8/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-2.8/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-2.85/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-2.85/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-2.85/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-2.85/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-3.3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-3.3/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-3.3/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-3.3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-3/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-3/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG102NA-3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-5/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-5/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
REG102NA-A/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102NA-A/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG102UA-3.3/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG102UA-5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

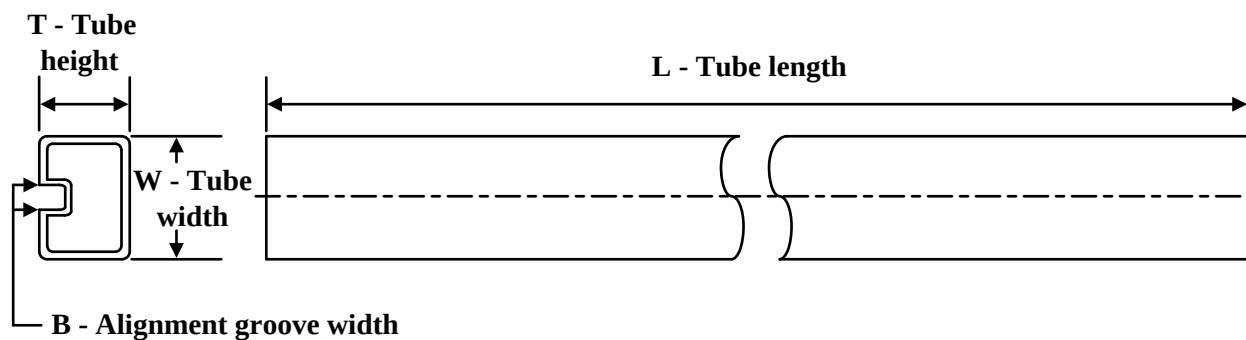


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG102GA-3.3/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG102GA-A/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG102NA-2.5/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG102NA-2.8/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG102NA-2.8/250	SOT-23	DBV	5	250	180.0	180.0	18.0
REG102NA-2.85/250	SOT-23	DBV	5	250	180.0	180.0	18.0
REG102NA-2.85/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG102NA-2.85/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG102NA-2.85/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
REG102NA-3.3/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG102NA-3.3/250	SOT-23	DBV	5	250	180.0	180.0	18.0
REG102NA-3.3/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
REG102NA-3.3/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG102NA-3/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG102NA-3/250	SOT-23	DBV	5	250	180.0	180.0	18.0
REG102NA-3/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
REG102NA-3/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG102NA-5/250	SOT-23	DBV	5	250	180.0	180.0	18.0

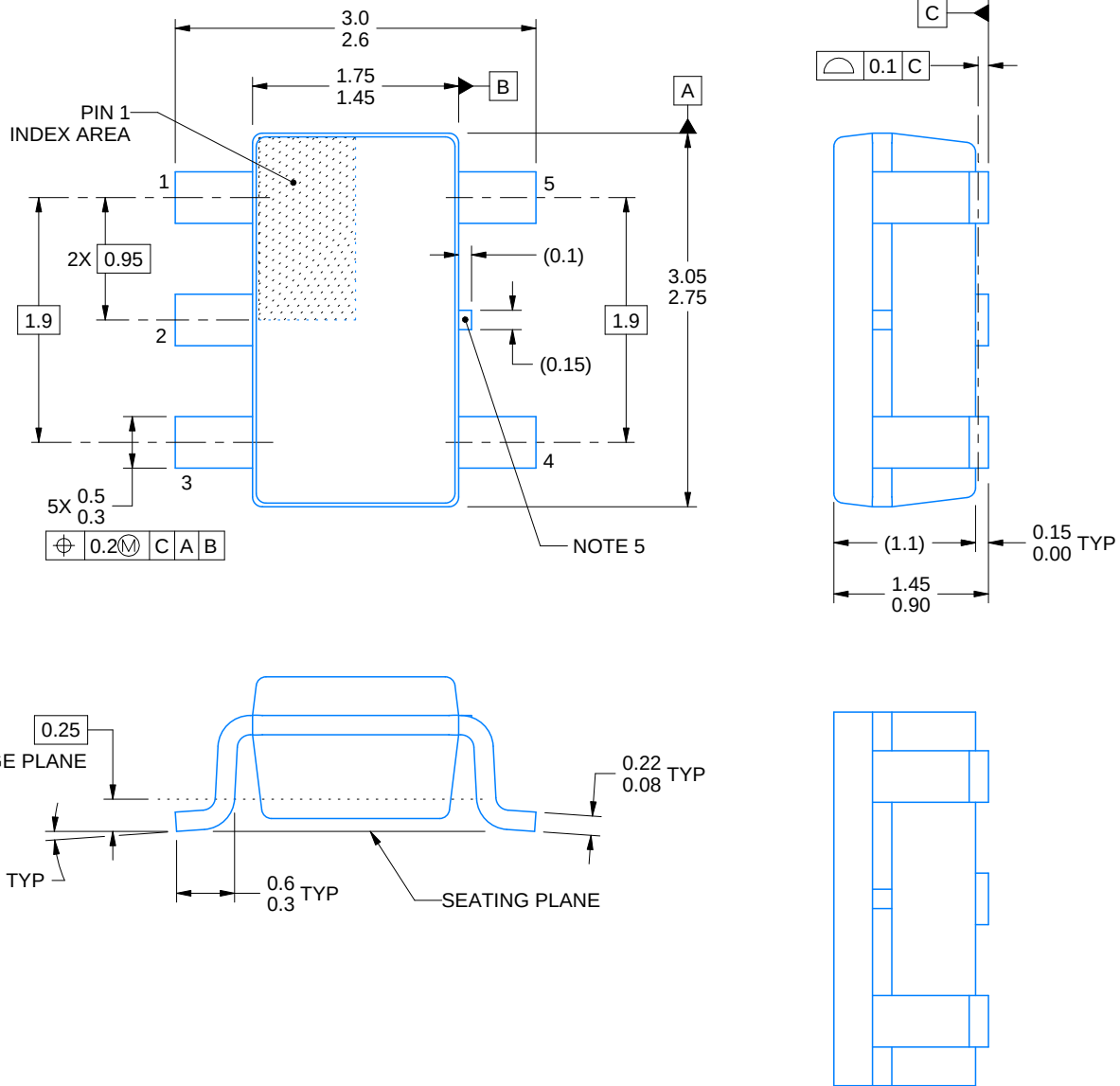
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG102NA-5/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG102NA-5/3K	SOT-23	DBV	5	3000	200.0	183.0	25.0
REG102NA-5/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
REG102NA-A/250	SOT-23	DBV	5	250	200.0	183.0	25.0
REG102NA-A/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG102UA-3.3/2K5	SOIC	D	8	2500	356.0	356.0	35.0
REG102UA-5/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
REG102GA-2.5	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-2.85	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-3	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-3.3	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-3.3G4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-5	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-A	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102GA-AG4	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
REG102UA-2.5	D	SOIC	8	75	506.6	8	3940	4.32
REG102UA-3	D	SOIC	8	75	506.6	8	3940	4.32
REG102UA-3.3	D	SOIC	8	75	506.6	8	3940	4.32
REG102UA-5	D	SOIC	8	75	506.6	8	3940	4.32
REG102UA-5G4	D	SOIC	8	75	506.6	8	3940	4.32



ALTERNATIVE PACKAGE SINGULATION VIEW

4214839/J 02/2024

NOTES:

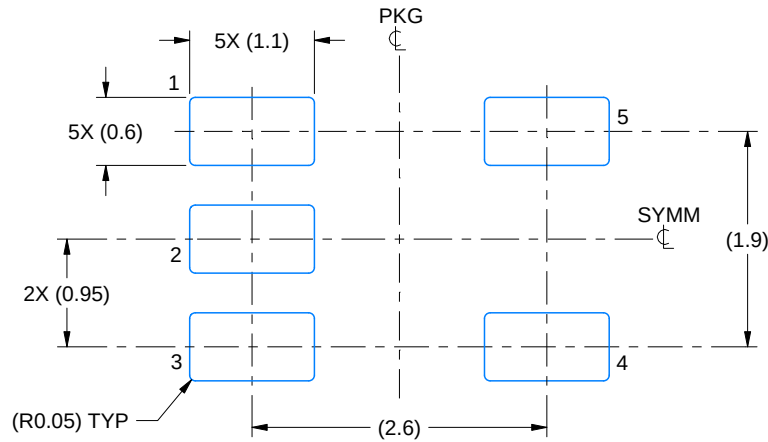
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

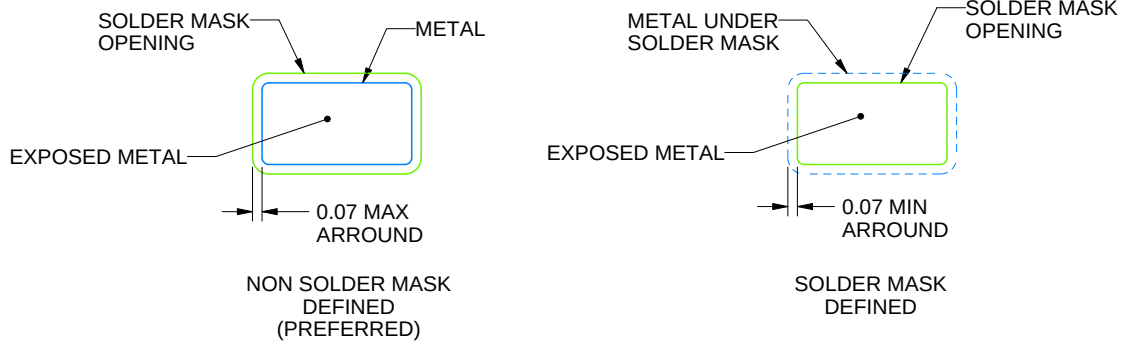
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

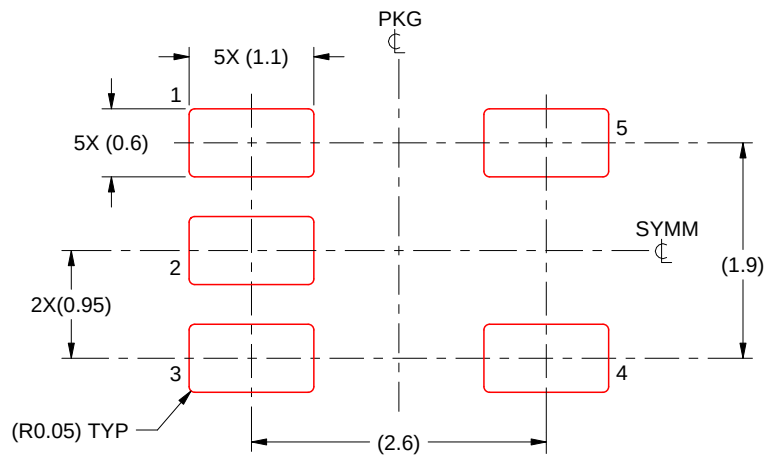
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

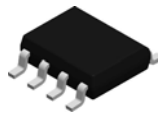


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

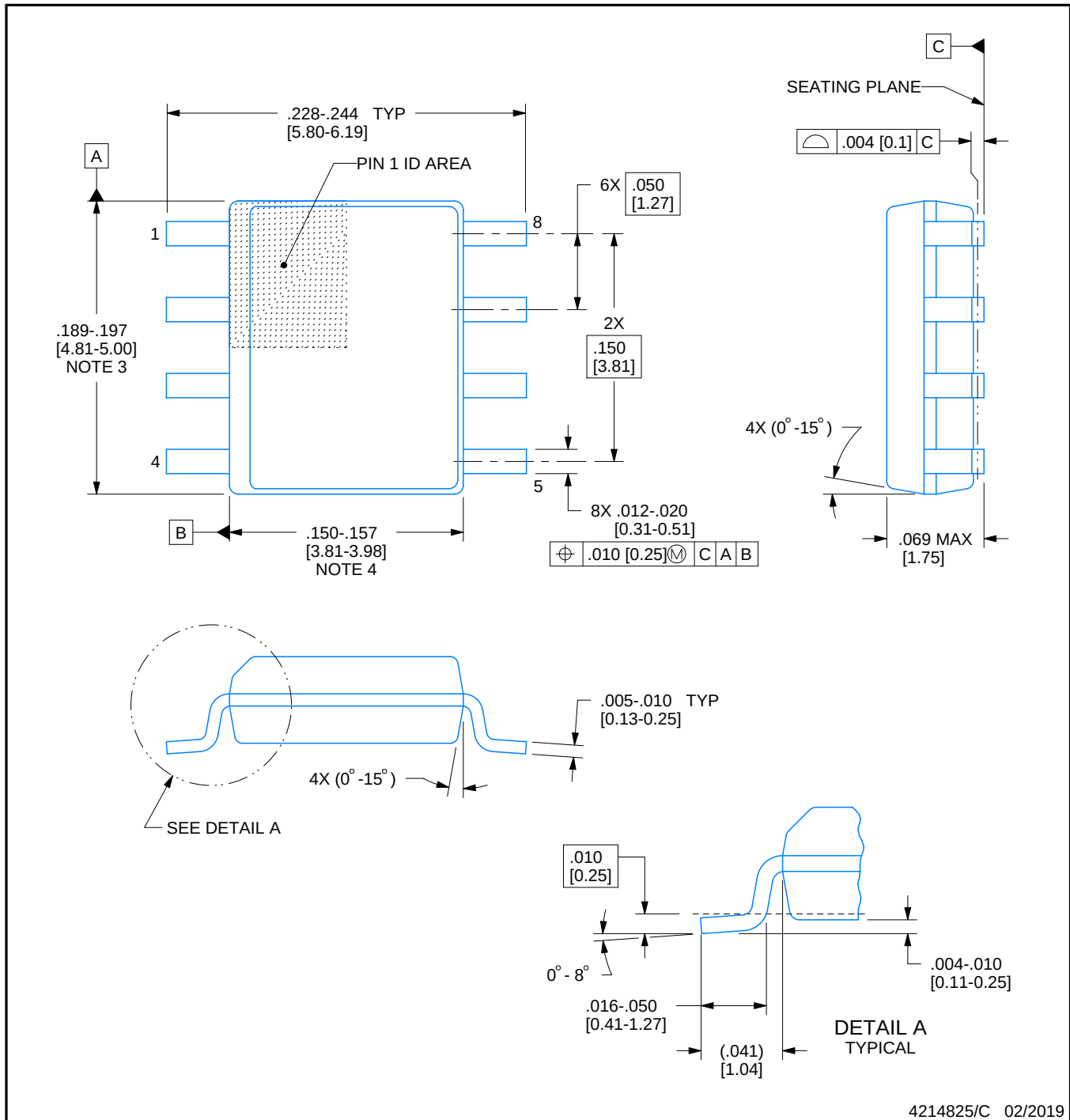


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

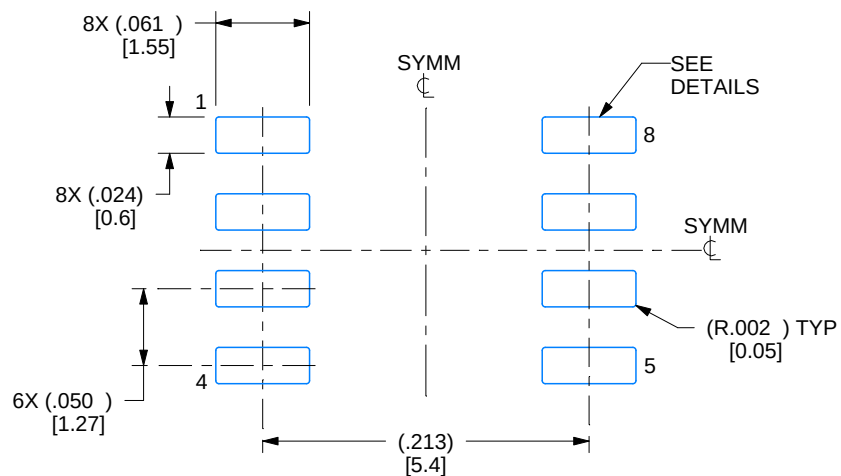
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

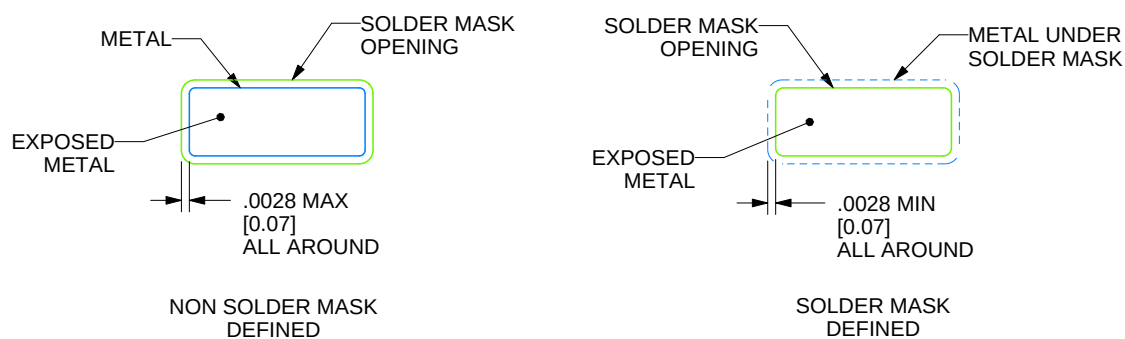
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

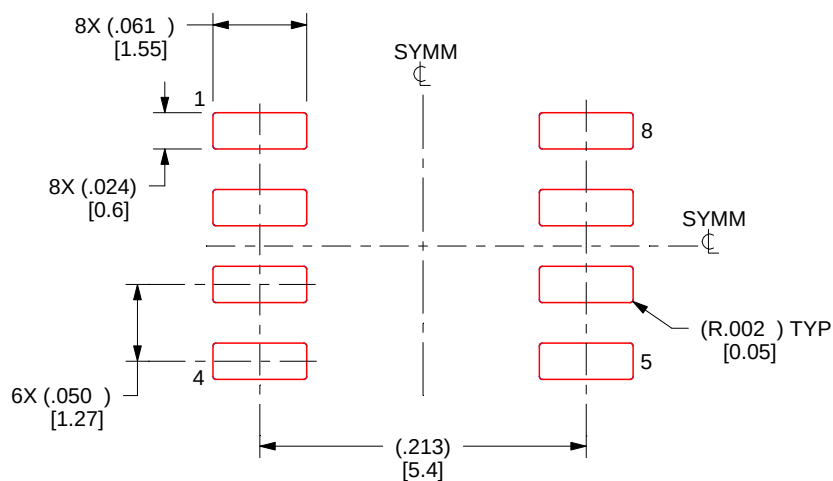
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

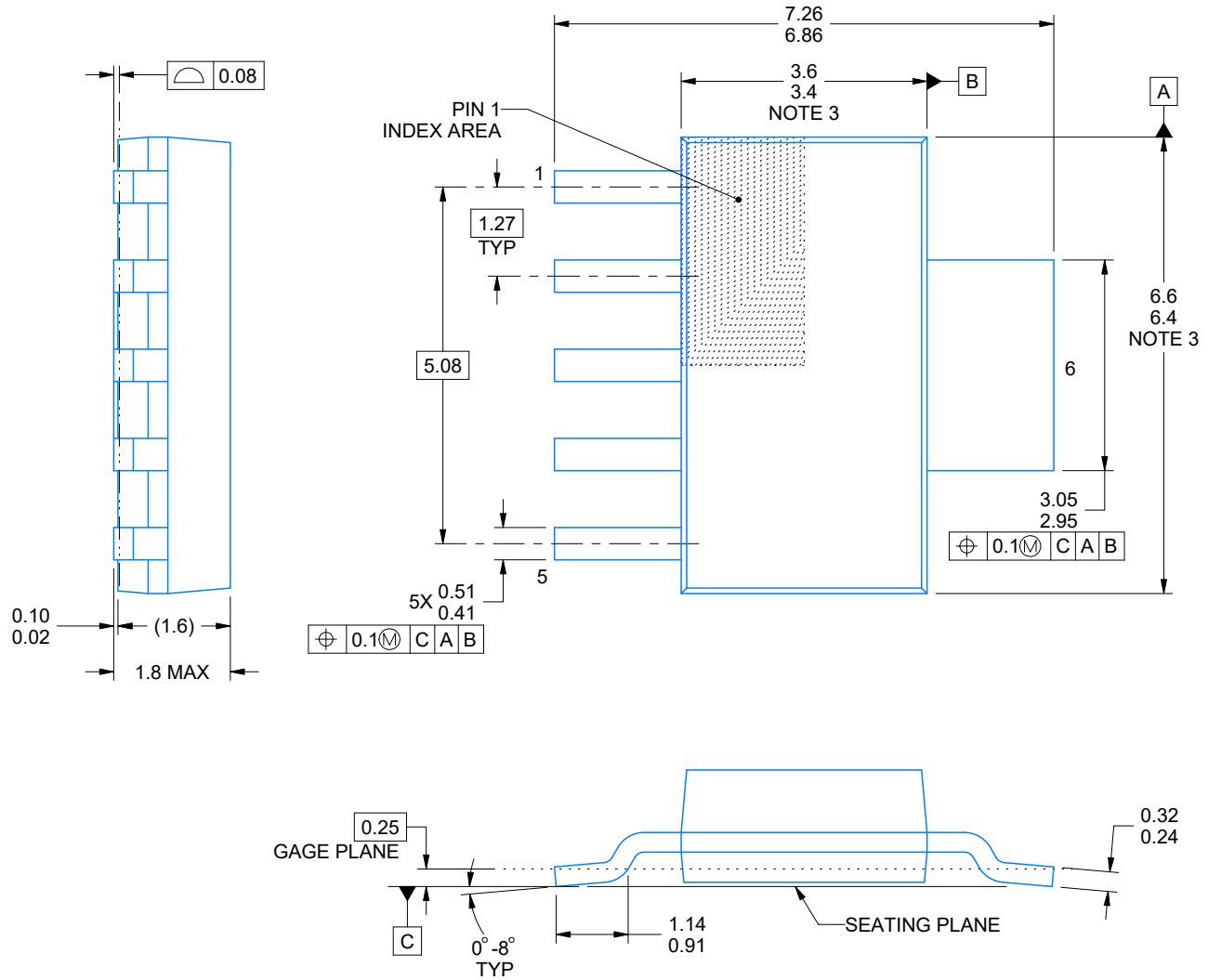
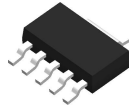


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214845/C 11/2021

NOTES:

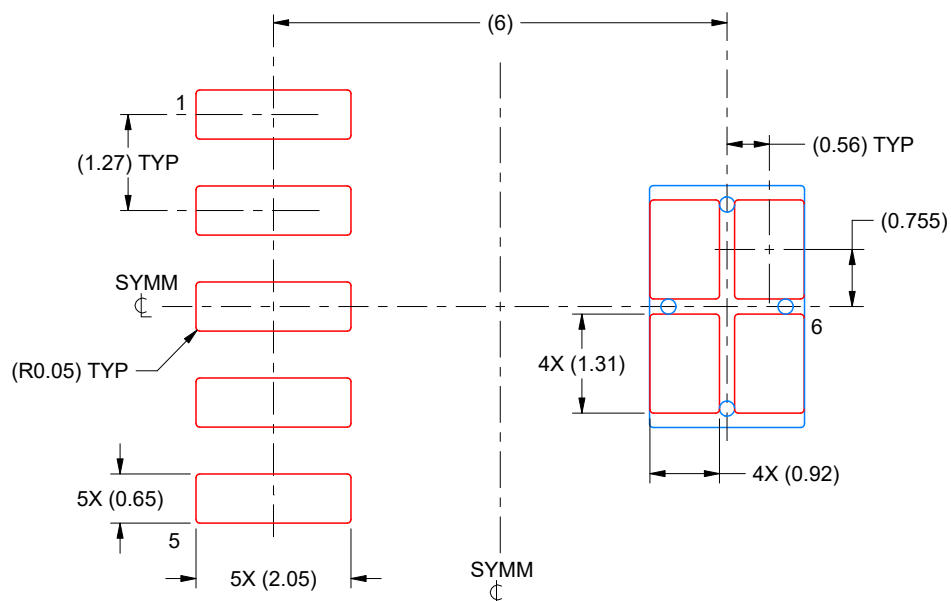
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE STENCIL DESIGN

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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