SNx4AHC126 Quadruple Bus Buffer Gates with 3-State Outputs

1 Features

- Operating range 2V to 5.5V V_{CC}
- Low delay, 3.8 ns (typical with 5-V supply)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Drive indicator LEDs
- Drive transmission lines with logic
- Enable or disable a digital signal

3 Description

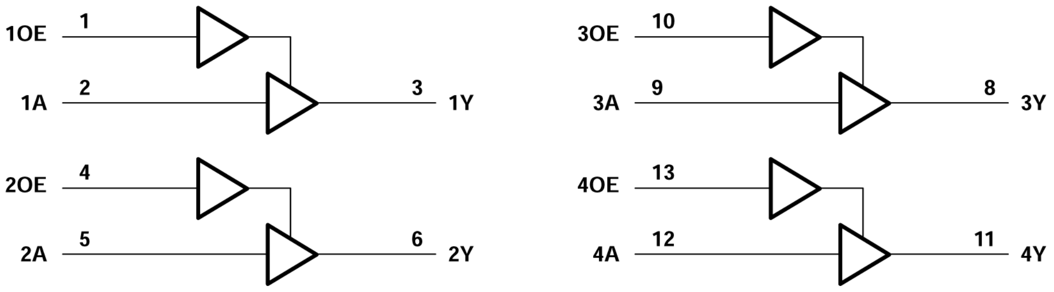
The SNx4AHC126 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs.

For the high-impedance state during power up or power down, OE can be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the drive.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (3)
SNx4AHC126	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

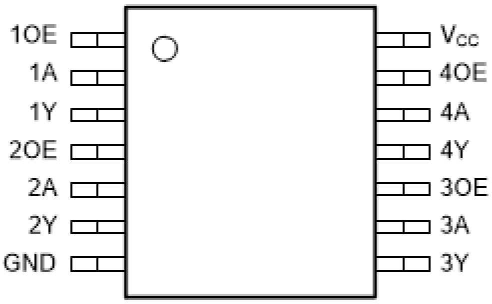


Figure 4-1. PW Package, 14-Pin (Top View)

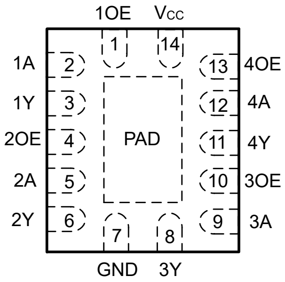


Figure 4-2. BQA Package, WQFN 14-Pin (Transparent Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1OE	1	I	Channel 1, output enable
1A	2	I	Channel 1, A input
1Y	3	O	Channel 1, Y output
2OE	4	I	Channel 2, output enable
2A	5	I	Channel 2, A input
2Y	6	O	Channel 2, Y output
GND	7	G	Ground
3Y	8	O	Channel 3, Y output
3A	9	I	Channel 3, A input
3OE	10	I	Channel 3, OE input
4Y	11	O	Channel 4, Y output
4A	12	I	Channel 4, A input
4OE	13	I	Channel 4, OE input
V_{CC}	14	P	Positive supply
Thermal Pad[2]		—	Thermal pad; connect to GND or leave floating

(1) I = input, O = output, P = power, G = ground
(2) BQA package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I (2)	Input voltage range		–0.5	7	V
V_O (2)	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I (1)	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH} (2)	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL} (2)	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature	SN74AHC126	–40	85	°C
		SN54AHC126	–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Recommended current values provided to maintain appropriate output state as per the relevant output voltage specification (V_{OL} for I_{OL}, V_{OH} for I_{OH}). See *Electrical Characteristics* table for details.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHC126						UNIT
		D	DB	DGV	N	NS	PW	
		14 PINS						
$R_{θJA}$	Junction-to-ambient thermal resistance	124.6					147.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	79.7					77.4	
$R_{θJB}$	Junction-to-board thermal resistance	81.2					90.9	
$Ψ_{JT}$	Junction-to-top characterization parameter	39.3					27.2	
$Ψ_{JB}$	Junction-to-board characterization parameter	80.8					90.2	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25 °C			–40 to +85 °C		–55 to +125 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44		0.5	
	I_{OL} = 8 mA	4.5 V			0.36		0.44		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1(1)	µA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.25				±2.5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4				40	µA
C_i	V_I = V_{CC} or GND	5 V		4	10		10			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40 to +85 °C		–55 to +125 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5.6(1)	8(1)	1	9.5	1(1)	9.5(1)	ns
t_{PHL}					5.6(1)	8(1)	1	9.5	1(1)	9.5(1)	
t_{PZH}	OE	Y	C_L = 15 pF		5.4(1)	8(1)	1	9.5	1(1)	9.5(1)	ns
t_{PZL}					5.4(1)	8(1)	1	9.5	1(1)	9.5(1)	
t_{PHZ}	OE	Y	C_L = 15 pF		7(1)	9.7(1)	1	11.5	1(1)	11.5(1)	ns
t_{PLZ}					7(1)	9.7(1)	1	11.5	1(1)	11.5(1)	
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	1	13	ns
t_{PHL}					8.1	11.5	1	13	1	13	
t_{PZH}	OE	Y	C_L = 50 pF		7.9	11.5	1	13	1	13	ns
t_{PZL}					7.9	11.5	1	13	1	13	
t_{PHZ}	OE	Y	C_L = 50 pF		9.5	13.2	1	15	1	15	ns
t_{PLZ}					9.5	13.2	1	15	1	15	
$t_{sk(o)}$			C_L = 50 pF			1.5(2)		1.5			ns

(1) (2)

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40 to +85 °C		–55 to +125 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.8(1)	5.5(1)	1	6.5	1(1)	6.5(1)	ns
t_{PHL}					3.8(1)	5.5(1)	1	6.5	1(1)	6.5(1)	
t_{PZH}	OE	Y	C_L = 15 pF		3.6(1)	5.1(1)	1	6	1(1)	6(1)	ns
t_{PZL}					3.6(1)	5.1(1)	1	6	1(1)	6(1)	
t_{PHZ}	OE	Y	C_L = 15 pF		4.6(1)	6.8(1)	1	8	1(1)	8(1)	ns
t_{PLZ}					4.6(1)	6.8(1)	1	8	1(1)	8(1)	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	1	8.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	1	8	ns
t_{PZL}					5.1	7.1	1	8	1	8	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	1	10	ns
t_{PLZ}					6.1	8.8	1	10	1	10	
$t_{sk(o)}$			C_L = 50 pF			1(2)		1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.9	–0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

5.10 Typical Characteristics

T_A = 25°C (unless otherwise noted)

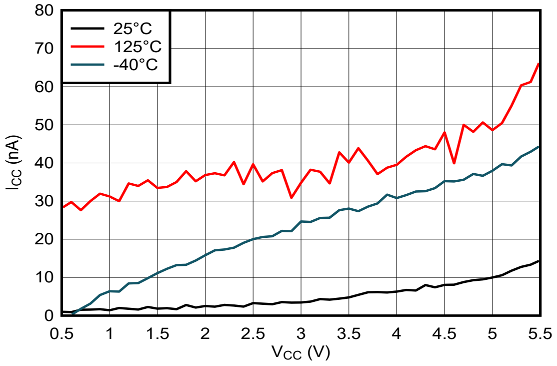


Figure 5-1. Supply Current Across Supply Voltage

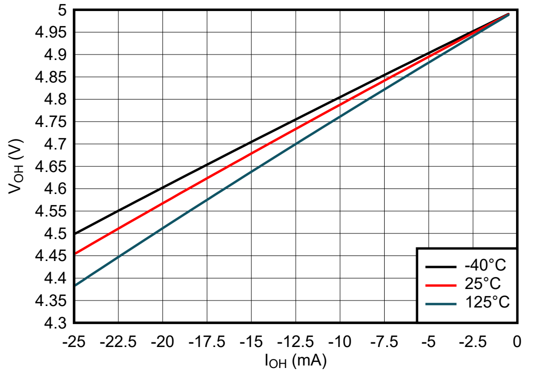


Figure 5-2. Output Voltage vs Current in HIGH State; 5-V Supply

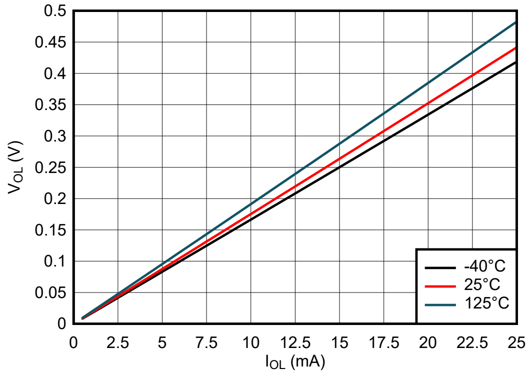


Figure 5-3. Output Voltage vs Current in LOW State; 5-V Supply

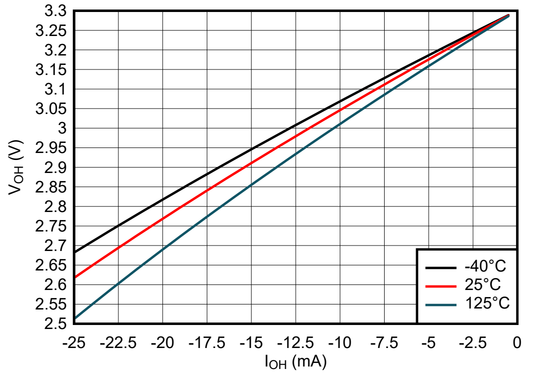


Figure 5-4. Output Voltage vs Current in HIGH State; 3.3-V Supply

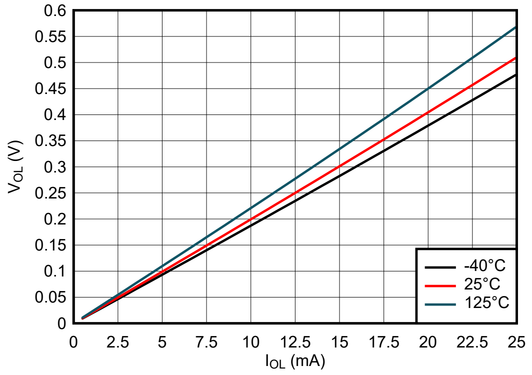


Figure 5-5. Output Voltage vs Current in LOW State; 3.3-V Supply

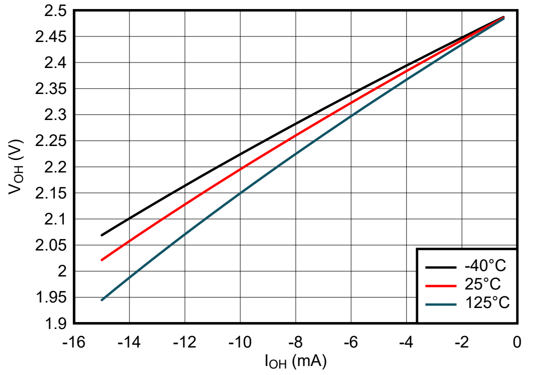


Figure 5-6. Output Voltage vs Current in HIGH State; 2.5-V Supply

5.10 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

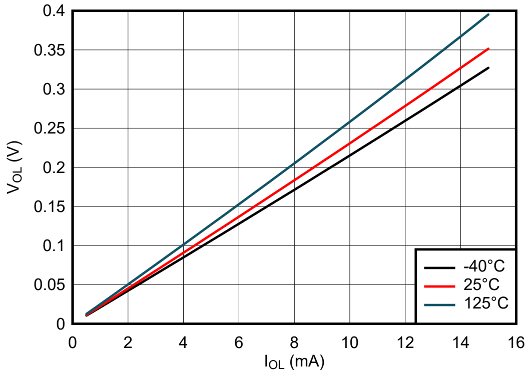


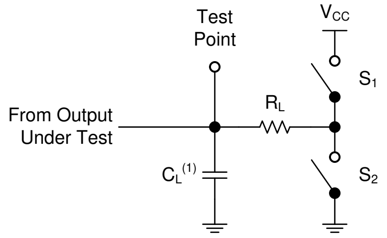
Figure 5-7. Output Voltage vs Current in LOW State; 2.5-V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5 ns.

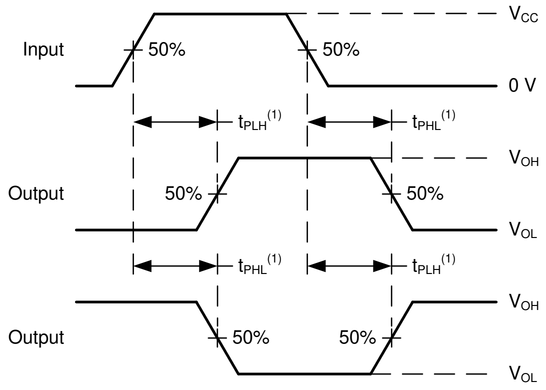
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH}, t_{PHL}	OPEN	OPEN	—	15pF, 50pF	—	ALL
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1 kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1 kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1 kΩ	15pF, 50pF	0.3V	> 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1 kΩ	15pF, 50pF	0.3V	> 2.5V



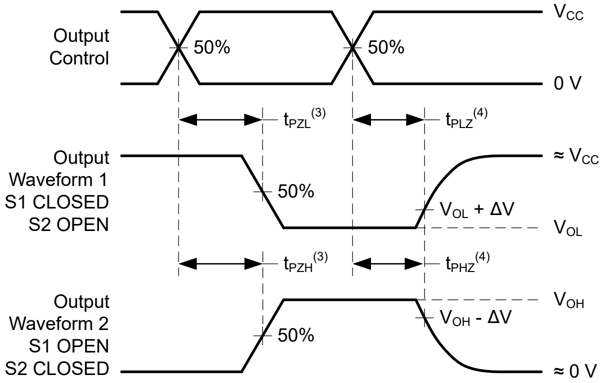
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

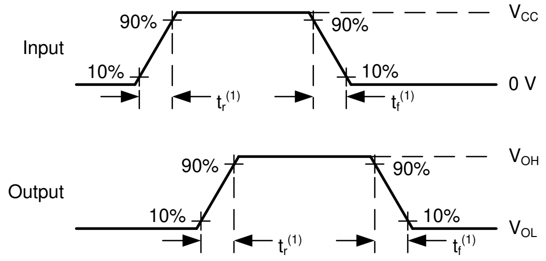
Figure 6-2. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

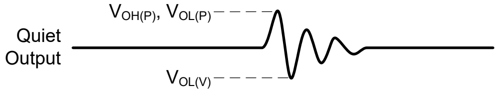
(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times



Noise values measured with all other outputs simultaneously switching.

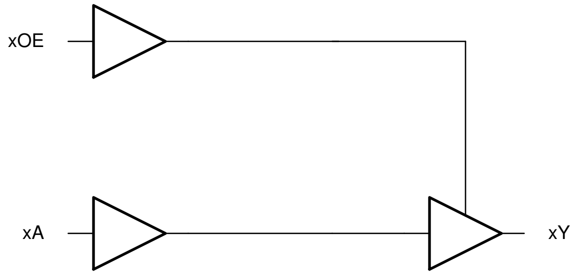
Figure 6-5. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function Y = A in positive logic.

7.2 Functional Block Diagram



One of four channels

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

As Figure 7-1 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION
Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

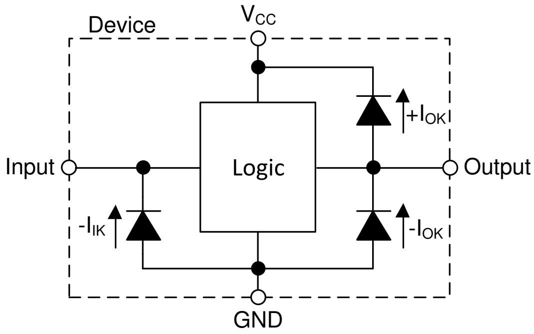


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
OE	A	Y
L	X	Z
H	L	L
H	H	H

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (August 2023) to Revision N (February 2024) **Page**

- Added thermal values for D package: RθJA = 124.6, RθJC(top) = 79.7, RθJB = 81.2, ΨJT = 39.3, ΨJB = 80.8, RθJC(bot) = N/A, all values in °C/W 5

Changes from Revision L (July 2003) to Revision M (August 2023) **Page**

- Changed the numbering format for tables, figures, and cross-references throughout the document................ 1
- Added the *BQA* package to the data sheet... 1
- Deleted the *J, W, D, DB, DGV, N, NS, and FK* packages from the data sheet.. 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686201Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201Q2A SNJ54AHC126FK	Samples
5962-9686201QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QDA SNJ54AHC126W	Samples
SN74AHC126BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC126	Samples
SN74AHC126DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC126N	Samples
SN74AHC126NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SNJ54AHC126FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201Q2A SNJ54AHC126FK	Samples
SNJ54AHC126W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QDA SNJ54AHC126W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC126, SN74AHC126 :

- Catalog : SN74AHC126

- Automotive : SN74AHC126-Q1, SN74AHC126-Q1

- Military : SN54AHC126

NOTE: Qualified Version Definitions:

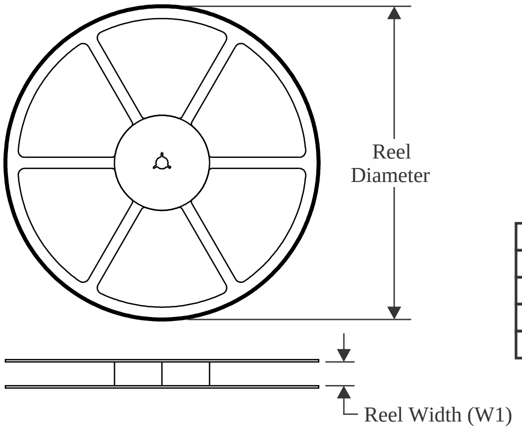
- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

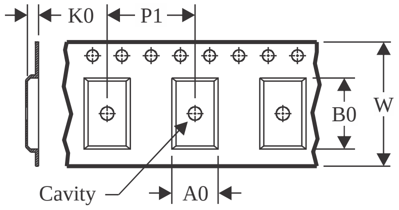
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

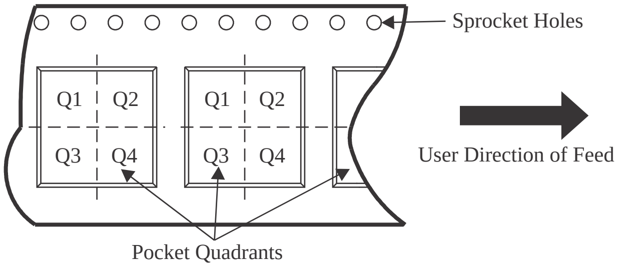


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

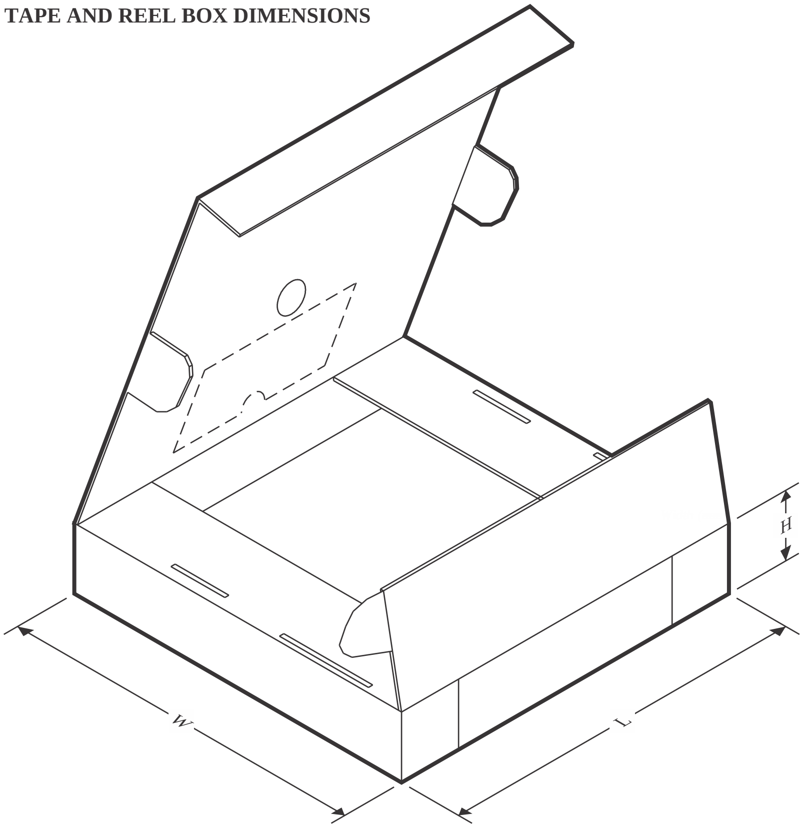
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC126BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC126NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

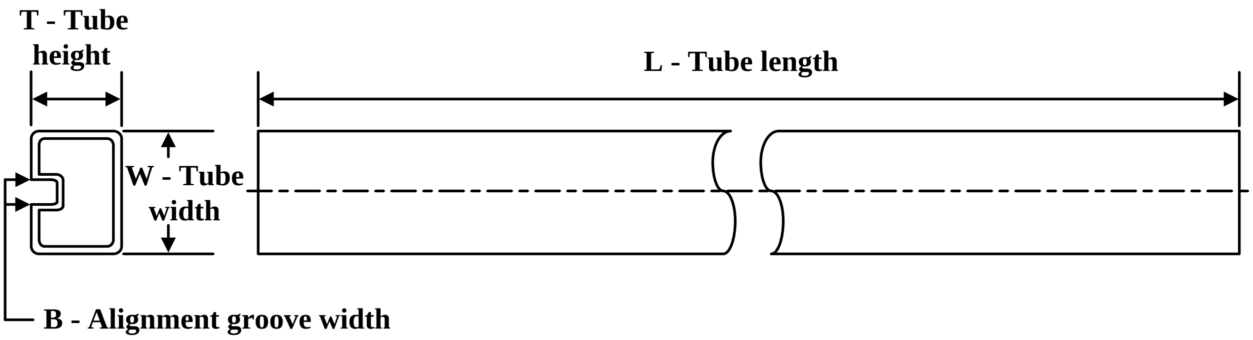
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC126BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC126DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC126DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC126NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC126PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC126PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9686201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686201QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC126FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC126W	W	CFP	14	25	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

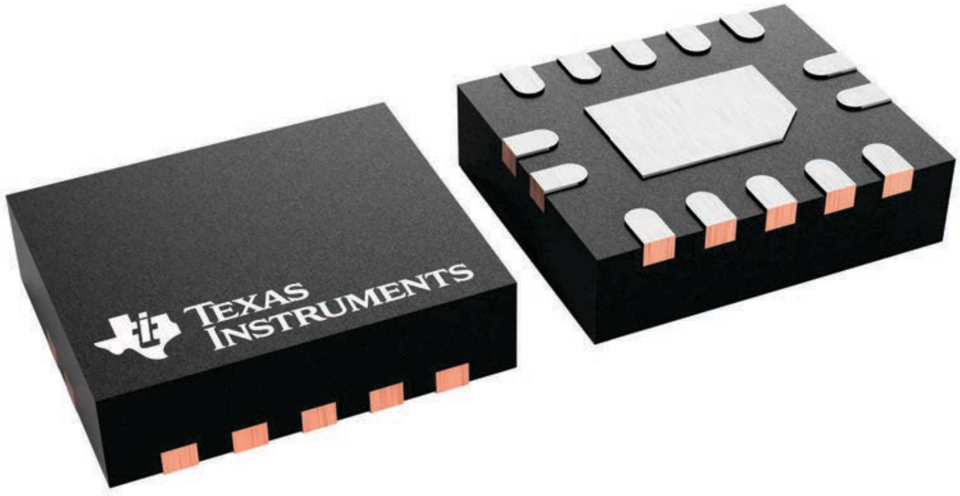
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

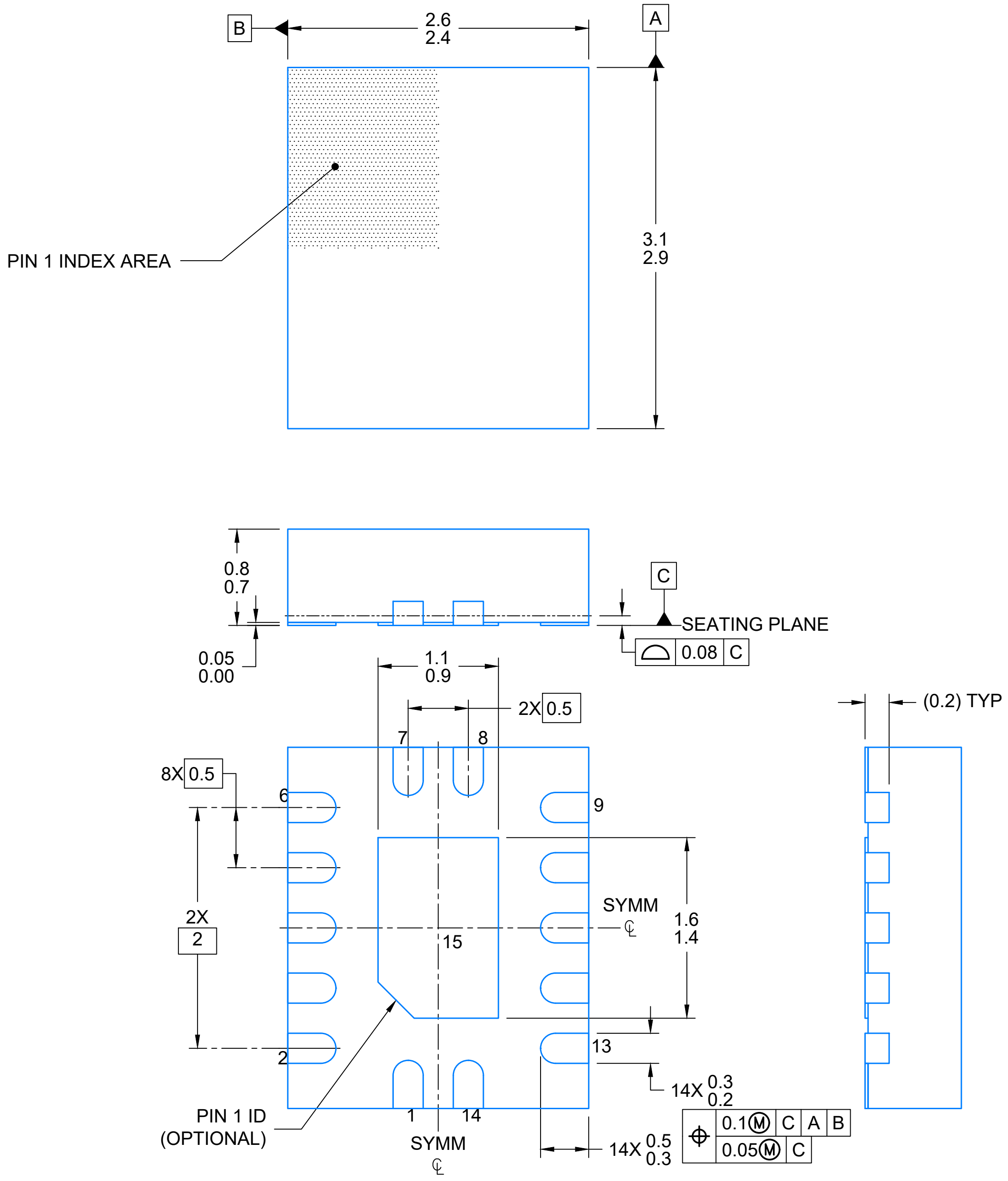


4227145/A

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

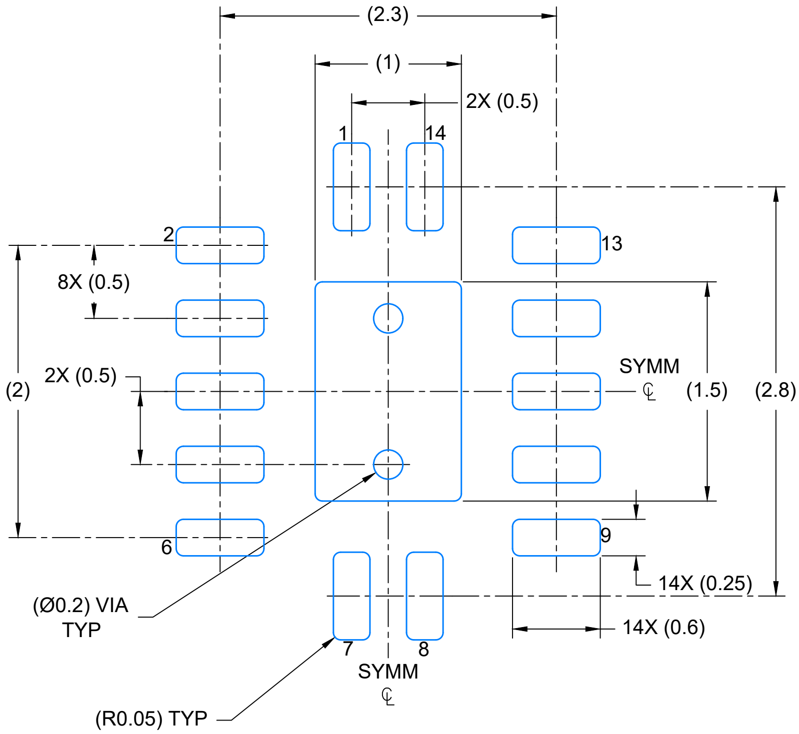


4224636/A 11/2018

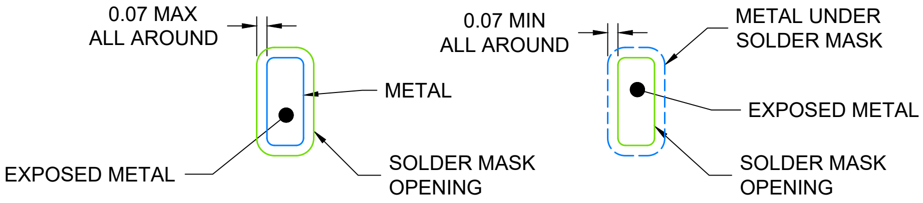
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



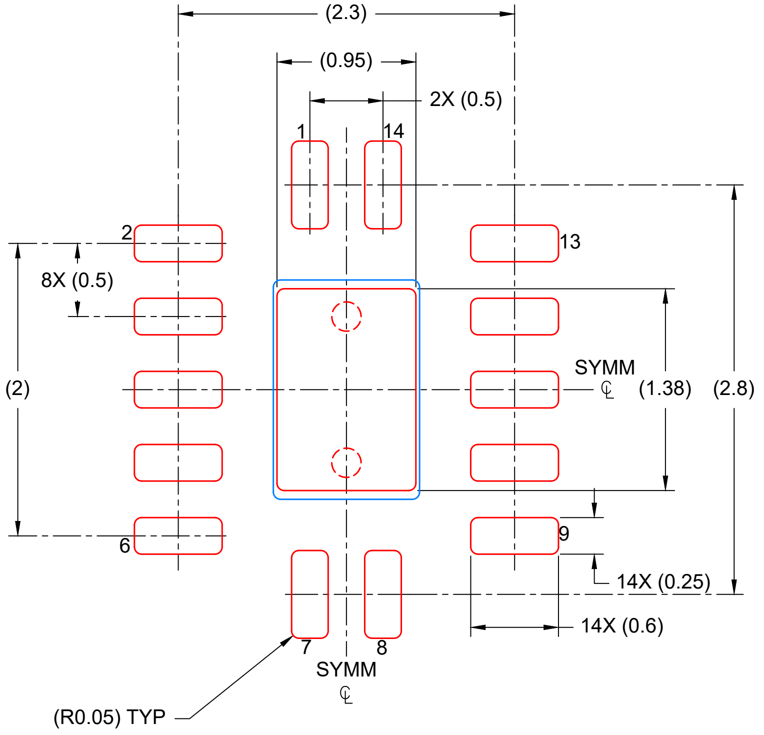
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

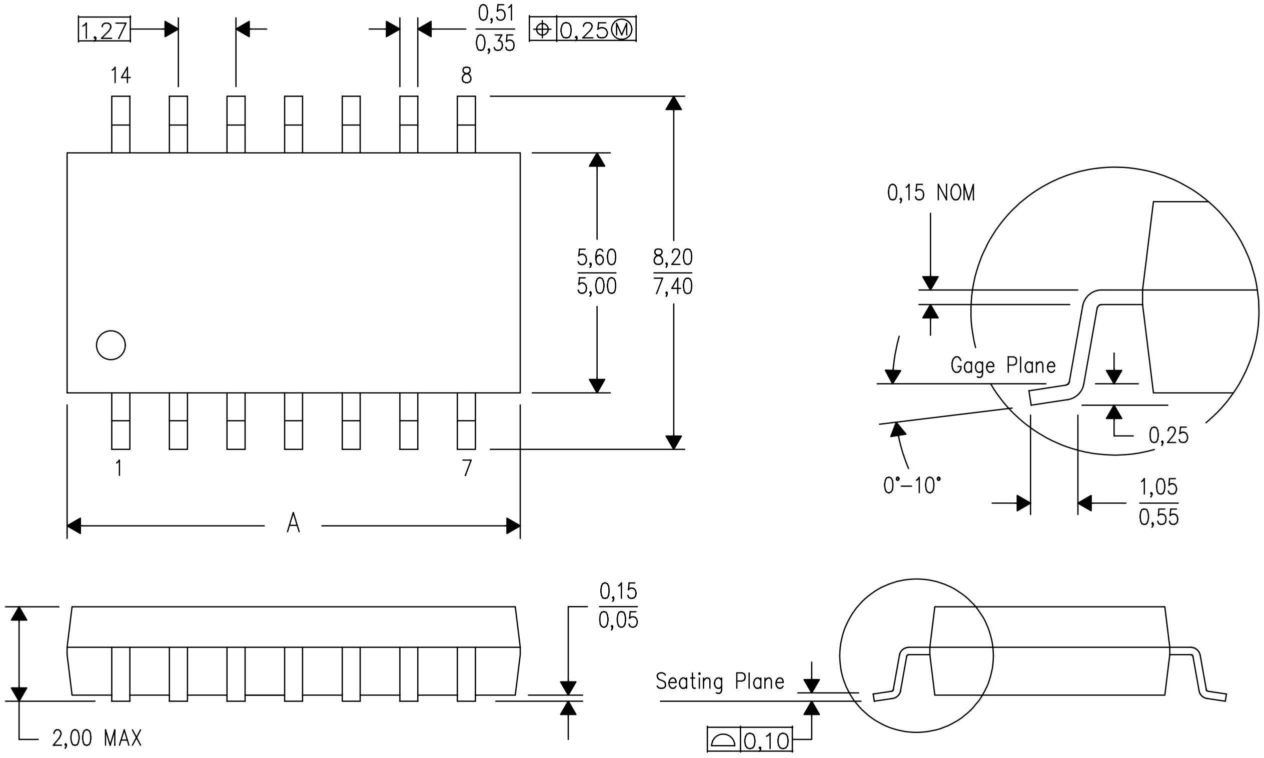
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

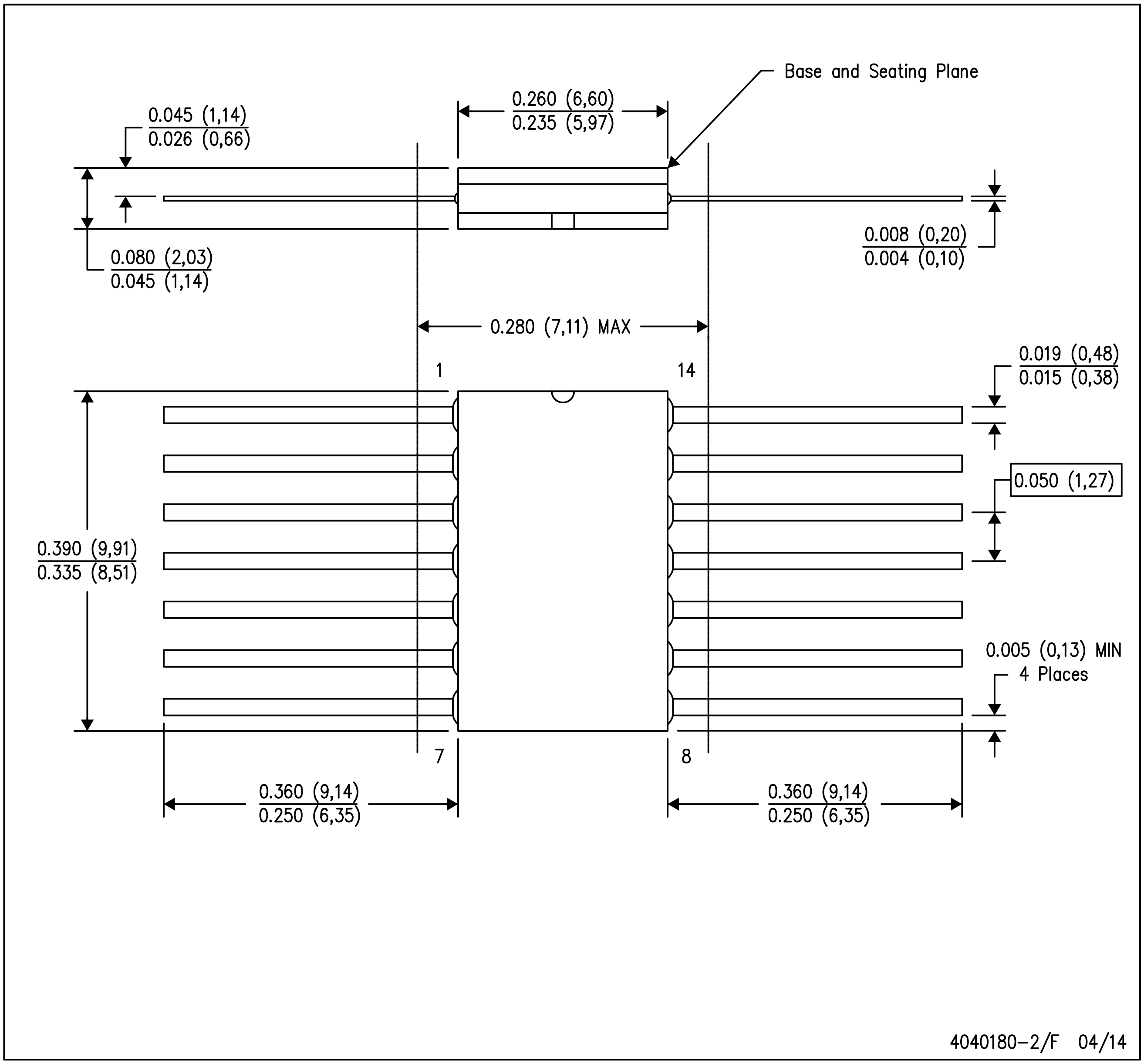


PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

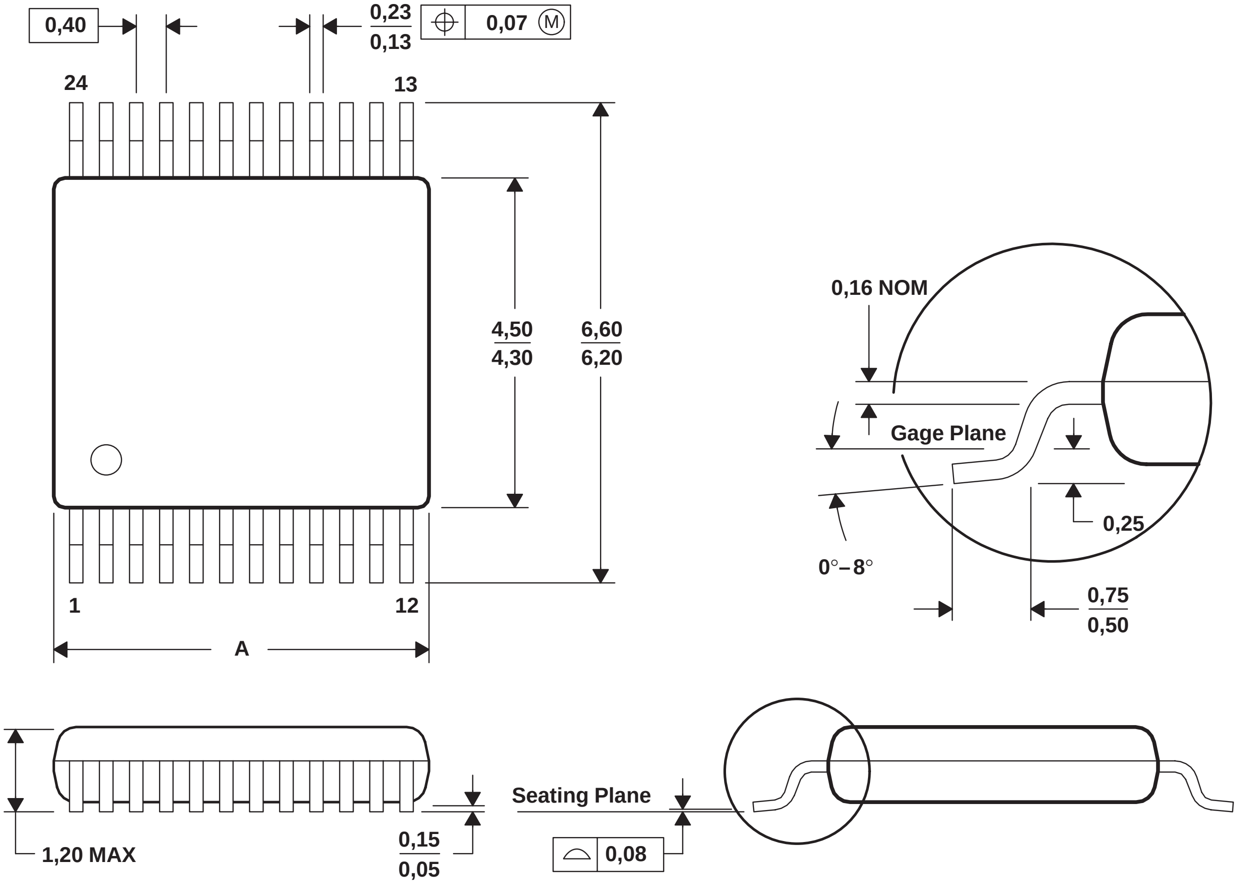
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

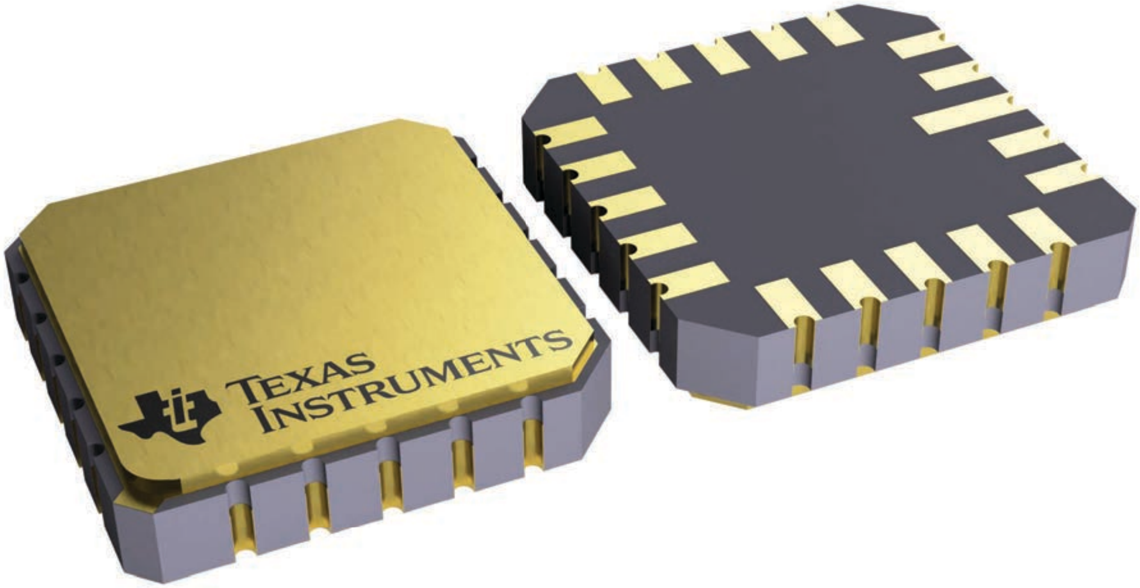
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

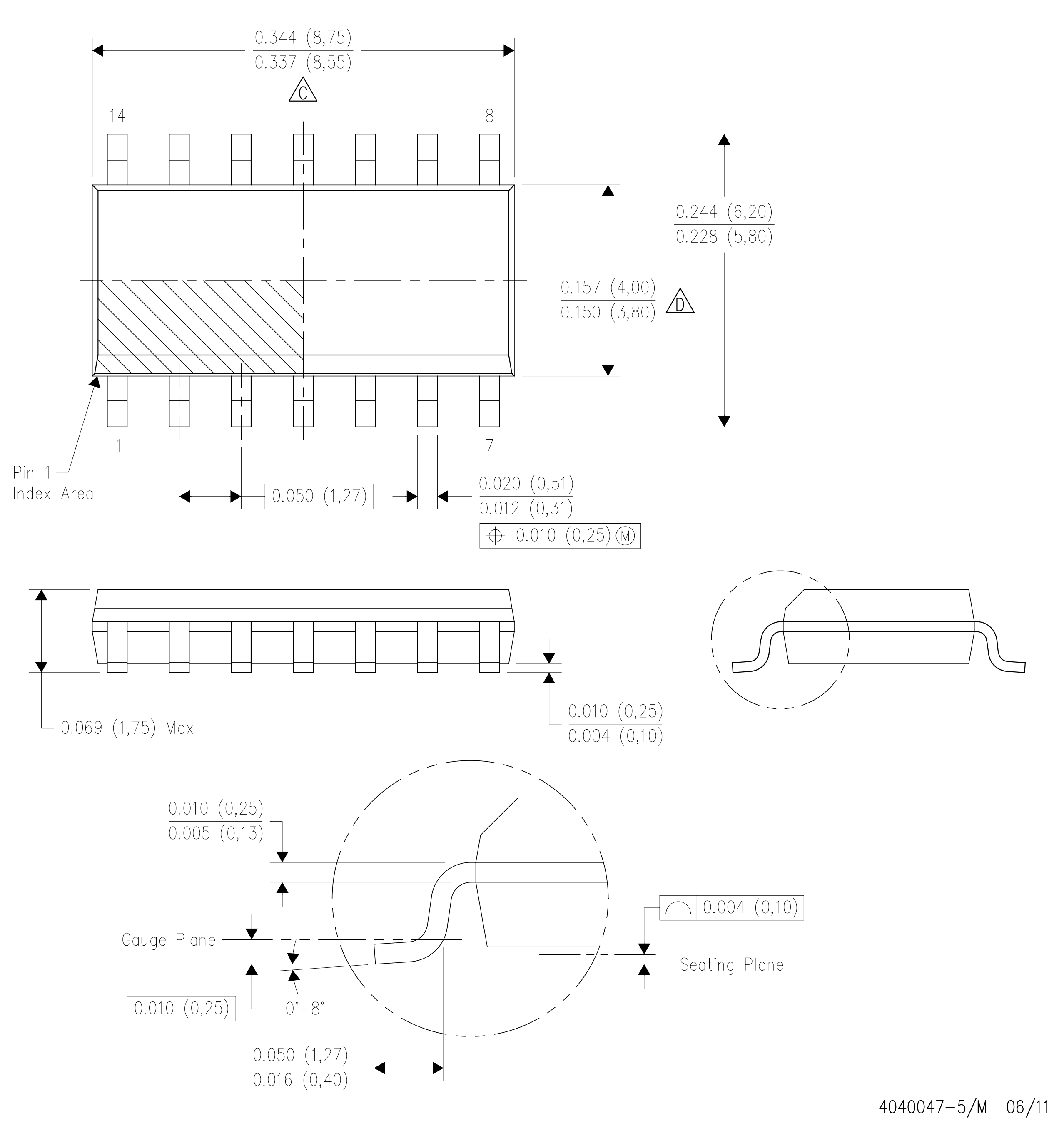
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



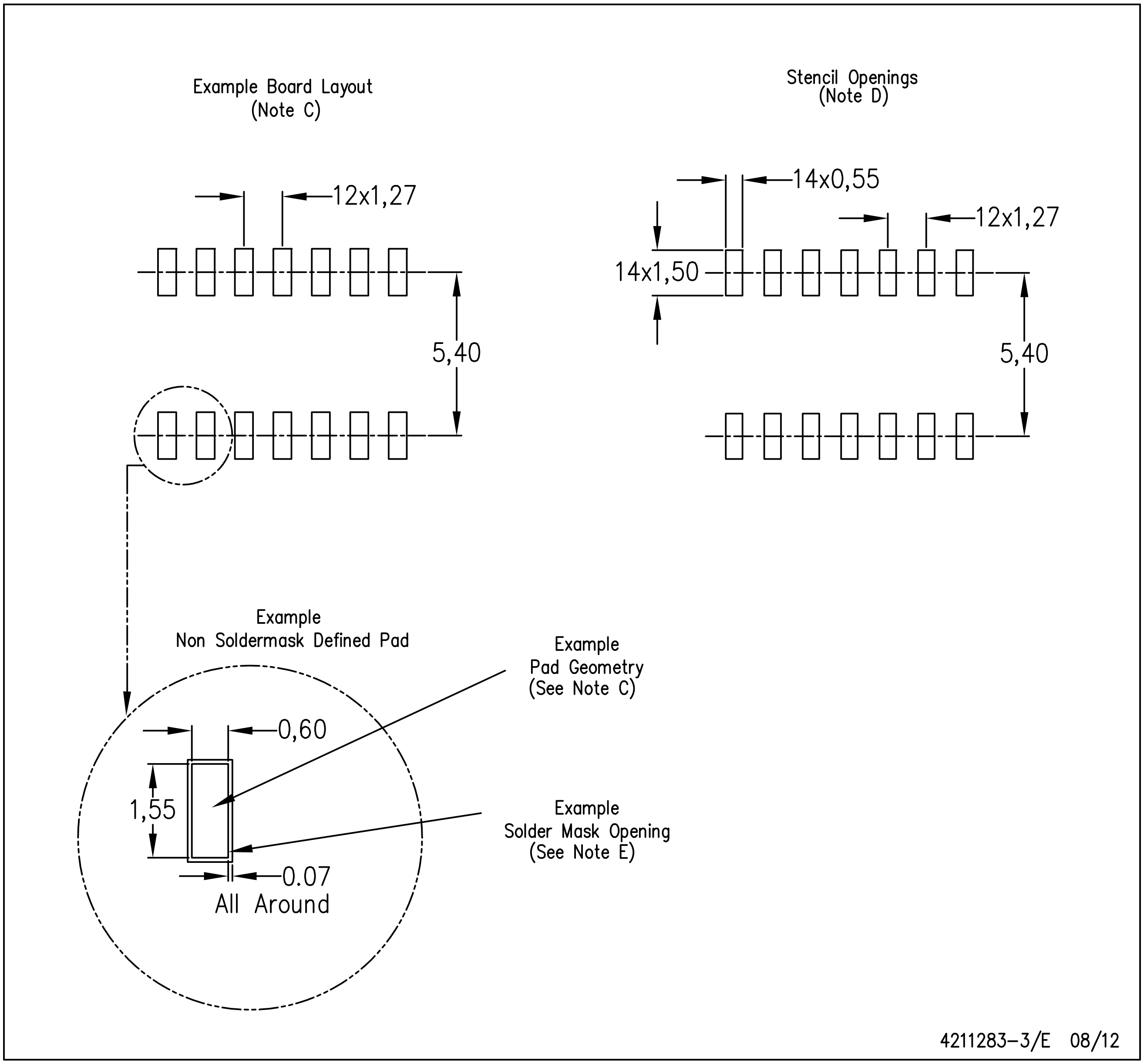
4229370\A\

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



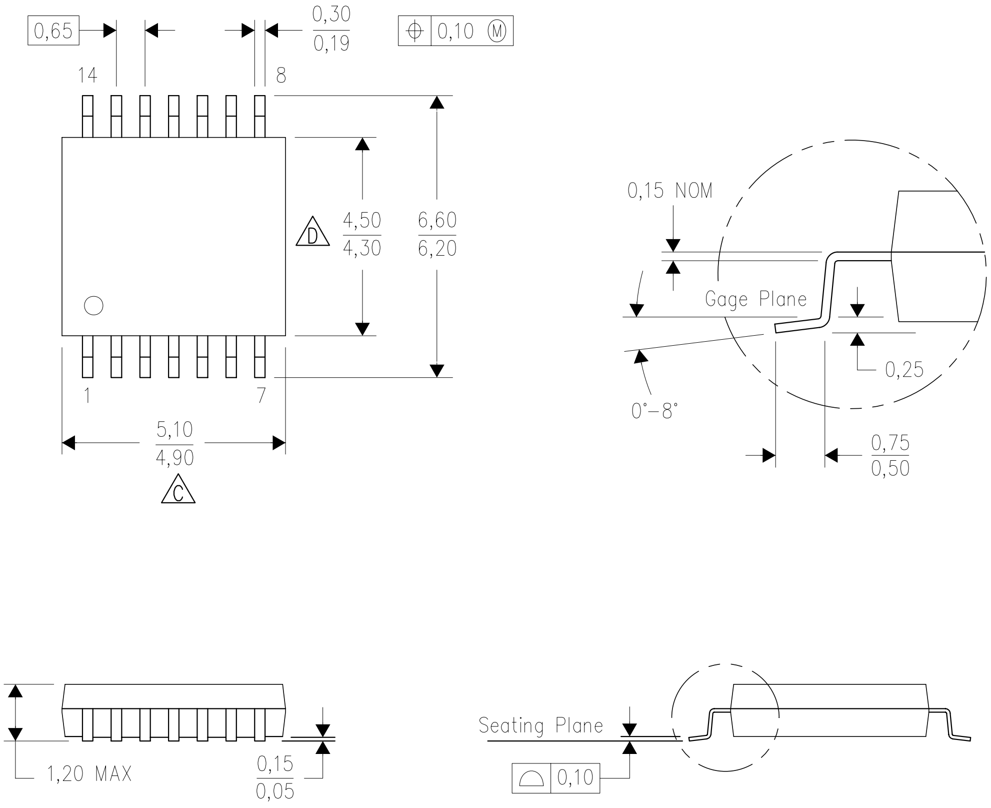
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

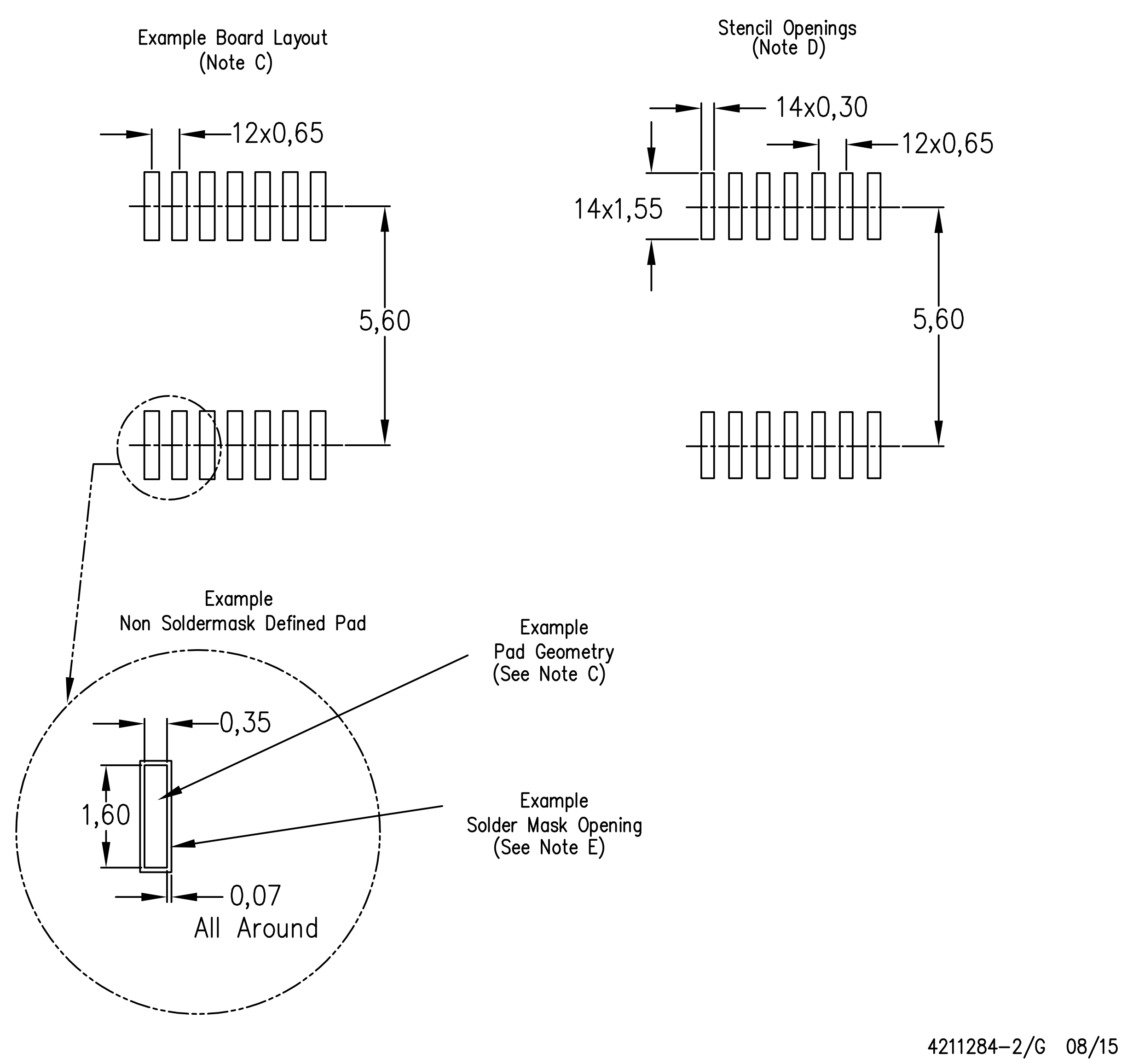
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

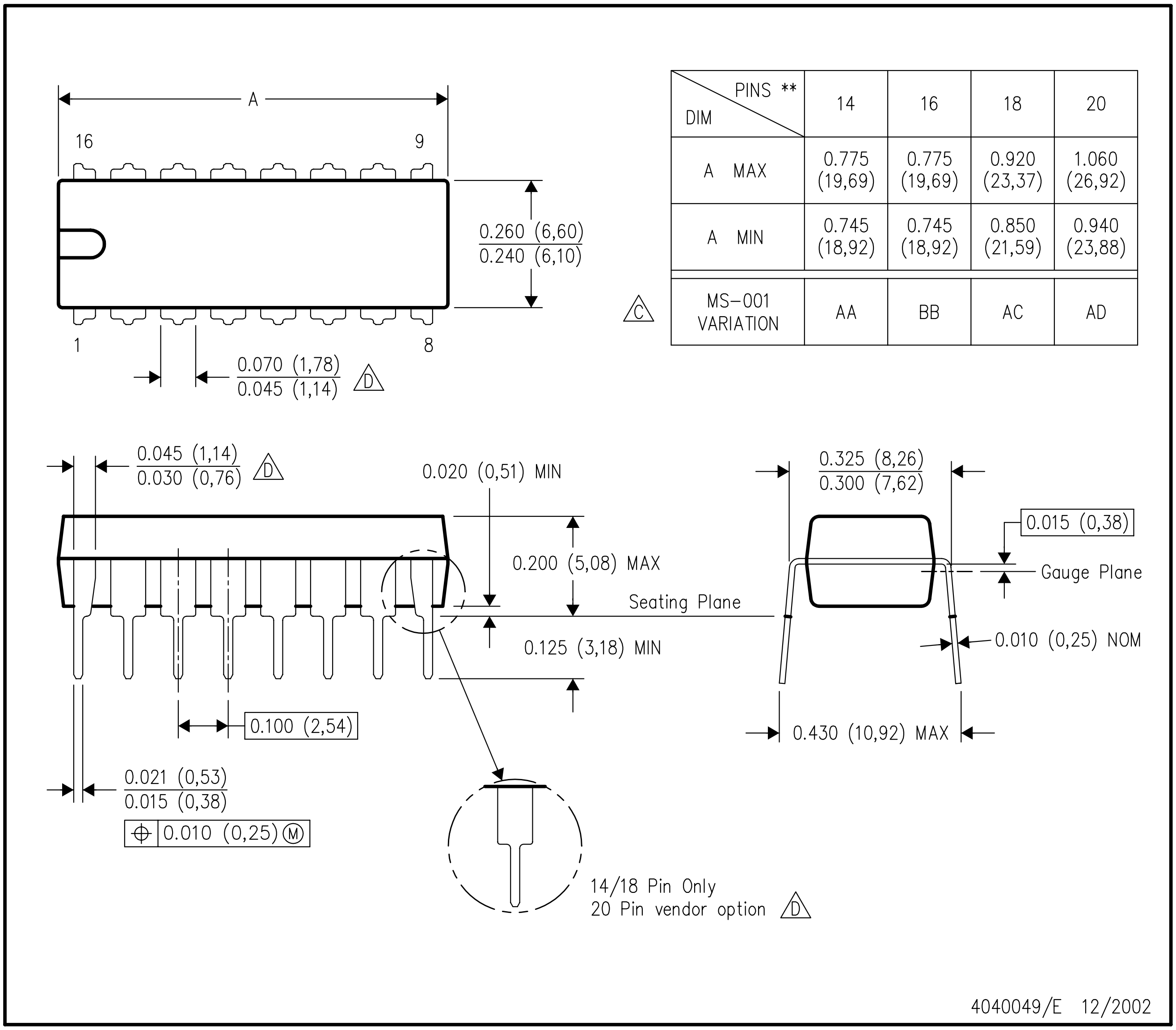
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

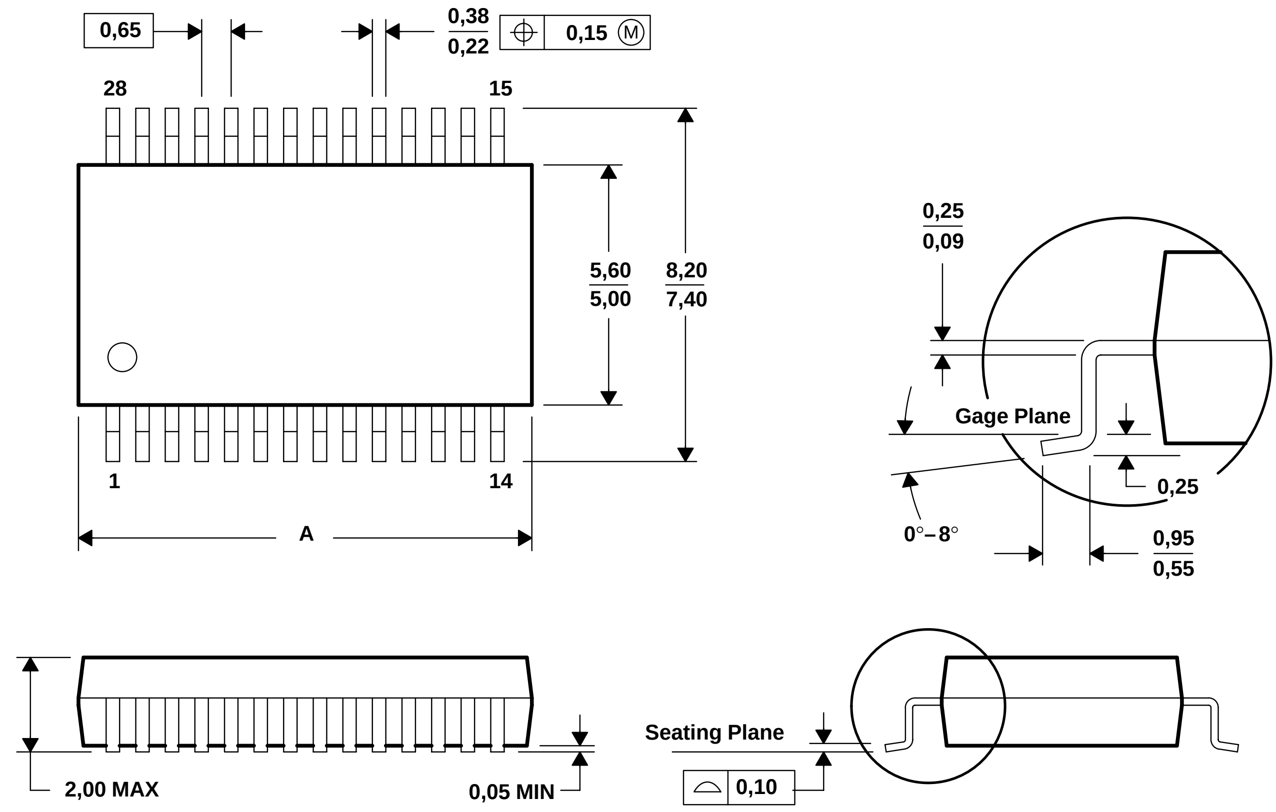
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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