

TS5A22364-Q1 0.65-Ω Dual SPDT Analog Switch with Negative Signaling Capability

1 Features

- Qualified for automotive applications
- Specified Break-Before-Make (BBM) switching
- Negative signal swing capability: Maximum swing From -2.75 V to 2.75 V ($V_{CC} = 2.75\text{ V}$)
- Internal shunt switch prevents audible click-and-pop when switching between two sources
- Low On-state resistance ($0.65\ \Omega$ typical)
- Low charge injection
- Excellent channel to channel On-state resistance matching
- 2.3-V to 5.5-V power supply (V_{CC})
- Latch-up performance meets 100 mA per AEC Q100-004
- ESD performance
 - 2500-V Human-Body Model tested per AEC Q100-002
 - 1500-V Charged-Device Model tested per AEC Q100-011

2 Applications

- Automotive infotainment
- Audio routing
- Industrial automation
- Medical imaging

3 Description

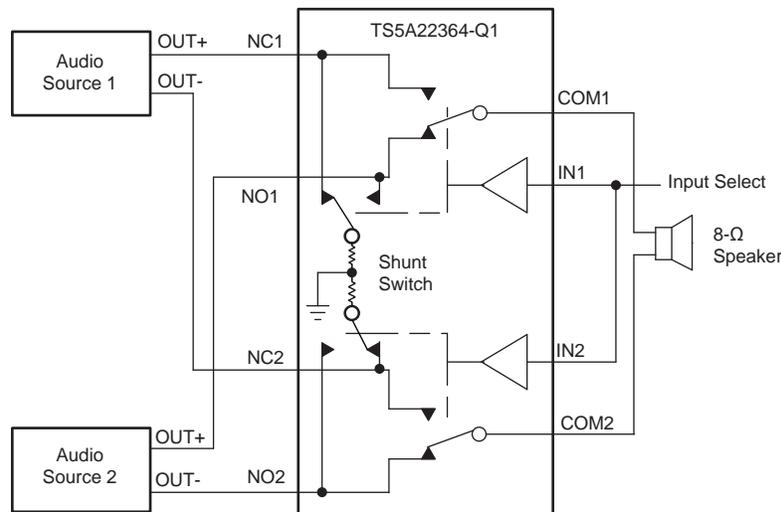
The TS5A22364-Q1 is a 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3 V to 5.5 V supply. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. Additionally, the TS5A22364-Q1 includes an internal shunt switch, which automatically discharges any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces the audible click-and-pop noise when switching between two sources. The break-before-make feature prevents signal distortion during the transfer of a signal from one path to another. Low On-state resistance, excellent channel-to-channel On-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|--------------|------------|-------------------|
| TS5A22364-Q1 | VSSOP (10) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Copyright © 2016, Texas Instruments Incorporated



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 Features | 1 | 8.2 Functional Block Diagram | 16 |
| 2 Applications | 1 | 8.3 Feature Description | 16 |
| 3 Description | 1 | 8.4 Device Functional Modes | 16 |
| 4 Revision History | 2 | 9 Application and Implementation | 17 |
| 5 Pin Configuration and Functions | 3 | 9.1 Application Information | 17 |
| 6 Specifications | 4 | 9.2 Typical Application | 17 |
| 6.1 Absolute Maximum Ratings | 4 | 10 Power Supply Recommendations | 19 |
| 6.2 ESD Ratings | 4 | 11 Layout | 20 |
| 6.3 Recommended Operating Conditions | 4 | 11.1 Layout Guidelines | 20 |
| 6.4 Thermal Information | 5 | 11.2 Layout Example | 20 |
| 6.5 Electrical Characteristics—2.5-V Supply | 5 | 12 Device and Documentation Support | 21 |
| 6.6 Electrical Characteristics—3.3-V Supply | 6 | 12.1 Receiving Notification of Documentation Updates | 21 |
| 6.7 Electrical Characteristics—5-V Supply | 7 | 12.2 Community Resources | 21 |
| 6.8 Typical Characteristics | 9 | 12.3 Trademarks | 21 |
| 7 Parameter Measurement Information | 12 | 12.4 Electrostatic Discharge Caution | 21 |
| 8 Detailed Description | 16 | 13 Mechanical, Packaging, and Orderable Information | 21 |
| 8.1 Overview | 16 | | |

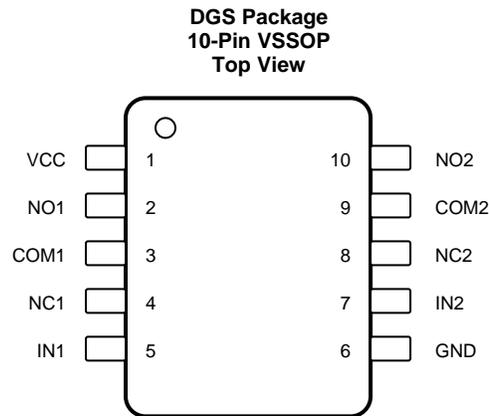
4 Revision History

Changes from Original (October 2014) to Revision A

Page

- | | |
|---|----------|
| • Changed device status from <i>Product Preview</i> to <i>Production Data</i> | 1 |
|---|----------|

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|------|-----|--|
| NO. | NAME | | |
| 1 | VCC | I | Supply power |
| 2 | NO1 | I/O | Normally open (NO) signal path, switch 1 |
| 3 | COM1 | I/O | Common signal path, switch 1 |
| 4 | NC1 | I/O | Normally closed (NC) signal path, switch 1 |
| 5 | IN1 | I | Digital control pin to connect COM1 to NO1, switch 1 |
| 6 | GND | — | Ground |
| 7 | IN2 | I | Digital control pin to connect COM2 to NO2, switch 2 |
| 8 | NC2 | I/O | Normally closed (NC) signal path, switch 2 |
| 9 | COM2 | I/O | Common signal path, switch 2 |
| 10 | NO2 | I/O | Normally open (NO) signal path, switch 2 |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

| | | MIN | MAX | UNIT | |
|-----------------------|--|---|----------------|------|----|
| V_{CC} | Supply voltage ⁽³⁾ | -0.5 | 6 | V | |
| V_{NC} | Analog voltage on NC1-NC2 pin ^{(3) (4) (5)} | $V_{CC} - 6$ | $V_{CC} + 0.5$ | V | |
| V_{NO} | Analog voltage on NO1-NO2 pin ^{(3) (4) (5)} | | | | |
| V_{COM} | Analog voltage on COM1-COM2 pin ^{(3) (4) (5)} | | | | |
| $I_{I/OK}$ | Analog port diode input clamp current | $V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NC}, V_{NO}, V_{COM} > V_{CC}$ | -50 | 50 | mA |
| I_{NC} | On-state switch continuous current | $V_{NC}, V_{NO}, V_{COM} = 0$ to V_{CC} | -150 | 150 | mA |
| I_{NO} I_{COM} | On-state switch peak current ⁽⁶⁾ | | -300 | 300 | |
| I_{RSH} | Off-state switch shunt resistor current | | -20 | 20 | mA |
| V_{IN} | Digital input voltage | | -0.5 | 6.5 | V |
| I_{IK} | Digital input clamp current ^{(3) (4)} | $V_{IN} < 0$ | -50 | 50 | mA |
| I_{CC} I_{GND} | Continuous current through V_{CC} or GND | | -100 | 100 | mA |
| T_{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration <10% duty cycle.

6.2 ESD Ratings

| | | MIN | MAX | UNIT | |
|-----------|-------------------------|---|-------|------|---|
| V_{ESD} | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | -2500 | 2500 | V |
| | | Charged device model (CDM), per AEC Q100-011 | -1500 | 1500 | |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------|---------------------|----------------|----------|------|
| V_{CC} | Supply voltage | 2.3 | 5.5 | V |
| V_{NC} | Signal path voltage | $V_{CC} - 5.5$ | V_{CC} | V |
| V_{NO} | | | | |
| V_{COM} | | | | |
| V_{IN} | Digital control | GND | V_{CC} | V |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ (2) | | TS5A22364-Q1 | | UNIT |
|-----------------------------------|--|--------------|--|------|
| | | DGS (VSSOP) | | |
| | | 10 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 163.3 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 56.4 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 83.1 | | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 6.8 | | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 81.8 | | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics—2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to +125°C (unless otherwise noted) ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|--|-------------------------|-------------------------|-----------------------|-------|-----------------|------|
| ANALOG SWITCH | | | | | | | | |
| Analog signal | V _{COM} V _{NO} V _{NC} | | | | V _{CC} – 5.5 | | V _{CC} | V |
| On-state resistance | R _{on} | V _{NC} or V _{NO} = V _{CC} , 1.5 V, V _{CC} = 5.5 V I _{COM} = –100 mA | 25°C –40°C to +125°C | 2.7 V | | 0.65 | 0.94 1.3 | Ω |
| On-state resistance match between channels | ΔR _{on} | V _{NC} or V _{NO} = 1.5 V, I _{COM} = –100 mA | 25°C –40°C to +125°C | 2.7 V | | 0.023 | 0.11 0.15 | Ω |
| On-state resistance flatness | R _{on(flat)} | V _{NC} or V _{NO} = V _{CC} , 1.5 V, V _{CC} = 5.5 V I _{COM} = –100 mA | 25°C –40°C to +125°C | 2.7 V | | 0.18 | 0.46 0.56 | Ω |
| Shunt switch resistance | R _{SH} | I _{NO} or I _{NC} = 10 mA | –40°C to +125°C | 2.7 V | | 25 | 55 | Ω |
| On-state leakage current | I _{COM(ON)} | V _{NC} and V _{NO} = floating, V _{COM} = V _{CC} , V _{CC} = 5.5 V | 25°C –40°C to +125°C | 2.7 V | –200 | | 200 2500 | nA |
| DIGITAL CONTROL INPUTS (IN)⁽²⁾ | | | | | | | | |
| Input logic high | V _{IH} | | –40°C to +125°C | | 1.4 | | V _{CC} | V |
| Input logic low | V _{IL} | | –40°C to +125°C | | | | 0.4 | V |
| Input leakage current | I _{IH} , I _{IL} | V _{IN} = V _{CC} or 0 | 25°C –40°C to +125°C | 2.7 V | –250 | | 250 250 | nA |
| DYNAMIC | | | | | | | | |
| Turnon time | t _{ON} | V _{COM} = V _{CC} , R _L = 300 Ω | 25°C –40°C to +125°C | 2.5 V 2.3 V to 2.7 V | | 44 | 80 120 | ns |
| Turnoff time | t _{OFF} | V _{COM} = V _{CC} , R _L = 300 Ω | 25°C –40°C to +125°C | 2.5 V 2.3 V to 2.7 V | | 22 | 70 70 | ns |
| Break-before-make time | t _{BBM} | | 25°C | 2.5 V | 1 | 7 | | ns |
| Charge injection | Q _C | V _{GEN} = 0, R _{GEN} = 0, | 25°C | 2.5 V | | 215 | | pC |
| On-State NC, NO, COM capacitance | C _{COM(ON)} | V _{COM} = V _{CC} or GND, Switch ON, f = 10 MHz | 25°C | 2.5 V | | 370 | | pF |
| Digital input capacitance | C _I | V _{IN} = V _{CC} or GND | 25°C | 2.5 V | | 2.6 | | pF |
| Bandwidth | BW | R _L = 50 Ω, –3 dB | 25°C | 2.5 V | | 17 | | MHz |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, [SCBA004](#).

Electrical Characteristics—2.5-V Supply (continued)

 $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|-----------------|--|-----------------|-------|-----|------|---------------|
| Off-state isolation | O_{ISO} | $R_L = 50 \Omega$ $f = 100 \text{ kHz}$, See Figure 21 | 25°C | 2.5 V | | -66 | dB |
| Crosstalk | X_{TALK} | $R_L = 50 \Omega$ $f = 100 \text{ kHz}$, See Figure 22 | 25°C | 2.5 V | | -75 | dB |
| Total harmonic distortion | THD | $R_L = 600 \Omega$, $C_L = 35 \text{ pF}$ $f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 24 | 25°C | 2.5 V | | 0.01 | % |
| SUPPLY | | | | | | | |
| Positive supply current | I_{CC} | V_{COM} and $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} = \text{floating}$ | 25°C | 2.7 V | 0.2 | 1.1 | μA |
| | | | -40°C to +125°C | | | | |
| | | $V_{COM} = V_{CC} - 5.5 \text{ V}$, $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} = \text{floating}$ | -40°C to +125°C | 2.7 V | | 3.3 | μA |

6.6 Electrical Characteristics—3.3-V Supply

 $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|--|-------------------------|----------------|-------|----------|----------|
| ANALOG SWITCH | | | | | | | |
| Analog signal | V_{COM} V_{NO} V_{NC} | | | $V_{CC} - 5.5$ | | V_{CC} | V |
| On-state resistance | R_{on} | V_{NC} or $V_{NO} \leq V_{CC}$, 1.5 V, $V_{CC} - 5.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$ COM to NO or NC, See Figure 14 | 25°C -40°C to +125°C | 3 V | 0.61 | 0.87 | Ω |
| On-state resistance match between channels | ΔR_{on} | V_{NC} or $V_{NO} = 1.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$ COM to NO or NC, See Figure 14 | 25°C -40°C to +125°C | 3 V | 0.024 | 0.13 | Ω |
| On-state resistance flatness | $R_{on(flat)}$ | V_{NC} or $V_{NO} \leq V_{CC}$, 1.5 V, $V_{CC} - 5.5 \text{ V}$, $I_{COM} = -100 \text{ mA}$ COM to NO or NC, See Figure 14 | 25°C -40°C to +125°C | 3 V | 0.12 | 0.46 | Ω |
| Shunt switch resistance | R_{SH} | I_{NO} or $I_{NC} = 10 \text{ mA}$ | -40°C to +125°C | 3 V | 25 | 40 | Ω |
| On-state leakage current | $I_{COM(ON)}$ | V_{NC} and $V_{NO} = \text{floating}$, $V_{COM} = V_{CC}, V_{CC} - 5.5 \text{ V}$ COM to NO or NC, See Figure 16 | 25°C -40°C to +125°C | 3.6 V | -200 | 200 | nA |
| | | | | | -2500 | 2500 | |
| DIGITAL CONTROL INPUTS (IN)⁽²⁾ | | | | | | | |
| Input logic high | V_{IH} | | -40°C to +125°C | | 1.4 | V_{CC} | V |
| Input logic low | V_{IL} | | -40°C to +125°C | | | 0.6 | V |
| Input leakage current | I_{IH}, I_{IL} | $V_{IN} = V_{CC}$ or 0 | 25°C -40°C to +125°C | 3.6 V | -250 | 250 | nA |
| | | | | | -250 | 250 | |
| DYNAMIC | | | | | | | |
| Turnon time | t_{ON} | $V_{COM} = V_{CC}$, $R_L = 300 \Omega$ $C_L = 35 \text{ pF}$, See Figure 18 | 25°C | 3.3 V | 34 | 80 | ns |
| | | | -40°C to +125°C | 3 V to 3.6 V | | 80 | |
| Turnoff time | t_{OFF} | $V_{COM} = V_{CC}$, $R_L = 300 \Omega$ $C_L = 35 \text{ pF}$, See Figure 18 | 25°C | 3.3 V | 19 | 70 | ns |
| | | | -40°C to +125°C | 3 V to 3.6 V | | 70 | |
| Break-before-make time | t_{BBM} | See Figure 19 | 25°C | 3.3 V | 1 | 7 | ns |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1 \text{ nF}$, See Figure 23 | 25°C | 3.3 V | | 300 | pC |
| On-State NC, NO, COM capacitance | $C_{COM(ON)}$ | $V_{COM} = V_{CC}$ or GND, $f = 10 \text{ MHz}$ See Figure 17 | 25°C | 3.3 V | | 370 | pF |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, [SCBA004](#).

Electrical Characteristics—3.3-V Supply (continued)

 $V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|------------|--|--|-----------------|----------|-----|-------|-----|---------------|
| Digital input capacitance | C_I | $V_{IN} = V_{CC}$ or GND | See Figure 17 | 25°C | 3.3 V | | 2.6 | | pF |
| Bandwidth | BW | $R_L = 50\ \Omega$, -3 dB | Switch ON, See Figure 20 | 25°C | 3.3 V | | 17.5 | | MHz |
| Off-state isolation | O_{ISO} | $R_L = 50\ \Omega$ | $f = 100\text{ kHz}$, See Figure 21 | 25°C | 3.3 V | | -68 | | dB |
| Crosstalk | X_{TALK} | $R_L = 50\ \Omega$ | $f = 100\text{ kHz}$, See Figure 22 | 25°C | 3.3 V | | -76 | | dB |
| Total harmonic distortion | THD | $R_L = 600\ \Omega$, $C_L = 35\text{ pF}$ | $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 24 | 25°C | 3.3 V | | 0.008 | | % |
| SUPPLY | | | | | | | | | |
| Positive supply current | I_{CC} | V_{COM} and $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} =$ floating | | 25°C | 3.6 V | | 0.1 | 1.2 | μA |
| | | | | -40°C to +125°C | | | 1.3 | | |
| | | $V_{COM} = V_{CC} - 5.5\text{ V}$, $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} =$ floating | | -40°C to +125°C | 3.6 V | | | 3.4 | μA |

6.7 Electrical Characteristics—5-V Supply⁽¹⁾

 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|--|------------------------------------|--|---|-----------------|----------------|----------------|-------|----------|----------|
| ANALOG SWITCH | | | | | | | | | |
| Analog signal | V_{COM} , V_{NO} , V_{NC} | | | | | $V_{CC} - 5.5$ | | V_{CC} | V |
| On-state resistance | R_{on} | V_{NC} or $V_{NO} = V_{CC}$, 1.6 V, $V_{CC} = -5.5\text{ V}$, $I_{COM} = -100\text{ mA}$ | COM to NO or NC, See Figure 14 | 25°C | 4.5 V | | 0.52 | 0.74 | Ω |
| | | | | -40°C to +125°C | | | 0.83 | | |
| On-state resistance match between channels | ΔR_{on} | V_{NC} or $V_{NO} = 1.6\text{ V}$, $I_{COM} = -100\text{ mA}$ | COM to NO or NC, See Figure 14 | 25°C | 4.5 V | | 0.04 | 0.23 | Ω |
| | | | | -40°C to +125°C | | | 0.30 | | |
| On-state resistance flatness | $R_{on(Flat)}$ | V_{NC} or $V_{NO} = V_{CC}$, 1.6 V, $V_{CC} = -5.5\text{ V}$, $I_{COM} = -100\text{ mA}$ | COM to NO or NC, See Figure 14 | 25°C | 4.5 V | | 0.076 | 0.46 | Ω |
| | | | | -40°C to +125°C | | | 0.5 | | |
| Shunt switch resistance | R_{SH} | I_{NO} or $I_{NC} = 10\text{ mA}$ | | -40°C to +125°C | 4.5 V | | 16 | 36 | Ω |
| On-state leakage current | $I_{COM(ON)}$ | V_{NC} and $V_{NO} =$ Floating, $V_{COM} = V_{CC}$, $V_{CC} - 5.5\text{ V}$ | See Figure 16 | 25°C | 5.5 V | | -200 | 200 | nA |
| | | | | -40°C to +125°C | | | -2500 | 2500 | |
| DIGITAL CONTROL INPUTS (IN)⁽²⁾ | | | | | | | | | |
| Input logic high | V_{IH} | | | -40°C to +125°C | | 2.4 | | V_{CC} | V |
| Input logic low | V_{IL} | | | -40°C to +125°C | | | | 0.8 | V |
| Input leakage current | I_{IH} , I_{IL} | $V_{IN} = V_{CC}$ or 0 | | 25°C | 5.5 V | | -250 | 250 | nA |
| | | | | -40°C to +125°C | | | -250 | 250 | |
| DYNAMIC | | | | | | | | | |
| Turnon time | t_{ON} | $V_{COM} = V_{CC}$, $R_L = 300\ \Omega$ | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 5 V | | 27 | 80 | ns |
| | | | | -40°C to +125°C | 4.5 V to 5.5 V | | | 80 | |
| Turnoff time | t_{OFF} | $V_{COM} = V_{CC}$, $R_L = 300\ \Omega$ | $C_L = 35\text{ pF}$, See Figure 18 | 25°C | 5 V | | 13 | 70 | ns |
| | | | | -40°C to +125°C | 4.5 V to 5.5 V | | | 70 | |
| Break-before-make time | t_{BBM} | $V_{NC} = V_{NO} = V_{CC}/2$, $R_L = 300\ \Omega$ | $C = 35\text{ pF}$, See Figure 19 | 25°C | 5 V | 1 | 3.5 | | ns |
| Charge injection | Q_C | $V_{GEN} = 0$, $R_{GEN} = 0$ | $C_L = 1\text{ nF}$, See Figure 23 | 25°C | 5 V | | 500 | | pC |

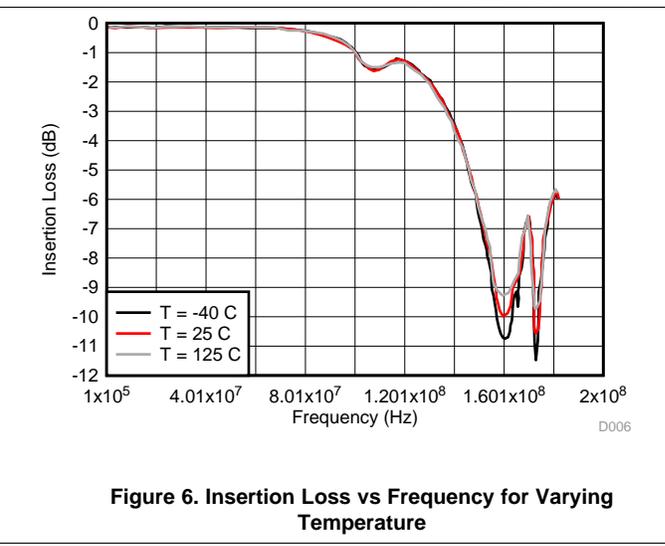
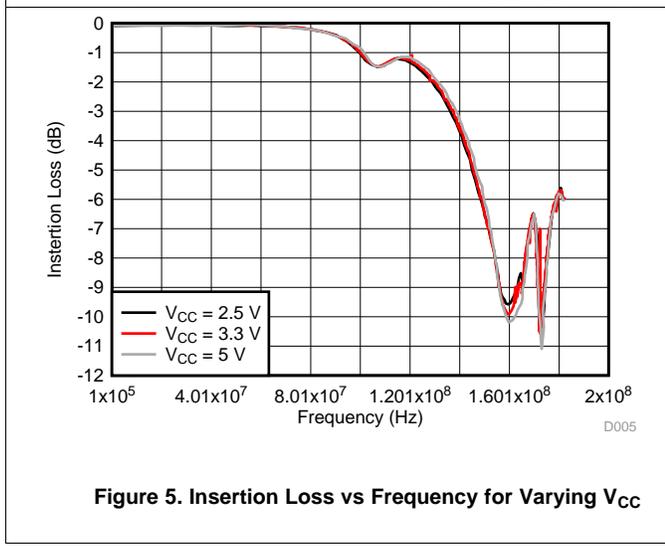
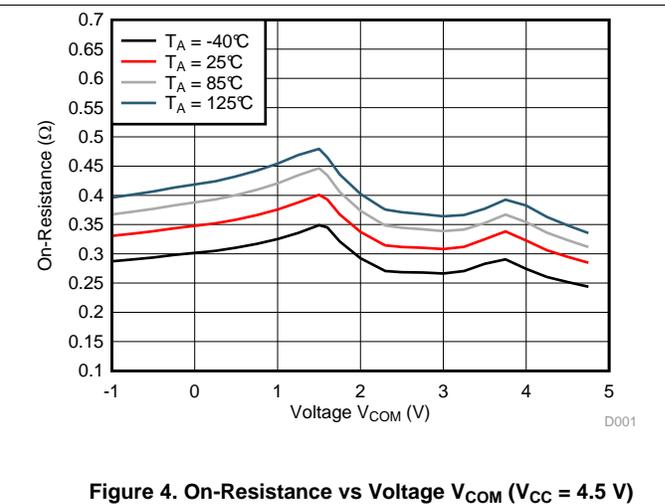
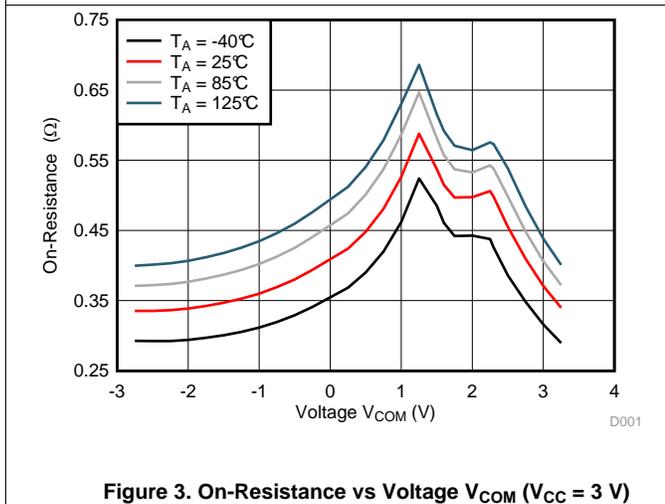
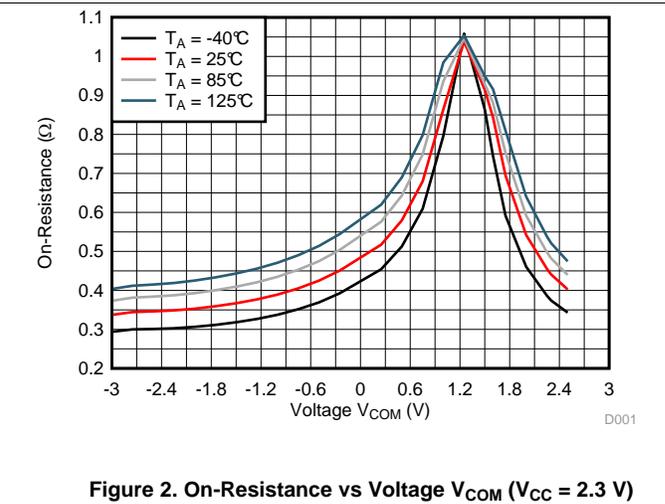
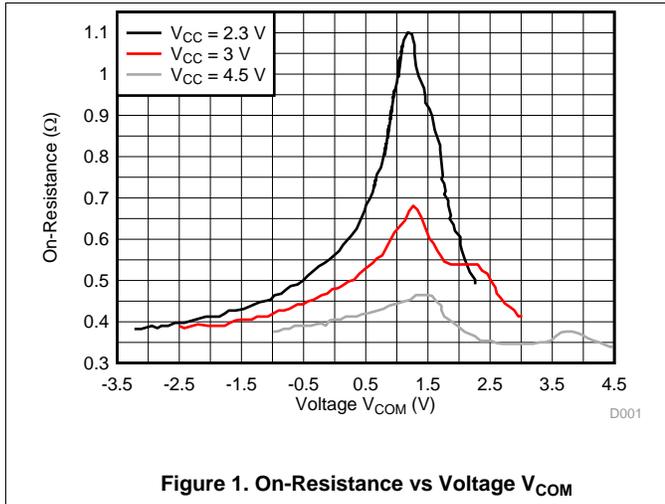
(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report, [SCBA004](#).

Electrical Characteristics—5-V Supply⁽¹⁾ (continued)
 $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|--|---------------|--|---|-------|----------|-----|---------------|-----|------|
| ON-State NC, NO, COM capacitance | $C_{COM(ON)}$ | $V_{COM} = V_{CC}$ or GND | See Figure 17 | 25°C | 5 V | | 370 | | pF |
| Digital input capacitance | C_I | $V_{IN} = V_{CC}$ or GND | See Figure 17 | 25°C | 5 V | | 2.6 | | pF |
| Bandwidth | BW | $R_L = 50 \Omega$ | See Figure 20 | 25°C | 5 V | | 18.3 | | MHz |
| Off-state isolation | O_{ISO} | $R_L = 50 \Omega$ | $f = 100 \text{ kHz}$, See Figure 21 | 25°C | 5 V | | -70 | | dB |
| Crosstalk | X_{TALK} | $R_L = 50 \Omega$ | $f = 100 \text{ kHz}$, See Figure 22 | 25°C | 5 V | | -78 | | dB |
| Total harmonic distortion | THD | $R_L = 600 \Omega$, $C_L = 35 \text{ pF}$ | $f = 20 \text{ Hz to } 20 \text{ kHz}$, See Figure 24 | 25°C | 5 V | | 0.009 | | % |
| SUPPLY | | | | | | | | | |
| Positive supply current | I_{CC} | V_{COM} and $V_{IN} = V_{CC}$ or GND, V_{NC} or $V_{NO} = \text{floating}$ | 25°C | 5.5 V | 0.2 | 1.3 | μA | | |
| | | | -40°C to +125°C | | 3.5 | | | | |
| | | $V_{COM} = V_{CC} - 5.5 \text{ V}$, $V_{IN} =$ V_{CC} or GND, V_{NC} or $V_{NO} =$ floating | -40°C to +125°C | | 5 | | | | |

6.8 Typical Characteristics



Typical Characteristics (continued)

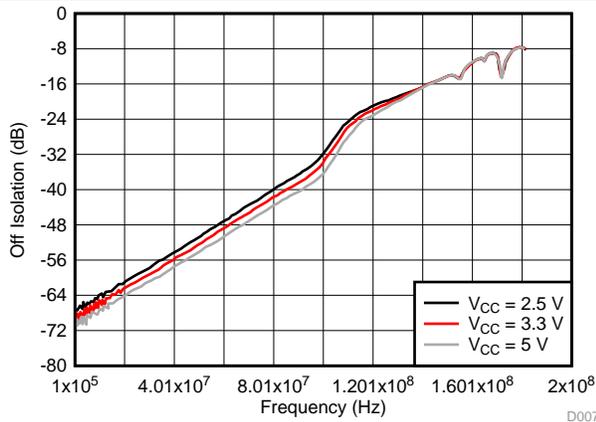


Figure 7. Off Isolation vs Frequency for Varying V_{CC}

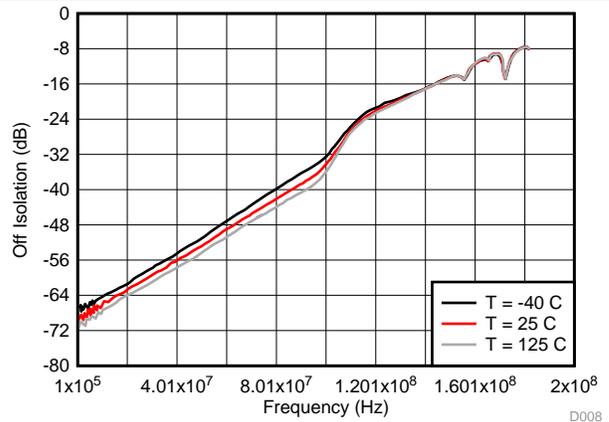


Figure 8. Off Isolation vs Frequency for Varying Temperature

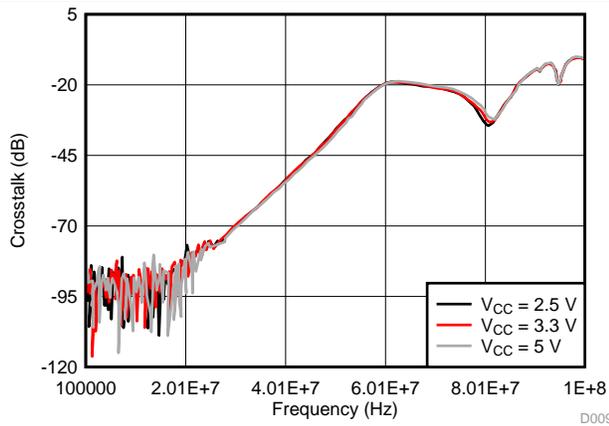


Figure 9. Crosstalk vs Frequency for Varying V_{CC}

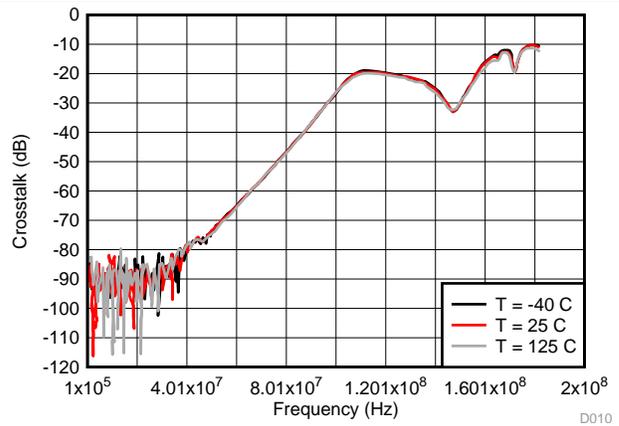


Figure 10. Crosstalk vs Frequency ($V_{CC} = 3.3\text{ V}$)

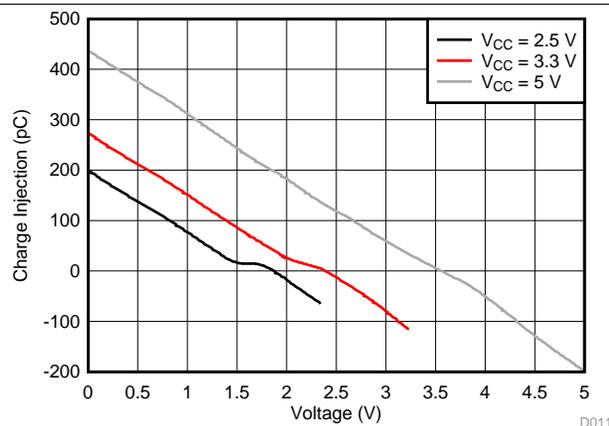


Figure 11. Charge Injection vs Voltage V_{COM}

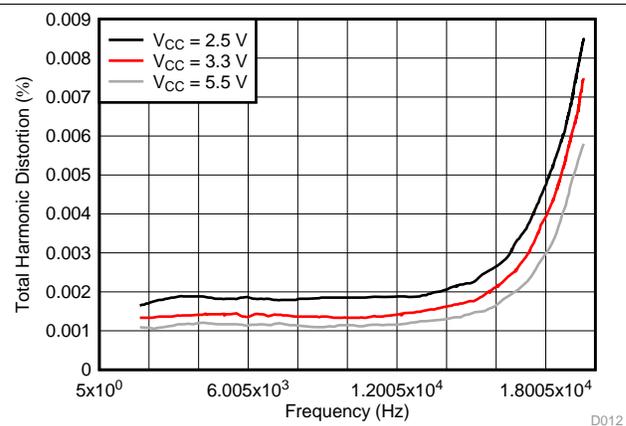
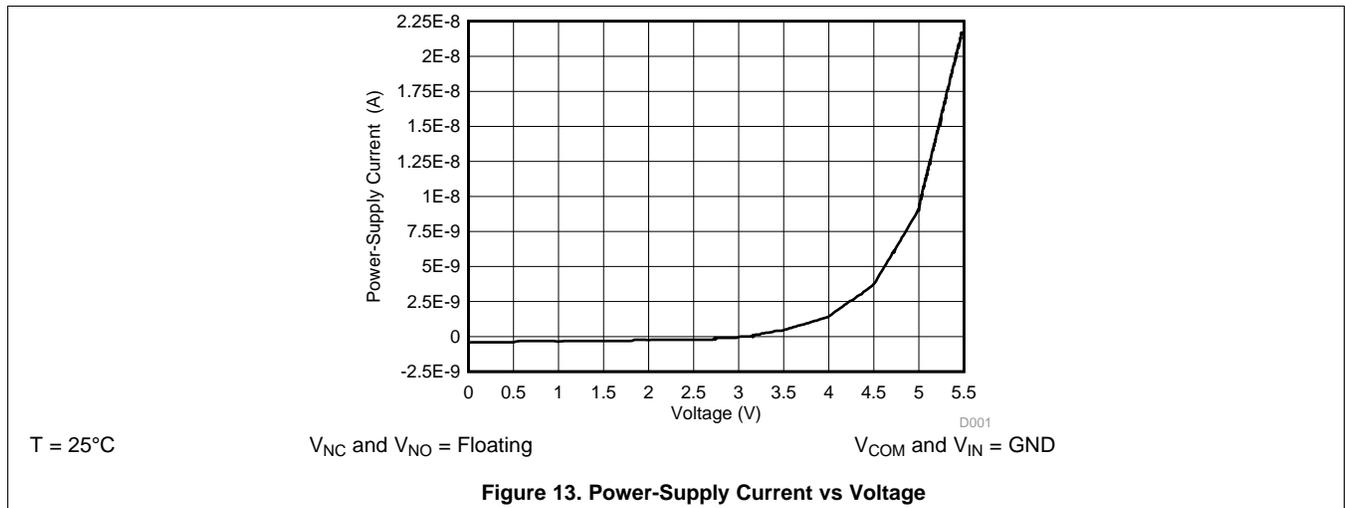


Figure 12. Total Harmonic Distortion vs Frequency

Typical Characteristics (continued)



7 Parameter Measurement Information

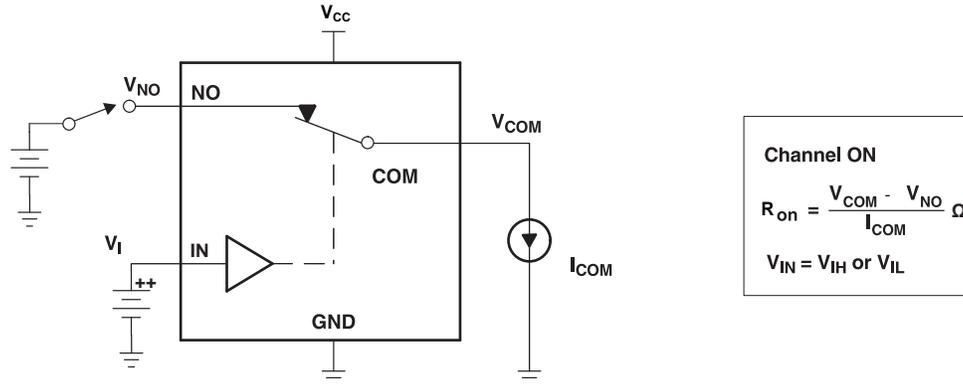


Figure 14. On-State Resistance (R_{on})

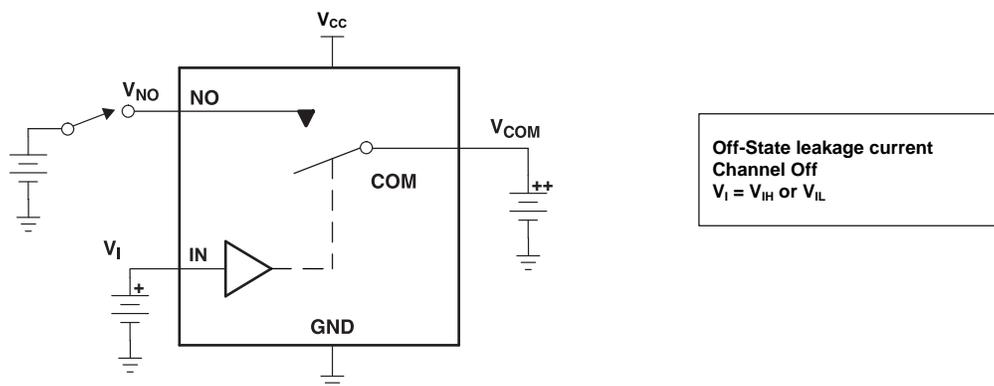
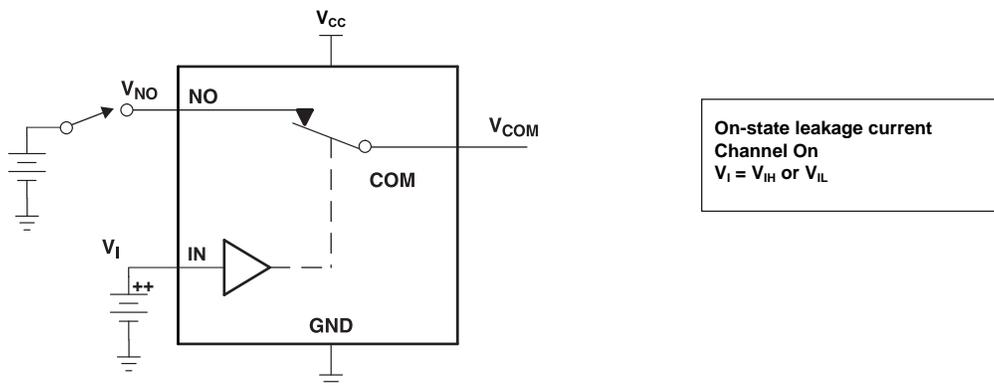


Figure 15. Off-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)



**Figure 16. On-State Leakage Current
($I_{COM(ON)}$, $I_{NO(ON)}$)**

Parameter Measurement Information (continued)

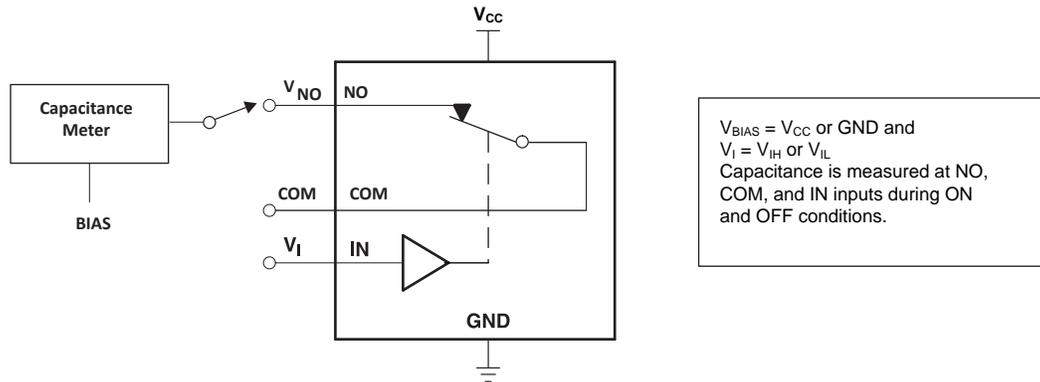
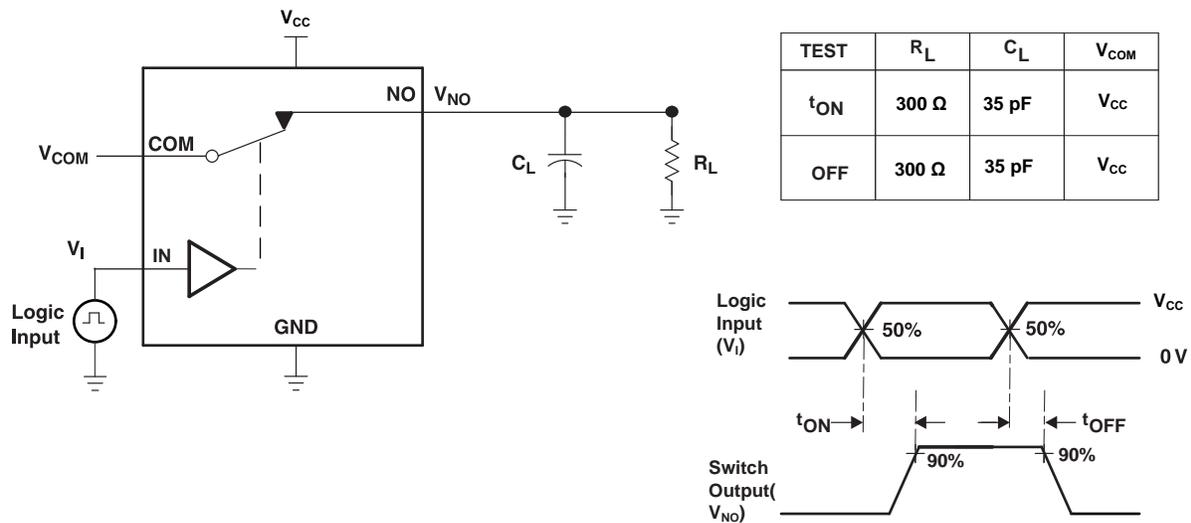


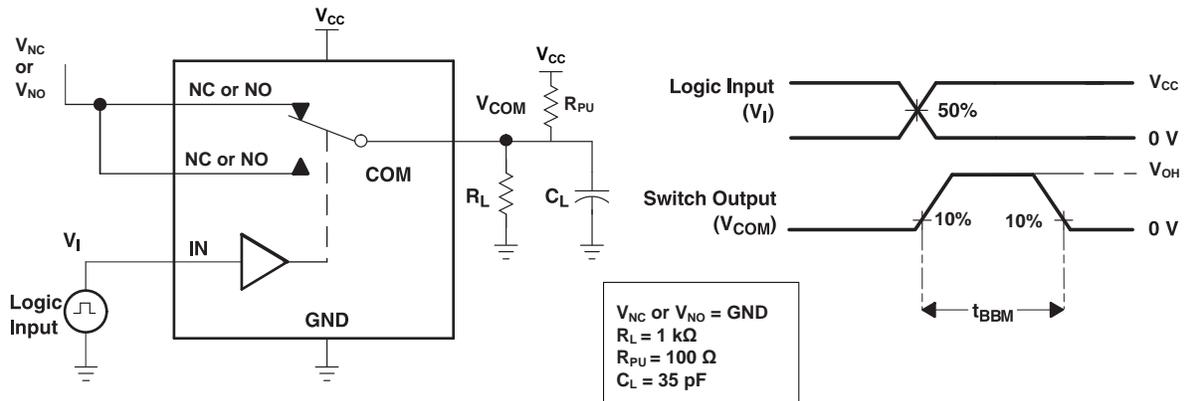
Figure 17. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 18. Turnon (t_{ON}) and Turnoff time (t_{OFF})

Parameter Measurement Information (continued)



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

Figure 19. Break-Before-Make Time (t_{BBM})

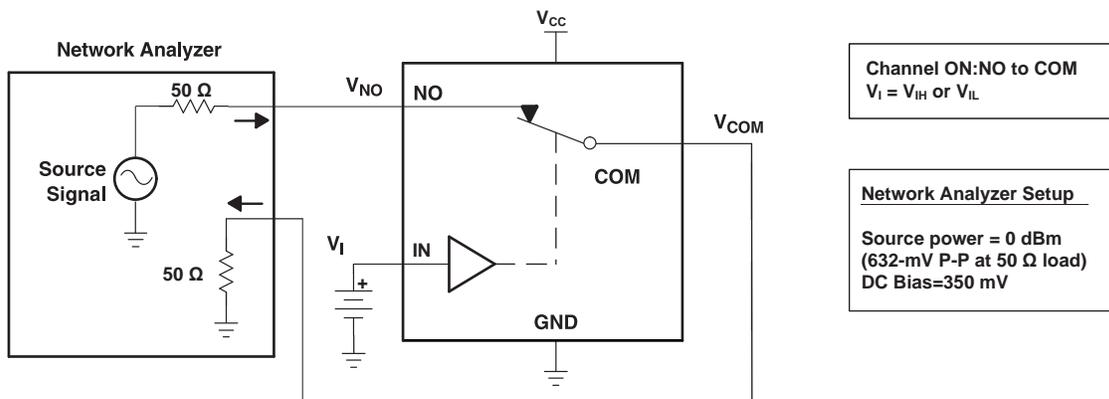


Figure 20. Bandwidth (BW)

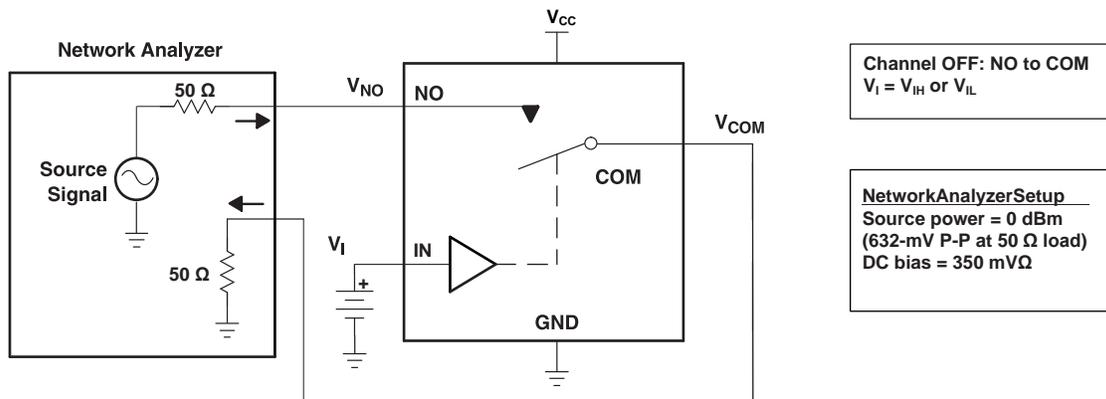


Figure 21. Off Isolation (O_{ISO})

Parameter Measurement Information (continued)

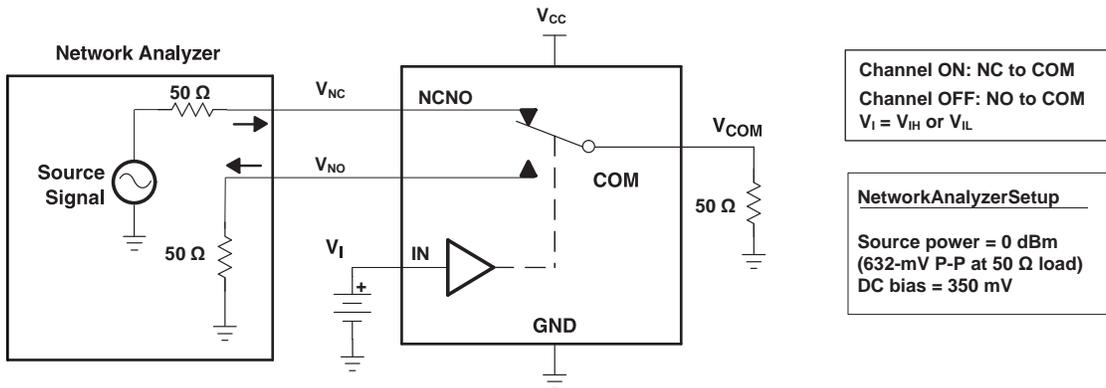
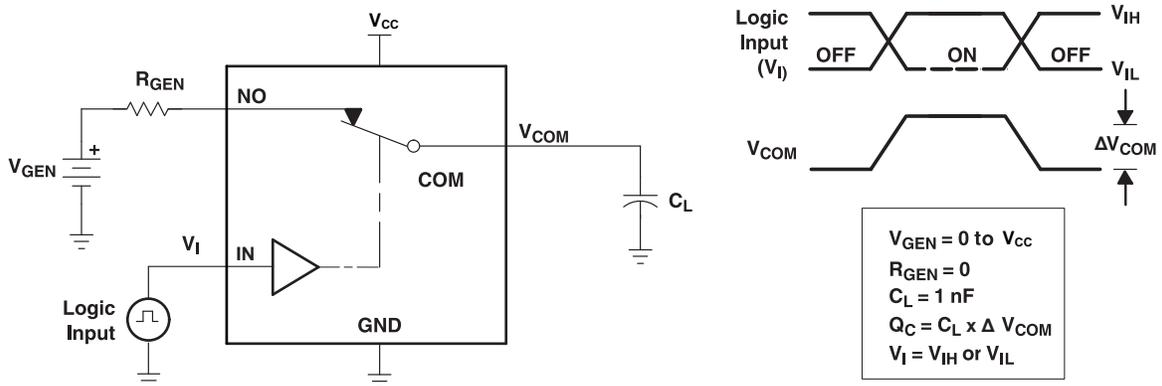
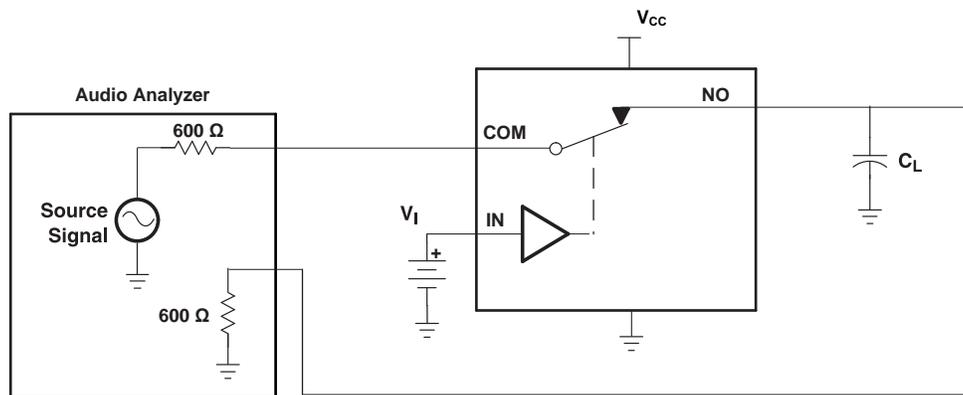
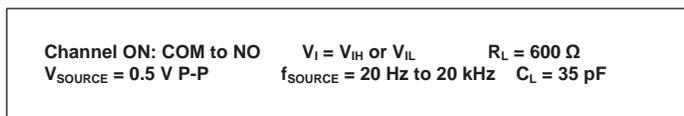


Figure 22. Crosstalk (X_{TALK})



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

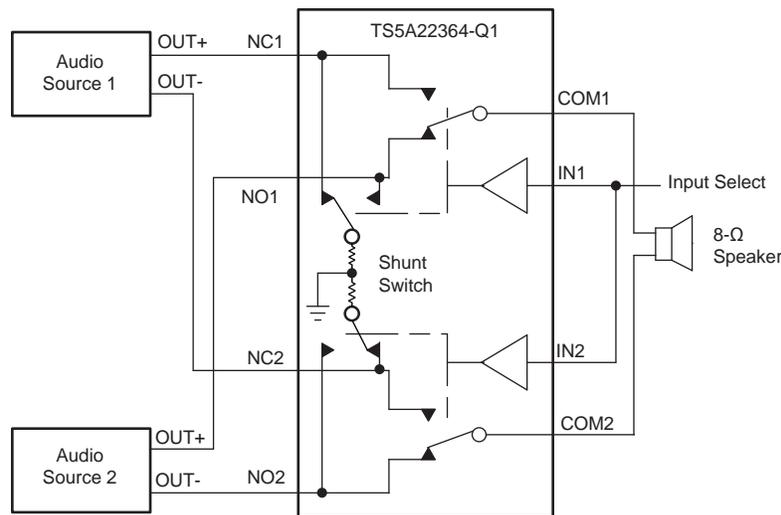
Figure 24. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A22364-Q1 is a 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3-V to 5.5-V power supply. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. Additionally, the TS5A22364-Q1 includes an internal shunt switch, which automatically discharges any capacitance at the NC or NO terminals when they are not connected to COM. This reduces the audible click-and-pop noise when switching between two sources. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low On-state resistance, excellent channel-to-channel On-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Click-and-Pop Reduction

The 50-Ω shunt switches on the TS5A22364-Q1 automatically discharge any capacitance at the NC or NO terminals when they are not connected to COM. This reduces the audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

8.4 Device Functional Modes

Table 1 shows the function table for the TS5A22364-Q1.

Table 1. Function Table

| IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|----|-------------------------|-------------------------|
| L | ON | OFF |
| H | OFF | ON |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Negative Signal Swing Capability

The TS5A22364-Q1 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single 2.3-V to 5.5-V supply. The input and output signal swing of the device is dependant on the supply voltage V_{CC} : the device can pass signals as high as V_{CC} and as low as $V_{CC} - 5.5$ V, including signals below ground with minimal distortion. The Off state signal path (either NC or NO) during the operation of the TS5A22364-Q1 cannot handle negative DC voltage.

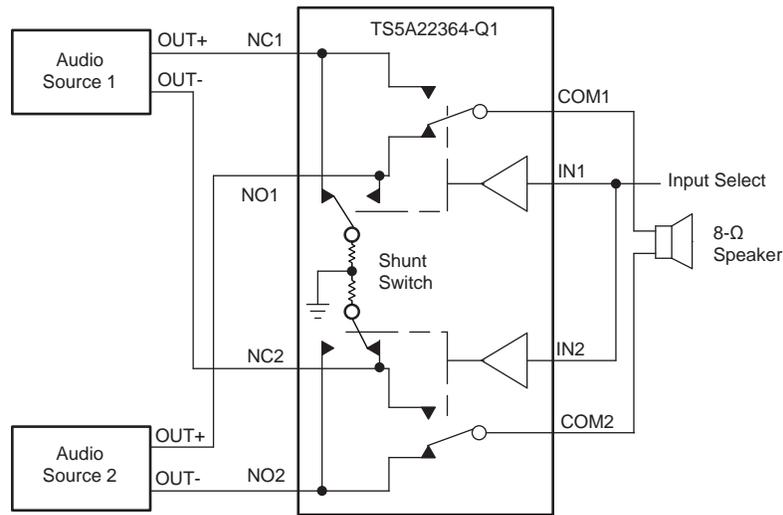
Table 2 shows the input-output signal swing the user can get with different supply voltages.

Table 2. Input-Output Signal Swing

| SUPPLY VOLTAGE, V_{CC} | MINIMUM (V_{NC}, V_{NO}, V_{COM}) = $V_{CC} - 5.5$ | MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC} | MINIMUM (V_{NC}, V_{NO}, V_{COM}) = $V_{CC} - 5.5$ | MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_{CC} |
|--------------------------|--|--|--|--|
| | ON State signal path | | OFF state signal path | |
| 5.5 V | 0 V | 5.5 V | 0 V | 5.5 V |
| 4.2 V | -1.3 V | 4.2 V | 0 V | 4.2 V |
| 3.3 V | -2.2 V | 3.3 V | 0 V | 3.3 V |
| 3 V | -2.5 V | 3 V | 0 V | 3 V |
| 2.5 V | -3 V | 2.5 V | 0 V | 2.5 V |

9.2 Typical Application

The 50- Ω shunt switches on the TS5A22364-Q1 automatically discharge any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops. See Figure 25.

Typical Application (continued)


Copyright © 2016, Texas Instruments Incorporated

Figure 25. Shunt Switch Block Diagram
9.2.1 Design Requirements

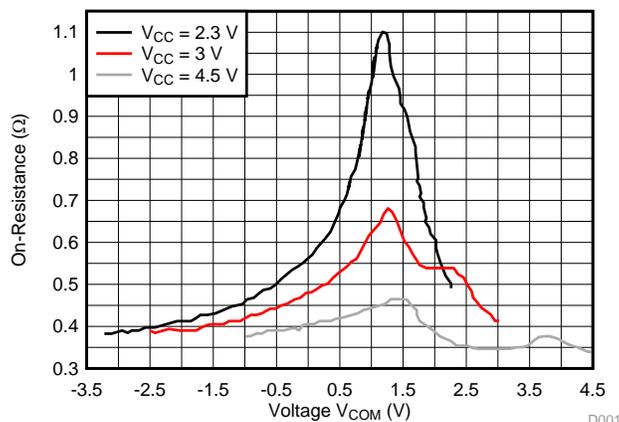
Tie the digitally controlled input select pins IN1 and IN2 to V_{CC} or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22364-Q1 operates from a single 2.3-V to 5.5-V supply and the input-output signal swing of the device is dependant of the supply voltage V_{CC} . The device passes signals as high as V_{CC} and as low as $V_{CC} - 5.5$ V. Use Table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Limit the current through the shunt resistor so as not to exceed the ± 20 mA.

Ensure that the device is powered up with a supply voltage on V_{CC} before a voltage can be applied to the signal paths NC and NO.

9.2.3 Application Curve

Figure 26. On-Resistance vs Voltage V_{COM}

10 Power Supply Recommendations

The TS5A22364-Q1 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100 μ s delay after VCC is at voltage before applying a signal on NC and NO paths.

It is also good practice to place a 0.1- μ F bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

11.2 Layout Example

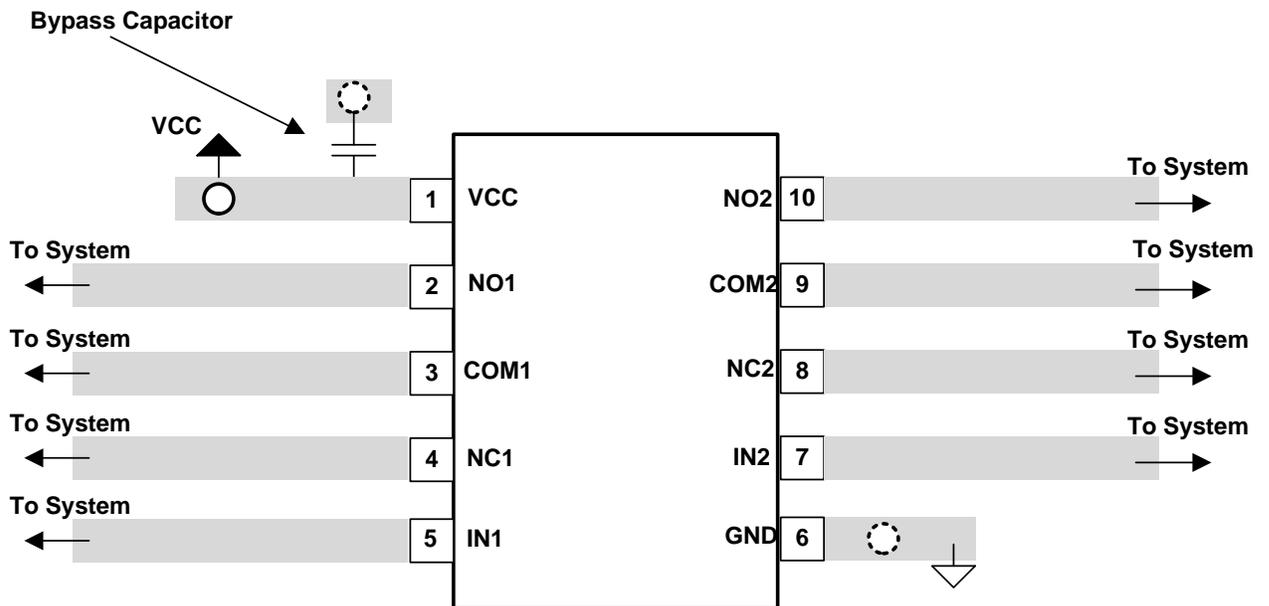


Figure 27. Layout Example of TS5A22364-Q1

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TS5A22364QDGSRQ1 | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | SJN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

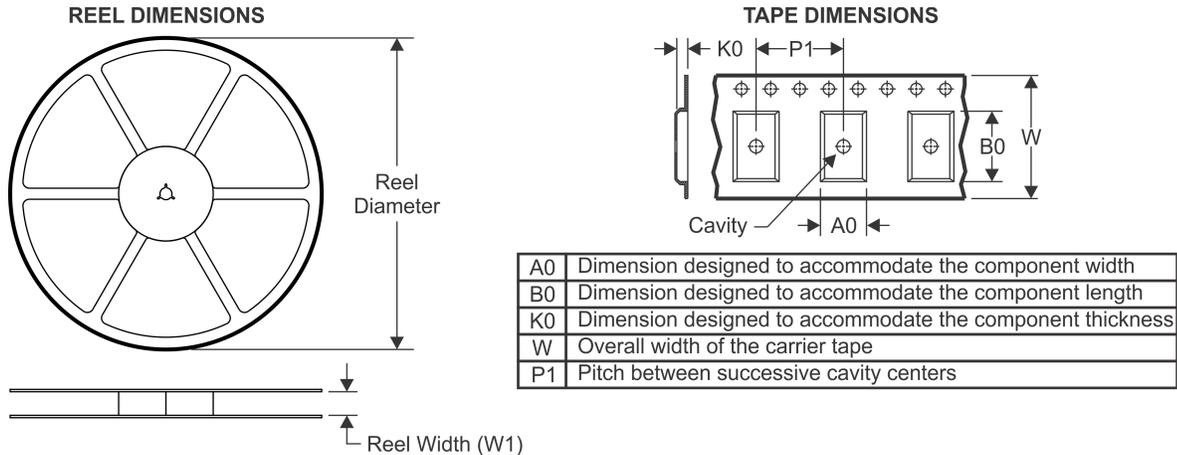
OTHER QUALIFIED VERSIONS OF TS5A22364-Q1 :

- Catalog: [TS5A22364](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS5A22364QDGSRQ1 | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS5A22364QDGSRQ1 | VSSOP | DGS | 10 | 2500 | 366.0 | 364.0 | 50.0 |

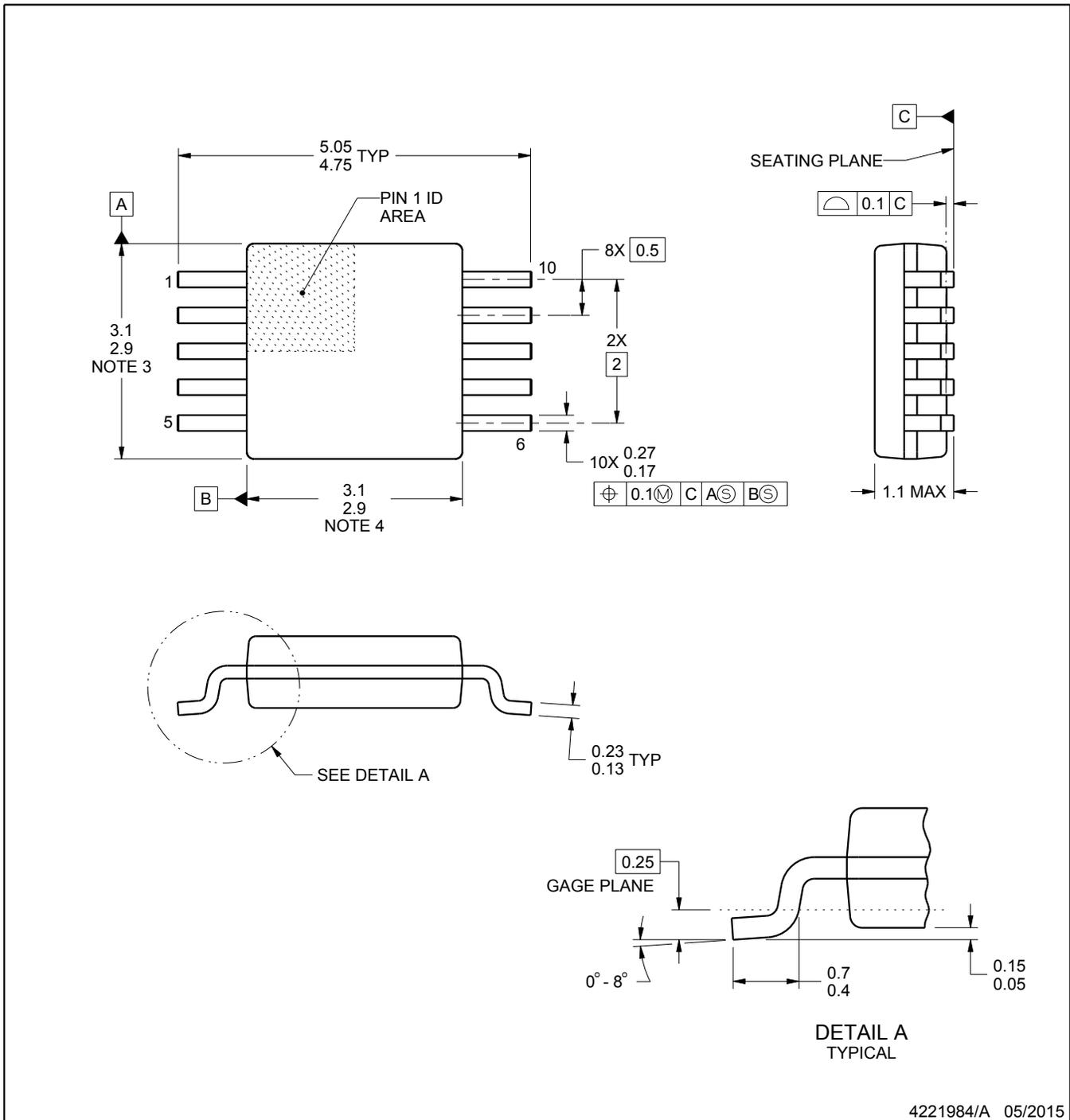
DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

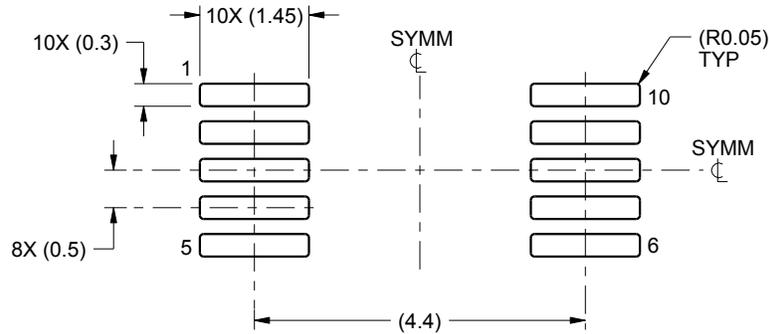
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

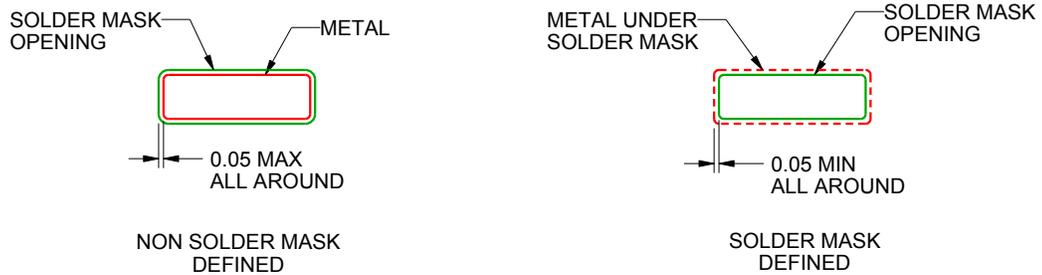
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

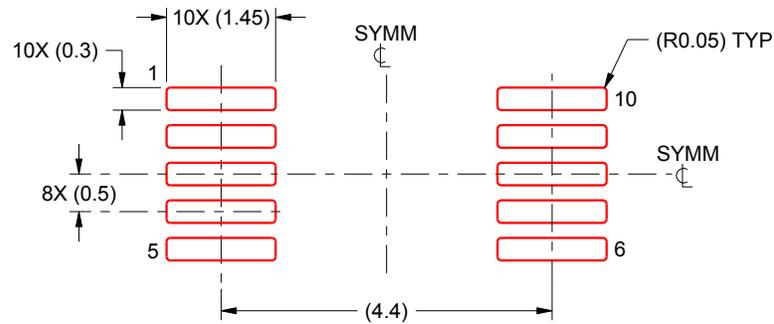
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated