LVC DESIGNER'S GUIDE

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TEXAS INSTRUMENTS

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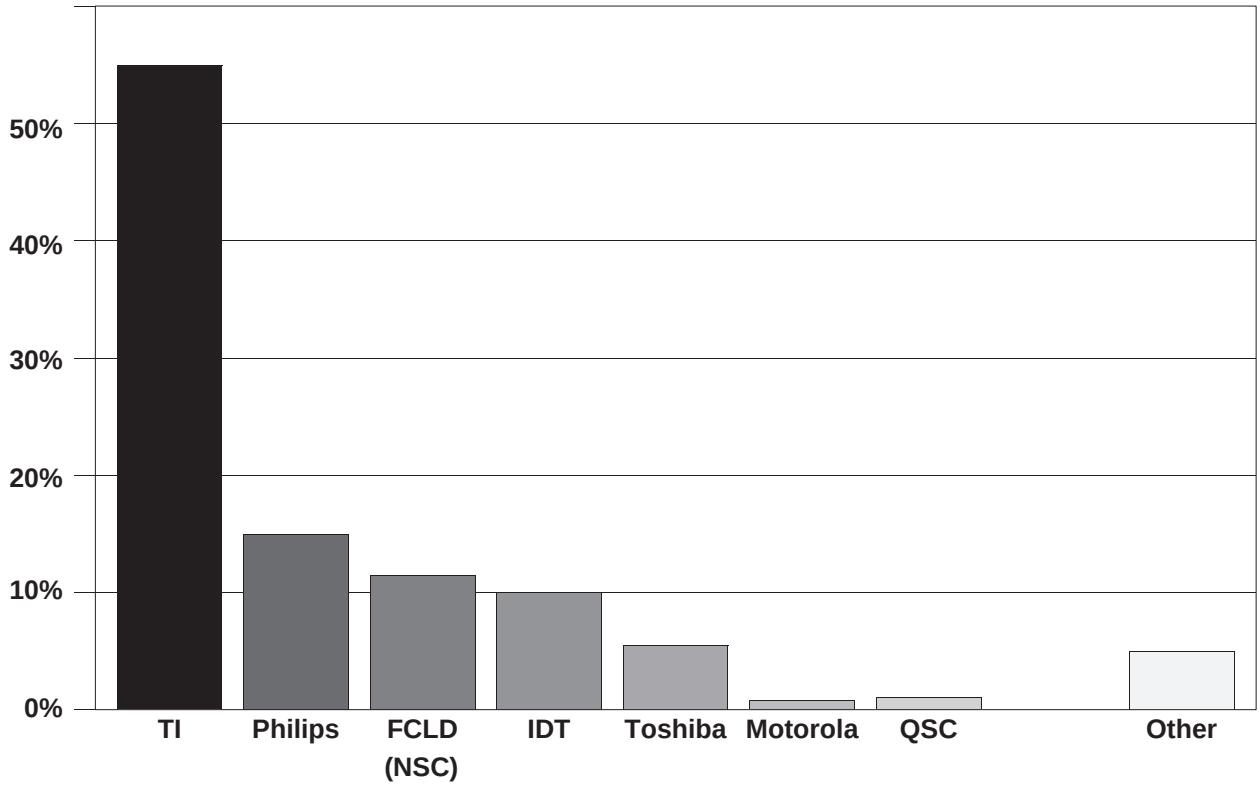
With the introduction of the LVT device family, TI began the move toward faster speeds, lower power dissipation, and smaller end equipment. TI followed with LVC, LV, and ALVC.

No other company has a broader, more complete line of 3.3-V logic devices. No matter what your performance needs, TI has a device family specifically designed for you.

It is no wonder TI is the world's leading 3.3-V logic manufacturer.

1H96 3.3-V Logic Market Shares



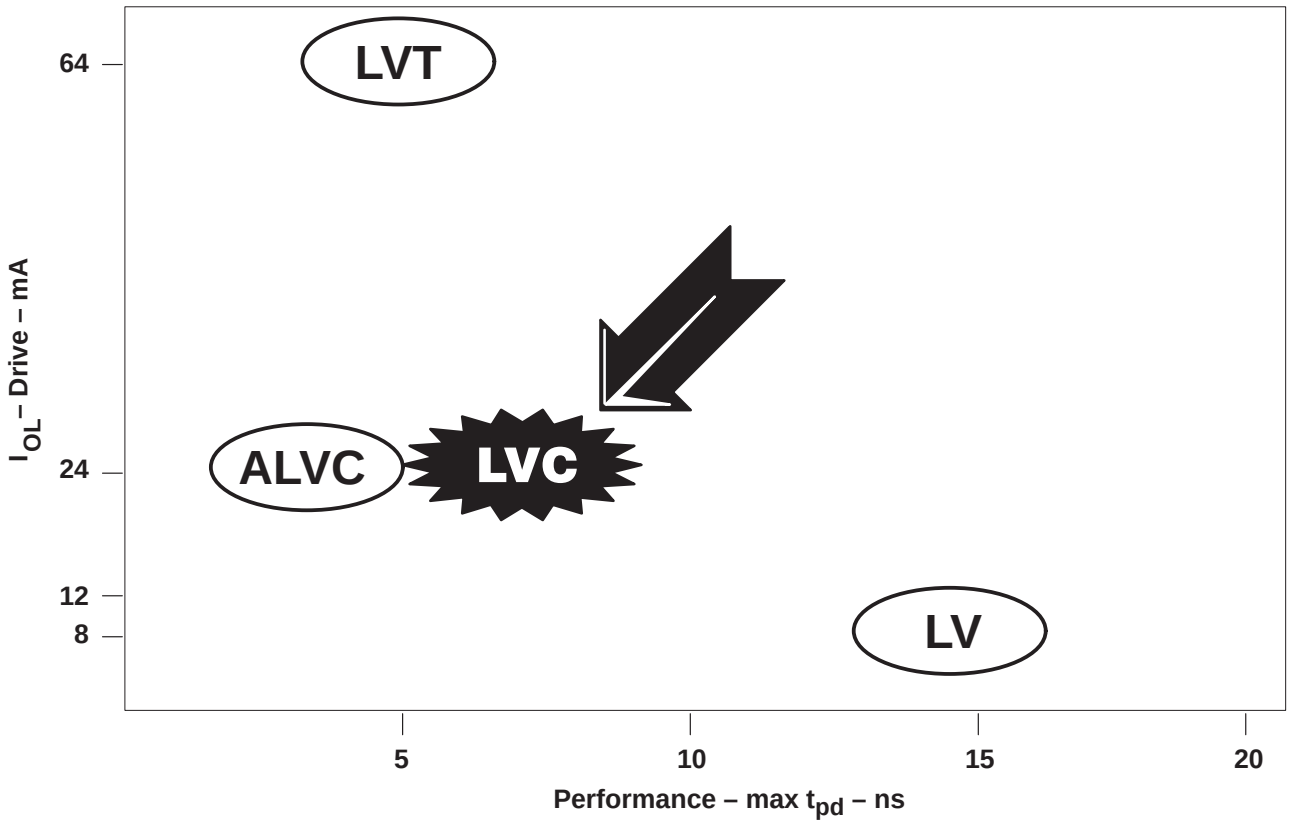
TI: No. 1 in Low-Voltage Logic

Source: Insight Onsite

TI has a full range of low-voltage (3.3-V) logic products. In fact, TI is the only logic manufacturer with a 3.3-V logic device family at every price/performance node (see **Appendix D**).

Lately, there has been much interest in LVC, the 5-V tolerant logic device family designed for medium performance needs (speed = 6.5 ns and drive = 24 mA). This designer's guide was created to answer customers' questions.

Section 1 contains general characterization information about LVC. **Section 2** contains data from direct-comparison tests conducted by TI's Advanced System Logic group. **Appendices A–E** include complete listings of the fully 5-V tolerant LVC device family, a list of frequently asked questions, and packaging information.



TI Low-Voltage Offerings

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THE CASE FOR LOW VOLTAGE

LVL, or low-voltage logic, in the context of this designer's guide, refers to devices designed specifically to operate from a 3.3-V power supply. Initially, an alternative method of achieving low-voltage operation was to use a device designed for 5-V operation, but power it with a 3.3-V supply. Although this resulted in 3.3-V characteristics, this method resulted in significantly slower propagation time. Subsequently, parts were designed to operate using a 3.3-V power supply. **Section 1** describes this category of devices.

A primary benefit of using a 3.3-V power supply as opposed to the traditional 5-V power supply is the reduced power consumption. Because power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage, a reduction in any one of these is beneficial. Supply voltage has a square relationship in the reduction of power consumed, whereas load capacitance and frequency of operation have a linear effect. As a result, a small decrease in the supply voltage yields significant reduction in the power consumption. **Equation 1** provides the dynamic component of the power calculation. (The calculation for computing the total power consumed is provided in *Power Considerations* in this section.)

$$P_D(\text{dynamic}) = [\ (C_{pd} + C_L) \times V_{CC}{}^2 \times f\ ]N_{SW} \quad \textbf{(1)}$$

Where: C_{pd} = Power dissipation capacitance (F)
C_L = External load capacitance (F)
V_{CC} = Supply voltage (V)
f = Operating frequency (Hz)
N_{SW} = Total number of outputs switching

A reduction of power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature. This may provide the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery when a system is not powered by a regulated power supply.

Although a complete migration may not be feasible for a particular application, beginning to integrate 3.3-V components in a system still has benefits. If system parts are designed using 3.3-V parts, then when the remaining parts become available, converting the system completely to 3.3-V parts is a much smaller task. For example, having the internal parts of a personal computer powered from a 3.3-V power supply while having the memory powered from a 5-V power supply is a fairly common current configuration. Although LVL devices are not used throughout the entire design, this system is easily adapted to a complete 3.3-V system when 3.3-V memory becomes cost effective.

CONSIDERATIONS FOR INTERFACING TO 5-V LOGIC

Interfacing 3.3-V devices to 5-V devices requires consideration of the logic switching levels of the driver and the receiver. **Figure 1–1** illustrates the various switching standards for 5-V CMOS, 5-V TTL, and 3.3-V TTL. The switching levels for the 5-V TTL and the 3.3-V TTL are identical, whereas the 5-V CMOS switching levels are different. The impact of this must be considered when interfacing 3.3-V systems with 5-V systems.

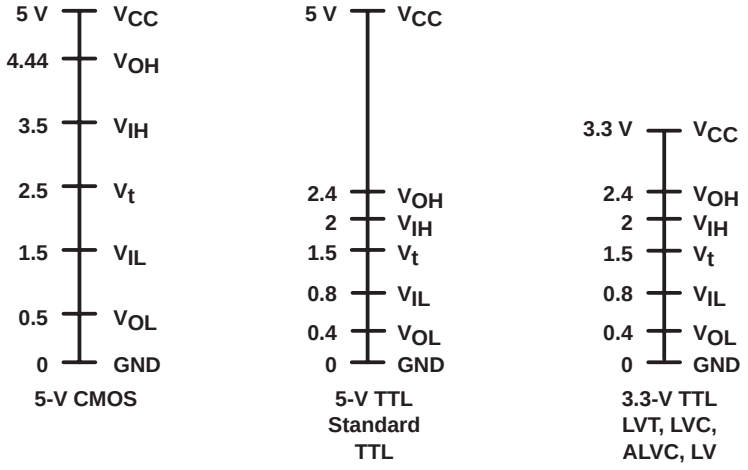
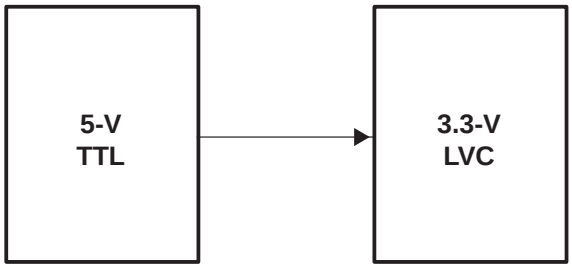


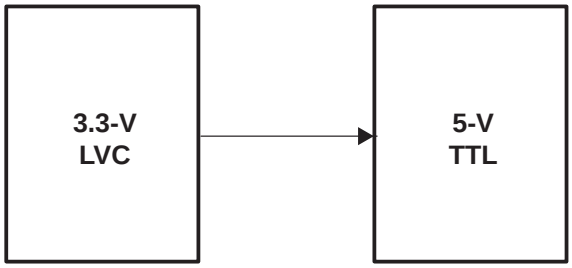
Figure 1–1. Comparison of 5-V CMOS, 5-V TTL, and 3.3-V TTL Switching Standards

Depending on the specific parts used in a system, four different cases can result. These cases are illustrated in **Figure 1–2**.

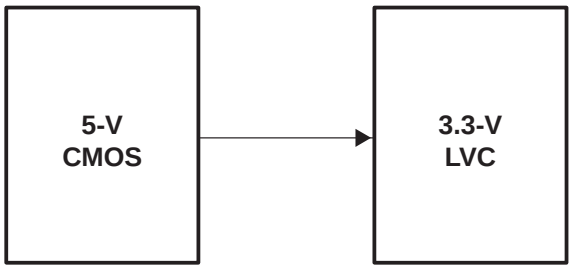
Case 1: 5-V TTL Device Driving 3.3-V TTL Device (LVC)



Case 2: 3.3-V TTL Device (LVC) Driving 5-V TTL Device



Case 3: 5-V CMOS Device Driving 3.3-V TTL Device (LVC)



Case 4: 3.3-V TTL Device (LVC) Driving 5-V CMOS Device

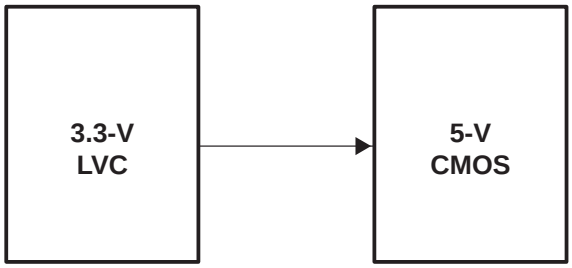


Figure 1–2. Summary of Four Cases When Interfacing 3.3-V Devices With 5-V Devices

Case 1

Case 1 addresses a 5-V TTL device driving a 3.3-V TTL device. As shown in **Figure 1–1**, the switching levels for 5-V TTL and 3.3-V LVC are the same. Since 5-V tolerant devices can withstand a dc input of 6.5 V, interfacing these two devices does not require additional components or further design efforts.

TI's crossbar technology (CBT) switches can be used to translate from 5-V TTL to 3.3-V devices that are not 5-V tolerant. This is accomplished by using an external diode to create a 0.7-V drop (reducing 5 V to 4.3 V) with the CBT (of which the field effect transistor has a gate-to-source voltage drop of 1 V) that results in a net 3.3-V level. TI produces a CBTD device that incorporates the diode as part of the chip, thereby eliminating the need for an external diode.

Case 2

Case 2 occurs when a 3.3-V TTL device (LVC) drives a 5-V TTL device. The switching levels are the same and it is possible to interface in this configuration without additional circuitry or devices. Driving a 5-V device from a 3.3-V device without additional complications or circuitry may seem odd, but as long as the 3.3-V device produces V_{OH} and V_{OL} levels of 2.4 V and 0.4 V, the input of the 5-V device reads them as valid levels since V_{IH} and V_{IL} are 2 V and 0.8 V.

Case 3

Case 3 occurs when a 5-V CMOS device drives a 3.3-V TTL device (LVC). Two different switching standards that do not match (see **Figure 1–1**) are interfacing. Upon further analysis of the 5-V CMOS V_{OH} and V_{OL} and the 3.3-V LVC V_{IH} and V_{IL} switching levels, **Figure 1–1** shows that although a disparity exists, a 5-V tolerant 3.3-V device can function properly with 5-V CMOS input levels. With a 5-V tolerant LVC device, the configuration of a 5-V CMOS part driving a 3.3-V LVC part is possible.

Case 4

Case 4 occurs when a 3.3-V TTL device (LVC) drives a 5-V CMOS device. Two different switching standards are interfacing. As shown in **Figure 1–1**, the specified V_{OH} for a 3.3-V LVC is 2.4 V (higher output levels up to 3.3 V are possible), whereas the minimum required V_{IH} for a 5-V CMOS device is 3.5 V. As such, driving a 5-V CMOS device with a 3.3-V LVC (or any other standard 3.3-V logic) device is impossible because, even at the maximum V_{OH} of 3.3 V, the minimum V_{IH} of 3.5 V is never attained. To accommodate this occurrence, TI designed a series of split-rail devices; e.g., the SN74ALVC164245 and the SN74LVC4245, which have one side of the device powered at a 3.3-V level and the other side powered at a 5-V level. By having two different power supplies on the same device, the minimum voltage levels required for switching can be met and a 3.3-V logic part can essentially drive a 5-V CMOS device.

AC PERFORMANCE

A desirable objective is for systems to operate at faster speeds that allow less time for performing operations. For example, consider the impact a continually increasing operating frequency has on accessing memory or on performing arithmetic computations; the faster the system runs, the less time is available for other support functions to be performed.

To meet this need, advances have been made in the fabrication of integrated circuits (ICs). Specifically in the low-voltage arena, the LV, LVC, ALVC, and LVT logic family fabrication geometries have undergone changes that have consistently improved their performance. This is shown in **Figures 1–3 through 1–5**, which compare the propagation delay times of LV, LVC, ALVC, and LVT devices for differing values of operating free-air temperature, number of outputs switching, and load capacitance.

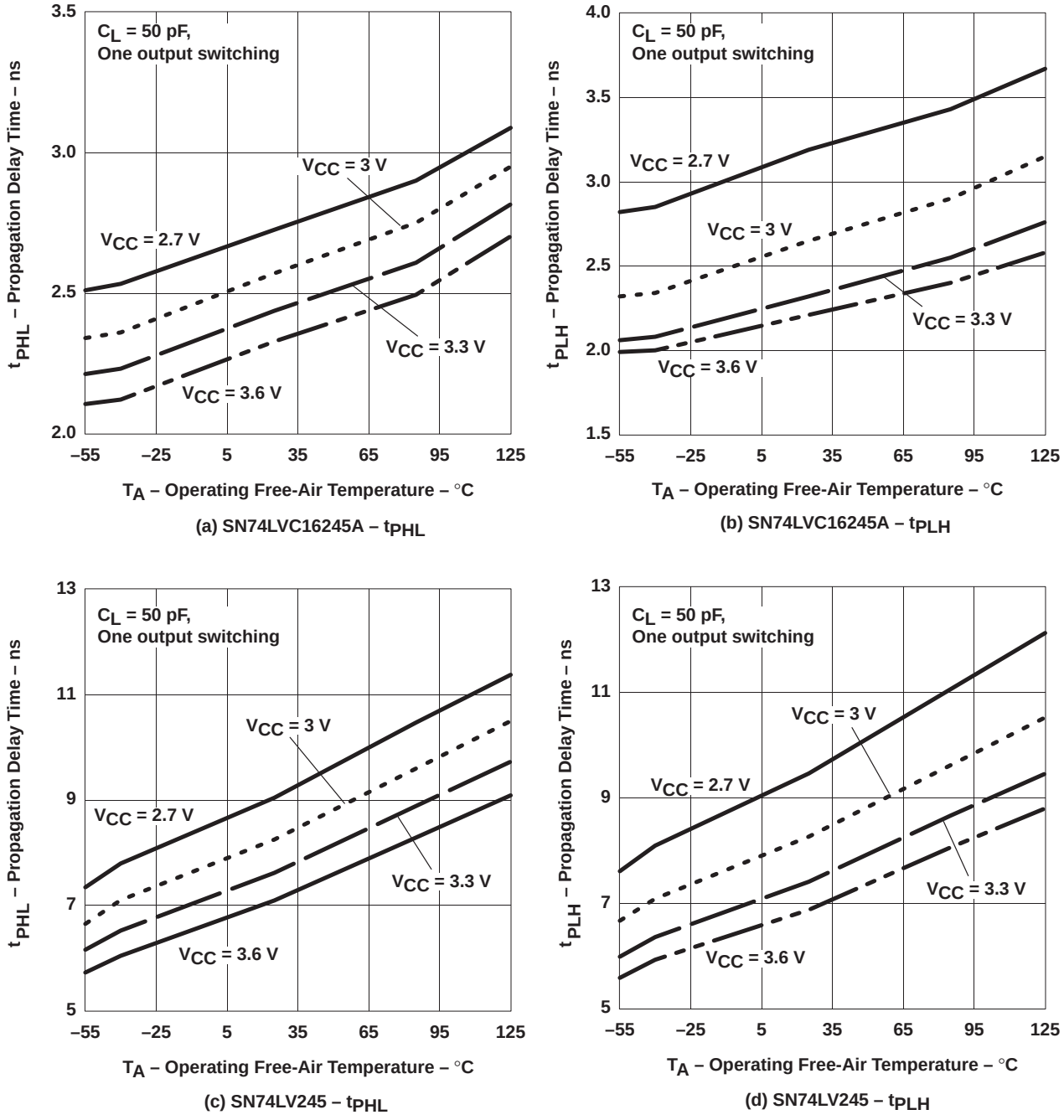
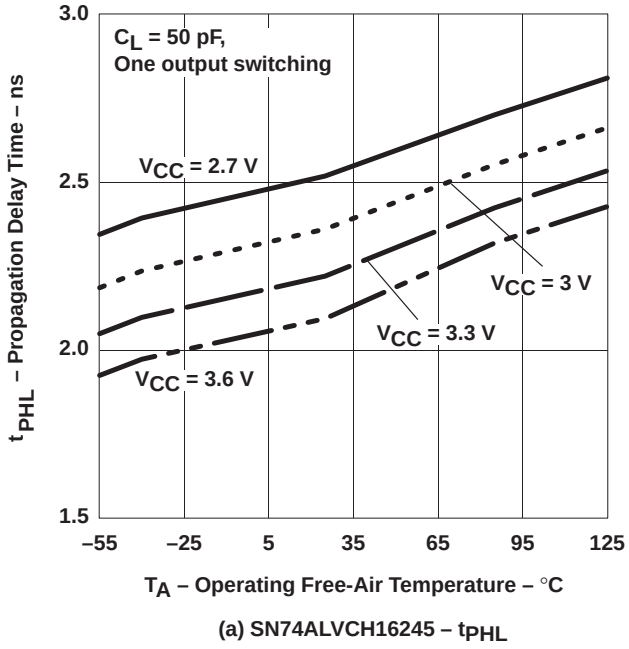
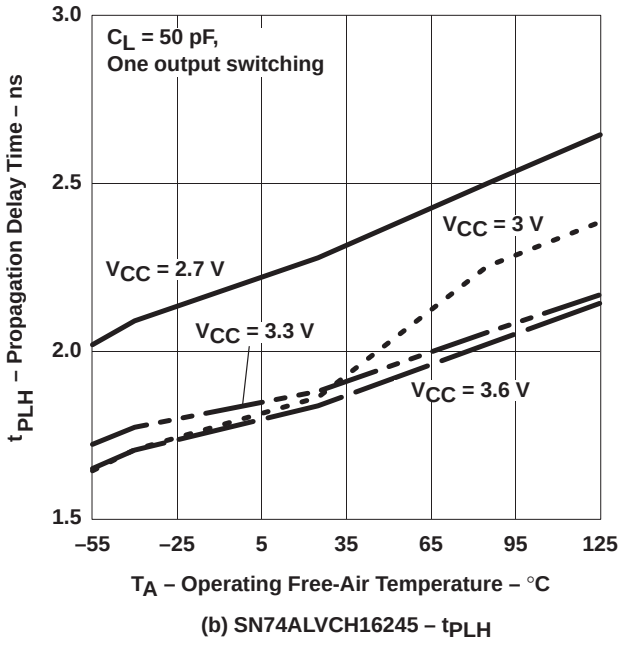


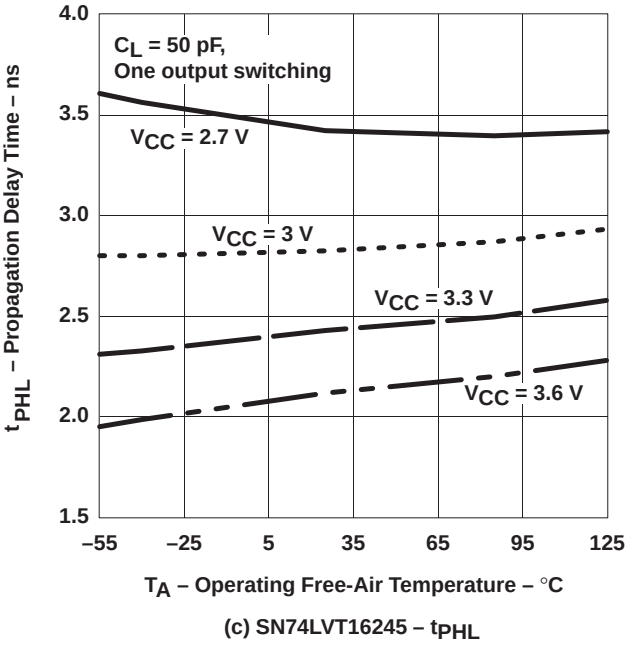
Figure 1–3. Propagation Delay Time Versus Operating Free-Air Temperature



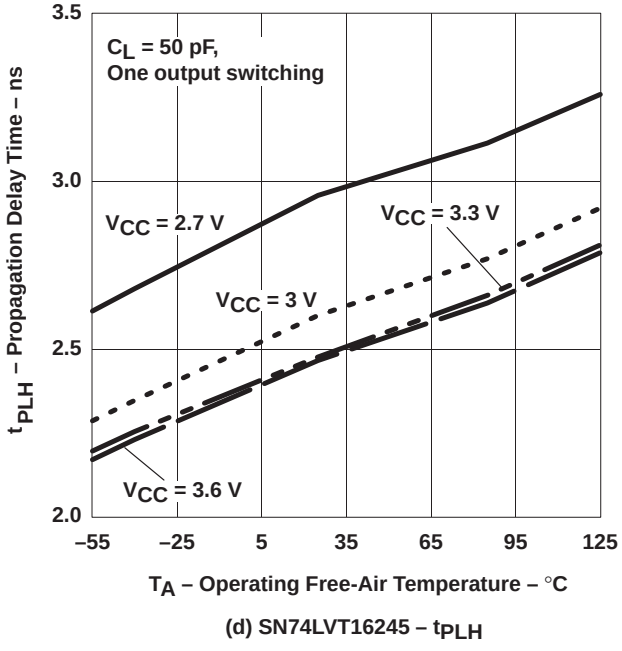
(a) SN74ALVCH16245 – t_{PHL}



(b) SN74ALVCH16245 – t_{PLH}



(c) SN74LVT16245 – t_{PHL}



(d) SN74LVT16245 – t_{PLH}

Figure 1–3. Propagation Delay Time Versus Operating Free-Air Temperature (Continued)

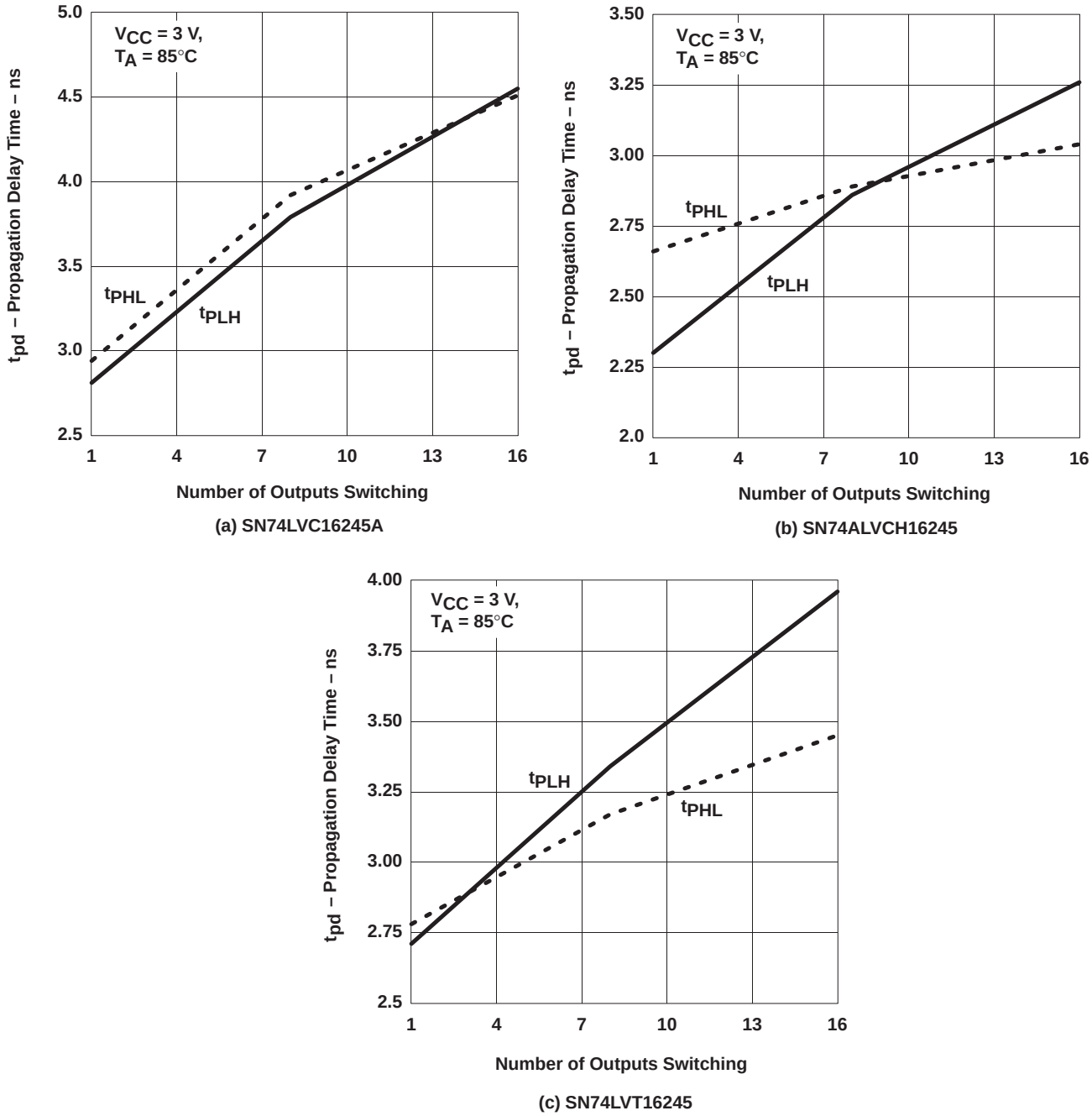


Figure 1–4. Propagation Delay Time Versus Number of Outputs Switching

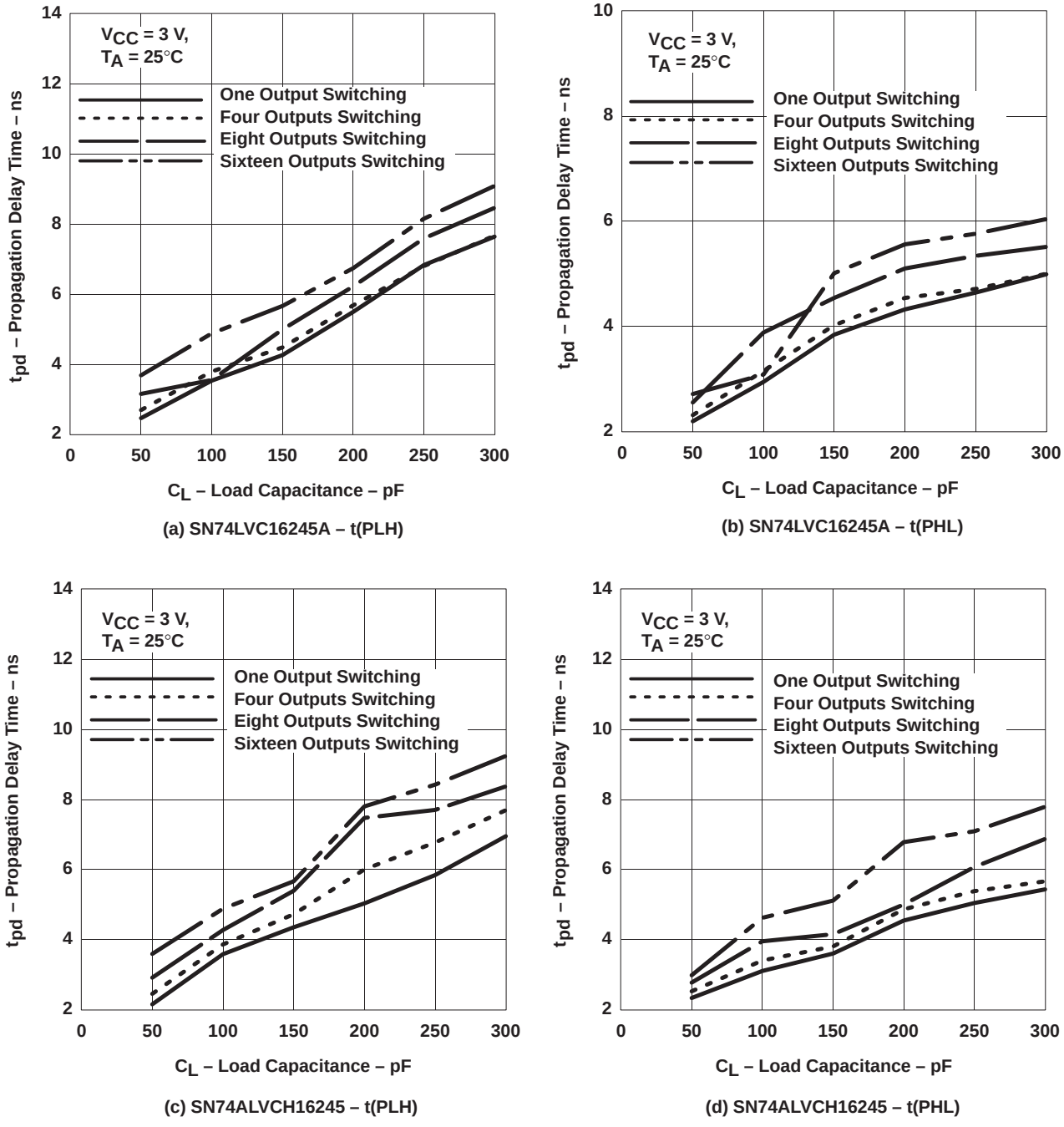


Figure 1–5. Propagation Delay Time Versus Load Capacitance

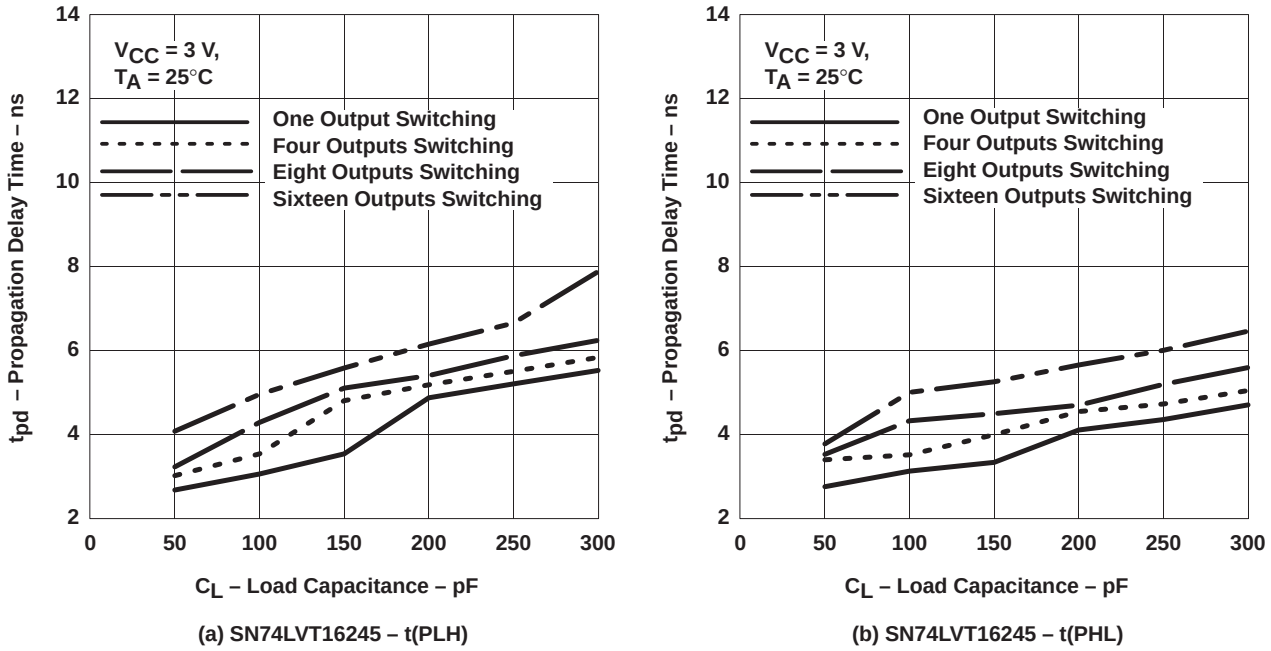


Figure 1–5. Propagation Delay Time Versus Load Capacitance (Continued)

POWER CONSIDERATIONS

The continued general industry trend is to make devices more robust and faster while reducing their size and power consumption. The LVC family of devices uses a CMOS output structure that has low power consumption and provides a medium drive current capability.

When calculating the amount of power consumed, both static (dc) and dynamic (ac) power must be considered. A variable when computing static power is I_{CC} and is provided in the data sheet for each specific device. The LVC family I_{CC} typically offers one-half of the LV family I_{CC}, one-fourth of the ALVC family I_{CC}, and a small fraction of the LVT family I_{CC}.

The majority of power consumed is dynamic due to the charging and discharging of internal capacitance and external load capacitance. The internal parasitic capacitances are known as C_{pd} and are expressed by **Equation 2**.

$$C_{pd} = [\ (I_{CC}(\text{dynamic}) \div (V_{CC} \times f)\ ] - C_L \quad \textbf{(2)}$$

Where: I_{CC} = Measured value of current into the device (A)
V_{CC} = Supply voltage (V)
f = Frequency (Hz)
C_L = External load capacitance (F)

When comparing the dynamic power consumed between LV, LVC, ALVC and LVT, **Figure 1–6** shows that pure CMOS devices (the LV, LVC, and ALVC families) consume approximately the same power as BiCMOS devices (the LVT family) around the frequency of 10 MHz, but consume significantly less power as the frequency approaches 100 MHz.

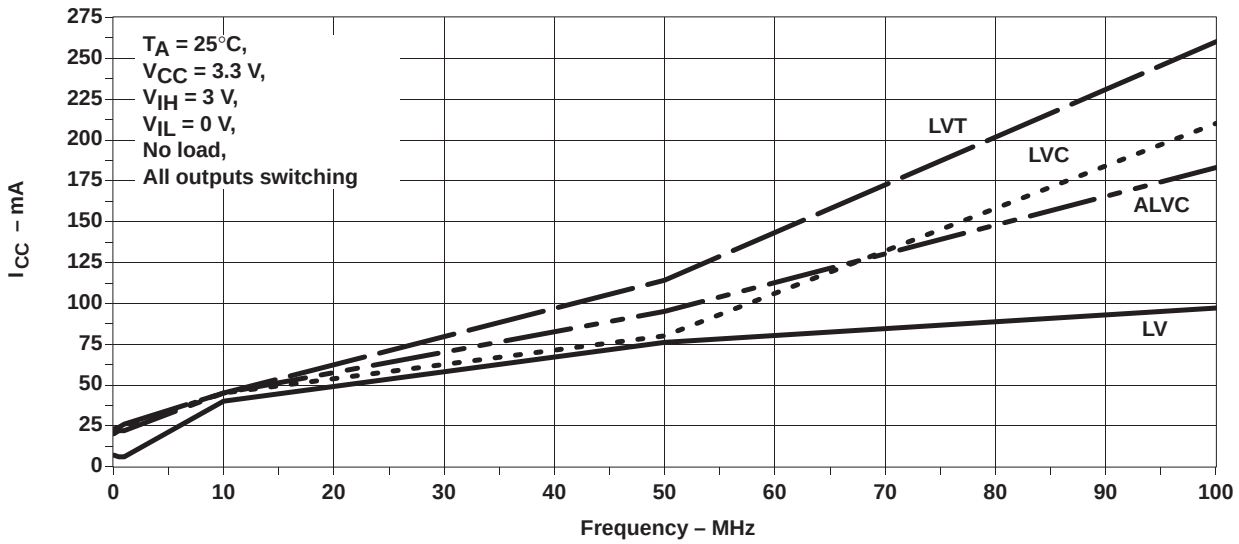


Figure 1–6. I_{CC} Versus Frequency

For an LVC device, the overall power consumed can be expressed by the following equation:

$$P_T = P_{(static)} + P_{(dynamic)} \quad \textbf{(3)}$$

Where:

for inputs with rail-to-rail signal swing:

$$P_S = V_{CC} \times I_{CC}$$
$$P_D = [\ (C_{pd} + C_L) \times V_{CC}{}^2 \times f\ ] \times N_{SW} \quad \textbf{(4)}$$

and for TTL-level inputs:

$$P_S = V_{CC}[\ I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\ ]$$
$$P_D = [\ (C_{pd} + C_L) \times V_{CC}{}^2 \times f\ ] \times N_{SW} \quad \textbf{(5)}$$

Where:
V_{CC} = Supply voltage (V)
I_{CC} = Power supply current (A)
C_{pd} = Power dissipation capacitance (F)
C_L = External load capacitance (F)
f = Operating frequency (Hz)
N_{SW} = Total number of outputs switching
N_{TTL} = Total number of outputs (where corresponding input is at the TTL level)
ΔI_{CC} = Power supply current (A) when inputs are at a TTL level
DC_d = % duty cycle of the data (50% = 0.5)

INPUT CHARACTERISTICS

The LVC family input structure is such that the 3.3-V CMOS dc V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V are ensured, meaning that while the threshold voltage of 1.5 V is typically where the transition from a recognized low input to a recognized high input occurs (see **Figure 1–7**), it is at the levels of 0.8 V and 2 V where the corresponding output state is ensured. Additionally, a reduction in overall bus loading exists in the LVC family due to the relatively high impedance and low capacitance characteristics of CMOS input circuitry.

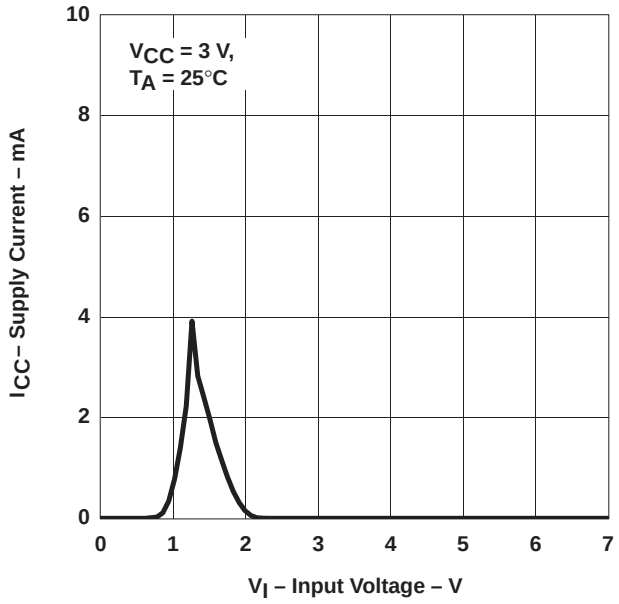


Figure 1–7. Supply Current Versus Input Voltage

LVC Input Circuitry

The simplified LVC input circuit shown in **Figure 1–8** consists of two transistors, sized to achieve a threshold voltage of 1.5 V (see **Figure 1–9**). Since V_{CC} is 3.3 V and the threshold voltage is commonly set to be centered around one-half of V_{CC} in a pure CMOS input (see **Figure 1–1**), additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage V_I is low, the PMOS transistor (Q_p) turns on and the NMOS transistor (Q_n) turns off, causing current to flow through Q_p, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when V_I is high, Q_n turns on and Q_p turns off, causing current to flow through Q_n, resulting in the output voltage (on the input stage) to be pulled low.

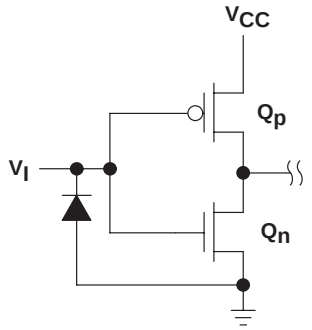


Figure 1–8. Simplified Input Stage of an LVC Circuit

Figure 1–9 is a graph of V_O versus V_I. An input hysteresis of approximately 100 mV is inherent to the LVC process geometry, which ensures the devices are free from oscillations by increasing the noise margin around the threshold voltage.

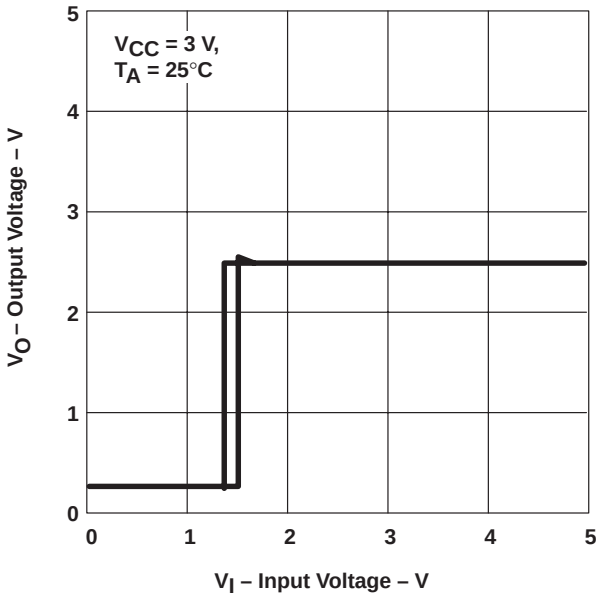


Figure 1–9. Output Voltage Versus Input Voltage

Figure 1–10 is a graph of I_I versus V_I. The inputs of all LVC devices are 5-V tolerant and have a recommended operating condition range from 0 V to 5.5 V. If the input voltage is within this range, the functionality of the device is ensured.

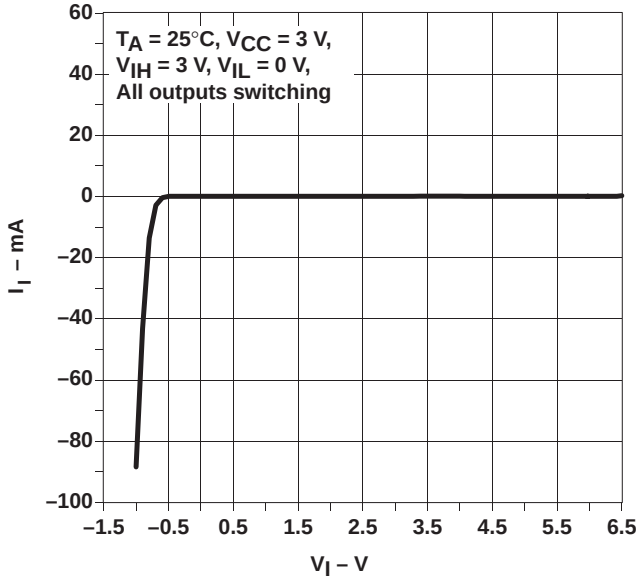


Figure 1–10. Input Current Versus Input Voltage

Input Current Loading

Minimal loading of the system bus occurs when using the LVC family due to the EPIC™ submicron process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 100 pA, as shown in **Figure 1–11** and **Table 1–1**. Capacitance for transceivers can be as low as 3.3 pF for C_i and 5.4 pF for C_{io}. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using LVC devices is minimal and, depending upon the logic family being used, bus loading can decrease as a result of using LVC parts.

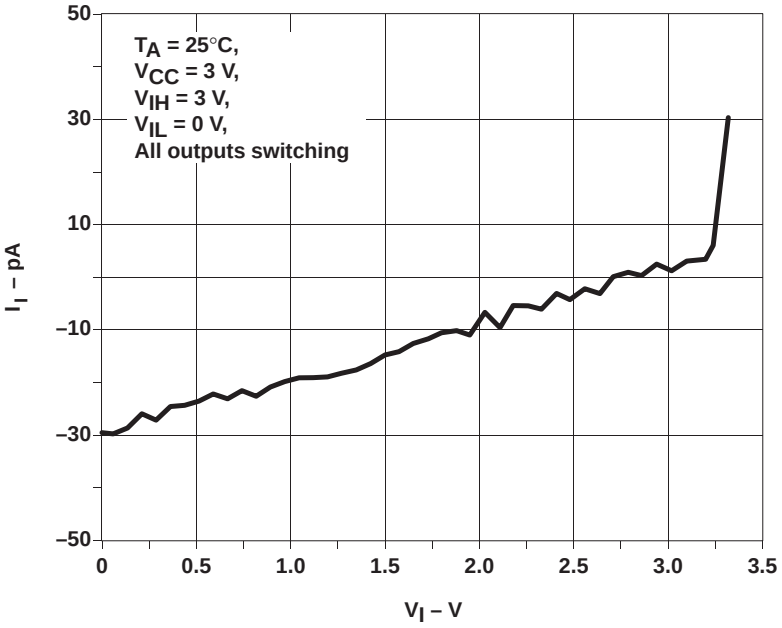


Figure 1–11. Input Leakage Current Versus Input Voltage

Table 1–1. Input Current Specifications

PARAMETER	TEST CONDITIONS		SN74LVC245A	
			MIN	MAX
I_I	V_I = 5.5 V or GND,	V_{CC} = 3.6 V		±5 µA
I_{OZ}†	V_O = V_{CC} or GND,	V_{CC} = MIN to MAX		±10 µA
I_{OZ}†	V_O = 3.6 V or 5.5 V,	V_{CC} = MIN to MAX		±50 µA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

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Supply Current Change (ΔI_{CC})

LVC devices operate using the switching standard levels shown in **Figure 1–1**. However, because the input circuitry is CMOS, an additional specification, ΔI_{CC}, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting. Although this situation exists whenever a low-to-high (or high-to-low) transition occurs, the transition usually occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the LVC part. Here, a dc voltage that is not at the rail, is applied to the input of the LVC device. The result is that both the n-channel transistor and the p-channel transistor are conducting and a path from V_{CC} to GND is established. This current is specified as ΔI_{CC} in the data sheet for each device and is measured one input at a time with the input voltage set at $V_{CC} - 0.6$ V, while all other inputs are at V_{CC} or GND. **Table 1–2** provides the ΔI_{CC} specification, which is contained in the data sheet for any LVC part.

Table 1–2. ΔI_{CC} Current Specifications

PARAMETER	TEST CONDITIONS			SN74LVC245A	
				MIN	MAX
ΔI_{CC}	One input at $V_{CC} - 0.6$ V,	Other inputs at V_{CC} or GND,	V_{CC} = 2.7 V to 3.6 V		500 µA

Proper Termination of Unused Inputs and Bus Hold

A characteristic of all CMOS input structures is that any unused inputs should not be left floating; they should be tied high to V_{CC} or low to GND via a resistor. The value of the resistor should be approximately 1kΩ. If the inputs are not tied high or low but are left floating, excessive output glitching or oscillations can result due to induced voltage transients on the parasitic lead inductance inherent to the device input and output structure.

Implementation of the bus-hold feature on select devices is a recent enhancement to the LVC logic family. Bus hold eliminates the need for floating inputs to be tied high or low by holding the last known state of the input until the next input signal is present. Bus hold is a circuit composed of two back-to-back inverters with the output fed to the input via a resistor. **Figure 1–12** is a simplified illustration of the bus-hold circuit. **Figure 1–13** shows $I_{I(hold)}$ as V_I is swept from 0 to 4 V. Bus hold is beneficial because of the decreased expense of purchasing additional resistors, reduced overall power consumption, and because it frees up limited board space.

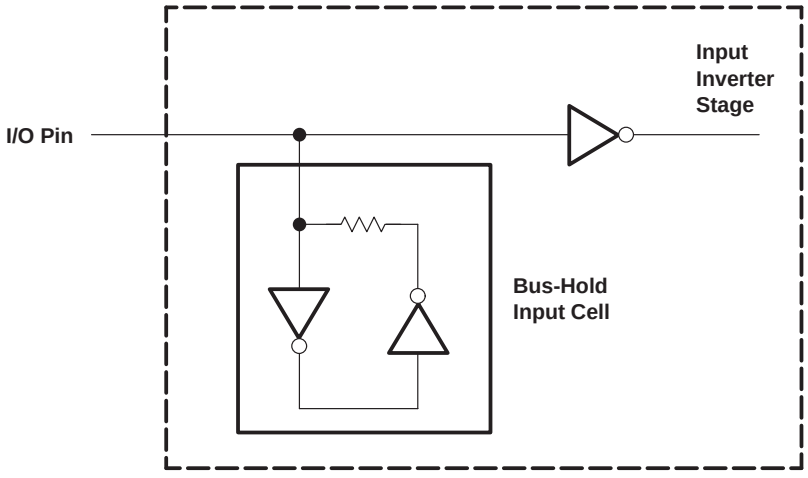


Figure 1–12. Bus Hold

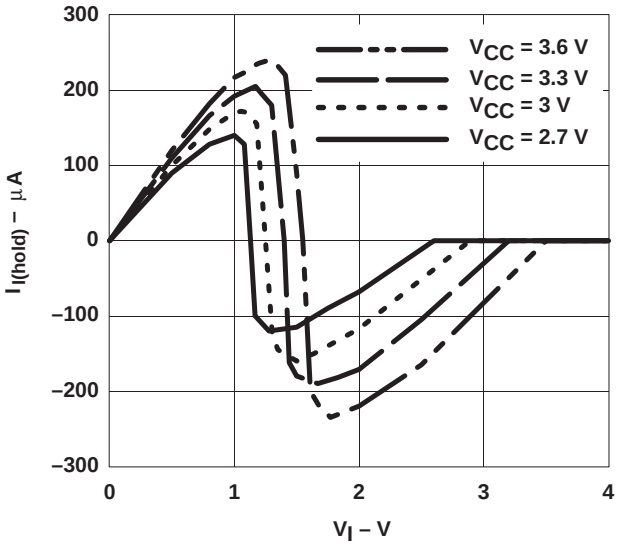


Figure 1–13. $I_{I(hold)}$ Versus V_I

Not all LVC devices have the bus-hold feature. Those that do are identified by the letter H added to the device name; e.g., SN74LVCH245. Additionally, any device with bus hold has an $I_{I(hold)}$ specification in the data sheet. Finally, bus hold does not contribute significantly to input current loading or output driving loading because it has a minimum hold current of 75 μA and a maximum hold current of 500 μA as shown in **Table 1–3**.

Table 1–3. Bus-Hold Specifications [$I_{I(hold)}$]

PARAMETER	TEST CONDITIONS		SN74LVC245	
			MIN	MAX
$\Delta I_{I(hold)}$	V_I = 0.8 V,	V_{CC} = 3 V	75 μA	
	V_I = 2 V,	V_{CC} = 3 V	–75 μA	
	V_I = 0 to 3.6 V,	V_{CC} = 3.6 V		±500 μA

OUTPUT CHARACTERISTICS

The LVC family uses a pure CMOS output structure. This is true of all low-voltage families except the LVT family, which uses both bipolar and CMOS circuitry. The LVC family has the dc characteristics shown in **Table 1–4**.

Table 1–4. LVC Output Specifications

PARAMETER	TEST CONDITIONS		SN74LVC244A		
			MIN	TYP	MAX
V_{OH}	I_{OH} = –100 µA,	V_{CC} = MIN to MAX	V_{CC} – 0.2 V		
	I_{OH} = –12 mA,	V_{CC} = 2.7 V	2.2 V		
	I_{OH} = –12 mA,	V_{CC} = 3 V	2.4 V		
	I_{OH} = –24 mA,	V_{CC} = 3 V	2.2 V		
V_{OL}	I_{OL} = 100 µA,	V_{CC} = MIN to MAX			0.2 V
	I_{OL} = 12 mA,	V_{CC} = 2.7 V			0.4 V
	I_{OL} = 24 mA,	V_{CC} = 3 V			0.55 V
I_{OZ}†	V_O = V_{CC} or GND,	V_{CC} = MIN to MAX			±10 µA
I_{OZ}†	V_O = 3.6 V to 5.5 V,	V_{CC} = MIN to MAX			±50 µA
C_o	V_O = V_{CC} or GND,	V_{CC} = 3.3 V		5 pF	

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

LVC Output Circuitry

Figure 1–14 shows a simplified output stage of an LVC circuit. When the NMOS transistor (Q_n) turns off and the PMOS transistor (Q_p) turns on and begins to conduct, the output voltage (V_O) is pulled high. Conversely, when Q_p turns off, Q_n begins to conduct and V_O is pulled low.

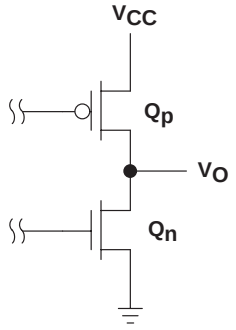


Figure 1–14. Simplified Output Stage of an LVC Circuit

Output Drive

Figure 1–15 illustrates values of I_{OL} and I_{OH} and the corresponding values of V_{OL} and V_{OH} for a typical LVC device.

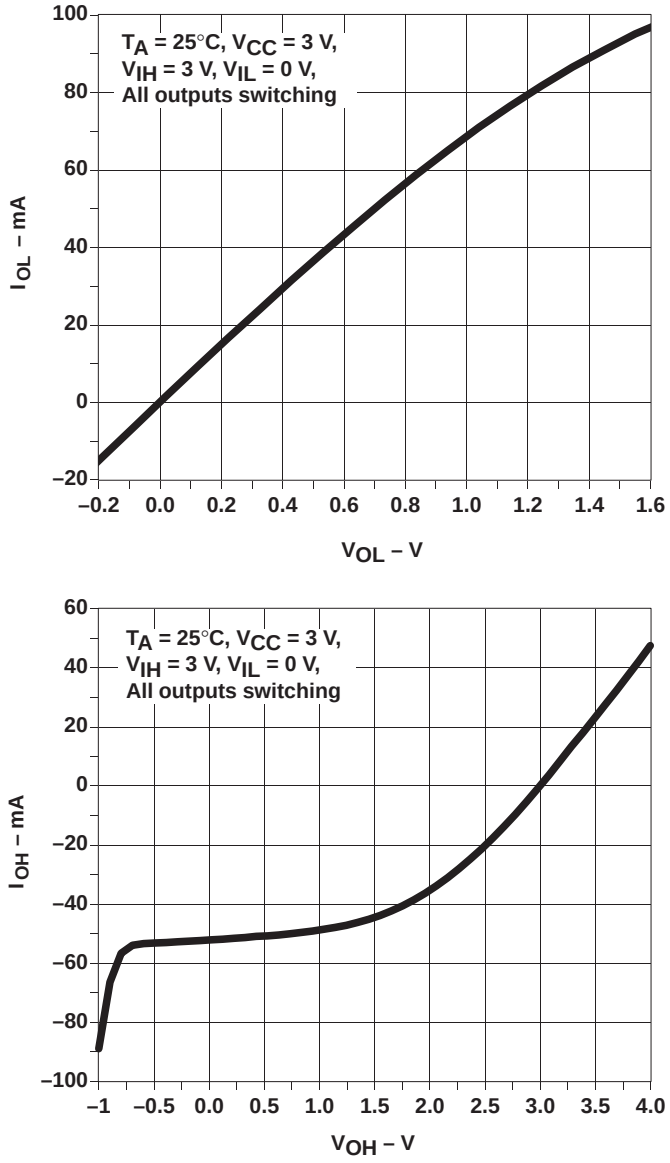


Figure 1–15. Typical LVC Output Characteristics

Partial Power Down

To partially power down a device, no paths from V_I to V_{CC} or from V_O to V_{CC} can exist. With the LVC family, a path from V_I to V_{CC} has never been an issue. However, early LVC devices that were not 5-V tolerant do have a path from V_O to V_{CC}. For these devices, when V_{CC} begins to diminish, a diode from V_O to V_{CC} begins to conduct and current flows, resulting in damage to the power supply and or to the device. Today, the 5-V tolerant LVC devices are designed in such a way that this path from V_O to V_{CC} is eliminated. As such, 5-V tolerant devices are capable of being partially powered down.

Proper Termination of Outputs

Depending on the trace length, special consideration may need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system may appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

Figure 1–16 illustrates five different techniques for terminating the outputs. The ideal situation is to identically match the impedance (Z_O) of the trace and eliminate all reflections. In practice, however, exactly matching Z_O is not always possible and settling for a close enough match that adequately minimizes the reflections may be the only option.

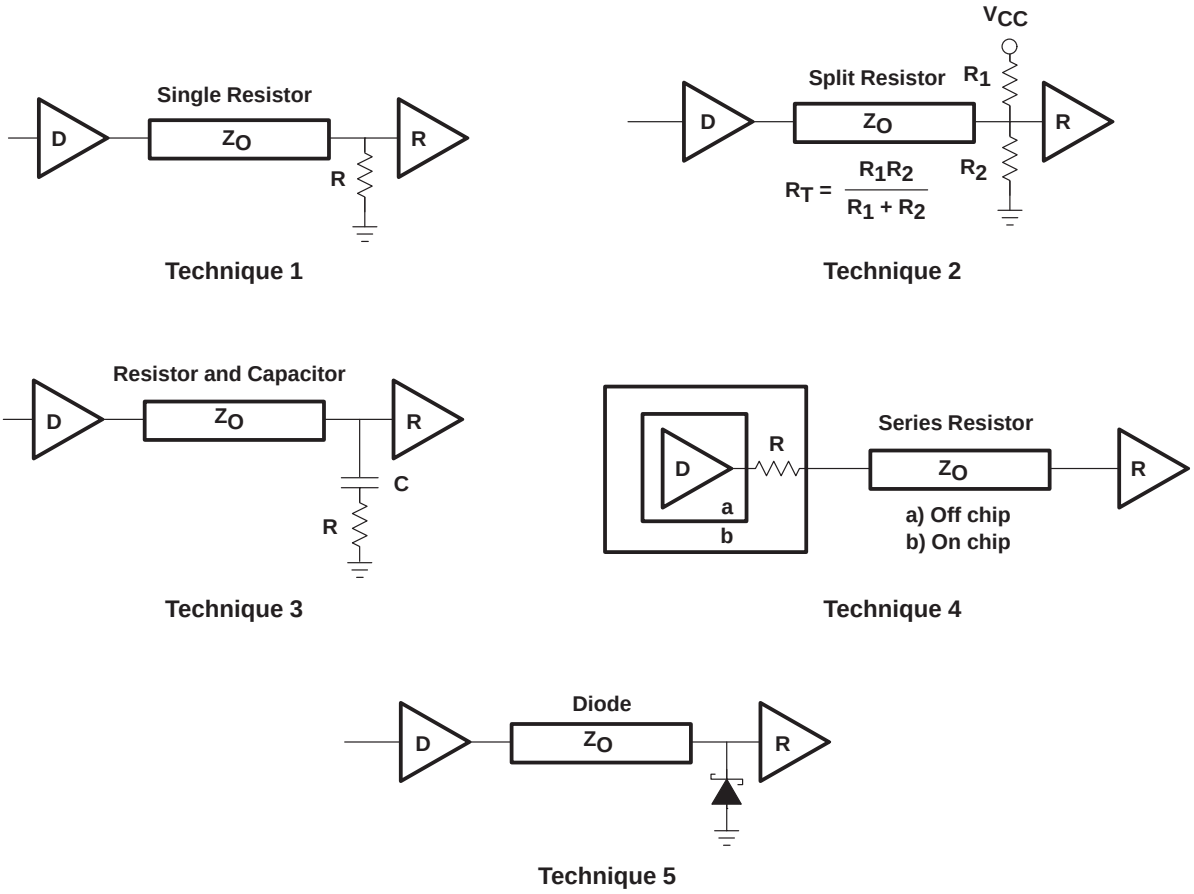


Figure 1–16. Termination Techniques

Technique 1

Technique 1 consists of a single resistor tied to GND. The ideal value of the resistor is $R = Z_O$, and the best placement for it is as close to the receiver as possible. A heavy increase in power occurs, but no further delay is present. There is a relatively low dc noise margin in this configuration.

Technique 2

Technique 2 involves two split resistors; one resistor (R_1) is tied to V_{CC} and the other (R_2) is tied to GND. The ideal value of the resistors is $R_1 = R_2 = 2Z_O$; $RT = (R_1 \times R_2)/(R_1 + R_2)$, and the best placement for the resistors is as close to the receiver as possible. Technique 2 results in a heavy increase in power, with no delay being experienced, and is primarily used in backplane designs where proper drive currents must be maintained.

Technique 3

Technique 3 has a capacitor in series with a resistor, both of which are running parallel to GND. The ideal value of the resistor is $R = Z_O$, and the value of the capacitor should be $60pF < C < 330$ pF. To determine the ideal value of the capacitor, it is recommended that a model simulation tool be used. The ideal placement of the resistor and capacitor is as close to the receiver as possible. Technique 3 has the highest amount of power consumed as the frequency increases, but no additional delay is experienced. Note that this termination technique can be optimized for only one given signal frequency.

Technique 4

Technique 4 consists of a resistor in series with the output of the driving device and can be divided into two alternatives, depending on whether the resistor is physically located on or off the driving device. If the resistor is not located on the device, the value of the resistor should be $R = Z_O - Z_D$, where Z_D is the output impedance of the driver, and the best placement is as close to the driver as possible. Although a delay occurs, no power increase is experienced and this technique has a relatively good noise margin. If the resistor is integrated on the device and part of the chip, its value is usually $25 =< R =< 33\ \Omega$. This setup has a slight delay, has no increase in power, has good undershoot clamping, and is useful for point-to-point driving.

Technique 5

Technique 5 consists of a diode to GND that should be located as close as possible to the receiver. An increase in power is not experienced, no delay occurs, and this configuration is useful for standard backplane terminations.

Technique 5 is the most attractive of all techniques since there is no power increase and no delay occurs. However, since the delay associated with Technique 4 is so minimal and since no additional devices are required, whereas in all the other techniques at least one additional component is required, Technique 4 is usually the technique recommended by the Advanced System Logic department of Texas Instruments.

These five techniques, together with their advantages and disadvantages, are summarized in **Table 1–5**.

Table 1–5. Termination Techniques Summary

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	SETS STATIC LINE LEVEL	DELAY	IDEAL VALUE	COMMENTS
Single resistor	1	Significant	Yes	No	$R = Z_O$	Low dc noise margin
Split resistor	2	Significant	Yes	No	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
Resistor and capacitor	2	Yes	No	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series resistor-off device	1	No	No	Yes	$R = Z_O - Z_D$	Good noise margin
Series resistor-on device	0	No	No	Small	$25 = < R = < 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

SIGNAL INTEGRITY

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

Simultaneous Switching

The phenomenon of simultaneous switching can be measured with respect to GND or with respect to V_{CC}. When measuring with respect to GND, the voltage output low peak (V_{OLP}) is the impact on one quiet, logic-low output when all the other outputs are switched from high to low. The converse is true when measuring simultaneous switching with respect to V_{CC}; i.e., the voltage output high valley (V_{OHV}) is the impact on one quiet, logic-high output when all the other outputs are switched from low to high. **Figure 1–17** shows an example of simultaneous switching with respect to V_{OLP} and V_{OHV}.

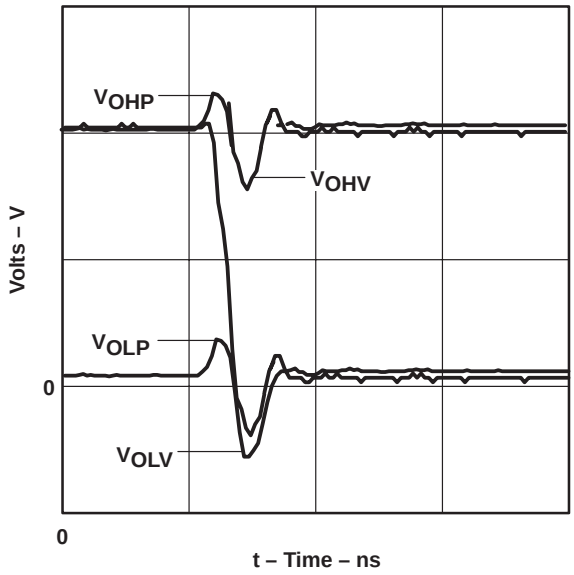


Figure 1–17. Simultaneous Switching Noise Waveform

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip to reduce mutual inductances between signals (see *Advanced Packaging* in this section). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing* application report or the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001A.

Acknowledgements

This section was written by Steven Culp, ABL applications engineering.

SECTION 2
LVC COMPARISON TO OTHER LOW-VOLTAGE LOGIC FAMILIES

List of Illustrations

List of Illustrations (continued)

List of Tables

INTRODUCTION

This section provides a data analysis of TI LVC, Fairchild (FCLD) [recently changed from National Semiconductor Corporation (NSC)] and Motorola (MOT) low-voltage CMOS with translation (LCX), and Integrated Device Technology (IDT) fast CMOS technology (FCT3) C grade logic families. The analysis is performed on typical data, which is measured in a laboratory. Application insight is provided as to the relative importance and practicality of the data from an engineering perspective.

Laboratory Testing Techniques

When selecting devices for the following experiments, devices that exhibited typical performance characteristics were chosen; these devices were then subjected to identical testing conditions. Unless otherwise noted, all tests were set up and conducted assuming normal data sheet parameters, i.e., standard loads, typical V_{CC} levels, and normal operating temperature. When appropriate, testing specifics are provided in the top left portion of the graphs.

PROPAGATION-DELAY TIME VERSUS LOAD CAPACITANCE VERSUS NUMBER OF OUTPUTS SWITCHING

Propagation-delay time is an important parameter because it is a direct indication of the speed of the device. As technology evolves, the general trend is for devices to become faster and propagation-delay time can be a primary parameter in determining whether or not a given logic family is suitable for a particular application.

The LVC, LCX, and FCT3 logic families are medium-speed families. While other logic families are available from TI and others that have faster performance times, speed is almost always an important consideration when using the LVC, LCX, and FCT3 families. Performing within the specifications provided in the data sheets is crucial and, depending on the particular application, typical values for propagation delay may also be important.

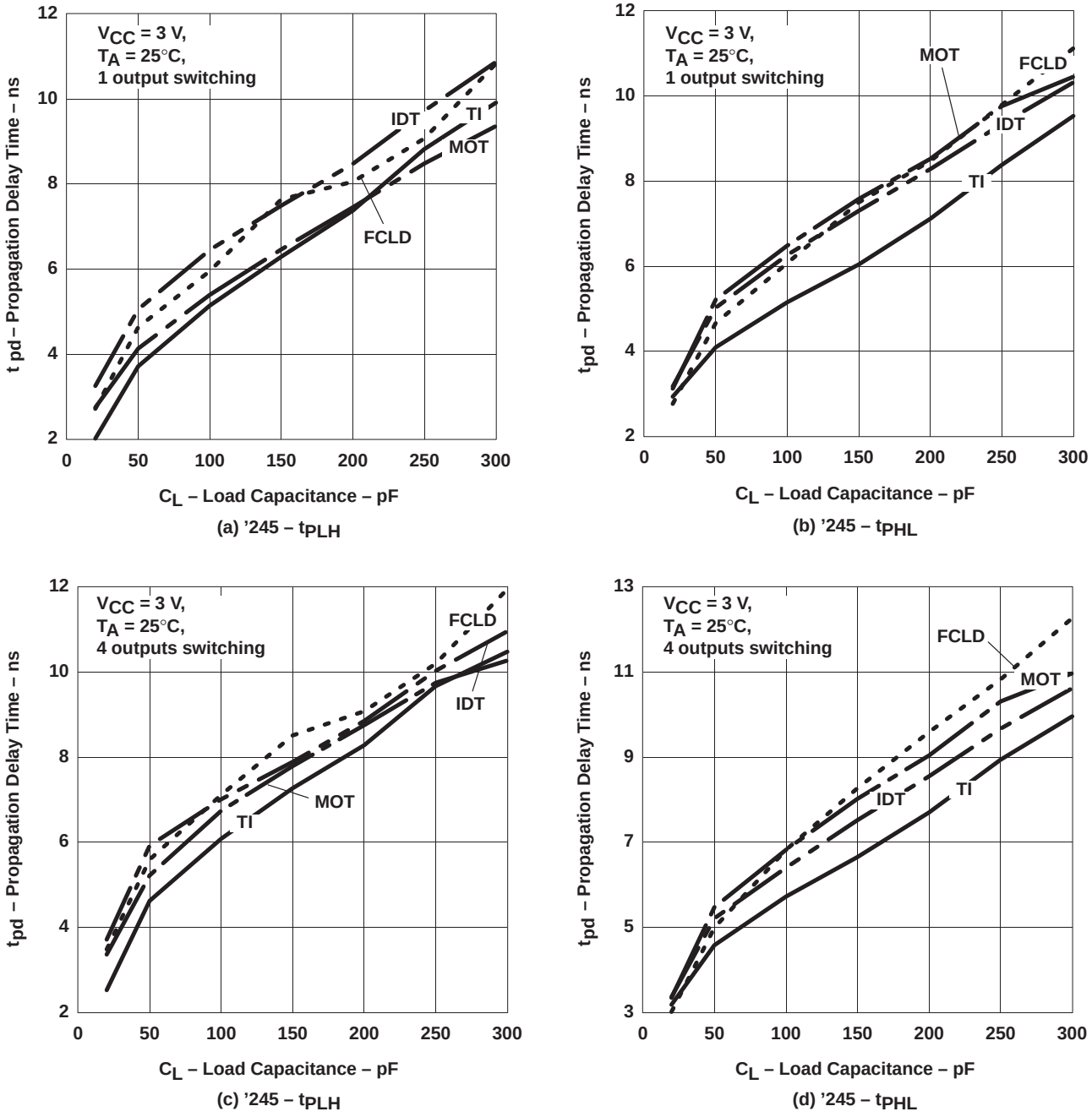
Figure 2–1 shows propagation-delay time versus load capacitance for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Separate graphs are provided for a single output switching, four outputs switching, and eight outputs switching. Additionally, a distinction is made between whether the output is switching from a low-to-high state or from a high-to-low state.

Looking at the raw numbers in the graphs, it is readily seen that TI's LVC245 is almost always faster than the other devices. The difference in speeds is usually very small at 20 pF and becomes rather noticeable at higher loading levels. The standard test load for most applications in which the LVC, LCX, and FCT3 families may be used is 50 pF, but they are also commonly used in systems that required up to 100-pF loading requirements. As shown in **Figures 2–1 and 2–2**, for those applications that require driving loads up to and beyond 100 pF, TI LVC devices are better suited than the other devices because, as a general rule, the TI devices have noticeably lower propagation-delay times, both at the lower loads and at the higher loads.

Figures 2–3 and 2–4 contain propagation-delay time versus load capacitance for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for a single output switching, four outputs switching, eight outputs switching, and 16 outputs switching. Additionally, a distinction is made between whether the output is switching from a low-to-high state or from a high-to-low state.

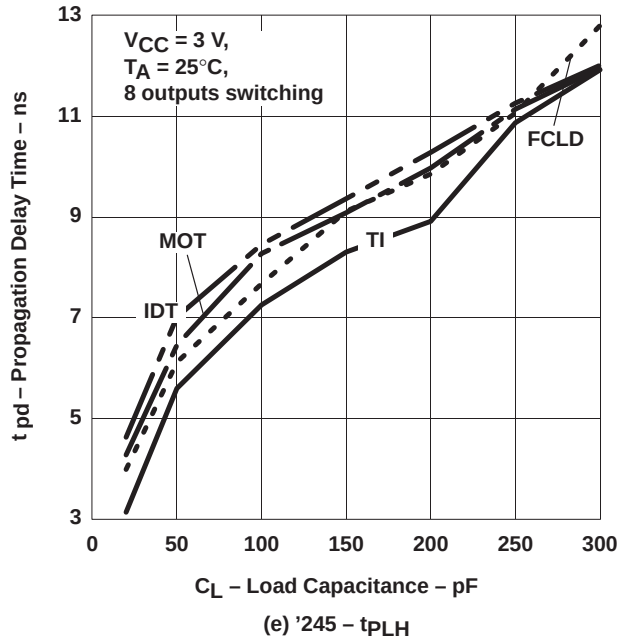
Looking at the raw numbers in the graphs in **Figures 2–3 and 2–4**, some differences are observed from the graphs in **Figures 2–1 and 2–2**. In all four cases (one, four, eight, and 16 outputs switching), TI's LVC16245 is fastest on the high-to-low transition and the slowest on the low-to-high transition. This difference, however, is largely academic; from a practical point of view, the differences in speed between load levels less than 100 pF are negligible. Most typical LVC applications employ load levels less than 100 pF; using the LVT logic family is suggested for higher loads.

Tables 2–1 through 2–7 contain equations for the lines illustrated in **Figures 2–1 through 2–4**. By using these equations, an exact, typical propagation-delay value can be computed for a specific load capacitance. The equations are provided in $y = mx + b$ format, where y is the propagation delay, m is the slope, and b is the y-intercept. All values are given in nanoseconds.

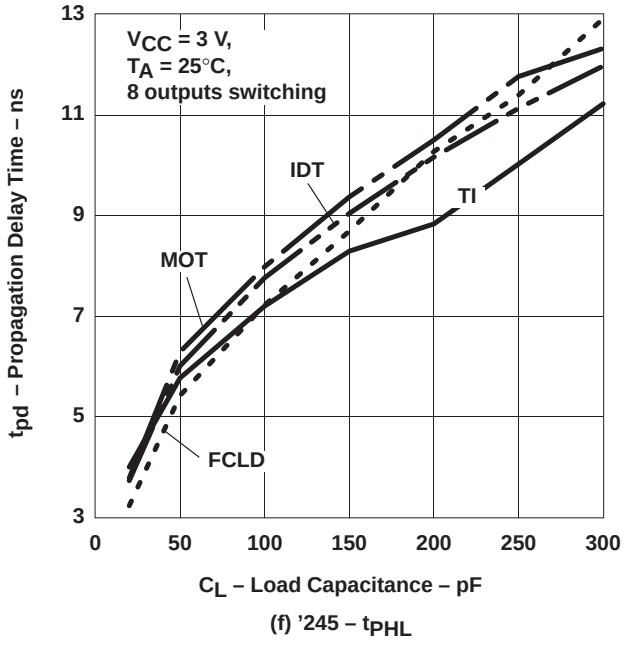


MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–1. ’245 Propagation-Delay Time Versus Load Capacitance



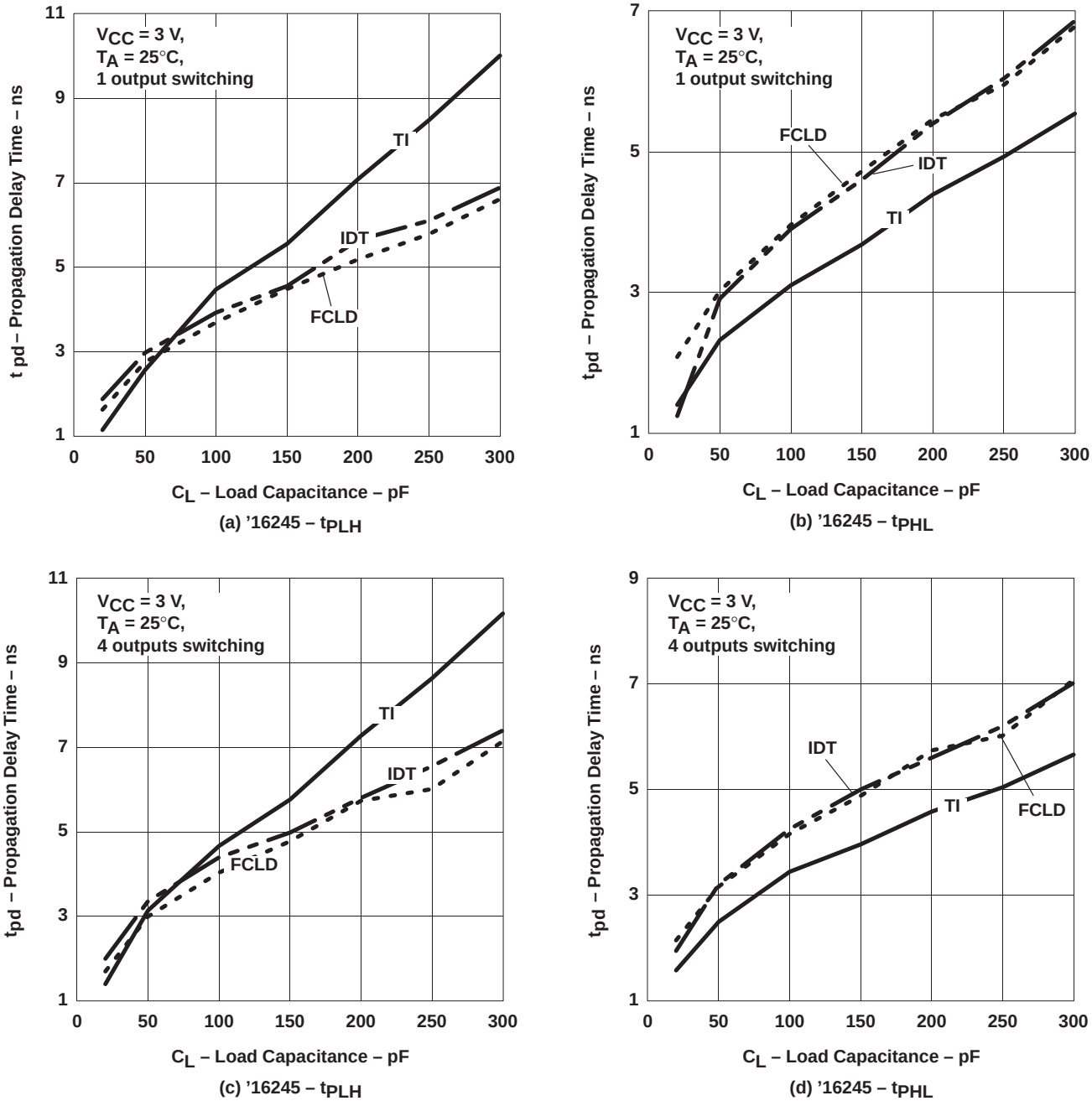
(e) ’245 – t_{PLH}



(f) ’245 – t_{PHL}

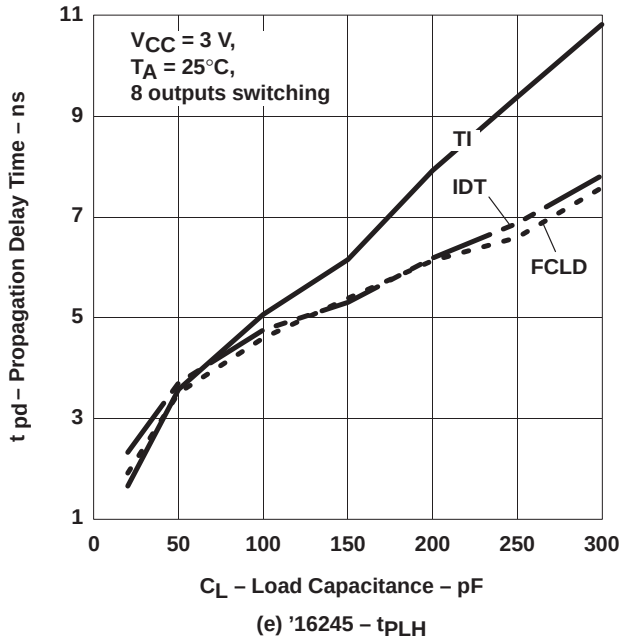
MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–1. ’245 Propagation-Delay Time Versus Load Capacitance (Continued)

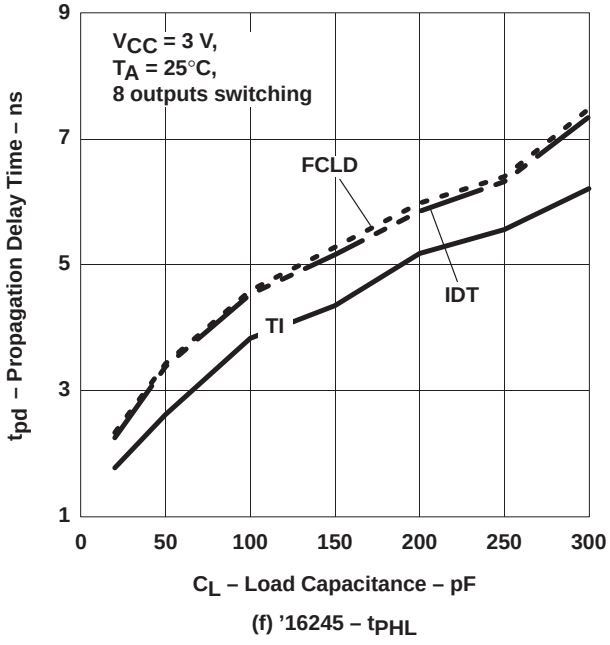


MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

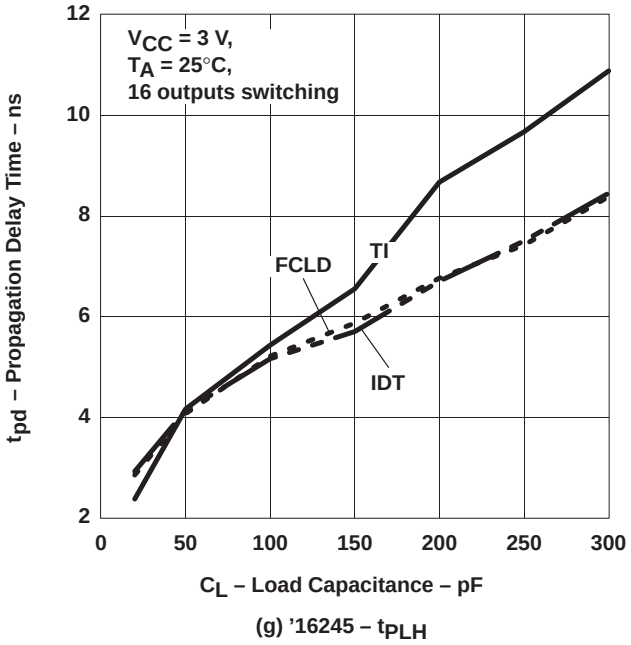
Figure 2–2. ’16245 Propagation-Delay Time Versus Load Capacitance



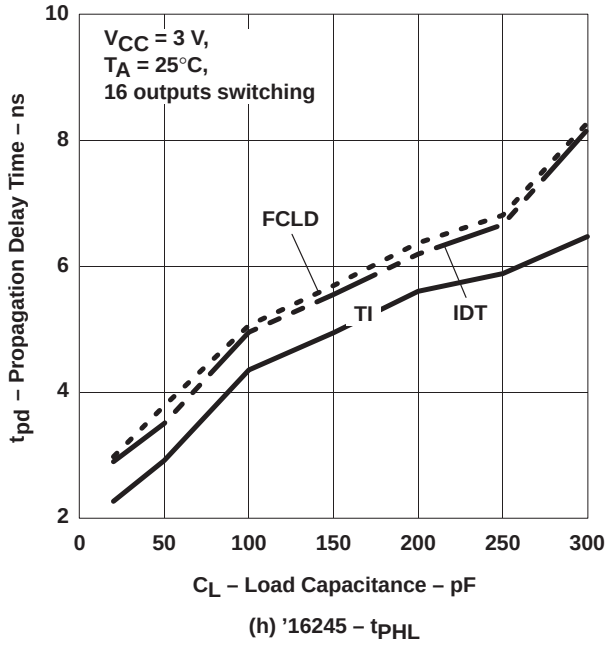
(e) ’16245 – t_{PLH}



(f) ’16245 – t_{PHL}



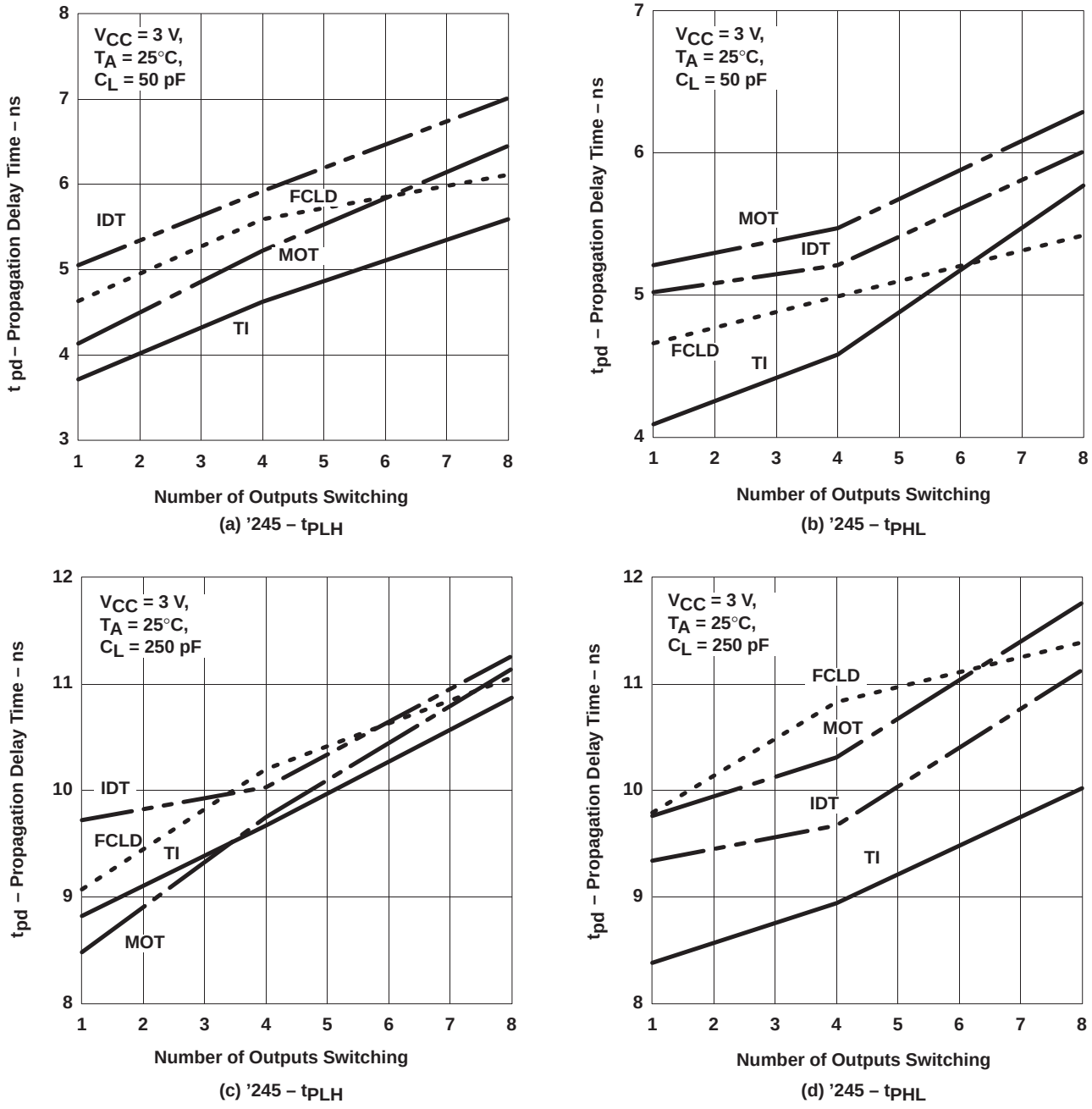
(g) ’16245 – t_{PLH}



(h) ’16245 – t_{PHL}

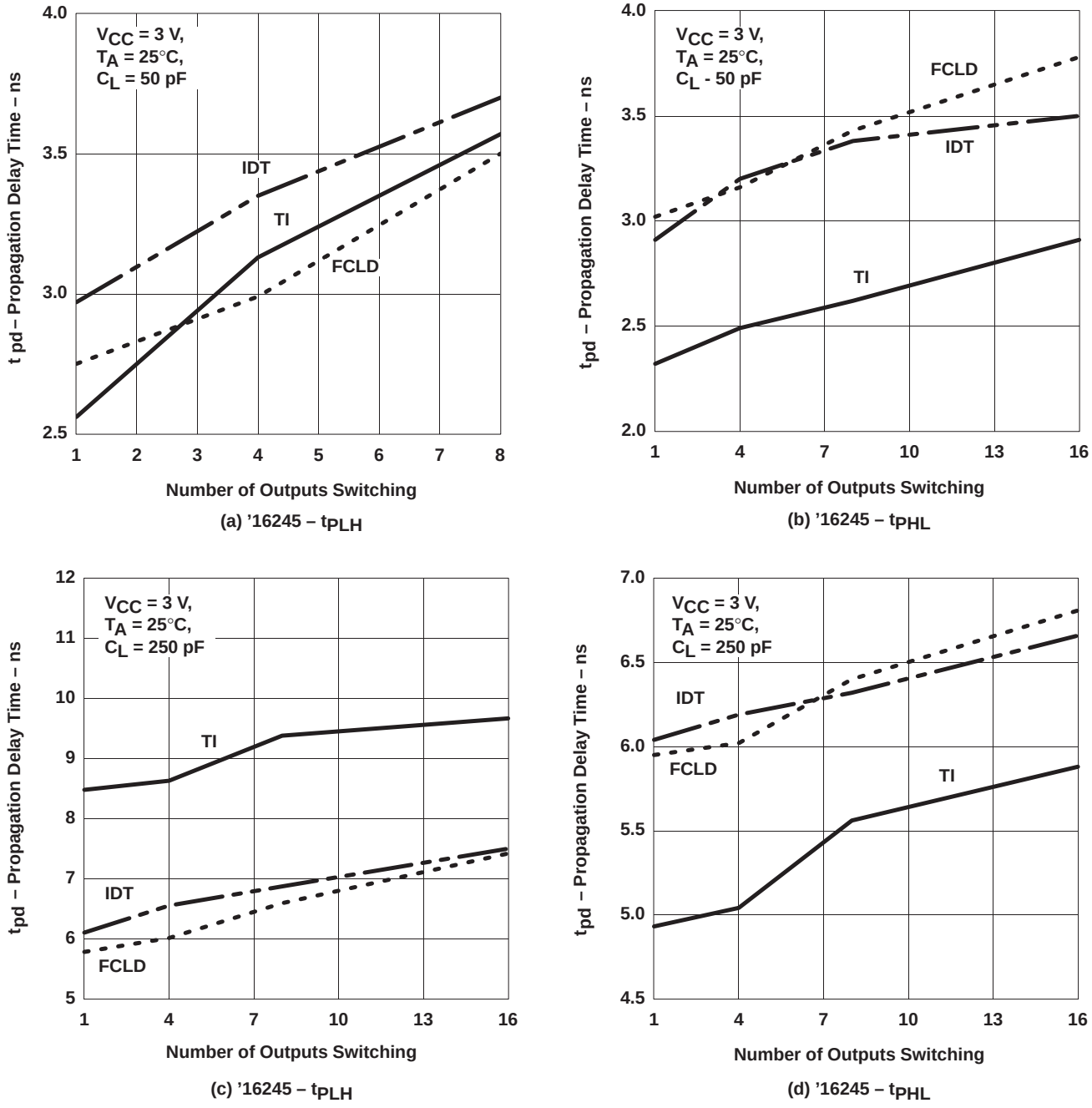
MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–2. ’16245 Propagation-Delay Time Versus Load Capacitance (Continued)



MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–3. '245 Propagation-Delay Time Versus Number of Outputs Switching



MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–4. ’16245 Propagation-Delay Time Versus Number of Outputs Switching

Table 2–1. Propagation-Delay Line Equations for TI LVC245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
LVC245	1 output switching,	Low-to-high transition	$t_{pd} = (0.0248) \times C_L + 2.47$
LVC245	1 output switching,	High-to-low transition	$t_{pd} = (0.02176) \times C_L + 3.0$
LVC245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.02344) \times C_L + 3.448$
LVC245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.02152) \times C_L + 3.504$
LVC245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.02532) \times C_L + 4.324$
LVC245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.0218) \times C_L + 4.68$

Table 2–2. Propagation-Delay Line Equations for FCLD LCX245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
LCX245	1 output switching,	Low-to-high transition	$t_{pd} = (0.0248) \times C_L + 3.39$
LCX245	1 output switching,	High-to-low transition	$t_{pd} = (0.02584) \times C_L + 3.368$
LCX245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.02544) \times C_L + 4.318$
LCX245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.02912) \times C_L + 3.534$
LCX245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.02676) \times C_L + 4.772$
LCX245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.02996) \times C_L + 3.922$

Table 2–3. Propagation-Delay Line Equations for IDT FCT3245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
FCT3245	1 output switching,	Low-to-high transition	$t_{pd} = (0.02328) \times C_L + 3.886$
FCT3245	1 output switching,	High-to-low transition	$t_{pd} = (0.0212) \times C_L + 3.96$
FCT3245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.02016) \times C_L + 4.912$
FCT3245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.02164) \times C_L + 4.128$
FCT3245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.02) \times C_L + 6.01$
FCT3245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.02384) \times C_L + 4.818$

Table 2–4. Propagation-Delay Line Equations for Motorola LCX245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
LCX245	1 output switching,	Low-to-high transition	$t_{pd} = (0.03516) \times C_L + 2.892$
LCX245	1 output switching,	High-to-low transition	$t_{pd} = (0.03048) \times C_L + 3.106$
LCX245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.0314) \times C_L + 3.54$
LCX245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.03052) \times C_L + 3.364$
LCX245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.02888) \times C_L + 4.286$
LCX245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.02936) \times C_L + 4.352$

Table 2–5. Propagation-Delay Line Equations for TI LVC16245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
LVC16245	1 output switching,	Low-to-high transition	$t_{pd} = (0.0298) \times C_L + 1.07$
LVC16245	1 output switching,	High-to-low transition	$t_{pd} = (0.01288) \times C_L + 1.676$
LVC16245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.02816) \times C_L + 1.722$
LVC16245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.01268) \times C_L + 1.856$
LVC16245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.029) \times C_L + 2.12$
LVC16245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.01436) \times C_L + 1.902$
LVC16245	16 outputs switching,	Low-to-high transition	$t_{pd} = (0.02688) \times C_L + 2.816$
LVC16245	16 outputs switching,	High-to-low transition	$t_{pd} = (0.01424) \times C_L + 2.198$

Table 2–6. Propagation-Delay Line Equations for FCLD LCX16245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
LCX16245	1 output switching,	Low-to-high transition	$t_{pd} = (0.01544) \times C_L + 1.978$
LCX16245	1 output switching,	High-to-low transition	$t_{pd} = (0.01504) \times C_L + 2.268$
LCX16245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.0166) \times C_L + 2.16$
LCX16245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.01568) \times C_L + 2.376$
LCX16245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.01632) \times C_L + 2.684$
LCX16245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.0162) \times C_L + 2.62$
LCX16245	16 outputs switching,	Low-to-high transition	$t_{pd} = (0.01724) \times C_L + 3.208$
LCX16245	16 outputs switching,	High-to-low transition	$t_{pd} = (0.018) \times C_L + 2.88$

Table 2–7. Propagation-Delay Line Equations for IDT FCT163245 Devices

DEVICE	TEST CONDITIONS		LINE EQUATION
FCT163245	1 output switching,	Low-to-high transition	$t_{pd} = (0.0156) \times C_L + 2.188$
FCT163245	1 output switching,	High-to-low transition	$t_{pd} = (0.0158) \times C_L + 2.12$
FCT163245	4 outputs switching,	Low-to-high transition	$t_{pd} = (0.0162) \times C_L + 2.54$
FCT163245	4 outputs switching,	High-to-low transition	$t_{pd} = (0.01528) \times C_L + 2.436$
FCT163245	8 outputs switching,	Low-to-high transition	$t_{pd} = (0.01648) \times C_L + 2.876$
FCT163245	8 outputs switching,	High-to-low transition	$t_{pd} = (0.01588) \times C_L + 2.586$
FCT163245	16 outputs switching,	Low-to-high transition	$t_{pd} = (0.01728) \times C_L + 3.266$
FCT163245	16 outputs switching,	High-to-low transition	$t_{pd} = (0.01868) \times C_L + 2.566$

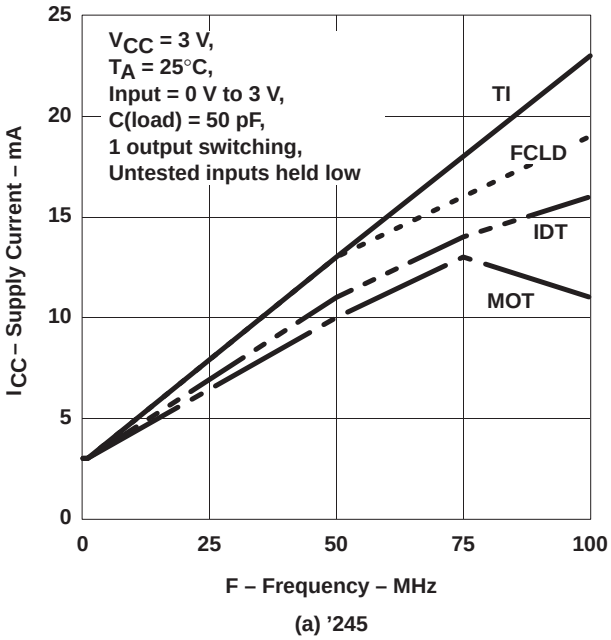
SUPPLY CURRENT VERSUS FREQUENCY

Supply current is critical because it is an indication of the amount of power consumed by the device. A small value for I_{CC} is desirable because reducing the amount of power consumed yields a host of benefits. Less power being consumed means less heat is generated and the problems of dissipating the heat are reduced. The reliability of a system also is enhanced as lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise.

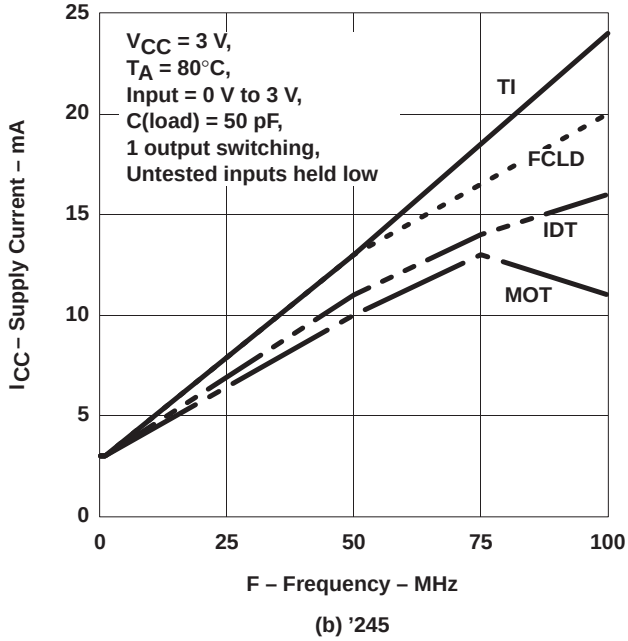
Figure 2–5 illustrates I_{CC} versus frequency data for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Additionally, a distinction is made between data taken at 25°C and 80°C.

Values of I_{CC} are basically identical between the families at values less than or equal to 50 MHz and all values remained relatively constant, regardless of the temperature. At frequencies greater than 50 MHz, a difference exists among the vendors in the values of I_{CC}, however, the difference is not significant. An explanation for graphs (a) and (b) in **Figure 2–5** is relevant, because although it appears that at frequencies higher than 50 MHz the FCLD LCX245 device draws less current, in actuality the FCLD device is beginning to break down, meaning that the output voltage is shrinking and making it appear that less current is flowing. Conversely, the TI part appears to draw more current, but it remains operational. In a similar fashion, the Motorola LCX245 device begins to break down at 100 MHz in graphs (a) and (b) and at 50 MHz in graphs (c) and (d), and the IDT FCT3245 device begins to break down at 100 MHz in graphs (c) and (d). As a general rule, the LVC, LCX, and FCT3 logic families are typically used at a frequency of 50 MHz or less and the values of I_{CC} at these frequencies are identical.

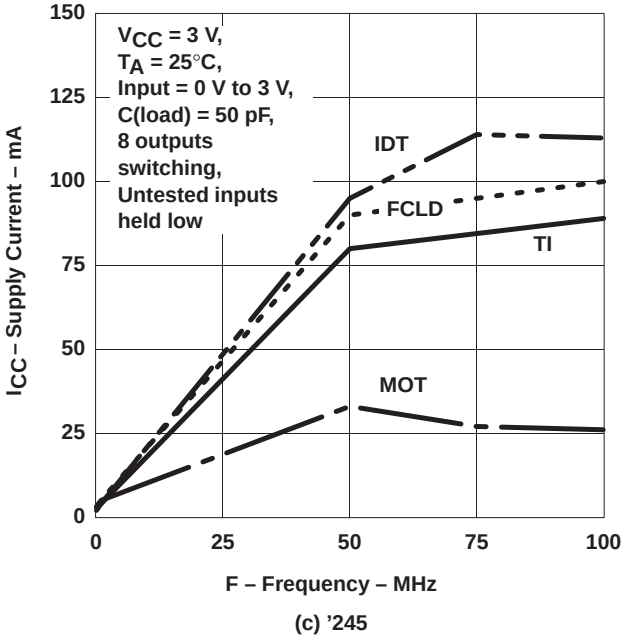
Figure 2–6 illustrates I_{CC} versus frequency data for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Additionally, a distinction is made between data taken at 25°C and 80°C.



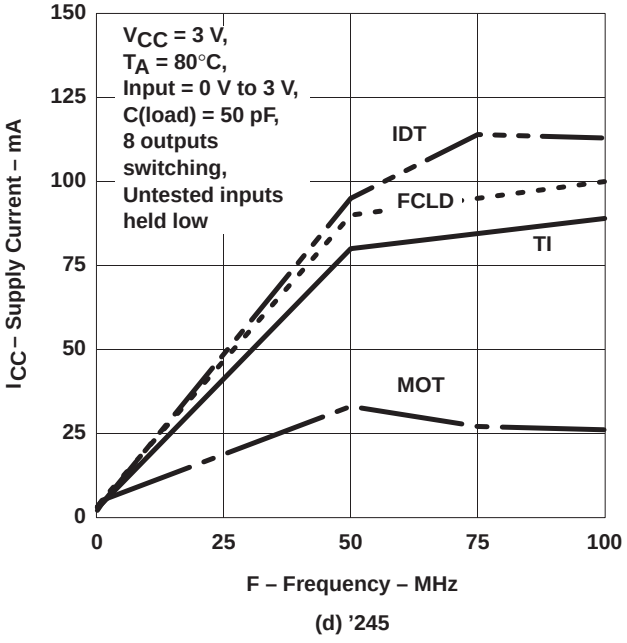
(a) ’245



(b) ’245



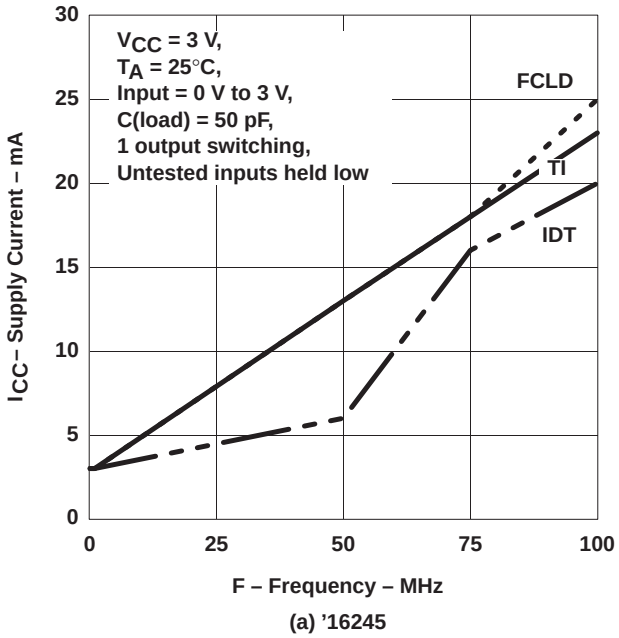
(c) ’245



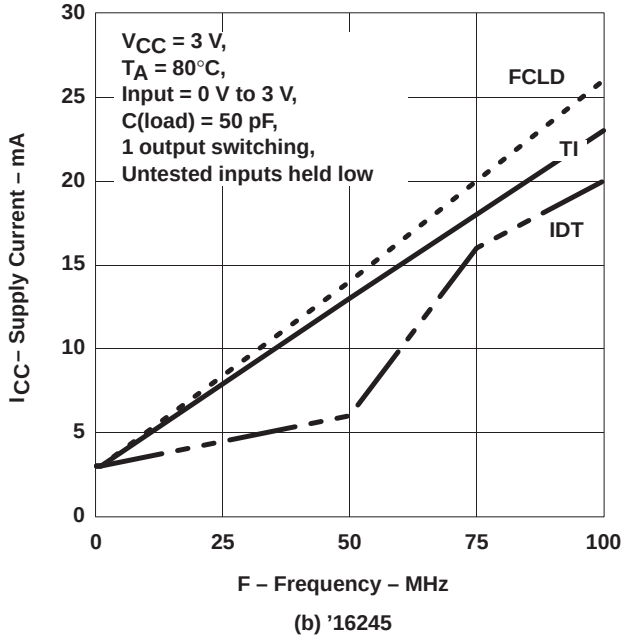
(d) ’245

MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

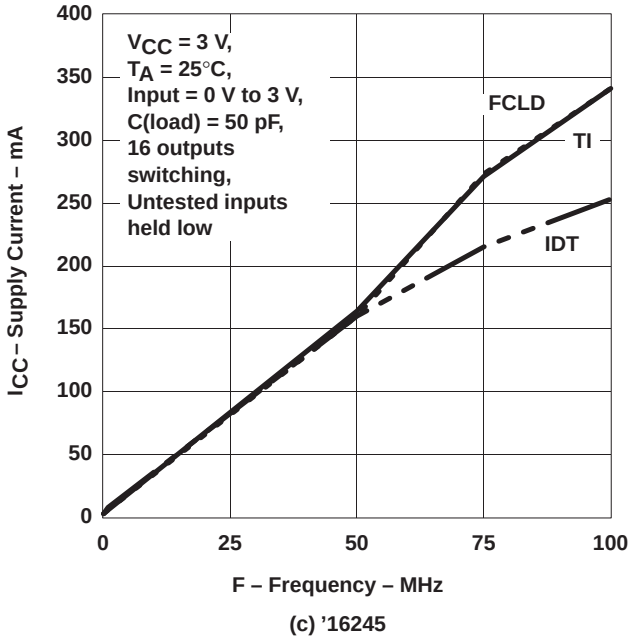
Figure 2–5. ’245 I_{CC} Versus Frequency



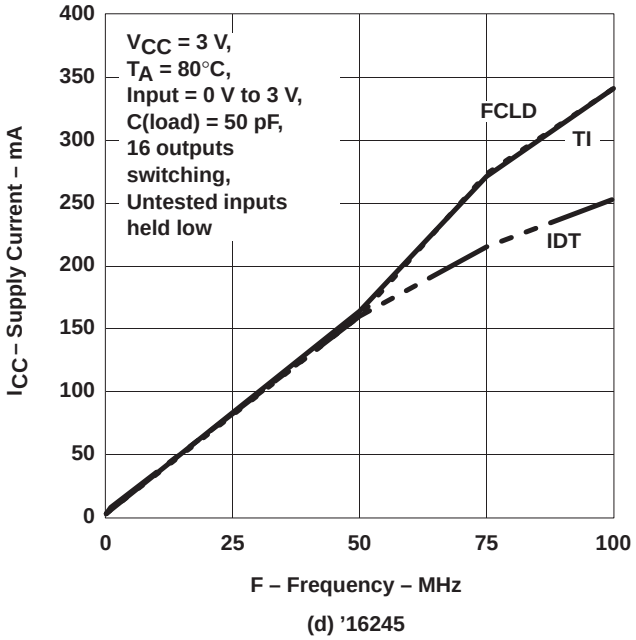
(a) ’16245



(b) ’16245



(c) ’16245



(d) ’16245

MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

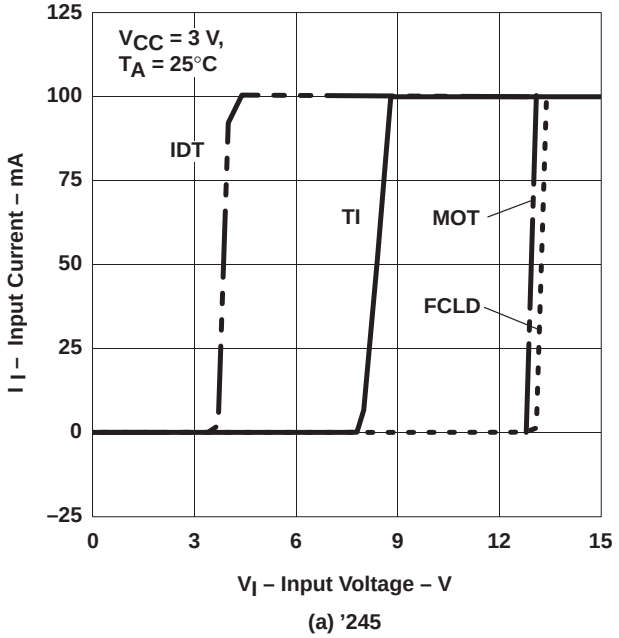
Figure 2–6. ’16245 I_{CC} Versus Frequency

MAXIMUM INPUT/OUTPUT VOLTAGE

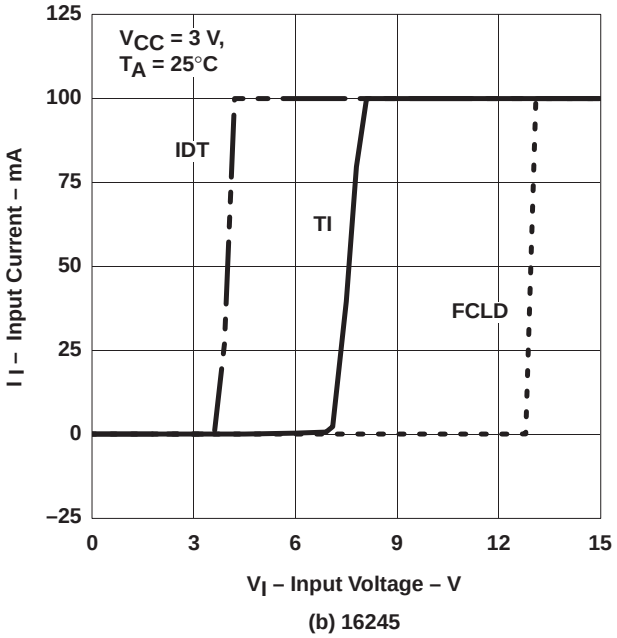
The maximum voltage that may be present at the input and output of a device is important up to the maximum level that external signals may reach, and beyond that is of marginal importance. The LVC, LCX, and FCT3 families specify maximum input and output voltages of 6.5 V to 7 V. **Figure 2–7** illustrates the appropriate curves for TI's LVC245, FCLD's LCX245, IDT's FCT3245, Motorola's LCX245, TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245.

In graph (a) of **Figure 2–7**, IDT's FCT3245 provides an overvoltage protection to 4 V, which means that a 5-V presence may cause damage to the device. In graph (b) of **Figure 2–7**, the same is true for IDT's FCT163245 device.

FCLD states that typical bench data shows an over-voltage tolerance of 13 V on their pins. In today's systems, however, the highest typical voltage is 5 V, which results in most LVC, LCX, and FCT3 devices not being exposed to voltages higher than 5.5 V to 6 V. The critical feature is that the device must be capable of withstanding a 5-V presence on the inputs and outputs without being damaged. Beyond the 5.5-V to 6-V limit, any additional overvoltage tolerance is of marginal benefit. Perhaps a more important consideration should be to determine how an overvoltage of such magnitude could occur and to assess the second- and third-order effects that a presence of 13 V would have on other parts of the system.



(a) ’245



(b) 16245

MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–7. Input Current Versus Input Voltage

OUTPUT-SIGNAL SLEW RATE

Output-signal slew is the rate at which the output voltage rises or falls from 10% to 90% of its magnitude. Initially, fast values of t(rise) and t(fall) may seem desirable. In actuality, however, values of t(rise) and t(fall) need to be taken in conjunction with several other parameters to achieve an overall performance determination of the device. For example, a slower edge rate is beneficial because less ground bounce occurs; however, a drawback of a slower edge rate is that the propagation-delay times tend to increase. Because output-signal slew, propagation delay, simultaneous-switching noise, and EMI are all interrelated, a value judgment on the performance of a device based on any of these parameters in isolation cannot be accurately made; they are all interrelated and must be assessed in their entirety.

Figure 2–8 contains output-signal slew data for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Separate graphs are provided for a single output switching and eight outputs switching.

Figure 2–8 shows that slew rates vary widely. Motorola's LCX245 was the most noteworthy as the fall time when eight outputs were switching showed poor performance and never reached the 10% mark. From an applications perspective, as previously mentioned, the difference in the slew rates must be assessed in conjunction with the increased propagation-delay time and reduced ground bounce and whether the resultant tradeoff is important to the specific application.

Figure 2–9 contains output-signal slew data for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for a single output switching and for 16 outputs switching.

Figure *Title* *Page*

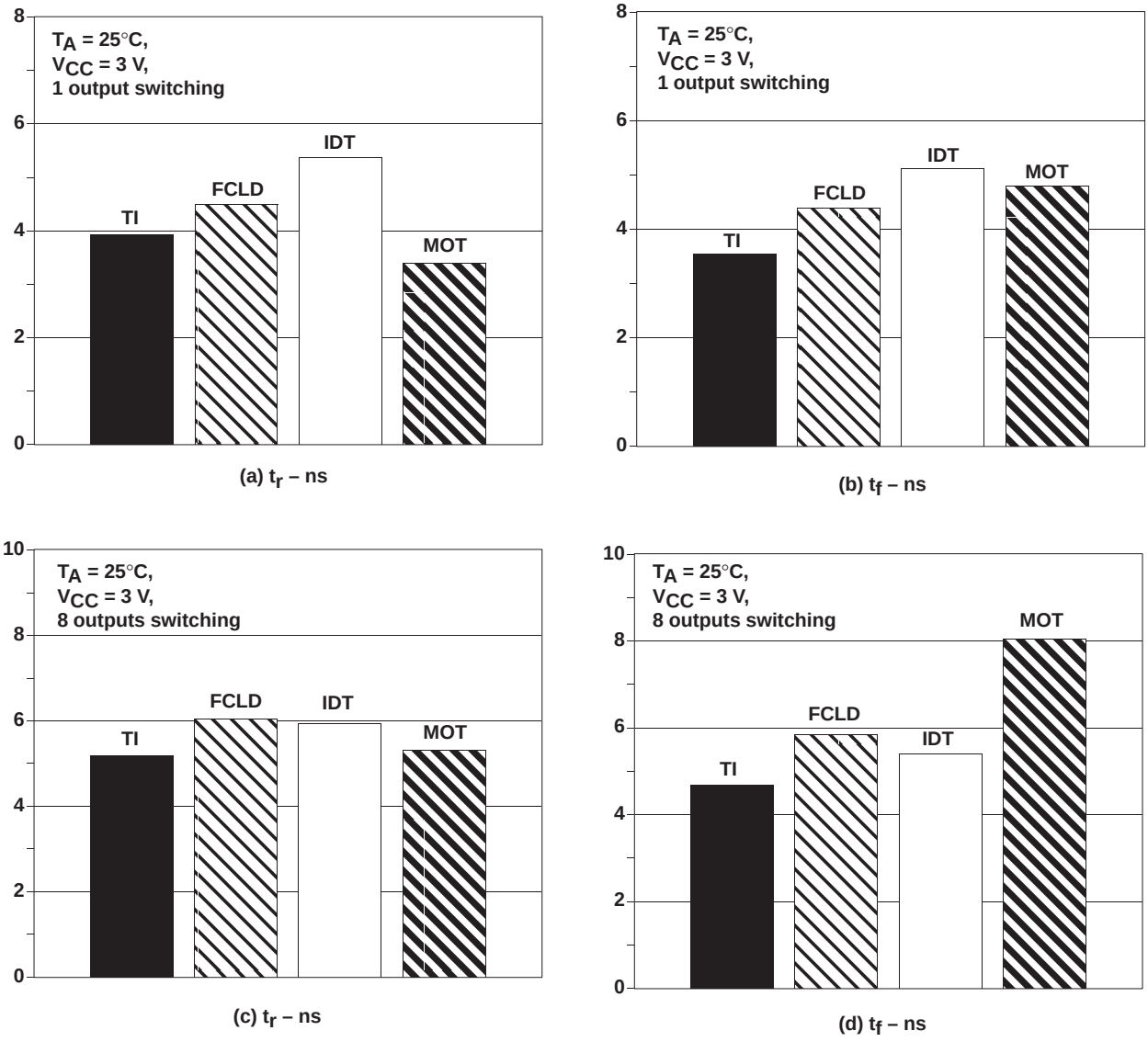
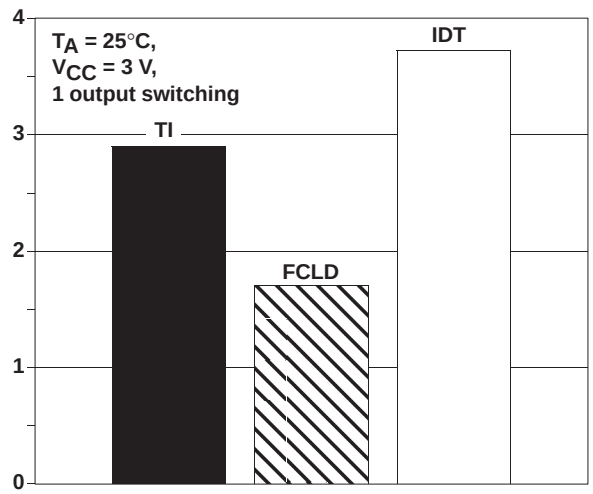
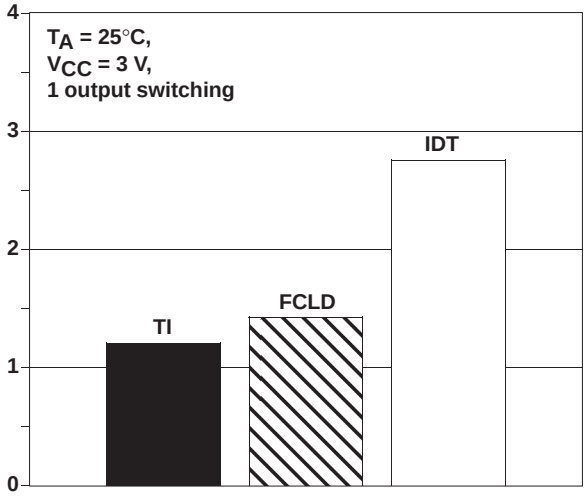


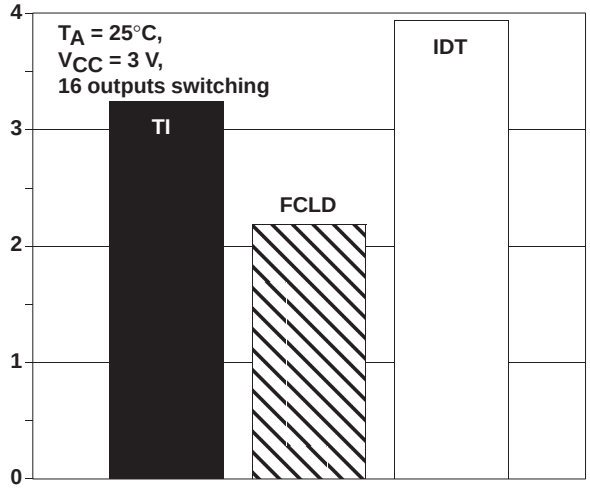
Figure 2–8. ’245 t_r and t_f



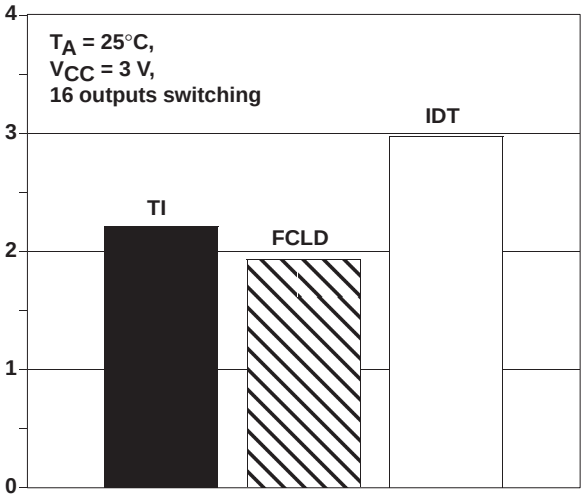
(a) t_r – ns



(b) t_f – ns



(c) t_r – ns



(d) t_f – ns

Figure 2–9. ’16245 t_r and t_f

SLOW-INPUT TRANSITION TIME

A slow-input test sheds light on the integrity of the device, specifically, how the device responds when the input voltage is slowly ramped from 0 to V_{CC} and then conversely, when the input voltage is slowly ramped from V_{CC} to GND. As the input voltage is ramping, the output voltage is monitored and once it begins to switch, the waveform is observed. If any nonmonotonic behavior is observed as the output traverses through the threshold region, then the device may be sensitive to a slow input, which can result in the output oscillating or false triggering.

Figures 2–10 through 2–17 contain slow-input transition time plots for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. **Figures 2–18 through 2–23** contain slow-input transition time plots for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. All devices examined show non-critical responses to the slow-input test.

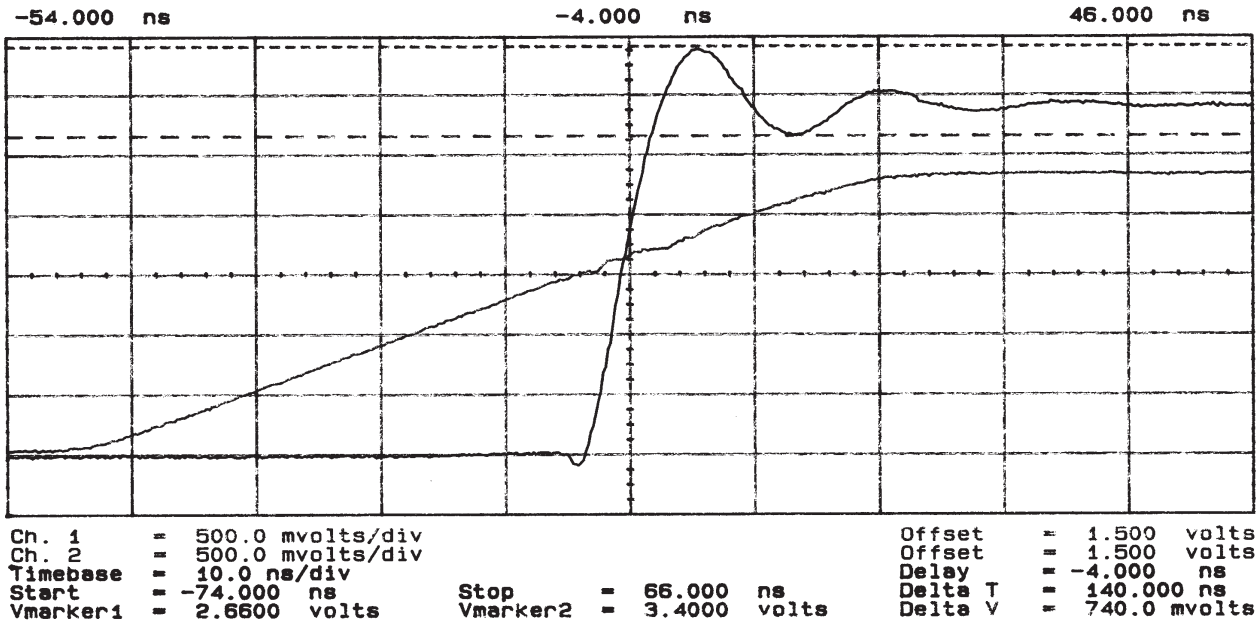


Figure 2–10. TI LVC245 Slow-Input Transition Time Plot

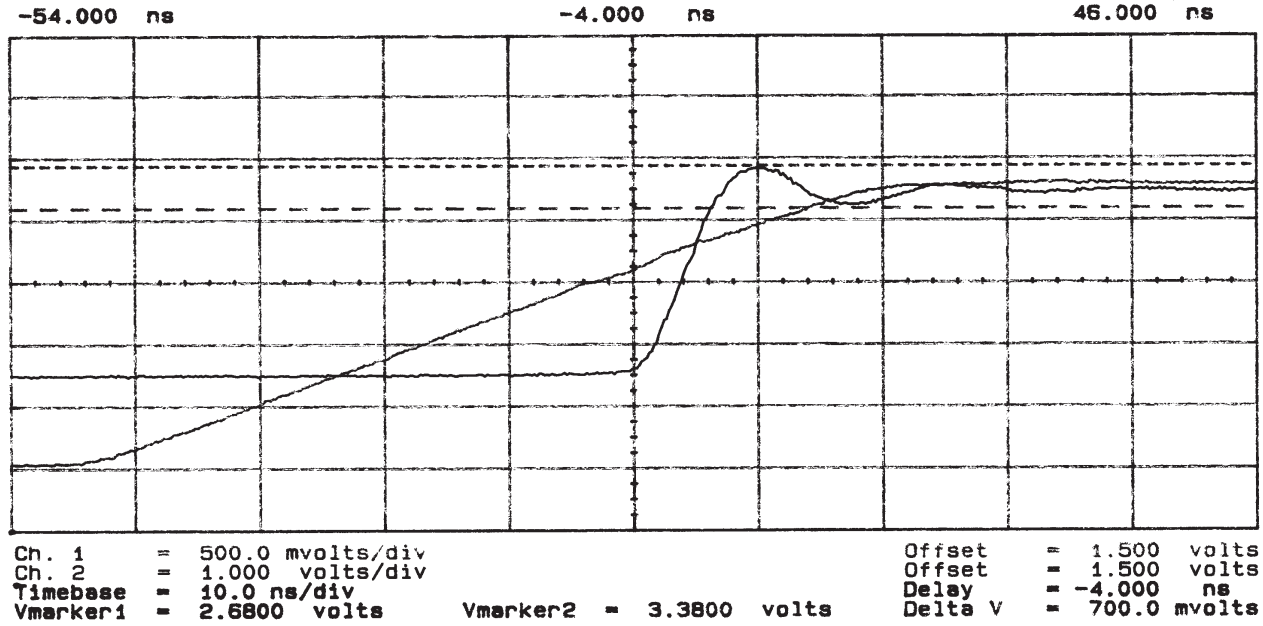


Figure 2–11. FCLD LCX245 Slow-Input Transition Time Plot

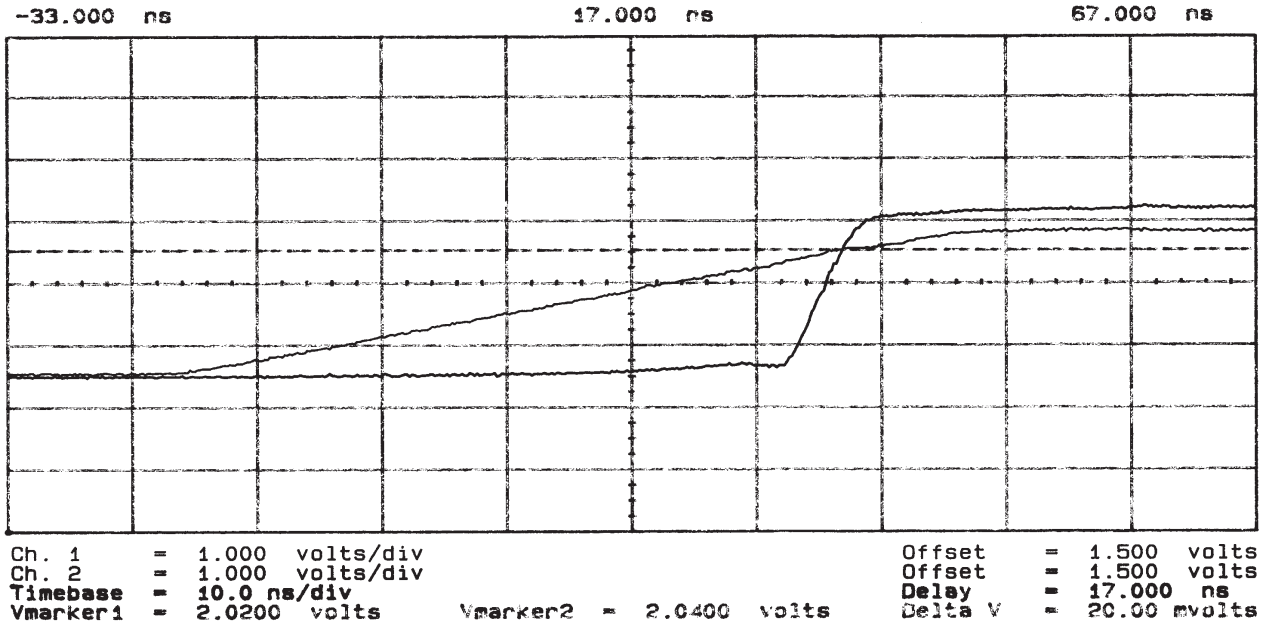


Figure 2–12. IDT FCT3245 Slow-Input Transition Time Plot

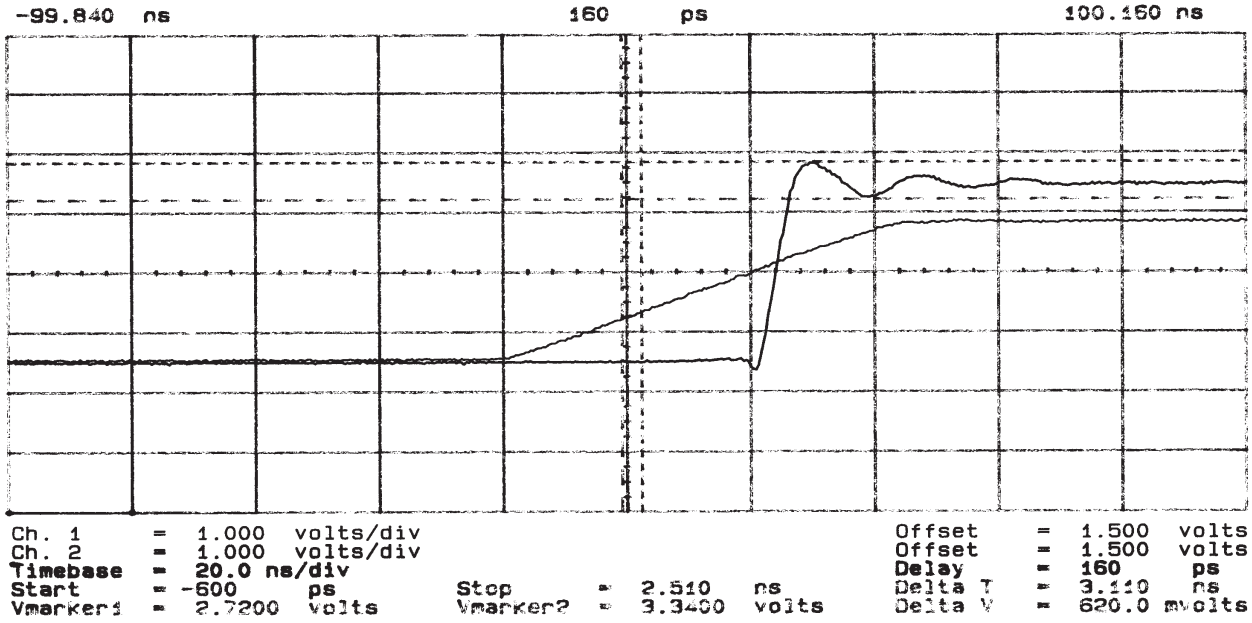


Figure 2–13. Motorola LCX245 Slow-Input Transition Time Plot

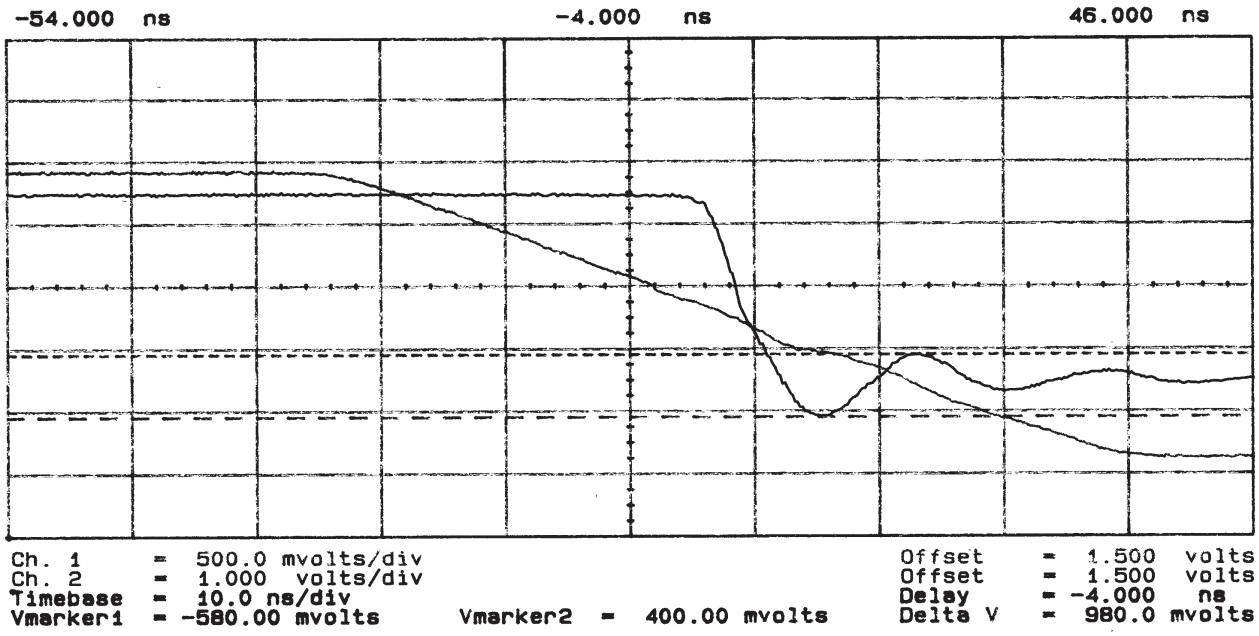


Figure 2–14. TI LVC245 Slow-Input Transition Time Plot

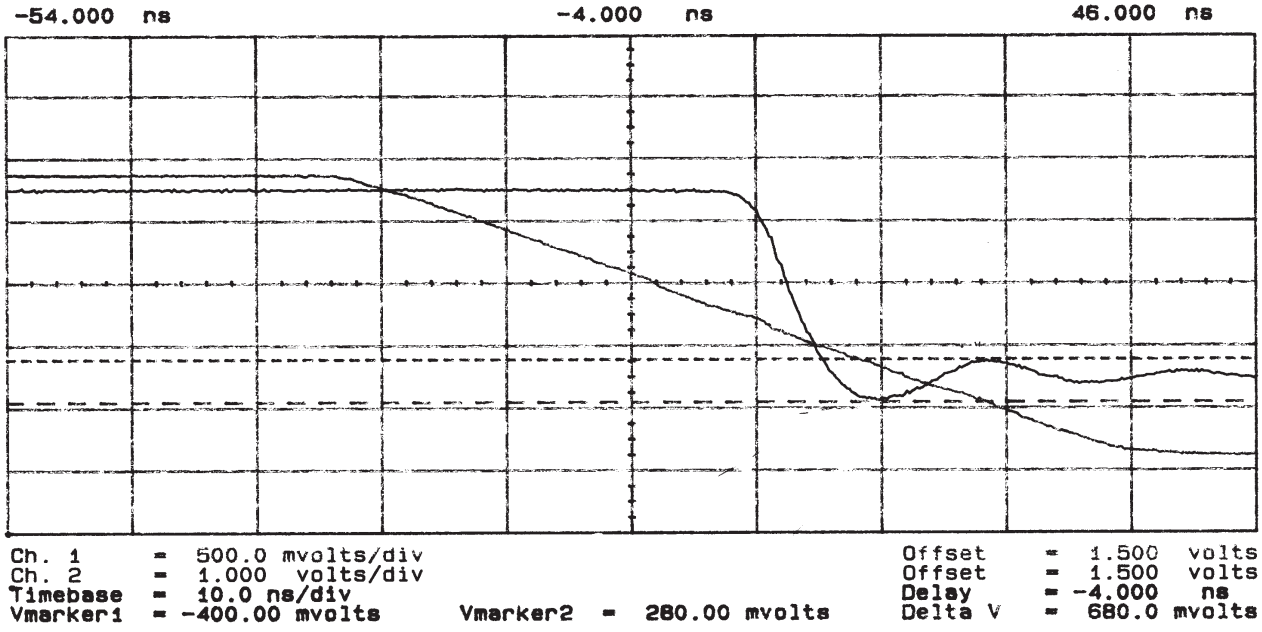


Figure 2–15. FCLD LCX245 Slow-Input Transition Time Plot

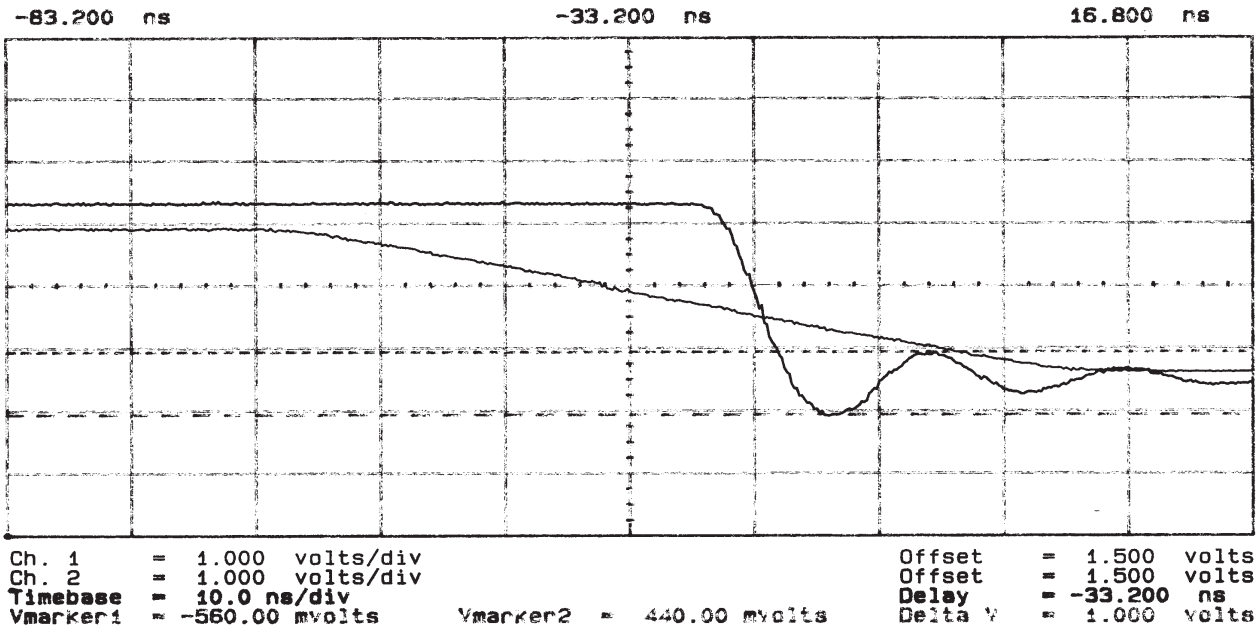


Figure 2–16. IDT FCT3245 Slow-Input Transition Time Plot

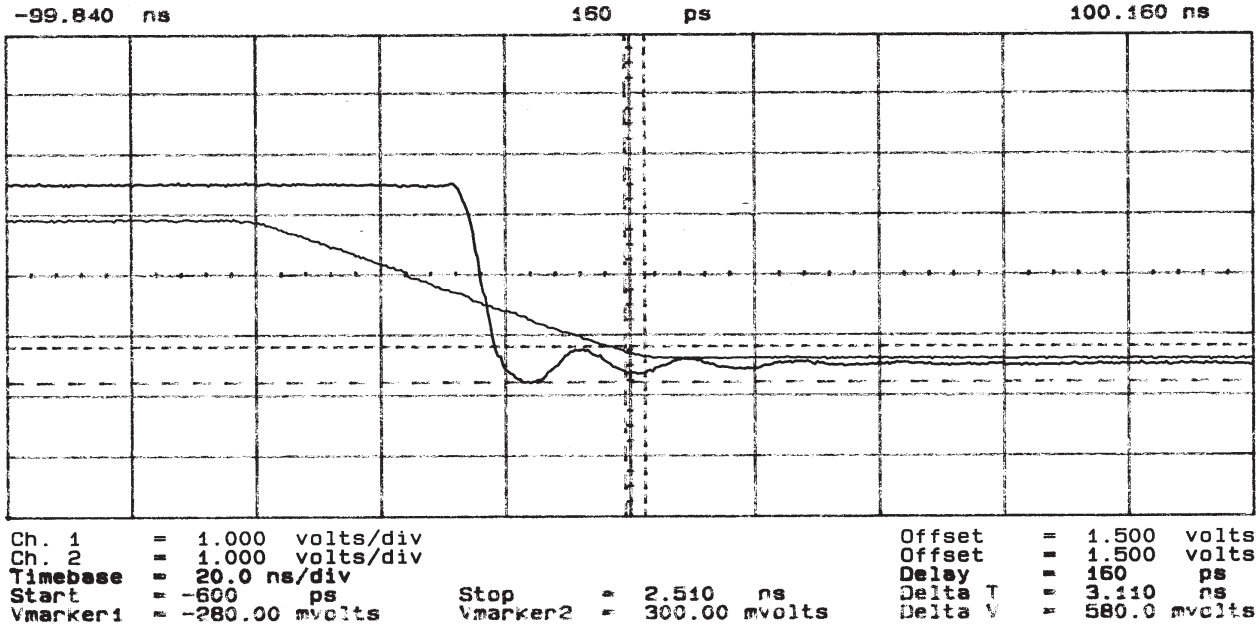


Figure 2–17. Motorola LCX245 Slow-Input Transition Time Plot

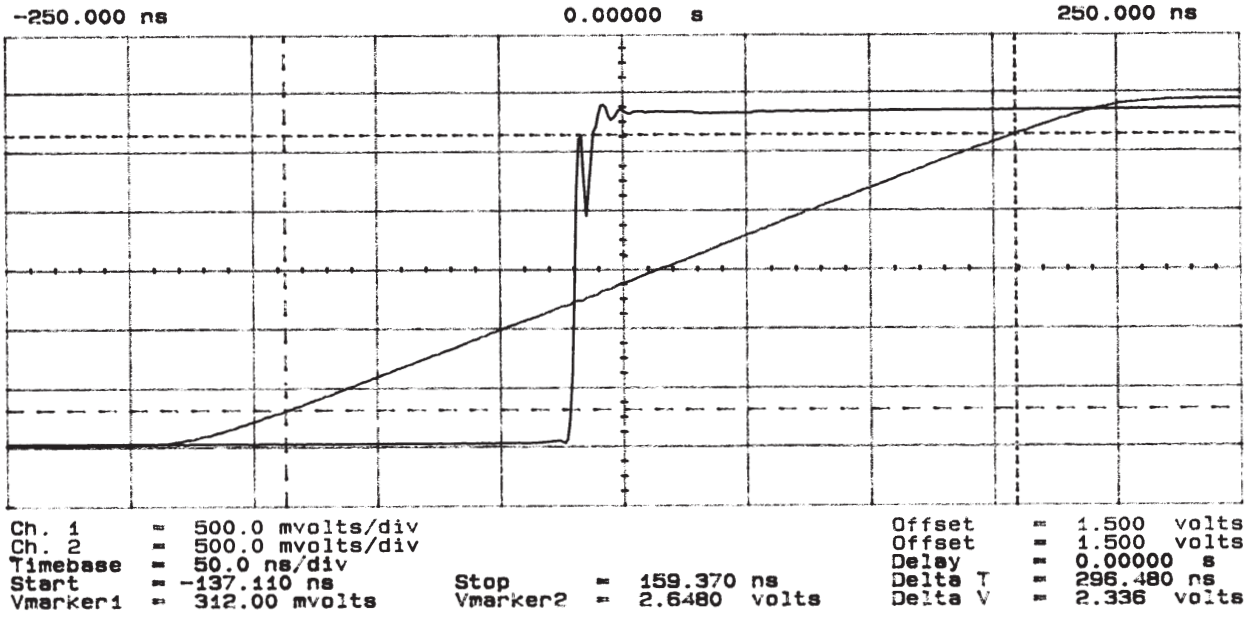


Figure 2–18. TI LVC16245 Slow-Input Transition Time Plot

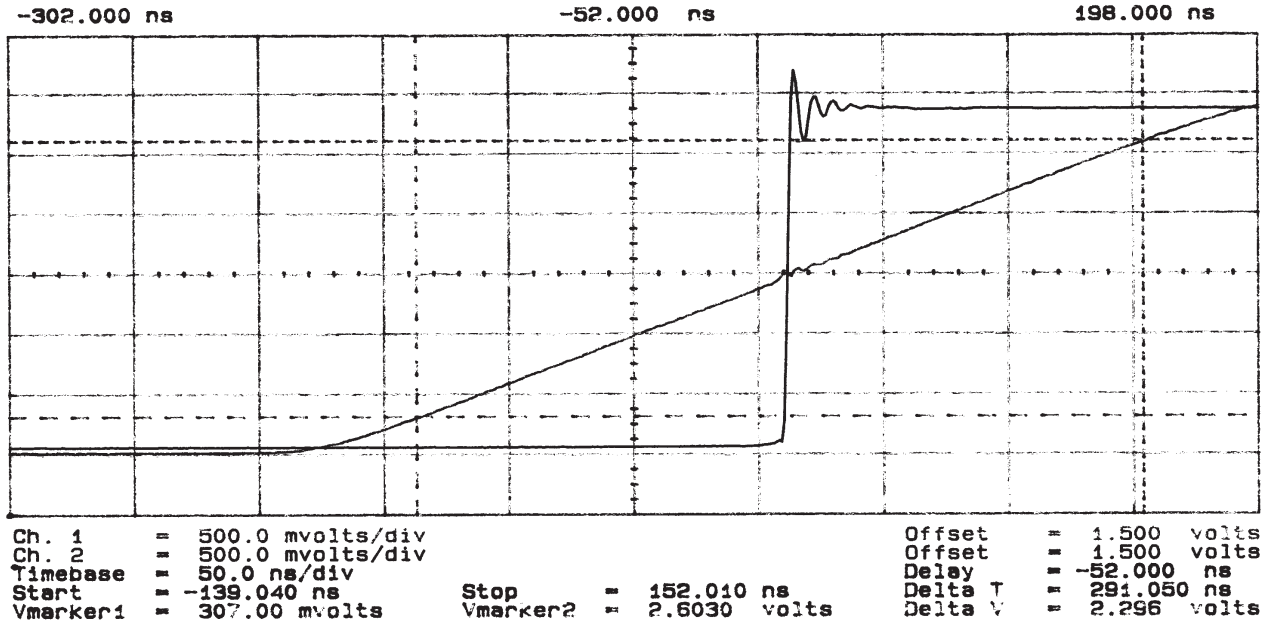


Figure 2–19. FCLD LCX16245 Slow-Input Transition Time Plot

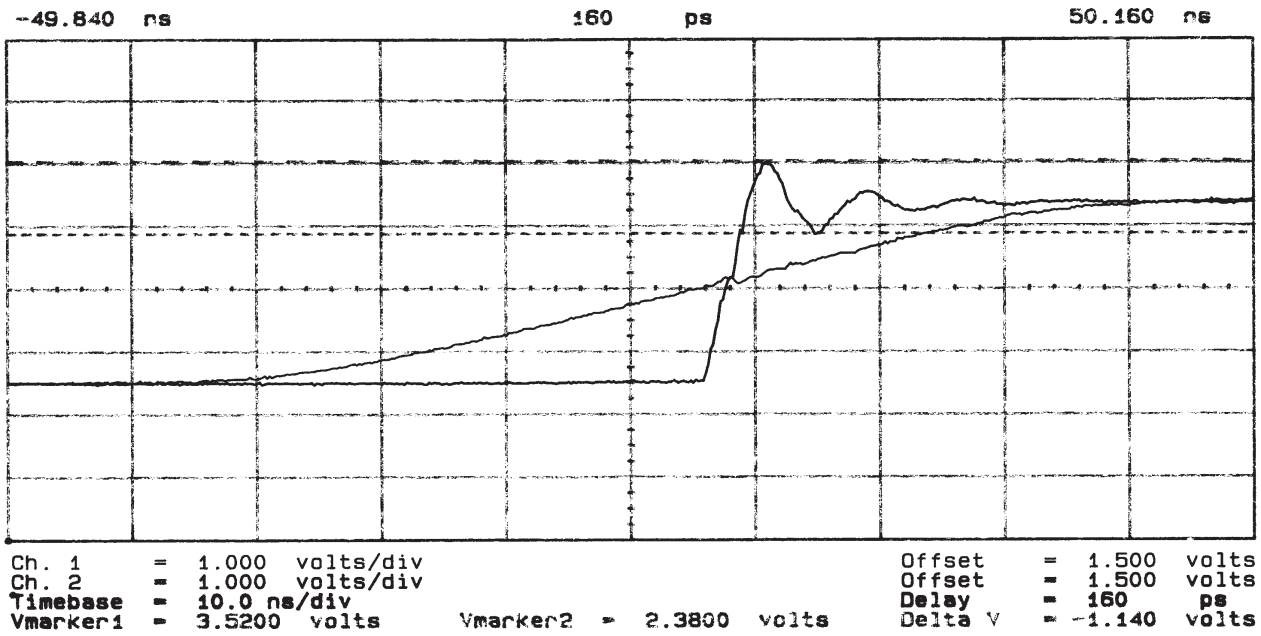


Figure 2–20. IDT FCT163245 Slow-Input Transition Time Plot

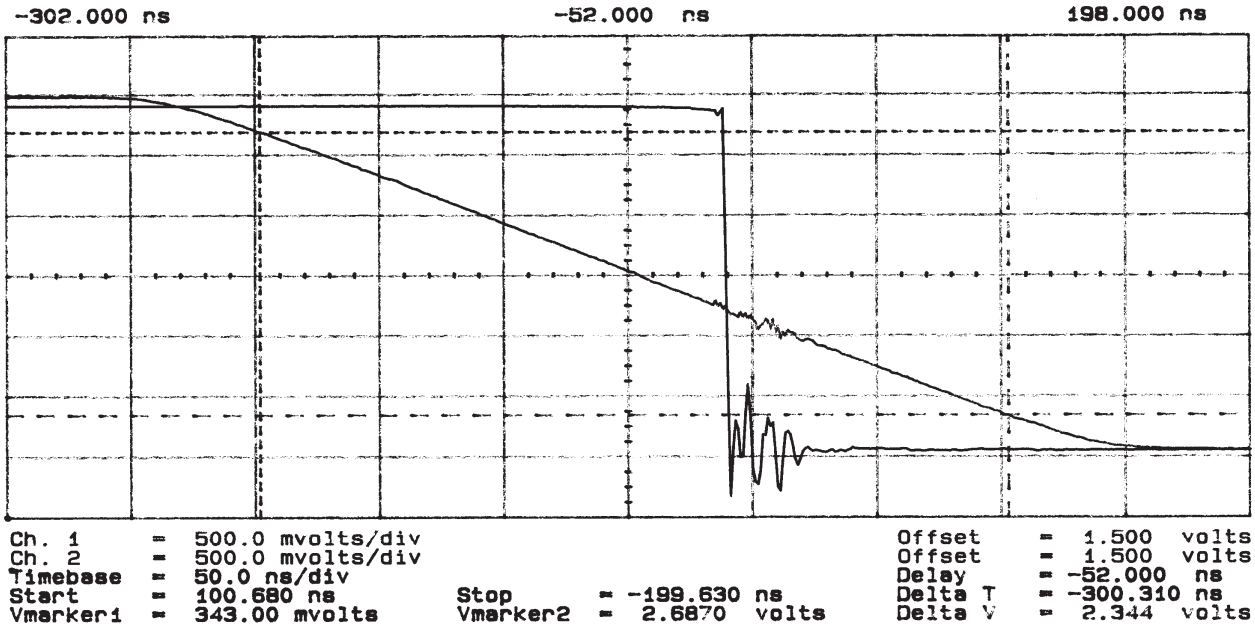


Figure 2–21. TI LVC16245 Slow-Input Transition Time Plot

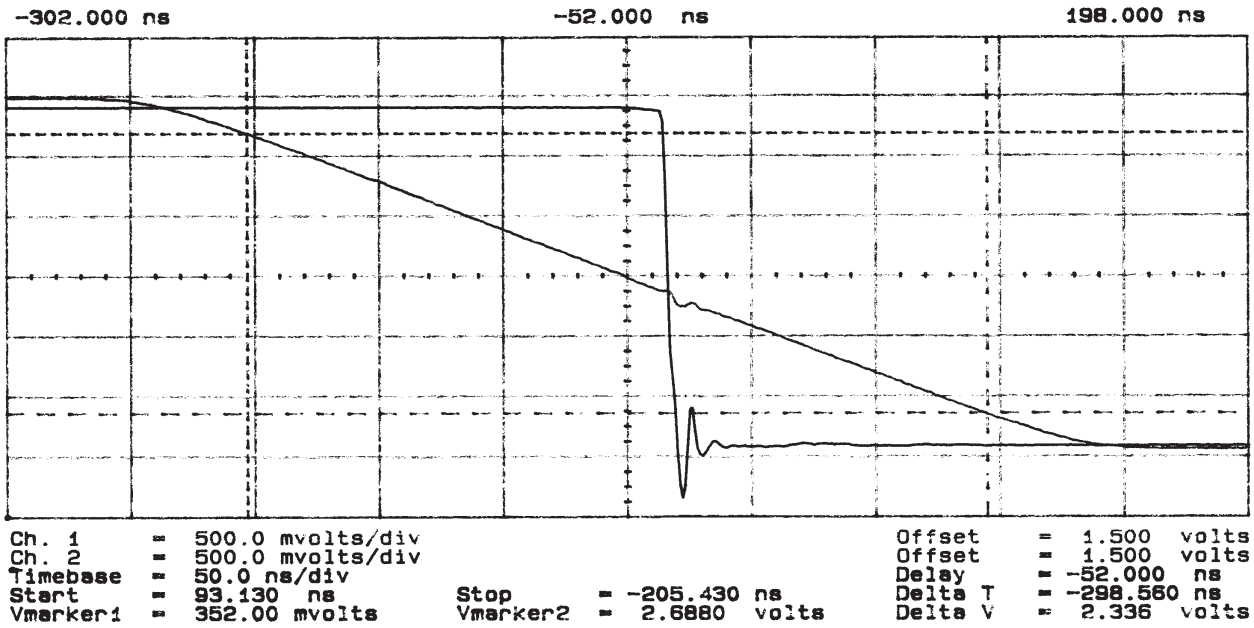


Figure 2–22. FCLD LCX16245 Slow-Input Transition Time Plot

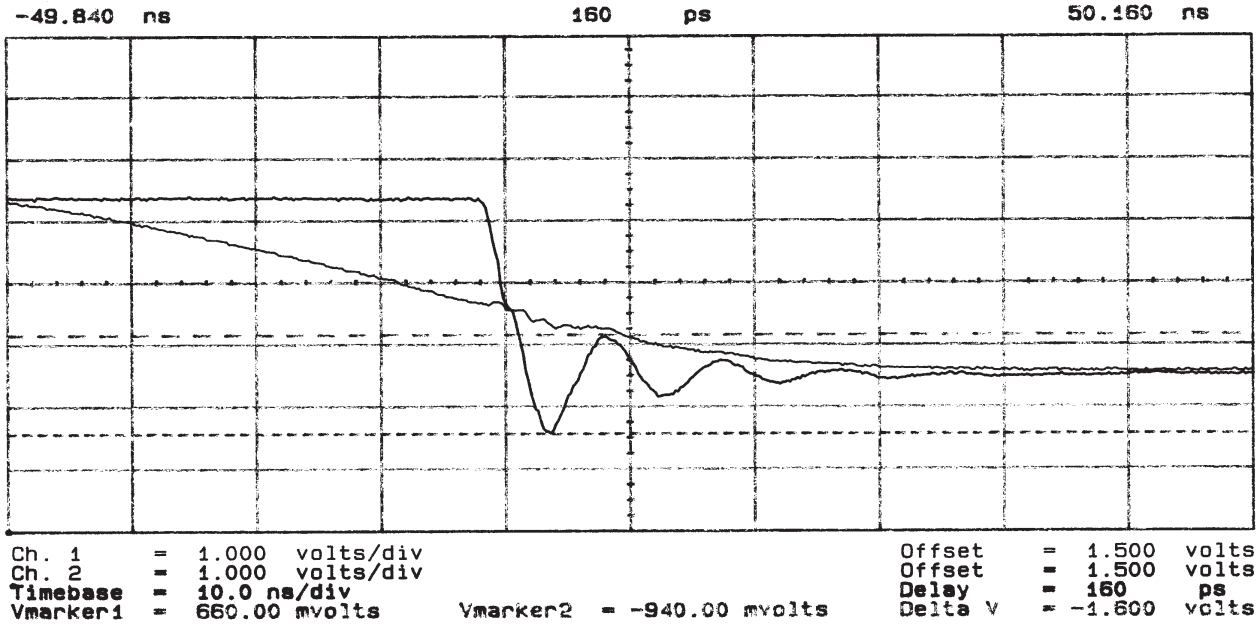


Figure 2–23. IDT FCT163245 Slow-Input Transition Time Plot

SIMULTANEOUS SWITCHING

Simultaneous switching is a method of measuring the magnitude of noise a device experiences while switching. Four measurements are commonly discussed. The method of measuring simultaneous switching (ground bounce) consists of holding one output low and switching all other outputs from a high state to a low state. Because of mutual inductance, transient current flows through the package and into the output pin that is being held low. This results in a rise in voltage and the output begins to ring. The peak of this ringing is called V_{OLP} (output low peak voltage) and is the most common and critical measure of ground bounce due to the relatively small noise margin between a valid output low state and beginning of the threshold region of 0.8 V. V_{OLV} (output low valley voltage) is the lowest point that the output that is being held low reaches.

In a similar fashion, two other measurements of simultaneous switching exist. In this scenario, a single output is held high and all other outputs are switched from a low state to a high state. Mutual inductance occurs and results in the output voltage dipping from its logic high state and ringing. The valley of this phenomenon is called V_{OHV} (output high valley voltage) and the peak is called V_{OHP} (output high peak voltage). These four measurements of simultaneous switching are illustrated in **Figure 2–24**.

Simultaneous switching is extremely important; if the value of V_{OLP} goes above 0.8 V, the threshold region is entered and the device could switch from a low state to a high state. Conversely, if the value of V_{OHV} drops below 2.0 V, the device could switch from a high state to a low state. For this reason, simultaneous-switching values are always closely monitored when designing, testing, and implementing devices.

Figures 2–25 through 2–32 contain simultaneous-switching data for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. **Figures 2–33 through 2–38** contain simultaneous-switching data for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for V_{OHV}, V_{OHP}, V_{OLV}, and V_{OLP}.

In all of the figures, graphs that plot V_{OLP} and V_{OHV} are the most critical. Anything above 0.8 V could result in the output switching from a low state to a high state, and anything below 2.0 V could result in the output switching from high to a low state. All devices are practically identical in performance and no significant differences exist.

For ease of comparison, **Tables 2–8 and 2–9** contain V_{OLP}, V_{OLV}, V_{OHV}, and V_{OHP} data for the '245 and '16245 devices, respectively.

Most of the data contained in **Tables 2–8 and 2–9** is fairly consistent. One exception is Motorola's LCX245 V_{OLP} value of 1.06 V. A value of 0.8 V or higher is enough to potentially switch the output from a low state to a high state; a value of 1.06 V is significantly beyond the limit.

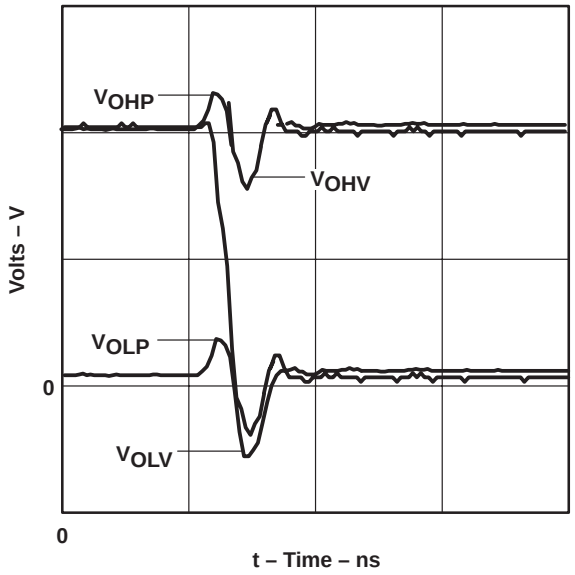


Figure 2–24. Simultaneous-Switching Waveforms

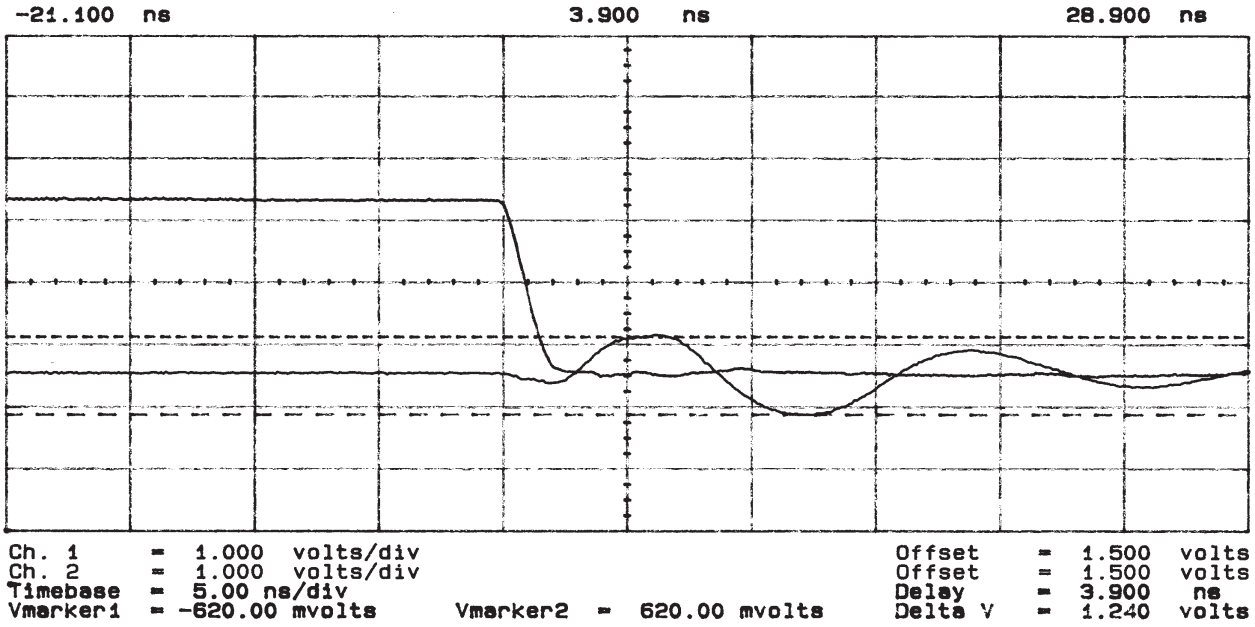


Figure 2–25. TI LVC245 Simultaneous-Switching Plot

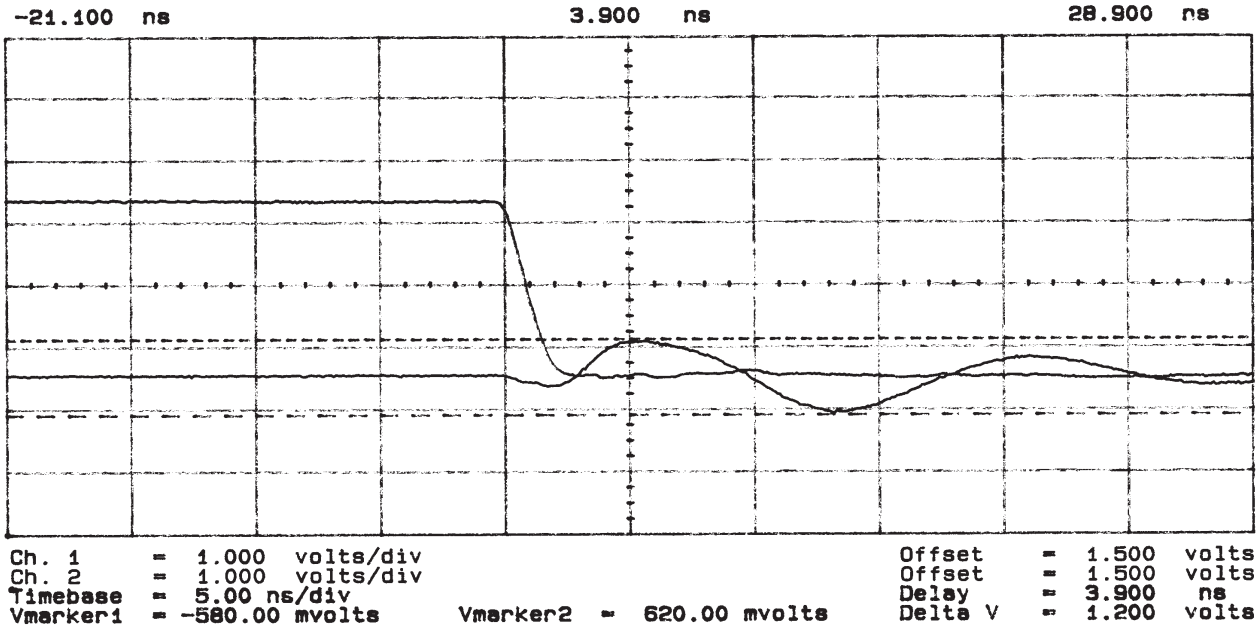


Figure 2–26. FCLD LCX245 Simultaneous-Switching Plot

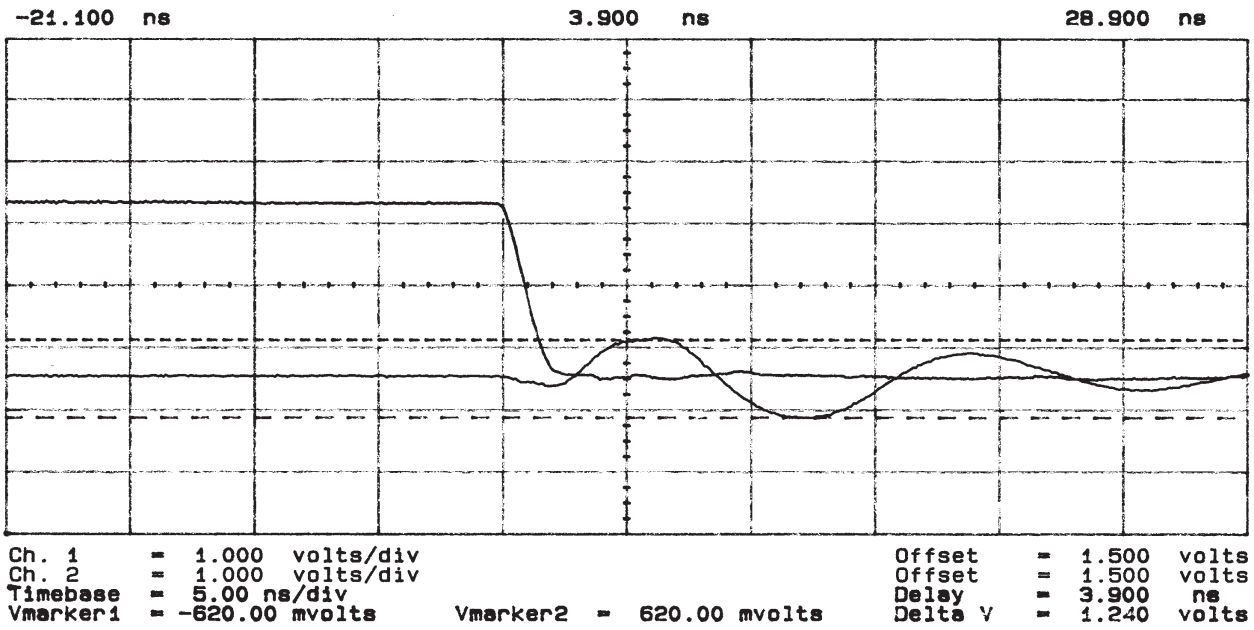


Figure 2–27. IDT FCT3245 Simultaneous-Switching Plot

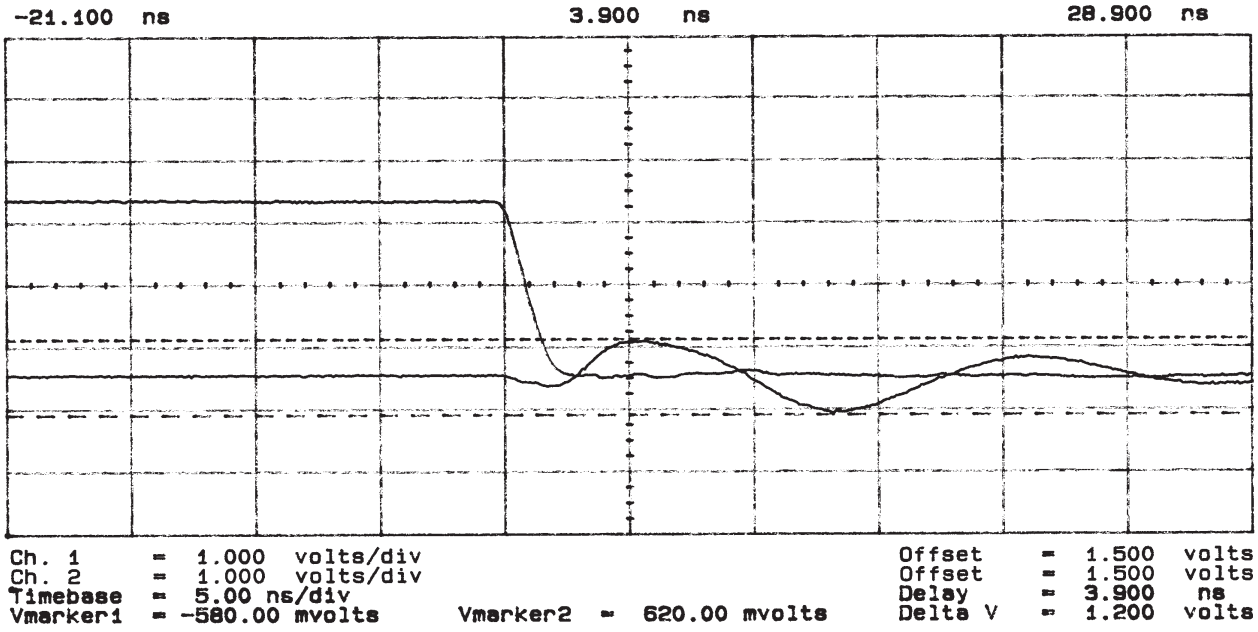


Figure 2–28. Motorola LCX245 Simultaneous-Switching Plot

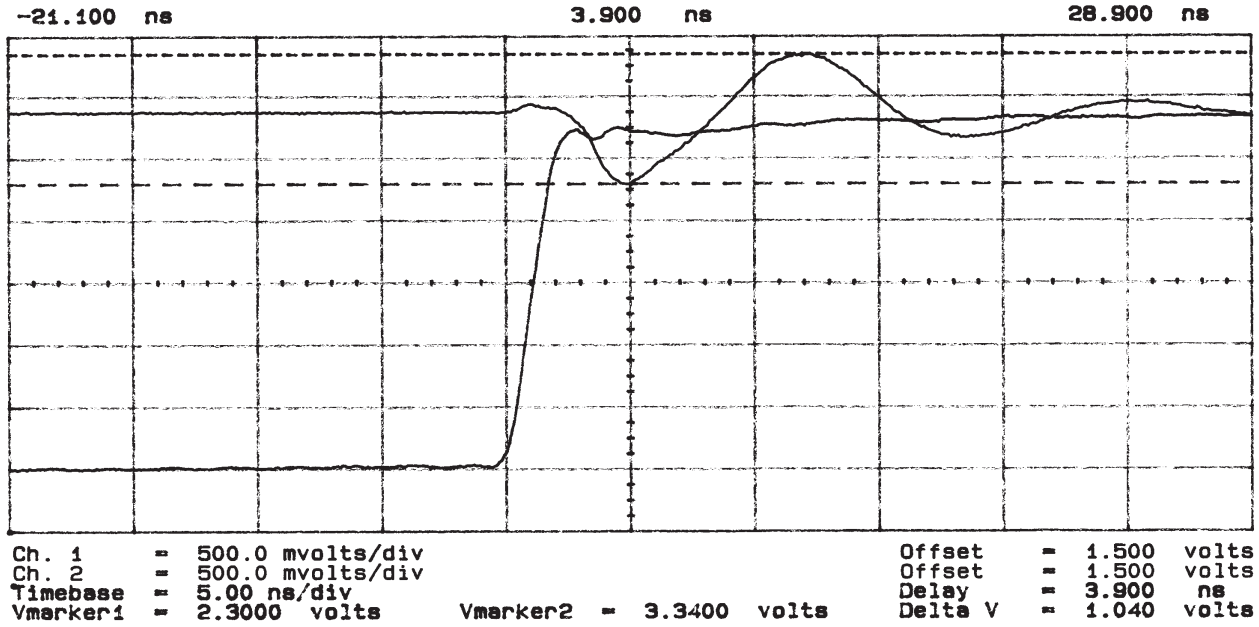


Figure 2–29. TI LVC245 Simultaneous-Switching Plot

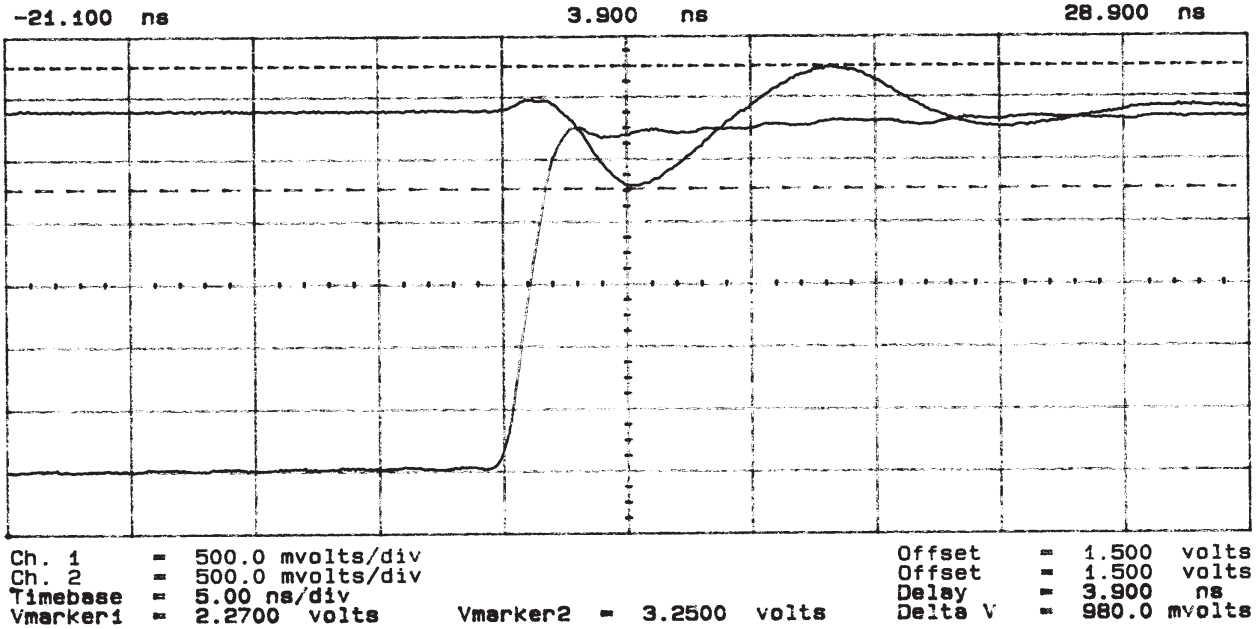


Figure 2–30. FCLD LCX245 Simultaneous-Switching Plot

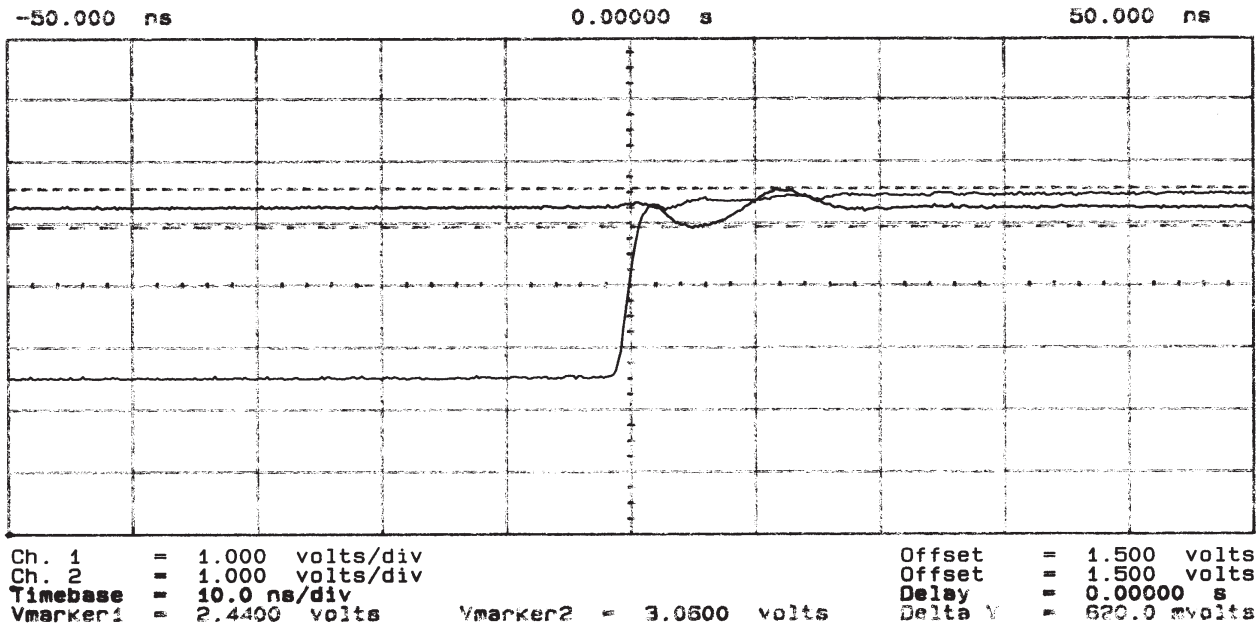


Figure 2–31. IDT FCT3245 Simultaneous-Switching Plot

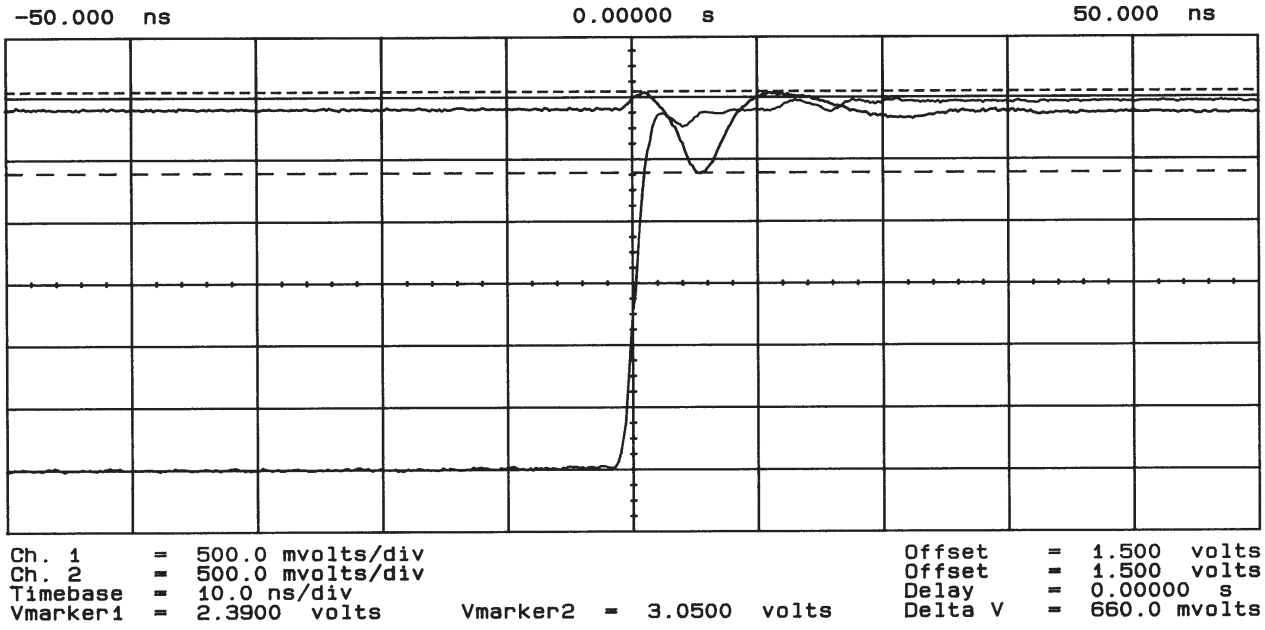


Figure 2–32. Motorola LCX245 Simultaneous-Switching Plot

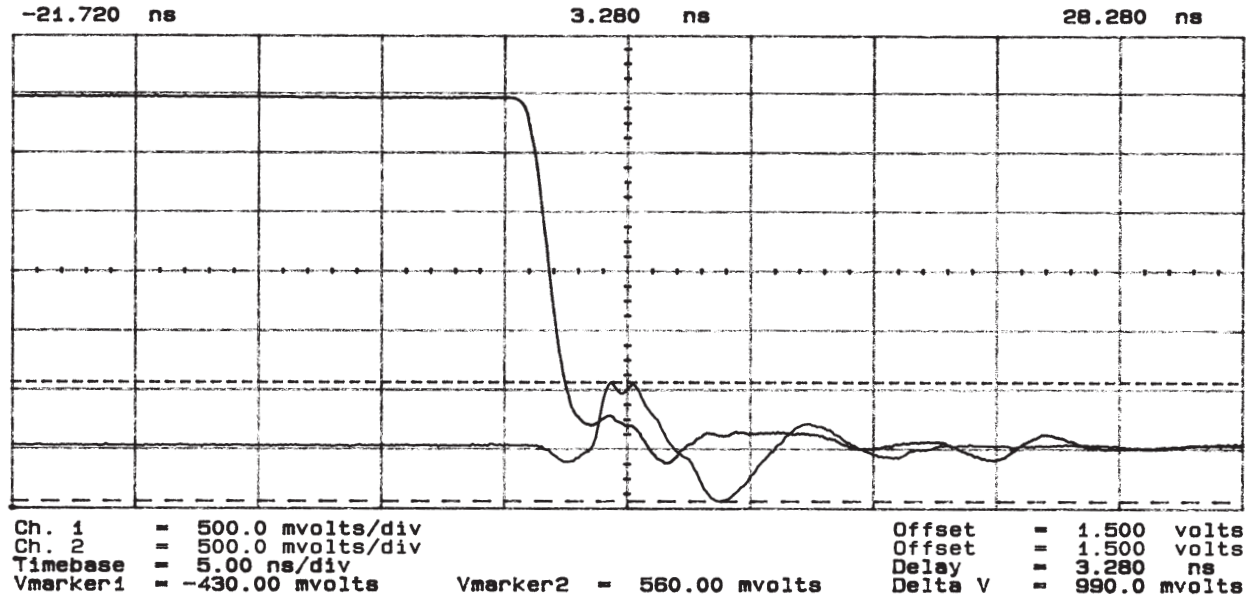


Figure 2–33. TI LVC16245 Simultaneous-Switching Plot

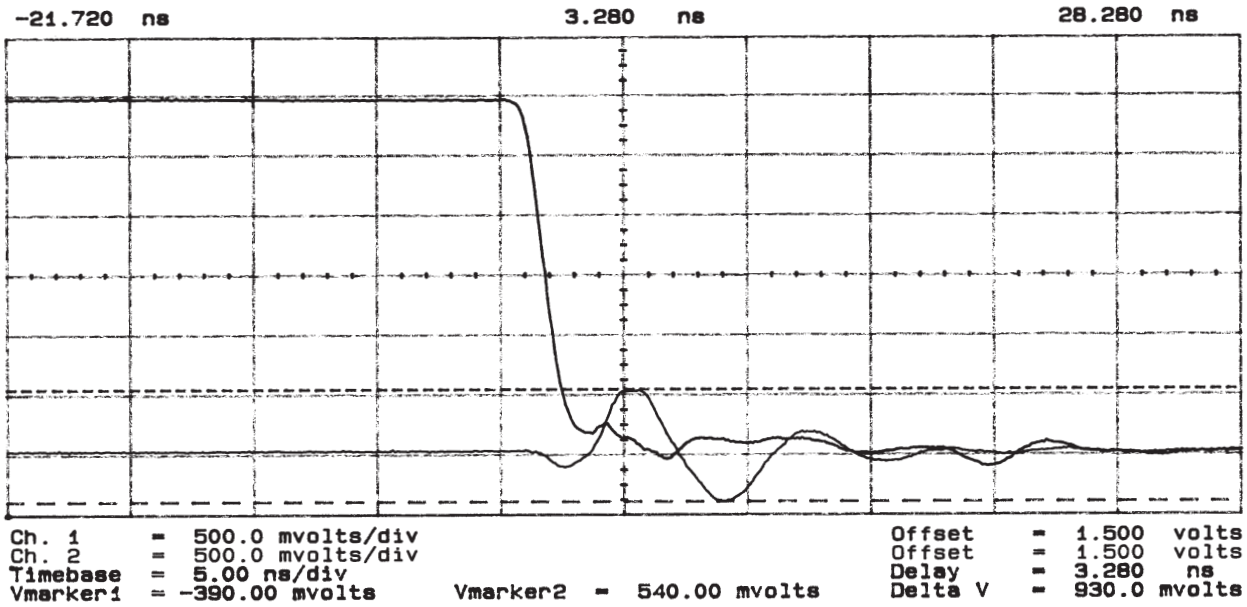


Figure 2–34. FCLD LCX16245 Simultaneous-Switching Plot

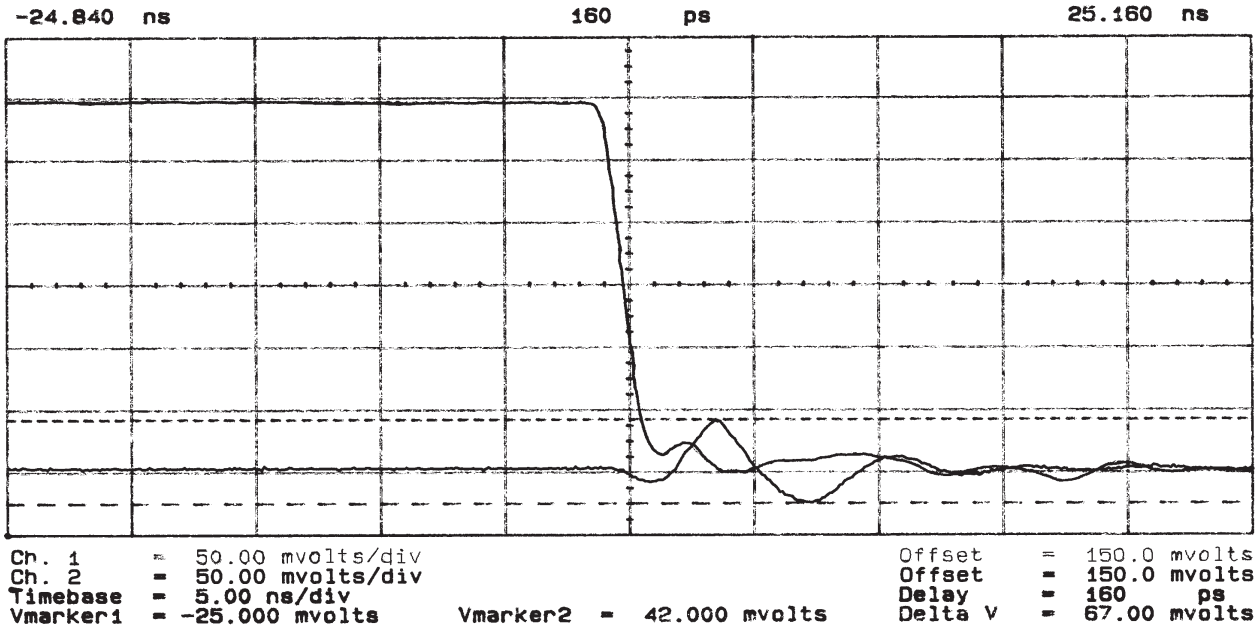


Figure 2–35. IDT FCT163245 Simultaneous-Switching Plot

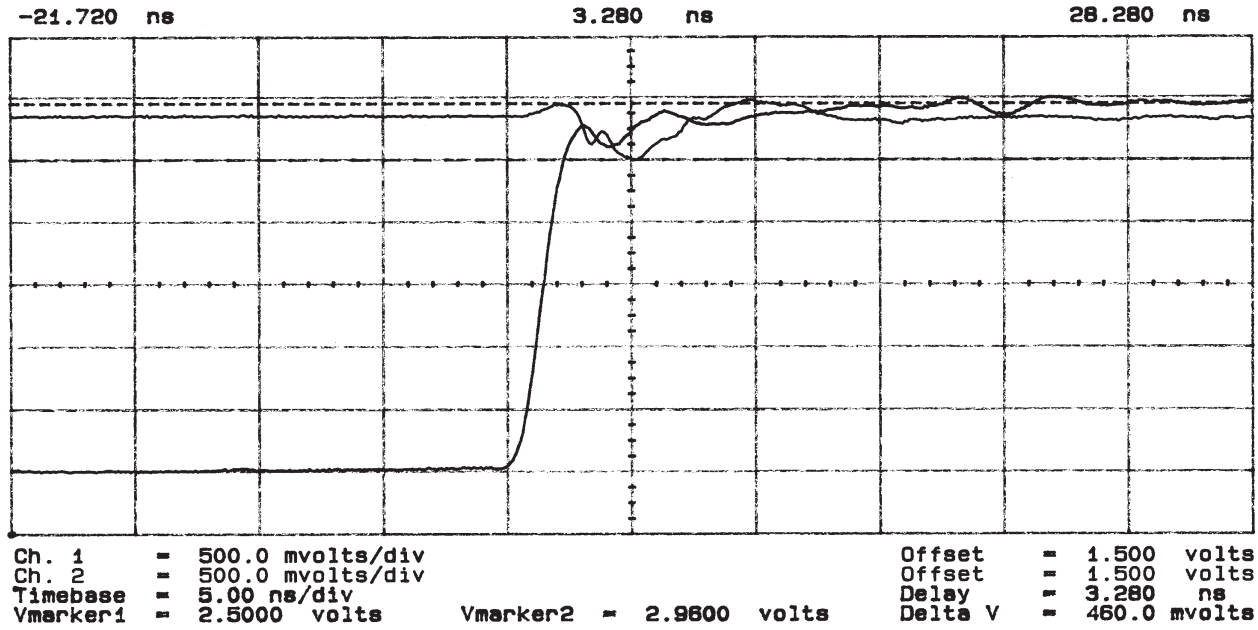


Figure 2–36. TI LVC16245 Simultaneous-Switching Plot

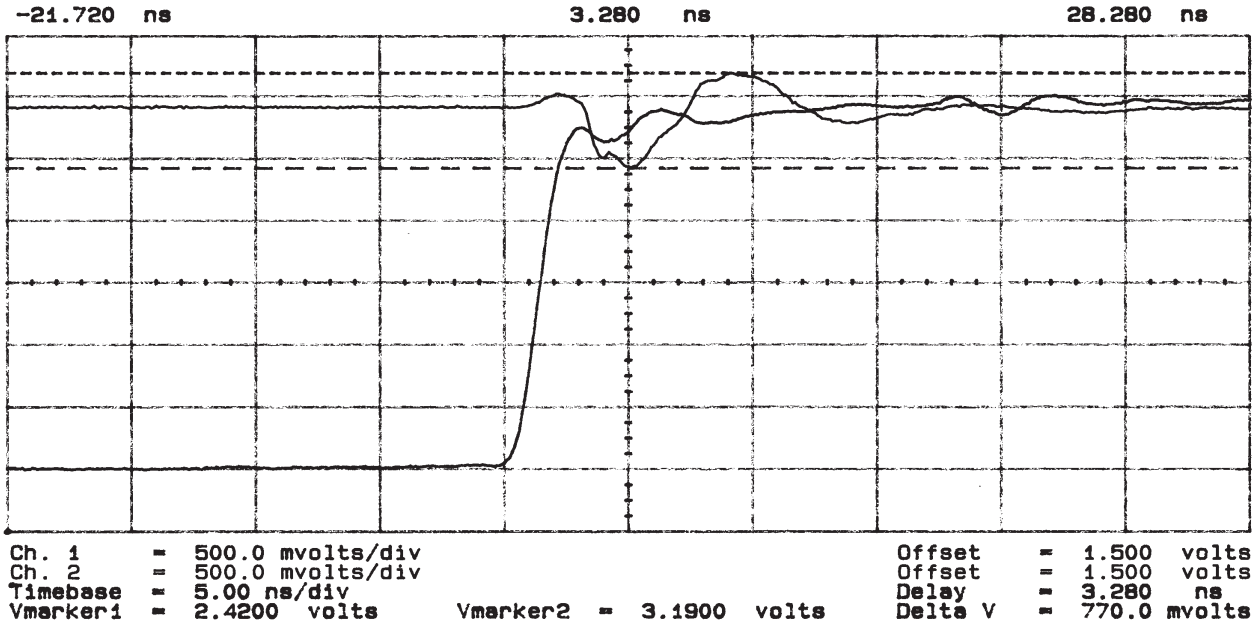


Figure 2–37. FCLD LCX16245 Simultaneous-Switching Plot

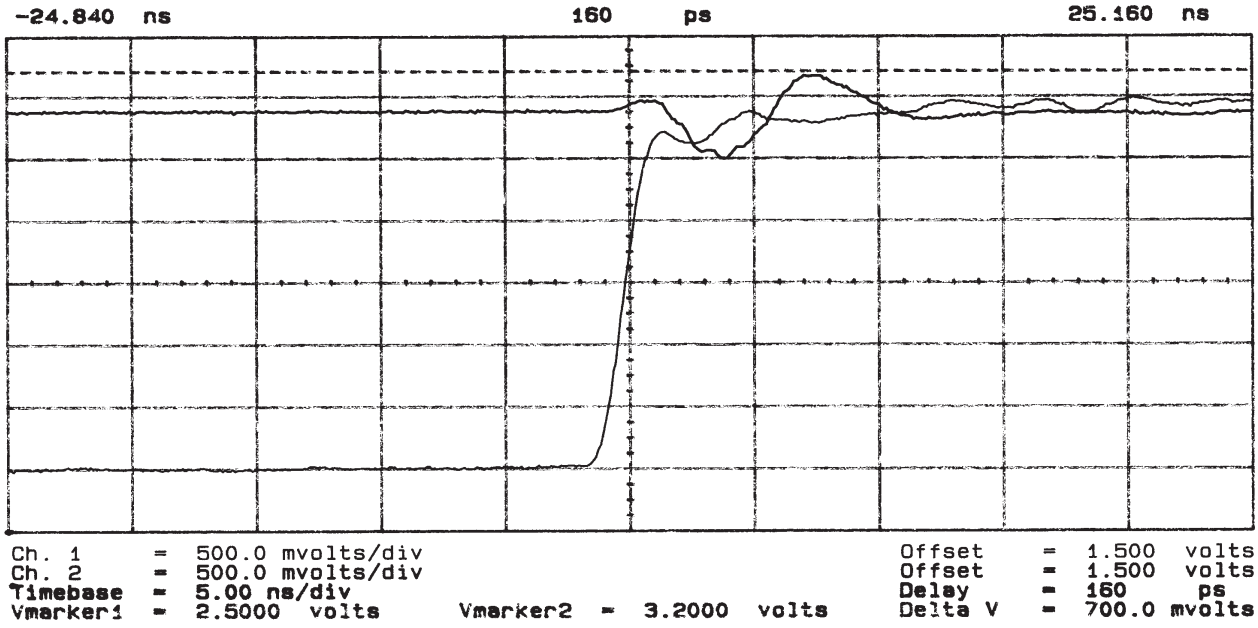


Figure 2–38. IDT FCT163245 Simultaneous-Switching Plot

Table 2–8. ’245 Simultaneous-Switching Data

DEVICE	V_{OLP}	V_{OLV}	V_{OHV}	V_{OHP}
LVC245 (TI)	0.62	–0.62	2.3	3.34
LCX245 (FCLD)	0.62	–0.58	2.27	3.25
FCT3245 (IDT)	0.65	–0.72	2.44	3.06
LCX245 (MOT)	1.06	–0.23	2.39	3.05

Table 2–9. ’16245 Simultaneous-Switching Data

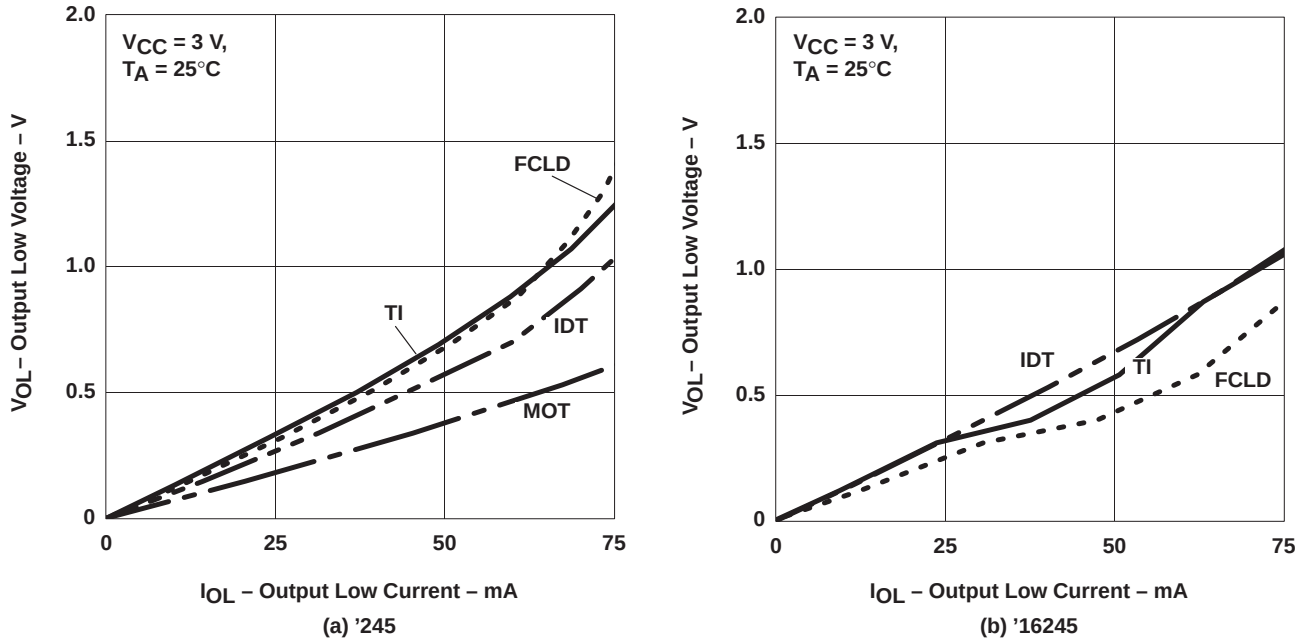
DEVICE	V_{OLP}	V_{OLV}	V_{OHV}	V_{OHP}
LVC16245 (TI)	0.56	–0.43	2.5	2.96
LCX16245 (FCLD)	0.54	–0.39	2.42	3.19
FCT163245 (IDT)	0.25	–0.42	2.5	3.2

V_{OL} VERSUS I_{OL}

A plot of the output low voltage versus the output low current gives an indication of the device's strength, specifically, a device designed to sink more current is stronger than a device designed to sink less current.

The LVC and LCX logic families have a medium drive capability of –24/24 mA and the FCT3 family has a drive capability of –8/24 mA. As such, they are commonly found in point-to-point applications. Along with propagation-delay time, simultaneous switching noise, etc., the capability of a device to drive a certain load is usually one of the distinguishing characteristics of a logic family; selecting a particular logic family because of its drive capabilities is a common occurrence. Although the LVC, LCX, and FCT3 logic families are probably not going to be used in systems in which large amounts of drive current are required, meeting the specifications provided in the data sheets is critical.

Figure 2–39 contains a plot of the output low voltage versus the output low current for TI's LVC245, FCLD's LCX245, IDT's FCT3245, Motorola's LCX245, TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. At the 24-mA level, all devices are significantly under the data sheet specification value for V_{OL} of 0.55 V. Furthermore, at the 0.55-V level, the actual value for TI's LVC245 is 37 mA and for TI's LVC16245, 49 mA.



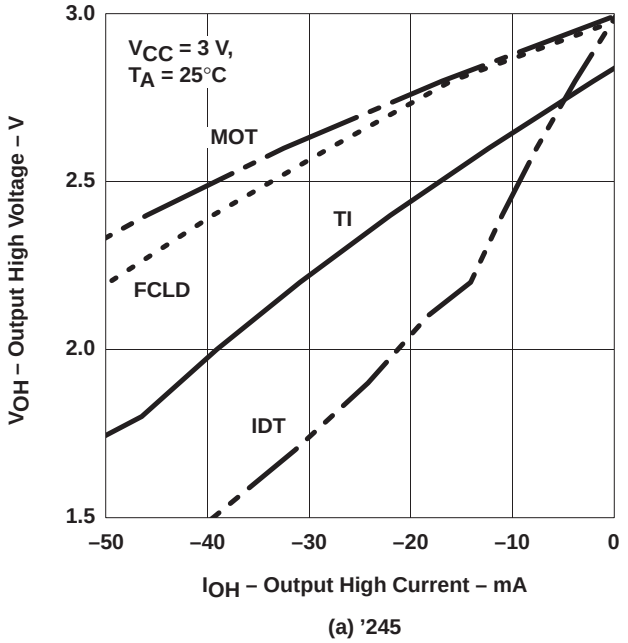
MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–39. ’245 and ’16245 V_{OL} Versus I_{OL}

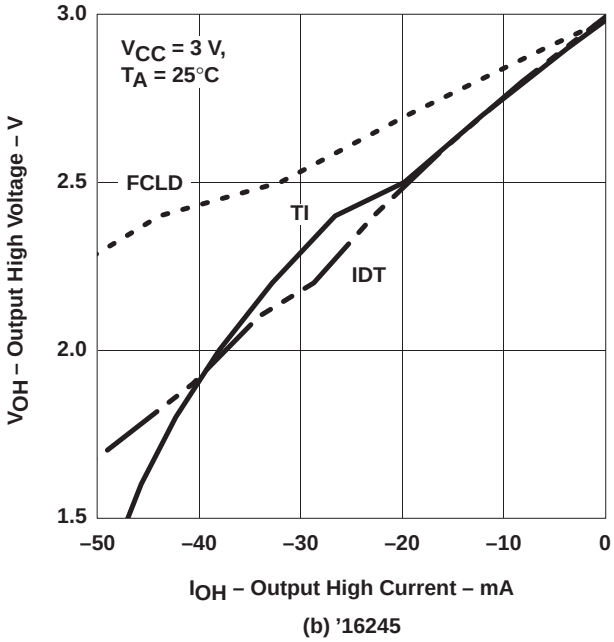
V_{OH} VERSUS I_{OH}

A plot of the output high voltage versus the output high current, in a fashion similar to the previous paragraphs, also gives an indication of the device's strength. A device designed to source more current is stronger than a device designed to source less current.

Figure 2–40 contains a plot of the output high voltage versus the output high current for TI's LVC245, FCLD's LCX245, IDT's FCT3245, Motorola's LCX245, TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. At the –24-mA point, the measured voltage of all devices except IDT's FCT3 are above the data sheet value specification for V_{OH} of 2.2 V (IDT specifies a minimum value of 2.4 V at –8 mA, which means these devices have a significantly lower high-level drive capability than all other devices tested) and at the actual voltage of 2.2 V, the measured current was –31 mA and –33 mA for TI's LVC245 and TI's LVC16245, respectively.



(a) ’245



(b) ’16245

MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–40. ’245 and ’16245 V_{OH} Versus I_{OH}

PROPAGATION-DELAY SKEW

Propagation-delay skew indicates the variance in propagation-delay times. Numerous types of skew are measured and, as a general rule, propagation-delay skew is usually not a critical factor in evaluating the performance of a device. Having similar propagation-delay times is desirable, but other parameters are usually considered to be more important.

When conducting this test, the propagation delay for each output was tested individually, and then the difference between the slowest and the fastest propagation was computed; for comparison purposes, competitors have labeled this value T_{os}(LH) and T_{os}(HL). **Figure 2–41** illustrates the method in which this test was conducted.

Figure 2–42 shows propagation-delay skews for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Separate graphs are provided for low-to-high and high-to-low transitions.

Figure 2–42 shows a difference in propagation-delay skew times, which, depending on the application, may be noteworthy. The magnitude of the difference in graph (a) is 180 ps and in graph (b) is 260 ps. If the device is being used as a clock driver, this skew may not be tolerable. The vast majority of applications probably would not be impacted by this amount of skew; however, with certain systems, this skew may be too large.

Figure 2–43 contains propagation-delay skews for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for low-to-high and high-to-low transitions.

The difference in the results presented in **Figure 2–43** is not particularly significant. Although there is a difference between the families, the magnitude of the difference is probably not large enough to significantly impact a particular application.

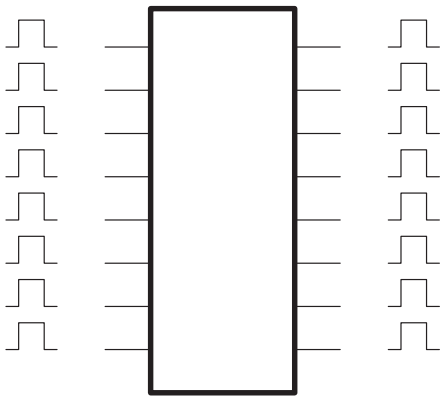
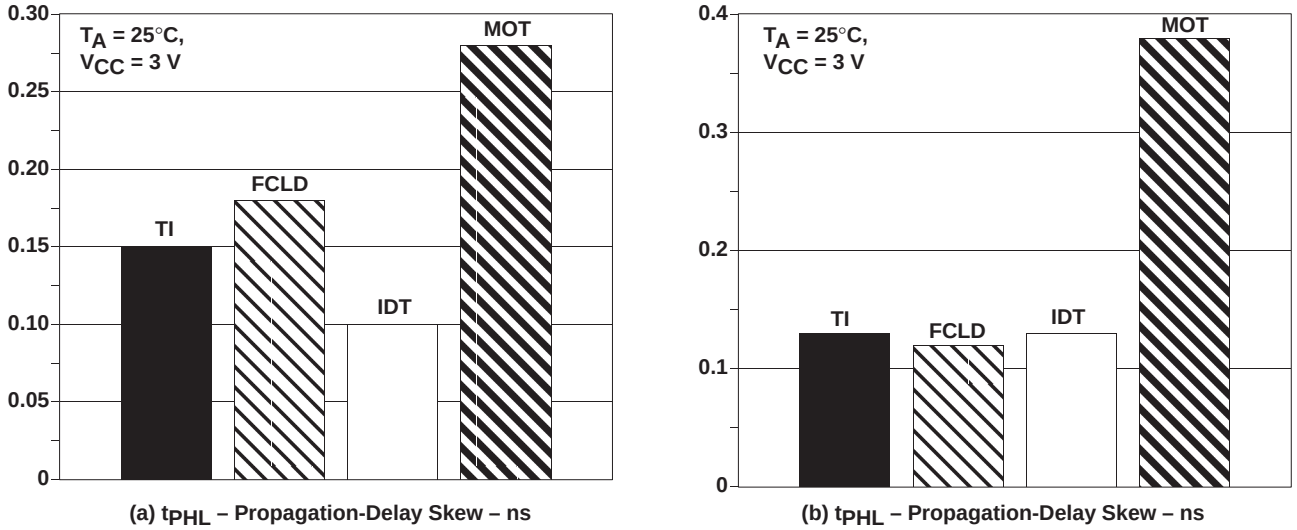


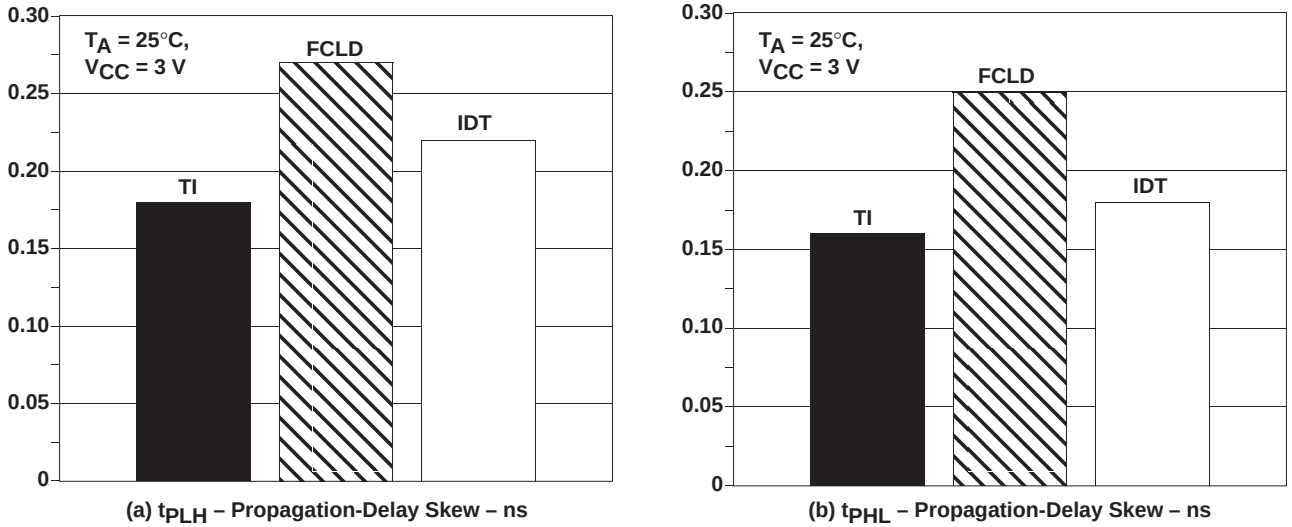
Figure 2–41. Test Setup for Propagation-Delay Skew



(a) t_{PHL} – Propagation-Delay Skew – ns

(b) t_{PHL} – Propagation-Delay Skew – ns

Figure 2–42. ’245 Propagation-Delay Skew



(a) t_{PLH} – Propagation-Delay Skew – ns

(b) t_{PHL} – Propagation-Delay Skew – ns

Figure 2–43. ’16245 Propagation-Delay Skew

OUTPUT-TO-OUTPUT SKEW

Output-to-output skew indicates the variance in the output switching times. This measurement for skew is fairly common and, as a general rule, is much more meaningful than the propagation-delay skew. If an application has a requirement for a minimum amount of skew, this is probably the parameter with which the engineer is concerned. When conducting this test, the inputs were tied together and switched and the difference in the outputs was subsequentially computed; for comparison purposes, competitors have labeled this value T_{SKO}. **Figure 2–44** illustrates the method in which this test was conducted.

Figure 2–45 contains propagation-delay skews for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Separate graphs are provided for low-to-high and high-to-low transitions.

The difference in the results presented in both graphs in **Figure 2–45** represent a difference of 210 ps, which, depending on the application, may be significant.

Figure 2–46 contains propagation-delay skews for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for low-to-high and high-to-low transitions.

The 160-ps difference presented in **Figure 2–46**, graph (b) may be significant. An application example of when this amount of skew may be too large, is if the device is being used for clock distribution or for high-frequency data buffering.

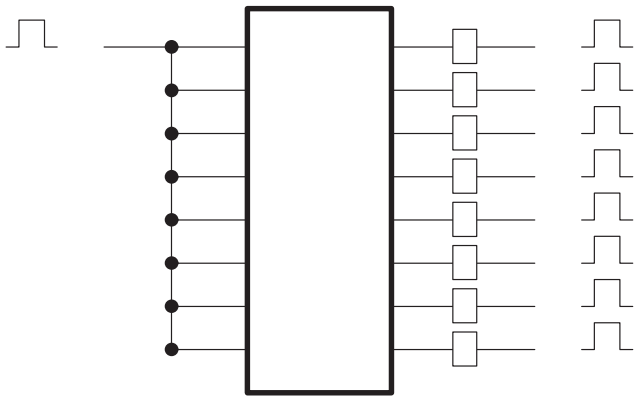
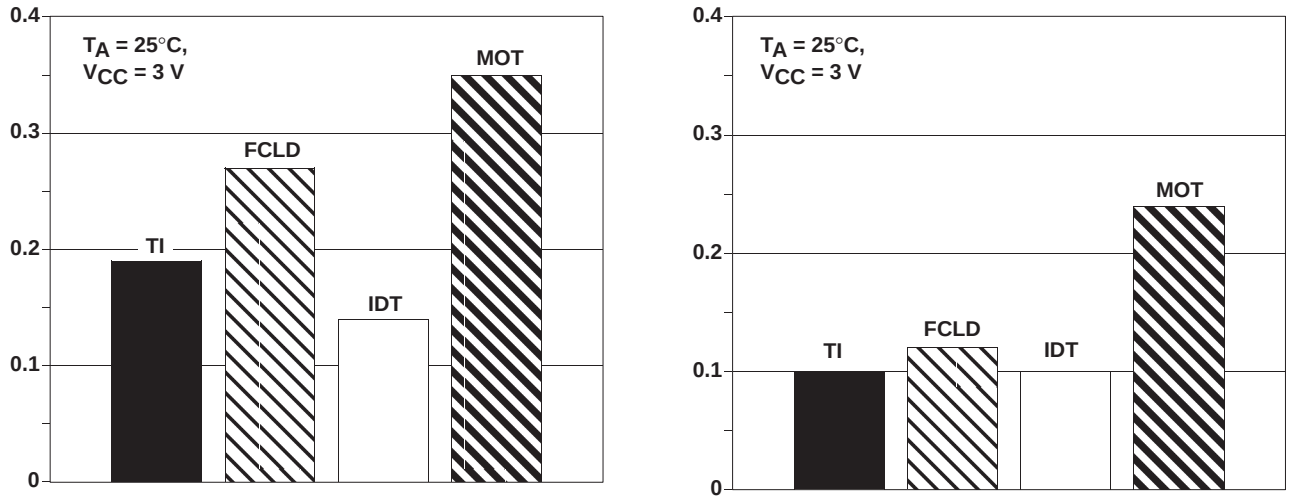


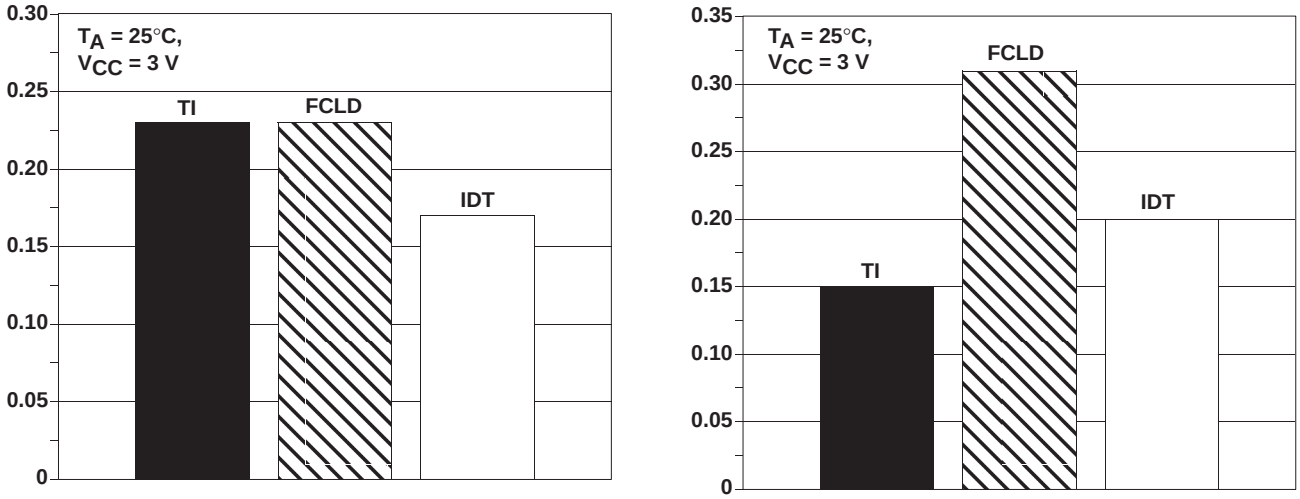
Figure 2–44. Test Setup for Output-to-Output Skew



(a) t_{PLH} – Output-to-Output Skew – ns

(b) t_{PHL} – Output-to-Output Skew – ns

Figure 2–45. ’245 Output-to-Output Skew



(a) t_{PLH} – Output-to-Output Skew – ns

(b) t_{PHL} – Output-to-Output Skew – ns

Figure 2–46. ’16245 Output-to-Output Skew

DYNAMIC-SWITCHING LEVELS

The dynamic-switching-level test was set up by clocking data from a low-to-high state into the device and sequentially lowering the magnitude of the input voltage until the output no longer switched; this parameter is known as V_{IHD} and is the minimum high level input for which the output responds normally. The ideal situation is for the device to switch at 1.5 V; theoretically, below 1.5 V, the device should not switch. The converse test was then performed. The data was clocked from a high-to-low state and the magnitude of the input voltage was sequentially decreased until the output no longer switched; this parameter is known as V_{ILD} and is the maximum low level input for which the output behaves normally. Ideally, this value should also be 1.5 V and theoretically, above 1.5 V, the device should not switch.

Figure 2–47 contains values for which the output no longer transitioned from a low state to a high state for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Separate graphs are provided for data and control pins.

Both graphs in **Figure 2–47** are relatively close to the threshold of 1.5 V; the difference between the logic families from an applications perspective is not really significant.

Figure 2–48 contains values for which the output no longer transitioned from a low state to a high state for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for data and control pins.

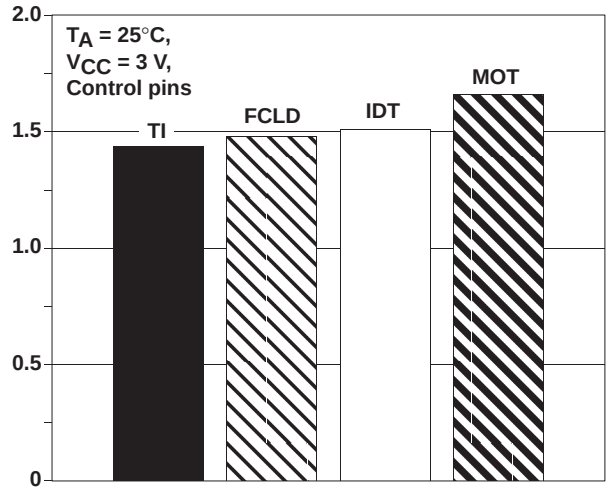
The difference in results in **Figure 2–48** are not particularly significant from an applications perspective.

Figure 2–49 contains values for which the output no longer transitioned from a high state to a low state for TI's LVC245, FCLD's LCX245, IDT's FCT3245, and Motorola's LCX245. Separate graphs are provided for data and control pins and the difference in magnitude presented in the graphs is not significant from an applications perspective.

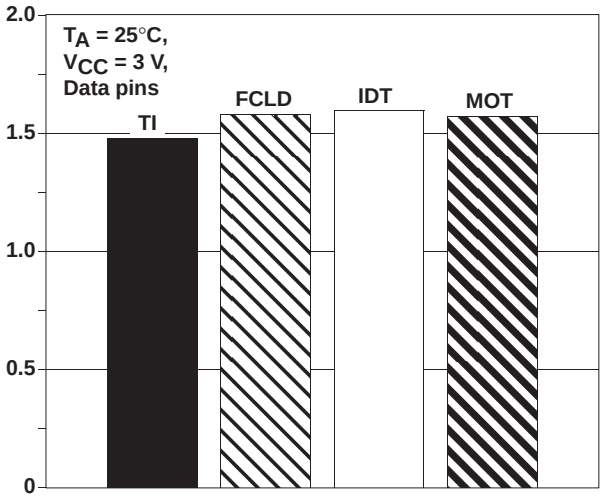
Figure 2–50 contains values for which the output no longer transitioned from a high state to a low state for TI's LVC16245, FCLD's LCX16245, and IDT's FCT163245. Separate graphs are provided for data and control pins and the difference in magnitude presented in the graphs is not significant from an applications perspective.

Another method of viewing this data is presented in **Figure 2–51**, where graphs of the output voltage versus the input voltage are presented.

In graph (b) of F**igure 2–51**, IDT's FCT163245 is switching more accurately than the other devices tested. From an applications perspective, these differences are relatively insignificant.

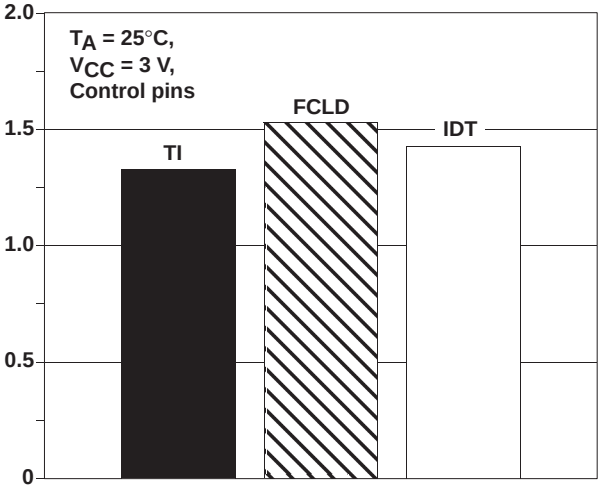


(a) ’245 – Dynamic-Switching Levels

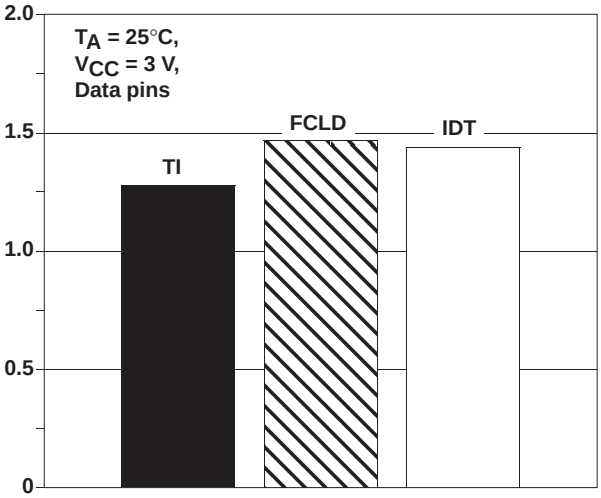


(b) ’245 – Dynamic-Switching Levels

Figure 2–47. ’245 V_{IHD} for Control and Data Pins

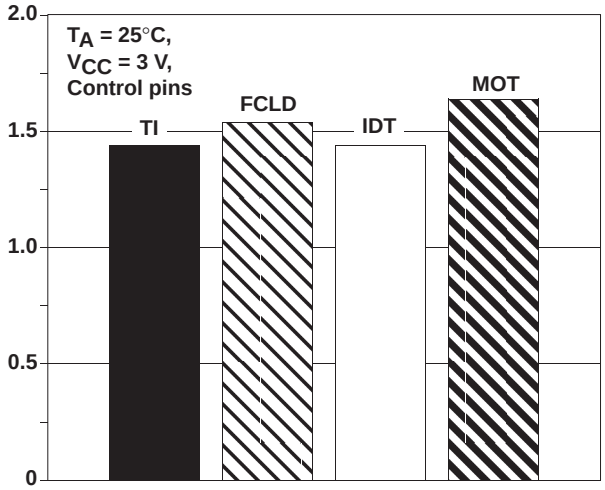


(a) ’16245 – Dynamic-Switching Levels

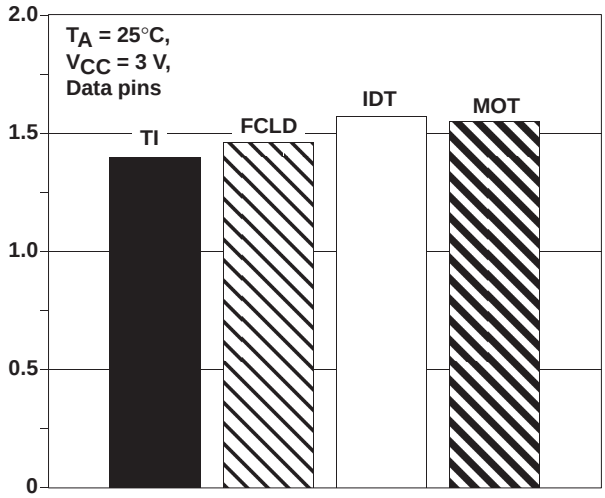


(b) ’16245 – Dynamic-Switching Levels

Figure 2–48. ’16245 V_{IHD} for Control and Data Pins

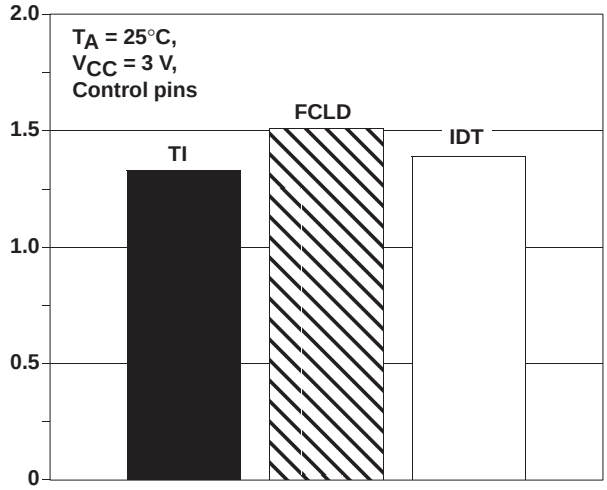


(a) ’245 – Dynamic-Switching Levels

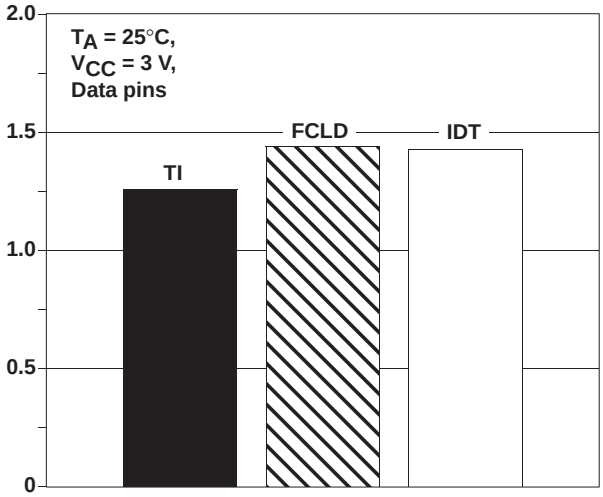


(b) ’245 – Dynamic-Switching Levels

Figure 2–49. ’245 V_{ILD} for Control and Data Pins

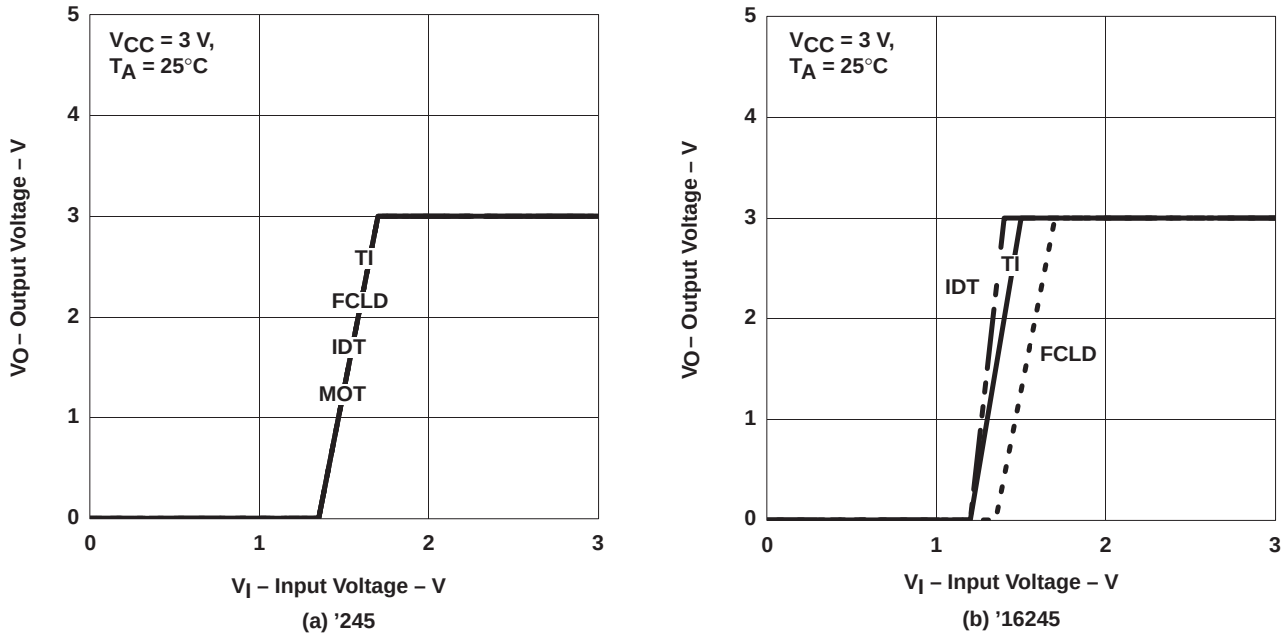


(a) ’16245 – Dynamic-Switching Levels



(b) ’16245 – Dynamic-Switching Levels

Figure 2–50. ’16245 V_{ILD} for Control and Data Pins



MANUFACTURER	IDENTIFICATION
Texas Instruments (TI)	
Fairchild (FCLD)	
Integrated Device Technology (IDT)	
Motorola (MOT)	

Figure 2–51. Output Voltage Versus Input Voltage

CONCLUSION

Tables 2–10 and 2–11 contain a summary of the testing results. A plus sign (+) indicates desirable characteristics, a zero (0) indicates average characteristics, and a negative sign (–) indicates unfavorable characteristics.

Table 2–10. ’245 Device Summary

MEASUREMENT	TI	FCLD	MOT	IDT
t_{pd}	+	0	0	0
I_{CC}	0	0	+	0
V_{IO}	+	+	+	–
Slew rate	+	+	0	–
Simultaneous switching	+	+	–	+
Output drive	0	+	+	–
Skew T_{os}	+	+	–	+
Skew $T_{sk(o)}$	+	0	–	+
Dynamic switching	+	+	+	+

Table 2–11. ’16245 Device Summary

MEASUREMENT	TI	FCLD	IDT
t_{pd}	0	0	0
I_{CC}	0	0	+
V_{IO}	+	+	–
Slew rate	0	0	–
Simultaneous switching	+	+	+
Output drive	0	+	0
Skew T_{os}	+	0	+
Skew $T_{sk(o)}$	+	0	+
Dynamic switching	+	+	+

Acknowledgements

This section was written by Steven Culp, ABL applications engineering.

APPENDIX A
LVC AND 5-V TOLERANCE

Since the LVC family uses a 3.3-V power supply, interfacing LVC devices with other components that use a 5-V power supply becomes a concern. If a low-voltage device is subjected to a 5-V presence at its inputs or outputs, it is critical that the device is not damaged. The term 5-V tolerance is used to imply that a presence of 5-V at either the input or output of a device will not damage it. Whether a device is capable of tolerating a 5-V presence only at the input, only at the output, or at both the input and output must be considered. As a result, when determining whether a device is considered to be 5-V tolerant, several issues must be addressed.

Every LVC device TI produces can be subjected to a 5-V presence at its input and not be damaged. This includes all of the gate-function, octal, and Widebus™ devices. Thus, all of TI's LVC devices are 5-V input tolerant.

Whether or not an LVC device can be subjected to a 5-V presence at its output requires further consideration. For the term 5-V output tolerant to be meaningful, the outputs of the device must be capable of being placed in the high-impedance state. Two LVC gate functions, all LVC octals, and all LVC Widebus™ devices have 3-state outputs, and it is to these devices only that the term 5-V tolerance applies. (The LVC gate functions that do not have 3-state outputs should not be connected to a bus and, therefore, should not be subjected to a 5-V presence. This means that 5-V output tolerance does not make sense for these devices since their outputs cannot be placed in the high-impedance state.) For those devices with outputs capable of being placed in the high-impedance state, 5-V output tolerance means that a presence of 5 V at its output does not damage the device.

TI is naming all 5-V tolerant devices with an A after the device number. For example, LVC16245A indicates that the device is 5-V tolerant. All LVC devices are 5-V input tolerant, and an A in a device name indicates that, if appropriate, the device is also 5-V output tolerant.

TI has released 33 devices that are 5-V tolerant. They are:

LVC Gates:
00A, 02A, 04A, U04A, 08A, 10A, 14A, 32A, 74A, 86A, 138A, 157A
These gates are 5-V input tolerant. Their outputs are not capable of being placed in the high-impedance state.

LVC Gates With 3-State Outputs:
125A, 257A
These gates are 5-V input tolerant. Their outputs are capable of being placed in the high-impedance state. TI plans to release these devices in 5-V output tolerant versions.

LVC Octals:
244A, H244A, 2244A, 245A, R2245A, H245A, 373A, 374A, 573A, 574A
These octals are 5-V input tolerant and 5-V output tolerant.

LVC Widebus™:
H16240A, 16244A, H16244A, 16245A, H16245A, H16373A, H16374A, H16540A, H16541A
These Widebus™ devices are 5-V input tolerant and 5-V output tolerant.

To summarize, all LVC devices are 5-V input tolerant and all LVC octal and Widebus™ devices with outputs capable of being placed in the high-impedance state are 5-V output tolerant (e.g., LVCXXXA).

Widebus is a trademark of Texas Instruments Incorporated.

33 LVC DEVICES IN PRODUCTION NOW†

LVC00A	LVC157A	LVCH16240A
LVC02A	LVC244A	LVC16244A
LVC04A	LVC2244A	LVCH16244A
LVCU04A	LVCH244A	LVC16245A
LVC08A	LVC245A	LVCH16245A
LVC10A	LVCH245A	LVCH16373A
LVC14A	LVCR2245A	LVCH16374A
LVC32A	LVC257A‡	LVCH16540A
LVC74A	LVC373A	LVCH16541A
LVC86A	LVC374A	
LVC125A‡	LVC573A	
LVC138A	LVC574A	

† As of September 1996
‡ These devices have 3-state outputs, but are only 5-V tolerant on the inputs.

APPENDIX C
FREQUENTLY ASKED QUESTIONS

Question 1: *What should I do if it appears that the device is producing a noisy signal?*

Answer: The most common reason an LVC device may appear to be producing a noisy signal is if the outputs have not been terminated properly. To reduce or eliminate reflections that are inherent with long trace lengths and transmission lines, one of five techniques must be used to match the impedance of the transmission line and thereby properly terminate the output. These five techniques are: single resistor, split resistor, resistor and capacitor, series resistor, and diode. See *Proper Termination of Outputs* in **Section 1** for a more detailed explanation of the techniques and the advantages and disadvantages of each method.

Question 2: *Is the LVC family 5-V tolerant?*

Answer: Yes. TI has released the most 5-V tolerant devices in the industry for the LVC (or competitor's equivalent) logic family. TI plans to continue releasing 5-V tolerant devices in 1996 and 1997.

Question 3: *Does the LVC family have the bus-hold feature?*

Answer: Some LVC parts have the bus-hold feature and others do not. The easiest way to determine if a particular device has bus hold is by the name of the device. If an H is present in the name; e.g., LVCH as opposed to LVC, then it does have bus hold. Another way to tell if bus hold has been implemented on a particular device is to examine the data sheet. If an $I_{I(hold)}$ specification is provided, then the part has bus hold.

Question 4: *Can I leave unused inputs floating?*

Answer: For an LVC part that does not have the bus-hold feature, unused data inputs and outputs enable control lines must be tied high to V_{CC} or low to GND via a resistor; a resistor value of around 1 kΩ is usually recommended. If a device has the bus-hold feature, then the unused data inputs do not require being tied high or low. See question 3 to determine if a device has the bus-hold feature.

Question 5: *What is the difference between LVC and LVCH, and also ALVC and ALVCH?*

Answer: LVCH indicates that a device has the bus-hold feature, whereas a part named LVC does not. The same applies to ALVC and ALVCH. Therefore, when referring to the family as a whole, the term ALVC is used, but when referring to an individual device, the term ALVCH is used.

Question 6: *Does the LVC family have built-in damping resistors on the outputs?*

Answer: Some LVC parts have built-in damping resistors and others do not. The easiest way to determine if a device has built-in damping resistors is by the name of the device. If the name has an additional 2, then the device has the built-in series damping resistors; if the name does not have an additional 2, then the device does not have them. Additionally, if the device name has an additional R as well as an additional 2, then the device in question is a bidirectional device and the series damping resistors are on both ports. (Only the series damping resistors on the output port, whether it be port A or port B, affect the operation of the device.) For example, the SN74LVC2244 is a unidirectional device that has built-in series damping resistors on the outputs, and the SN74LVCR2245 is a bidirectional device that has built-in series damping resistors on both A and B ports.

Question 7: *What is a split-rail device?*

Answer: A split-rail device has two different power supply pins on it. One side of the chip operates at V_{CCA} and the other side operates at V_{CCB}. In the LVC logic family, split-rail devices have V_{CCA} and V_{CCB} equal to 5 V and 3.3 V (this does not imply that the A port is always 5 V and the B port is always 3.3 V; they can be reversed, depending on the device).

LVC Comparison to Other LVL Families

To understand where LVC is positioned relative to TI's other low-voltage families, see **Figure D–1**, which graphs I_{OL} versus t_{pd} for LV, LVC, ALVC, and LVT. LVC is a medium-speed logic family with a medium-drive capability. Additionally, the output drive of 64 mA for the LVT family is due to the bipolar circuitry in its output stage. Only LVC and LVT are 5-V tolerant.

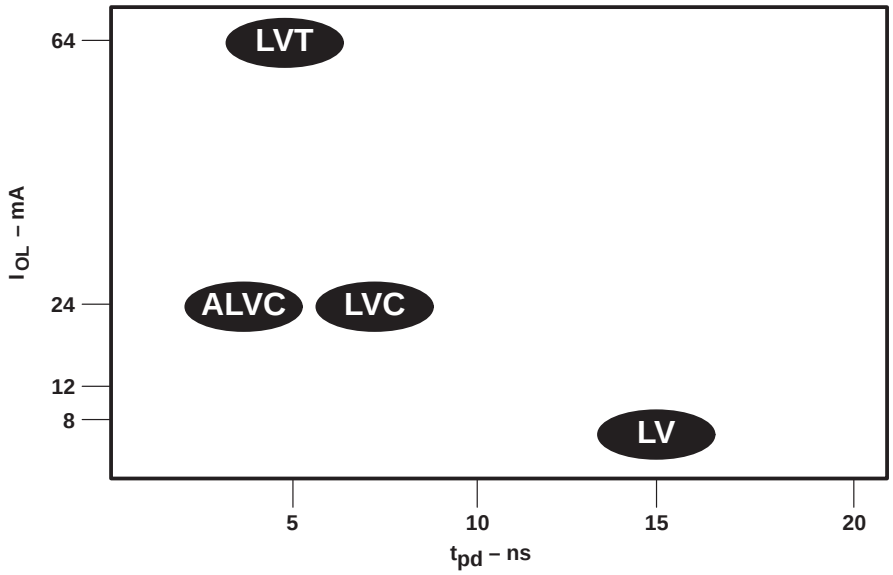


Figure D–1. Low-Voltage Product Positioning

Table D–1 provides a further comparison of specific family features.

Table D–1. LV, LVC, ALVC, and LVT Feature Comparison

PRODUCT FAMILY		LV	LVC	ALVC	LVT
Technology		CMOS	CMOS	CMOS	BiCMOS
5-V tolerant		No	Yes	No	Yes
Octals and gates		Yes	Yes	No	No
Widebus™		No	Yes	Yes	Yes
Bus hold		No	Yes†	Yes	Yes
Damping resistors		No	Yes†	Yes†	Yes†
C_{pd}	’244	40 pF	30 pF	N/A	N/A
	’16244	N/A	20 pF	19 pF	N/A
I_{CC}	’244	20 μA	10 μA	N/A	12 mA
	’16244	N/A	20 μA	40 μA	5 mA
ΔI_{CC}	’244	500 μA	500 μA	N/A	200 μA
	’16244	N/A	500 μA	750 μA	200 μA
dc output drive		–8 mA/8 mA	–24 mA/24 mA	–24 mA/24 mA	–32 mA/64 mA
t_{pd}	’244	14 ns	6.5 ns	N/A	4.1 ns
	’16244	N/A	5.2 ns	3.6 ns	4.1 ns
C_i	’244	3 pF	3.1 pF	6 pF	4 pF
C_o	’244	8 pF	5 pF	9 pF	8 pF

† Selected functions only

Widebus is a trademark of Texas Instruments Incorporated.

APPENDIX E
ADVANCED PACKAGING

Figure E–1 shows a comparison of the various packages in which LVC devices are available; for ease of analysis, 24-pin packages and 48-pin packages are included. (**Figure E–1** is not an all-inclusive list of pin counts and corresponding packages; e.g., the TSSOP package is available in both 20-pin and 24-pin format). Continued advancements in packaging are making more functionality possible with smaller space requirements.

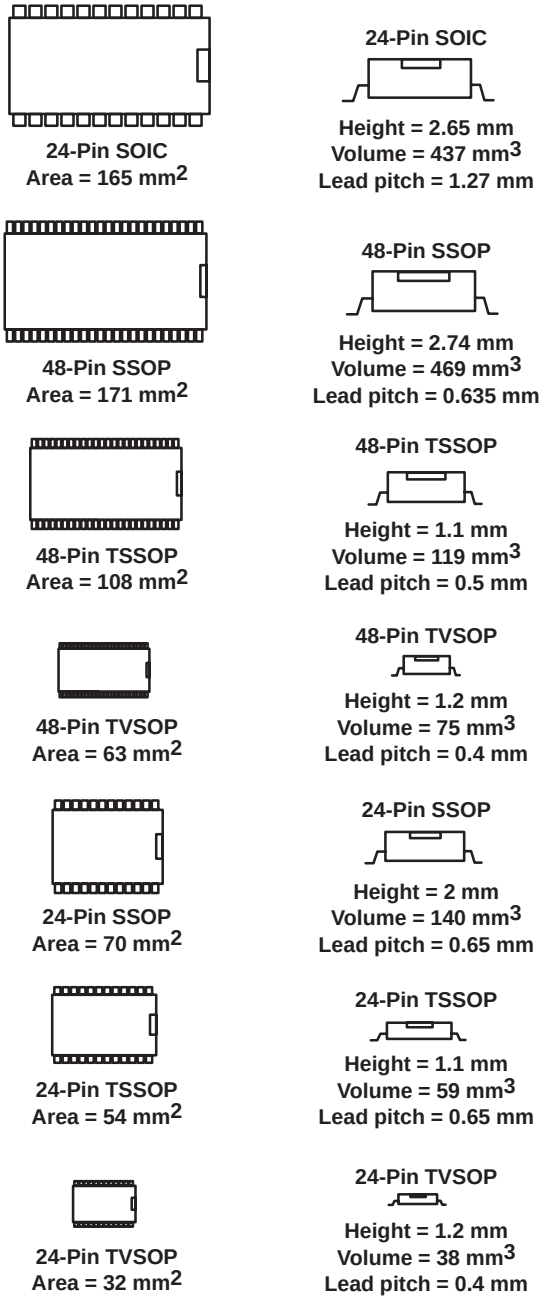


Figure E–1. LVC Packages

Figure E–2 shows a typical pinout structure for the 48-pin SSOP for the SN74LVC16245A. The flow-through design promotes ease of board layout and the GND and V_{CC} pins are distributed throughout the chip. This provides for simultaneous switching improvements (see *Signal Integrity in* **Section 1**).

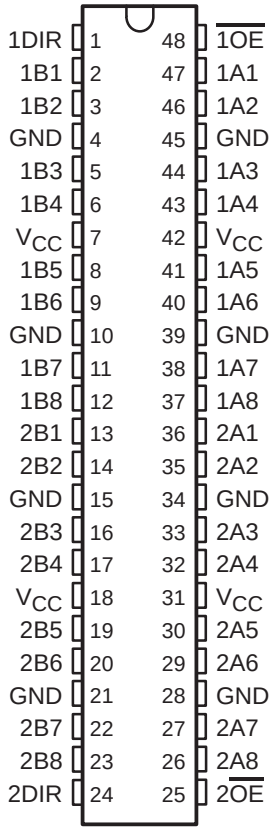


Figure E–2. SN74LVC16245A Pinout

For a comprehensive listing and explanation of TI's packaging options, consult the *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001B.