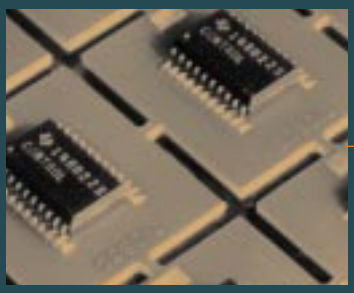
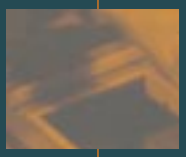
Texas Instruments





Palladium Lead Finish User's Manual

Douglas W. Romm

Introduction

Texas Instruments has introduced a revolutionary new lead finish into the Semiconductor industry. This plating technology consists of a copper base metal plated with nickel and palladium. The palladium acts as an oxidation barrier for the nickel which is the actual soldering surface. This palladium leadframe technology has replaced Sn/Pb coating for the majority of TI logic and linear devices.

The purpose of this document is to educate the user of palladium lead finish integrated circuit devices. Information is included which provides the background of this new lead finish. Solderability test issues are discussed in detail in section II. Topics concerning actual board mount of palladium devices are discussed in section III. Finally, the future with palladium lead finish is covered.

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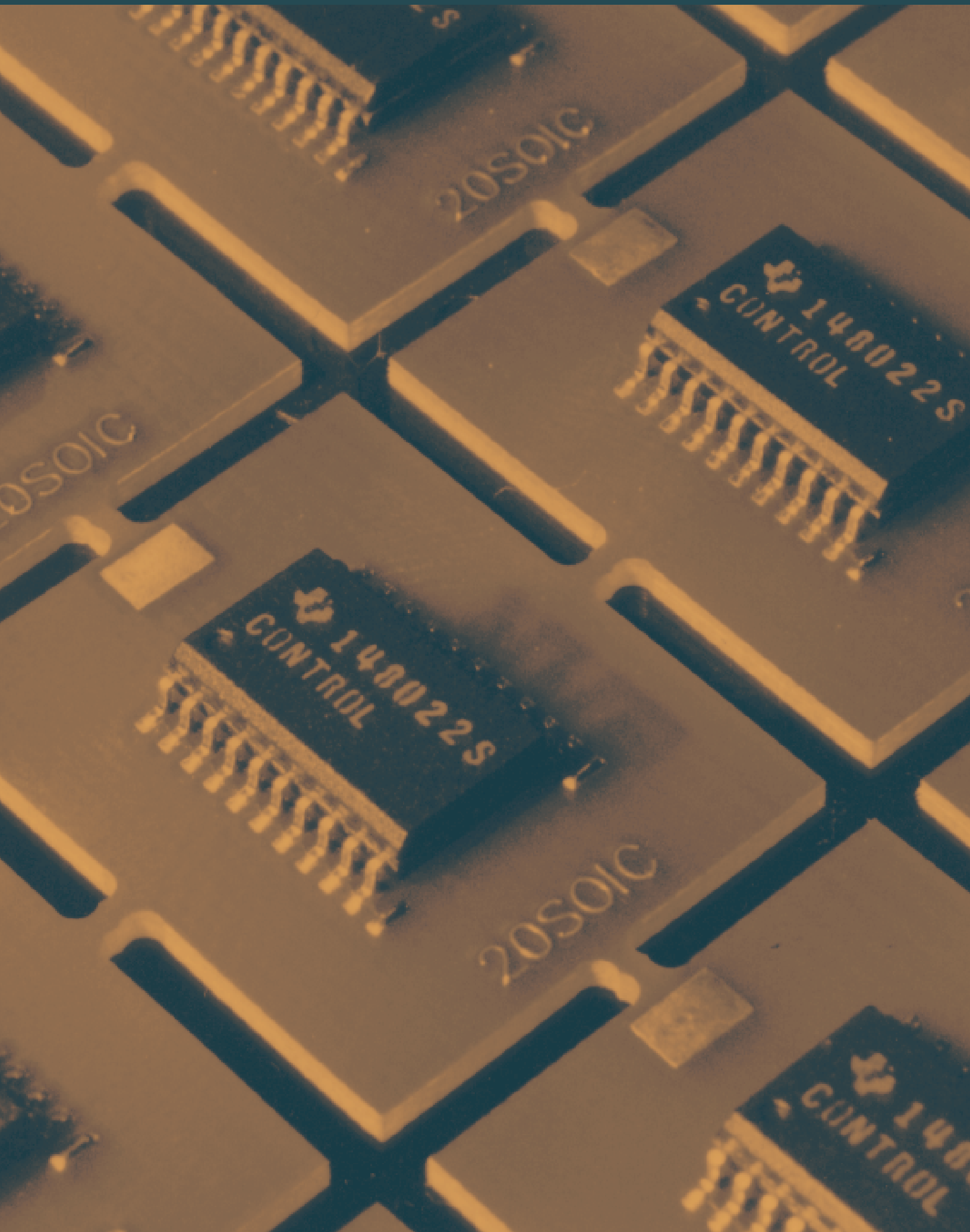
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Development

In 1989 Texas Instruments introduced palladium lead finish for integrated circuit devices. This finish was introduced to replace traditional Sn/Pb solder coatings. TI has developed a palladium pre-plating process for leadframes which has proven to have many advantages over Sn/Pb. A palladium plated leadframe is composed of a copper base metal, 40-60 microinches of nickel and 3 microinches of palladium (see figure 1).

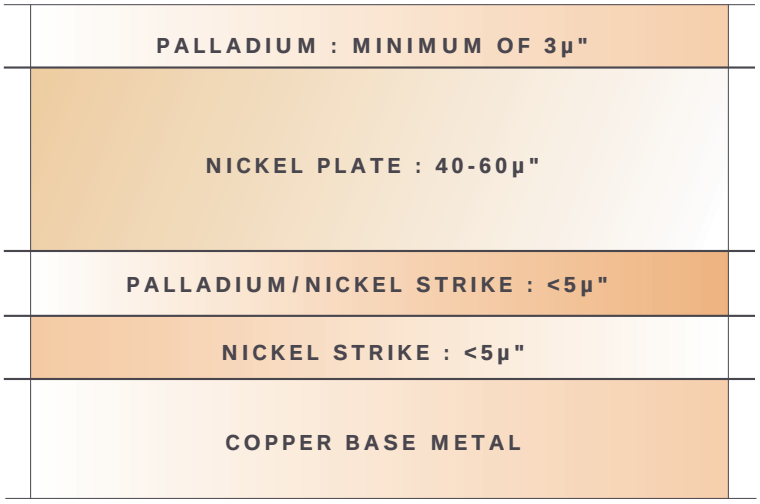


FIGURE 1 : Structure of TI Palladium Lead Finish

Palladium has several roles in the functionality of the finished IC package. The key role is to protect the underlying nickel plate from oxidation during the assembly process and during storage prior to use. Palladium, as a noble metal is well suited for this purpose. Also, since the stitch bond (the bond adjoining the wire to the leadframe) is now made directly to the nickel surface through the palladium instead of to a silver spot all silver is eliminated from the package. This eliminates the risk of silver migration causing extraneous electrical contacts.

Prior to the development of the palladium lead finish the majority of TI products used a Sn/Pb solder dipped lead finish. This finish was not practical for fine pitch devices (0.025” lead pitch or less). A search was undertaken in 1986 to

find an appropriate lead finish to replace solder dip. The option of solder plating was not chosen because of the corrosive chemicals in the plating solutions. The pre-plated palladium lead finish was developed within TI and was found to offer numerous advantages compared to Sn/Pb. Advantages for both assembly and end use are:

Eliminates Sn/Pb plating after molding

No solder flakes or burrs at the trim/operation

Conformal coating minimizes handling transport jams

Excellent adhesion for mold compound in most cases

Improved lead tip planarity versus Sn/Pb

Reduces assembly manufacturing cycle time

Excellent solderability of finished package

The initial concept of the palladium lead finish was developed in 1986 with extensive testing performed through 1987. Joint studies were performed with key computer and telecommunications customers in 1987. In 1989, TI's customer base was notified of the change to palladium lead finish. TI converted Small Outline Integrated Circuit (SOIC) packages in 1989 and Plastic Dual In-line (PDIP) packages in 1990. The Shrink Small Outline Package (SSOP) was developed in 1990 and was introduced in palladium lead finish. At this writing in October '94, TI has more than 7 billion palladium plated devices in the field.

The palladium serves to prevent oxidation of the nickel. During the soldering operation, the palladium dissolves into the solder and the solder joint is actually made with the underlying nickel plate. The dissolution rate of palladium in Sn/Pb solder is dependent upon the temperature of the solder (see Table 1). The dissolution rates for palladium indicate that in a typical solder reflow operation

TABLE 1 : Dissolution Rate of Palladium in Solder

SOLDER TEMPERATURE	Pd DISSOLUTION RATE
215C	0.7 µ"/sec
250C	2.8 µ"/sec

the palladium will be completely dissolved into the solder allowing the joint to be made to the nickel underlayer.

Palladium Plating Process

The process for palladium plating the leadframes described here consists of several steps: clean, activate, (proprietary, relatively thick, low porosity, nickel rich, barrier layer(s)), activate, and finally palladium plate. After each step there is appropriate rinsing.

The cleaning step removes stamping oil and light soil and is typical of that found in leadframe plating lines for silver spot plating. The first activation step reduces surface oxides and provides a surface compatible for deposition of the barrier layer(s) that follows. Particular care must be taken to plate a low stress and ductile nickel rich barrier layer, as the forming of the leads can cause cracking in nickel deposits.

The second activation step provides a surface ionically similar to the palladium plating bath and gives a fully reduced surface for plating. This is important to insure excellent adhesion of the palladium to the barrier layer and to minimize contamination of the palladium bath. Because the palladium layer is very thin, the microscopic appearance of the IC leadframe is dictated by the surface of the nickel barrier layer.

There are several operational advantages the palladium plating process has over conventional silver spot plating. First, there are no cyanides in this process. This eliminates significant safety issues and waste treatment costs. Second, since this is a flood or full plate process, there are no spot tooling costs. Plating line design and construction are relatively simple (no masking/timing issues). Third, product changeovers from one part number to another require zero down time.

Consistency and Control of Pd Plating Thickness

Pd thickness is controlled to provide a minimum of 3 microinches. To accomplish this, TI utilizes two techniques, both of which provide real-time process control on the reel-to-reel Pd plating lines.

The first is an in-line, X-ray fluorescence unit on every plating line which monitors Pd thickness at the end of the line. X-bar/R charts are maintained for each plating line with the newest lines having the capability to download XRF data automatically to a computer for SPC purposes.

The second technique is a computer controlled unit which monitors current, voltage, and plating line speed. With Faraday's Law, one can correlate these parameters with palladium thickness. If any monitored inputs begin to move outside a "normal" control range into a "yellow" control range, an alarm will sound to alert the operator. If parameters move into a "red" zone indicative of an out-of-specification condition, the line will automatically shut down.

Plating parameter files are maintained for each TI leadframe part number. To generate a parameter file, Pd thickness is mapped over a leadframe strip to ensure all areas on the leadframe get the minimum 3 microinches of Pd. Once the file is set, the plating operator types in the leadframe part number and the various parameters download to all the rectifiers. Together, these procedures ensure that all outgoing material meets the specification.

Suppliers

At this writing in October '94, there are three leadframe suppliers licensed to manufacture the TI nickel/palladium lead finish. They are:

- *TI Electronic Products Division*
- *Shinko*
- *Kyushu Matsushita (KME)*

EPD and Shinko are both licensed to sell palladium leadframes to TI as well as any other customers. KME is licensed to sell palladium leadframes to TI

only. There are ongoing efforts to license other leadframe suppliers with TI's proprietary (patent pending) Ni/Pd plating technology.

Evaluation Tests

Gold Wire Bond Reliability

Prior to use of palladium leadframes the gold wire bond was made to a silver spot on the nickel or bare copper leadframe. With this new leadframe technology, the wire bond is made directly to the surface of the nickel through the palladium, eliminating the need for a silver spot. The mechanical strength of the gold wire bond made to the palladium leadframe was compared to the strength of the wire bond made to silver spot leadframes. The wire bond tests included samples as made and also samples aged at 200°C for 168 hours. Test criteria included pull strengths and failure modes. There was no statistical difference between the control and palladium groups in the 100 wire samples tested (see Table 2). The reliability of the gold wire bonds was unaffected by the palladium plating.

TABLE 2 : Reliability of Gold to Palladium Wire Bonds (Wire Pull Test)

	Average (gm)	Standard Deviation (gm)	Ball	Neck	Span	Stitch
3µ in. Pd	7.81	1.57	0	73	27	0
3µ in. Pd (Aged)	6.81	1.15	0	8	92	0
Control	7.76	1.21	0	52	48	0
Control (Aged)	7.17	0.97	0	10	89	1

Aging: 200C for 168 hours; Sample size = 100 wires

Palladium Leadframe Adhesion to Mold Compound

Recent investigations have discovered a link between package integrity (as measured by the mold compound to leadframe member adhesion) and the reliability of the component. Palladium has a high surface free energy compared to most materials; therefore, superior adhesion to most mold compounds is predictable. In order to test this hypothesis, special molded units with pull-out tabs were assembled using a typical mold compound. The results of the pull tests are shown in Table 3.

The results indicate a much better adhesion performance for Pd plated samples, especially on copper base metals.

TABLE 3 : Palladium Adhesion to Mold Compound

SAMPLE	AVG	STD	LOW
Cu Cu	24.9 lb	10.5 lb	12.0 lb
Cu Pd	42.8 lb	2.1 lb	38.5 lb
DELTA %	72%	80%	221%
A 42	49.0 lb	3.8 lb	39.0 lb
A 42 Pd	60.1 lb	3.2 lb	53.0 lb
DELTA %	23%	16%	36%

Board Flex Testing of Palladium SOIC Packages

Solder joint fatigue was investigated using a special fixture that flexed a daisy chain board around a blade with a 50.8cm radius. A daisy chain board is designed to have a sequential electrical connection through the board mounted IC device starting with “Pin 1”. This allows for continuity testing through all pins of the board mounted devices. Eight continuity test flex boards were each assembled with 20 pin SOIC devices (54 units per board). Palladium devices

were mounted on four of the boards while solder dipped parts were mounted on the other four boards for comparison. Boards were run for 1150 cycles. To test for intermetallics and/or poor solder joints, some boards were populated with 8-hour steam aged devices and some board assemblies were aged for one week at 125°C. No breaks in the daisy chain were observed in the flexed or the straight position for any of the samples. The results indicate that palladium SOIC packages will not experience problems due to mechanical or thermal stress failures.

Filament Growth Testing

Testing was performed in order to determine whether palladium dendrites will grow in the presence of moisture and high bias. Palladium PDIP packages were stored in an 85°C/85% relative humidity environment with alternate leads biased at 50 V for one week. Following this exposure, a microscope search was made to visually locate any dendritic growths that may have been induced by the voltage/humidity conditions. Microscope search for partial or whole dendrites concluded that filament growth did not occur.

Solder Joint Strength

Pull tests were performed in order to determine the quality of palladium solder joints on the basis of mechanical strength. For this test, joint strength was measured by isolating the soldered lead and then pulling it away from the board with a force test chuck. Results are shown in Table 4.

TABLE 4 : Lead Pull Results for Palladium Solder Joints After Heat Aging

Sample	0 hrs	8 hrs	16 hrs	24 hrs
3µ" Palladium	5.17 lbf	5.95	5.85	4.71
Solder Dip Control	5.07	4.51	5.55	5.50

The sample size for this test was 20 leads per group. These results demonstrate equal performance for solder dip and palladium solder joint strengths. Minimum pull strengths for all groups were >3.0lbs.

Dye Penetration Tests

Dye penetration tests were performed to compare palladium plated SOIC devices with solder dipped components. The 20 pin SOIC devices saw dye exposure (FL-50 dye) for 4 hours at 620 KPA followed by bake for 1 hour at 120°C. Results are shown in Table 5. These results show the improved ability of the palladium to minimize contaminant's moving along the plastic-lead interface when compared to a typical Cu/Ag spot leadframe with solder dipped lead finish.

TABLE 5 : Dye Penetration Results

Sample	Sample Size/ # Showing Dye Penetration
Cu/Ag Spot	14/11
Palladium Plated	14/0

Environmental Tests

Reliability Tests

Tables 6 and 7 show the reliability test results completed through extended test periods for palladium PDIP and SOIC packages. This data compares favorably with product built with solder dipped leads.

TABLE 6 : Environmental Test Data for Bare Palladium Dual In-Line Packages

Test	Sample Size	Read Point	ALS00	ALS174	LS245	ALS245	75154	TL082
HTRB 150	129	168	0	0	0	0	0	0
		500	0	0	0	0	0	0
		1000	0	0	0	0	0	0
BIAS 85/85	129	168	0	0	0	0	0	0
		500	0	0	0	0	0	0
		1000	0	0	0	0	0	0
Temp Cycle (-65/+150°C)	195	100	0	0	0	0	0	0
		500	0	0	0	0	0	0
		1000	0	0	0	0	0	0
Thermal Shock (0/100)	129	100	0	0	0	0	0	0
		500	0	0	0	0	0	0
		1000	0	0	0	0	0	0
Autoclave (121/15)	77	240	0	0	0	0	0	0
		500	0	0	0	0	0	0
		1000	0	0	0	0	0	0
Solderability (No Aging)	22	0	0	0	0	0	0	0
Solderability (8 hrs steam)	32	8	0	0	0	0	0	0
Solderability (168 hrs/125°C)	32	8	0	0	0	0	0	0
Salt Atmos.	22	24	0	0	0	0	0	0

TABLE 7 : Environmental Test Data for Bare Palladium SOIC Packages

Test	Sample Size	Read Point	373DW	7406D	S373DW	ALS04D	S05D	ALS244DW
OP LIFE	129	500 1000 2000		0 0 0				
HTRB 150	129	500 1000 2000	0 0 0		0 0 0	0 0	0 0	0 0
Storage 150	45	500 1000				0 0	0 0	0 0
Bias 85/85	129	500 1000 1500 2000	0 0 1* 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0
Temp Cycle -65/+150	195	100 500 1000	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
Autoclave (121/15)	77	240 500 750 1000 2000	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0
Solderability (8 hrs steam)	10	8	0	0	0	0	0	0
Lead Adhesion	15		0	0	0	0	0	0
Salt Atmos.	22	24	0	0	0	0	0	0

*ESD Failure

Initial Customer Feedback

A major TI customer in Colorado tracked solder joint repair on its board mount assembly process to compare repair rates before and after the conversion to TI palladium lead finish. Figure 2 graphically shows the data in Table 8. This customer made the conversion to palladium devices in May 1989. From the data and graphs, it can be seen that the solder joint repair rate (ppm) for TI palladium devices was approximately half that of the Sn/Pb devices after conversion. Similar comments have been made by other customers upon conversion to TI palladium lead finish devices.

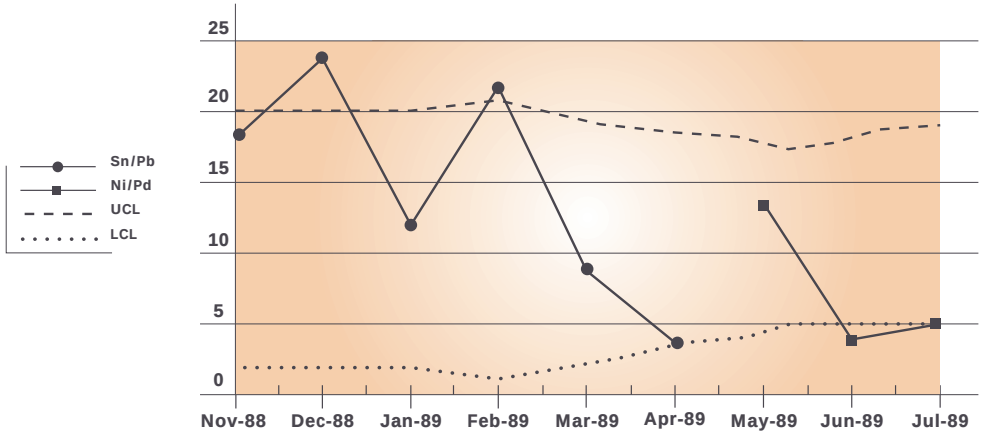


FIGURE 2 : Customer Qualification of TI NI/Pd Solder Joint Repair Rate in PPM

TABLE 8 : Solder Joint Defects (Nov 88 – July 89)

	Joint Defects	Part Volume	Joint Volume	Joint Defect (PPM)
Sn/Pb	119	425023	8500460	14
Ni/Pd	60	406618	8132360	7
Total	179	831641	16632820	11

Palladium PDIP Devices

The solderability test procedure commonly used for both through-hole and surface mount components is referred to as the “Dip-and-Look Test”. During Dip-and-Look testing, the component is fluxed at room temperature and then dipped into molten solder. Solderability testing of palladium PDIP devices is not a problem for most users. Test procedure can however affect results.

Excessive flux applied to PDIP units of any lead finish will continue to vaporize throughout and after the solder dip, causing the solder surface to be disturbed (W.R. Russell, October 1989). This phenomenon can be observed as “popping” when the excess flux contacts the molten solder.

With palladium PDIP units TI recommends that flux immersion be controlled so flux does not contact the package body. This recommendation follows simple logic as solderability of the leads is of interest and not solderability of the plastic package body. Better results can be achieved if flux is applied only up to the standoff on the lead. During the solder immersion the flux slowly travels up the lead so the solder will actually wick above the standoff. Precisely controlling the amount of flux applied to the leads will improve solderability test results on palladium PDIP units.

Palladium SOIC Devices

Test parameters and procedures can affect solderability test results on palladium surface mount devices. Occasionally the user will encounter palladium non-wet holes on the lead surface after performing a Dip-and-Look test. Variations in solder temperature and solder immersion time will affect the rate at which the palladium dissolves off the surface of the lead during the solderability test. It is important to bear in mind during this discussion that the standard Dip-and-Look solderability test does not include a pre-heat of the flux prior to solder immersion. Also, in the standard solderability test the solder immersion is per-

formed using a very short immersion time into a static solder pot. These factors can all contribute to palladium non-wet holes during solderability testing which would not occur during actual board mount reflow.

The intention of the palladium layer is to prevent oxidation of the nickel prior to the reflow operation. The palladium will be completely removed from the lead surface during a normal solder wave or IR reflow process. Also, there is a very thin organic film present on the lead surface of finished IC devices. This layer of organics is present due to exposure to the air and will be present on any metallic surface (not just palladium leadframes). Typically the organic layer consists of carbon, oxygen, and various other elements. This layer of organics must be removed from the lead surface before dissolution of the palladium will begin.

Flux is composed of two main ingredients, namely solvents and activators. In a typical surface mount or wave solder operation the solvents burn off during the pre-heat stage. Once the solvents are removed from the flux, the activators begin to act on the lead surface. The flux activators clean the lead surface so proper wetting can occur.

During a standard Dip-and-Look solderability test the first few seconds of solder immersion are used to remove the solvents from the flux. With palladium devices the order of wetting is (1) solvents removed from the flux, (2) activators act upon the organic layer, (3) palladium is dissolved, (4) wetting occurs to the nickel underlayer. Occasionally a short solder immersion with no pre-heat of the flux will delay dissolution of the palladium.

TI has added a flux pre-heat step to its Dip-and-Look solderability test for surface mount devices. After flux immersion the IC leads are heated over a hot plate at 100°C for 60 seconds. Once the leads are pre-heated solder immersion is performed. This pre-heat step allows the flux solvents to be burned off and speeds up the flux activation. Pre-heating also brings the lead temperature closer to the temperature of the solder. By pre-heating the IC leads after flux immer-

sion, palladium dissolution can take place immediately upon solder immersion. Addition of this flux pre-heat step has been shown to aid in dissolution of the palladium and improve solderability test results.

Bear in mind that the purpose of the solderability test is to determine solderability of the surface to be soldered, in this case, the nickel layer. If the palladium does not completely dissolve due to the test procedure or parameters, a failure to the 95% solder coverage criteria may occur. Addition of a flux pre-heat step is justified because it will aid in dissolution of the palladium and therefore help to expose the underlying nickel layer. Also, recall that in a normal wave solder or surface mount reflow operation the palladium layer will be completely dissolved.

Steam Age Solderability Test

In the electronics industry, steam aging of finished IC units is a test method often used to simulate shelf storage. Typically, 8 hours of steam aging is used to simulate one year of shelf storage in a high humidity environment. IC devices are steam aged for 8 hours prior to solderability testing.

Steam age solderability testing of palladium plated IC devices poses a challenge for many users. It is TI's experience that palladium lead finish devices are more sensitive than Sn/Pb coated components to variations in the steam age test procedure, equipment, and parameters. However, with proper control of the steam age process, passing solderability test results can be achieved consistently.

There are basically two types of steam age systems in use across the industry. One type is a glass beaker which sits on a hot plate and is filled with DI water to a specified level. The IC units rest on a perforated plate which is made of plastic or ceramic. The plate is suspended at a height of 1.5" above the surface of the water (see Figures 3 and 4).

FIGURE 3 :
Beaker Steam Age Set-up

FIGURE 4 :
Close up of Beaker Steam Age Set-up

The second type of steam ager is a rectangular box made of Teflon® coated stainless steel (see Figure 5). With this type of steam age system, the units are placed in drawers which are inserted into the chamber. Each drawer has a perforated bottom panel which allows the steam to pass through.

Steam Age Solderability Test Evaluations on Palladium Devices

Initially when TI converted to palladium lead finish, variability in steam age solderability test results was encountered. Much work was performed to understand the factors that influence steam age results with palladium lead finish devices. Palladium users can achieve consistently passing steam age results with proper control and maintenance of the equipment. Below is a summary of evaluations performed. Conclusions and recommendations follow the evaluation data.

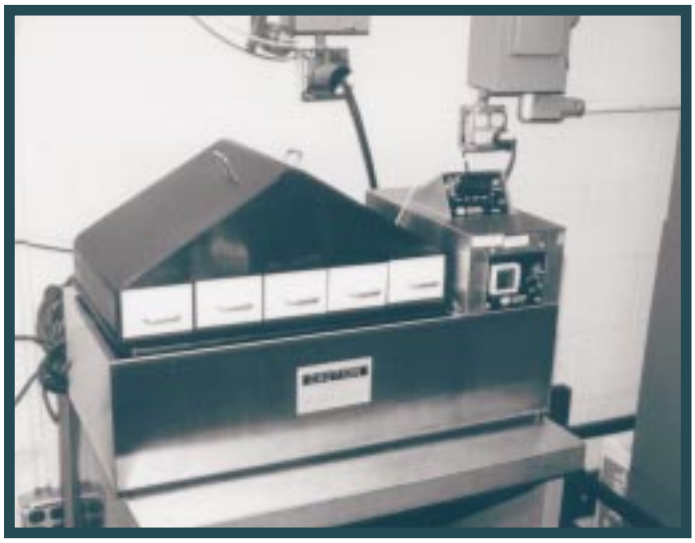


FIGURE 5 : Mountaingate Engineering Steam Age System

Evaluation 1 : Steam Ager Location and Water Quality Affect on Solderability Performance

This evaluation was conducted using palladium plated SOIC devices and had two main goals. First, this test was to show any difference that might exist in steam ager performance between two different TI sites (Dallas Environmental Test Lab and Sherman Reliability Lab) using the same type of equipment (Mountaingate chamber). Second, the study was performed to determine the effect of water quality on steam age solderability performance.

The evaluation consisted of steam aging samples twice per week at each site for one month and drawing a water sample from the steam age chamber, before aging each of the samples. These samples were from one assembly manufacturing lot which had consistently passed the steam age solderability test with Sherman's beaker steam age set-up and in Sherman's Mountaingate chamber when it was new. Steam aged samples from both Dallas and Sherman were then split and dipped at each site. The water samples were sent to the analytical lab and analyzed for anions, cations, conductivity/resistivity and total organic carbons.

Summary of Dipping Results:

- *All steam aged groups (Dallas and Sherman) dipped in Dallas did not show any statistical differences. Likewise all steam aged groups dipped in Sherman did not show any statistical differences.*
- *Statistically comparing groups steam aged at a common location and dipped in both Dallas and Sherman showed no differences.*
- *Thirty groups were steam aged and tested per TI internal specifications and 25 of those groups had failures.*

These results indicated that steam ager performance did not vary between the two sites involved when using the same type of equipment.

Summary of Water Analysis Results:

- *No significant differences between the water samples was observed when comparing the anions and cations.*
- *Analysis of total organic carbons showed no significant differences between the samples drawn prior to aging (around 1ppm). However, the sample drawn after aging the parts showed 4.1ppm of total organic carbons.*
- *The resistivity of the DI water source in Sherman is around 14MOHMS. Once the aging chamber is filled with water the resistivity at zero hours drops to 1.3MOHMS. Eight hours later the resistivity was 0.68MOHMS and 4 days later the resistivity was down to 0.074MOHMS.*

This water analysis showed that location did not affect water quality at time zero or over time.

Evaluation 2: Multi-site Steam Age Solderability Correlation of Palladium PDIP units

Seven different TI sites were involved in this evaluation. All of the sites

in this study except for Sherman and Taiwan used a Beaker type steam age system. Sherman and Taiwan both used a Mountaingate steam age chamber.

Each site received three tubes of 20 pin palladium PDIP devices all from the same manufacturing lot built in Malaysia. The samples supplied to each site were as follows:

- Tube 1 - Parts steam aged in Sherman and dipped at each site
- Tube 2 - Parts aged and dipped at each site
- Tube 3 - Parts aged at each site and returned to Sherman for dipping.

Inspection correlation results are shown in Table 9.

TABLE 9 : Inspection Correlation Results

	Tube 1		Tube 2		Tube 3
	Inspected		Inspected		Inspected
Site	Site	Sherman	Site	Sherman	Sherman
Germany	0	0	0	0	0
Portugal	4	0	0	0	0
Malaysia	0	0	0	1	0
Taiwan	0	1	2	3	4
Philippines	0	0	1	1	0
Hiji	19	2	1	0	1

A summary of the results is as follows:

- Inspection correlation between the sites and Sherman was generally good with the exception of Porto and Hiji results on Tube 1.
- There was no difference in results when parts were aged at a common site and dipped in the different locations with the exception of the Tube 1 samples dipped in Hiji. Also note how results from the same sites compare between Tubes 2 and 3 in the statistical analysis below (i.e. Germany parts aged and dipped in Germany averaged 3.6 mils compared to parts aged in Germany but dipped in Sherman which averaged 3.7 mils).
- The largest source of variation occurred within parts from Tubes 2 and 3 which were aged at different locations using different steam aging equipment. Taiwan and Sherman had statistically worse results. Both sites used the Mountaingate steam aging equipment.

Statistical Results:

All samples were inspected again in Sherman by recording the largest non-wet area on any one lead of each unit. The non-wet areas are expressed as a diameter. Statistical comparisons of the averages of the groups are shown in Figures 10-12. The probability limits (confidence intervals) were tabulated across the tables to aid in comparing each site's average with the statistical limits of the entire population. A group is considered statistically different from the entire population if its average non-wet diameter is outside of the probability limits.

TABLE 10 : Results for Tube 1, Aged at Sherman and Dipped at Each Site {units in mils}

	Germany	Portugal	Malaysia	Taiwan	Philippines	Hiji	Sherman
99% Prob Limit	18.05	18.05	18.05	18.05	18.05	18.05	18.05
95% Prob Limit	16.91	16.91	16.91	16.91	16.91	16.91	16.91
Site Average	8.9	5.7	11.8	11.2	10.4	17.3*	13.5
95% Prob Limit	5.61	5.61	5.61	5.61	5.61	5.61	5.61
99% Prob Limit	4.47	4.47	4.47	4.47	4.47	4.47	4.47

*Group is statistically different than others with at least a 95% confidence level.

TABLE 11 : Results for Tube 2, Aged and Dipped at Each Site {units in mils}

	Germany	Portugal	Malaysia	Taiwan	Philippines	Hiji	Sherman
99% Prob Limit	16.14	16.14	16.14	16.14	16.14	16.14	16.14
95% Prob Limit	15.19	15.19	15.19	15.19	15.19	15.19	15.19
Site Average	3.6*	6.3	11.5	21.3*	11.4	3.3*	15.3*
95% Prob Limit	5.82	5.82	5.82	5.82	5.82	5.82	5.82
99% Prob Limit	4.87	4.87	4.87	4.87	4.87	4.87	4.87

*Group is statistically different than others with at least a 95% confidence level.

TABLE 12 : Results for Tube 3, Aged at Each Site and Dipped in Sherman {units in mils}

	Germany	Portugal	Malaysia	Taiwan	Philippines	Hiji	Sherman
99% Prob Limit	17.28	17.28	17.28	17.28	17.28	17.28	17.28
95% Prob Limit	16.07	16.07	16.07	16.07	16.07	16.07	16.07
Site Average	3.7*	10.6	10.6	20.5*	7.9	8.8	N/A
95% Prob Limit	4.63	4.63	4.63	4.63	4.63	4.63	4.63
99% Prob Limit	3.42	3.42	3.42	3.42	3.42	3.42	3.42

*Group is statistically different than others with at least a 95% confidence level.

Analytical Results from Central Research Lab

Samples from Evaluations 1 and 2 were submitted to CRL for analysis.

FTIR (Fourier Transform Infrared Spectroscopy):

This technique is a more sensitive form of infrared spectroscopy and was used to identify any possible organic compounds on the lead surfaces.

1. The results from the analysis of steam aged non-wet areas showed that an organic was present which was identified as mold compound or some constituent of the mold compound (i.e. release agent).
2. Non-aged samples analyzed using FTIR showed very little or no mold compound present on the leads.
3. FTIR was also used to analyze a sample of the water taken from Sherman's steam age equipment during Evaluation 1. The analysis showed mold compound was present in the water.

AES (Auger Electron Spectroscopy):

This technique along with sputter etching was used to identify the percentage of elements present on the palladium lead surfaces and the depth profile of these elements. The leads analyzed were the same ones which were analyzed using FTIR.

TABLE 13 : Auger Results for Non-Aged Pd Units and Aged Non-Wet Areas

Sputter Depth	Elements	Non-Aged	Aged Non-wet	Delta
Surface	Palladium	18.18%	0.3%	-17.88%
	Nickel	2.03%	3.37%	1.34%
	Carbon	66.93%	76.32%	9.39%
	Oxygen	5.65%	8.08%	2.43%
	Other	7.21%	11.93%	4.72%
520 Angstroms [2.05 microinches}	Palladium	47.89%	0.48%	-47.41%
	Nickel	5.36%	5.34%	-0.02%
	Carbon	32.05%	62.52%	30.47%
	Oxygen	14.70%	12.79%	1.91%
	Other	0.0%	18.87%	18.87%
1040 Angstroms {4.09 microinches}	Palladium	99.77%	16.56%	-83.21%
	Nickel	0.0%	1.84%	1.84%
	Carbon	0.0%	51.76%	51.76%
	Oxygen	0.23%	0.36%	0.13%
	Other	0.0%	29.48%	29.48%
1560 Angstroms {6.14 microinches}	Palladium	100.00%	23.52%	-76.48%
	Nickel	0.0%	0.0%	0.0%
	Carbon	0.0%	24.09%	24.09%
	Oxygen	0.0%	2.44%	2.44%
	Other	0.0%	49.95%	49.95%

1. The results showed leads from the non-aged parts had an organic layer of carbon which was about 2 microinches thick. One-hundred percent palladium was reached somewhere between 2 and 4 microinches.
2. The steam aged, non-wet areas had an organic layer of carbon which exceeded 6 microinches in thickness (limit of sputter capability) with only 24% palladium present at that depth.
3. The quantity and depth of oxygen is relatively consistent between the non-aged sample and the aged, non-wet sample which indicates oxidation is not the culprit for causing non-wets.

Conclusions

The majority of the steam-aged palladium PDIP solderability non-wets appear to result from the palladium adsorbing an organic during the steam aging process. The organic has been identified as mold compound or some constituent of the mold compound. The same organic has also been found in the steam ager water.

The severity of the organic adsorption, hence non-wets, appears to be a function of the steam ager cleanliness. This seems to be the case since the samples steam aged in cleaned beaker style agers performed better than samples steam aged in cleaned Mountaingate agers. The Mountaingate agers have the advantage of controlling the water level and environmental temperature, however the poorer performance of palladium devices in these agers can be attributed to the difficulty in cleaning its Teflon-coated, stainless steel surface which has more surface roughness than glass beakers. Sherman's Mountaingate steam ager yielded 0 failures out of 9 steam aged groups when it was new but, as time progressed the results of the steam aged groups from the same manufacturing lot worsened even though the Mountaingate chamber was cleaned on a regular basis.

The test results above led TI to make progress in the area of steam age solderability testing of palladium plated IC devices. The following recommendations are made for the palladium user who desires to perform steam age testing:

- *Do not handle the units without wearing finger cots or plastic gloves. Handle the units by the package body only, never touching the leads. If possible hold the units with tweezers by gripping the package body.*
- *Clean the steam age chamber prior to each test initiated. Use fresh DI water with every test.*
- *Place the units in the the chamber in a "dead-bug" position. Do not let the leads touch between adjacent units.*

Palladium users have seen tremendous improvement in steam age test results simply by following the recommendations above. Palladium lead devices are more sensitive to changes in the test equipment and procedure, but with proper controls, passing results can be achieved.

Wetting Balance Test

The wetting balance test (sometimes called a meniscograph) is one method for solder wetting comparisons. The wetting balance test measures the forces imposed by the molten solder upon the test specimen as the specimen is dipped into and held in the solder bath. This wetting force is measured over time and plotted. Initially, the buoyant force is negative indicating that the solder has not yet begun to wet to the specimen. The force imposed by the solder approaches zero as the solder begins to wet to the specimen. One commonly used performance measure is the time to cross the zero axis of wetting force. This point indi-

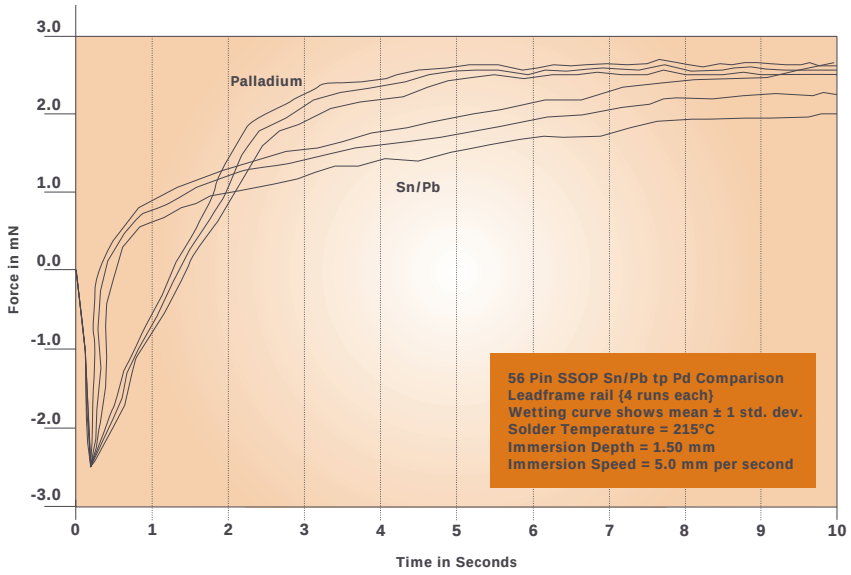


FIGURE 6 : Typical Wetting Balance Curves for Pd and Sn/Pb Leads

cates the transition from non-wetting (F<0) to wetting (F>0).

Typical wetting balance curves for both palladium lead finish and Sn/Pb lead finish devices are shown in Figure 6. Palladium lead finish devices typically have a slight delay in wetting associated with dissolution of the palladium. Usually the palladium devices will require 0-0.4 seconds longer to cross the zero line versus Sn/Pb coated devices. However, palladium devices reach their maximum wetting force more quickly than Sn/Pb devices.

Palladium users should understand that a slightly longer time to wet during the wetting balance test does not indicate a wetability issue with the palladium devices during actual reflow. In the wetting balance test, typically a rosin based, non-activated flux is used. In the actual reflow operation an activated flux is normally used. Also, in the reflow process the units encounter a pre-heat step which activates the flux. With flux activation, the lead surface is cleaned and wetting occurs more rapidly. Also, with pre-heating the temperature of the leads is closer to the reflow temperature.

An L8 designed experiment was performed to quantify the effect of solder temperature, flux pre-heat, and flux type upon the time to wet with palladium PDIP devices. Two different solder temperatures were evaluated, namely 215°C and 245°C. Leads were tested with and without a pre-heat. The pre-heat step was accomplished by holding the lead approximately 1/8" above a hot plate for 20 seconds. The lead temperature reached 150°C. Also, Alpha 100 rosin based flux

TABLE 14 : Test Matrix and Results for Wetting Balance Experiment

Run	Solder Temperature	Pre-Heat	Flux Type	Mean Time-to-Zero
1	215	No	R	1.62
2	215	No	RMA	0.34
3	215	Yes	R	1.13
4	215	Yes	RMA	0.3
5	245	No	R	0.38
6	245	No	RMA	0.23
7	245	Yes	R	0.38
8	245	Yes	RMA	0.22

was compared to Alpha 611 water soluble flux. The sample size for each experimental test run was 3 leads. The test matrix and average Time-to-Zero values are outlined in Table 14.

In order to analyze the data compiled in Table 2, the SAS program PROC ANOVA was used. The program calculated an F-value for each of the three factors and each of the two factor interactions. The Analysis of Variance (ANOVA) table generated from PROC ANOVA is shown in Table 15. In order to determine the significance of the F-values for each factor and interaction, F tables were used with $df_f = 1$ and $df_e = 16$. The values of F at the various levels of P are tabulated in Table 16.

In comparing the calculated F-values with the F table it can be seen that the factors of flux and solder temperature are significant with a probability of 99.5%. The interaction between flux and solder temperature is also significant with a probability of 99.5%.

TABLE 15 : Analysis of Variance (ANOVA) Table for Wetting Balance Experiment

Source	DF	Anova SS	Mean Sq	F Value
Pre-heat	1	0.03645	0.03645	1.38
Flux	1	0.73205	0.73205	27.68
Solder Temperature	1	0.59405	0.59405	22.46
Pre-heat X Temperature	1	0.0338	0.0338	1.28
Pre-heat X Flux	1	0.0242	0.0242	0.91
Flux X Temperature	1	0.405	0.405	15.31
Residual	1	0.02645	0.02645	

TABLE 16 : F-Test values for df_f= 1, df_e = 16

For p=	F=
0.25	1.42
0.10	3.05
0.05	4.49
0.025	6.12
0.01	8.53
0.005	10.58

TABLE 17 : Effects Table

Level	Pre-heat	Flux	Solder Temperature
Low	0.6425	0.8775	0.8475
High	0.5075	0.2725	0.24
Effect	0.135	0.605	0.6075
Best Case Setting	On	RMA	245°C

From the effects table (Table 17) it can be seen that the best case settings are pre-heat on, RMA flux, and 245°C solder temperature. These results are intuitive because it would be expected that these settings would decrease the time to wet. These results do, however, demonstrate a statistically significant difference between results with palladium leads that are tested with typical wetting balance parameters and actual board mount process parameters. The wetting times seen with palladium leads using standard wetting balance parameters were acceptable. However, when actual process parameters are used, the wetting times are reduced greatly. This indicates that in the actual board mount process the palladium will be completely dissolved and wetting will take place.

Surface Mount Solderability Test Method

The Surface Mount Solderability Test has been adopted by the Electronic Industries Association Soldering Technology Committee. This test method simulates the actual reflow environment that surface mount devices will encounter in a board mount application. Testing has shown this method is more applicable for surface mount devices than the traditional Dip-and-Look method. This test method is recommended for palladium-plated surface mount devices because actual board mount performance can be predicted.

Many users in the industry have recognized the need for a "use test" which would closely predict performance of surface mount devices in a reflow process. Solder bridging often results when using the Dip-and-Look method on fine pitch devices. The Surface Mount Solderability Test method allows for more accurate solderability prediction as bridging is not encountered. Also, test parameters such as very short solder immersion time, low solder temperature, and lack of pre-heat can negatively affect solderability prediction when using the Dip-and-Look method. The Surface Mount Solderability Test method has proven to more closely demonstrate the performance of surface mount devices in the actual reflow environment versus the Dip-and-Look method.

This section will provide background data which validates the test method itself and then data will be presented to show the advantage to using this test method to predict board mount performance of palladium surface mount devices.

Introduction

Solderability testing of finished integrated circuit (IC) packages is performed in order to predict performance of these devices in an actual printed circuit board reflow process. The "Dip-and-Look" (DNL) test method is the electronics industry standard test method for solderability testing the leads of finished IC devices (ANSI/JSTD-002). This test method consists of immersing the IC

leads into a rosin type flux for 5-10 seconds prior to immersion into molten 63% Sn/ 37% Pb solder for 5-10 seconds. Upon removal from the solder, the leads are cleaned and visually inspected. The percentage of the lead surface not wetted by the solder is calculated. Industry standards specify that "all terminations shall exhibit a continuous solder coating free from defects for a minimum of 95% of the critical surface area of any individual termination".

In a typical production environment, an Infrared/Convection Reflow (IR) furnace or Vapor Phase Reflow (VPR) is used to heat the solder paste to the melting temperature. The printed circuit board encounters a pre-heat in the range of 150-170°C. Once pre-heated, the board temperature rises to 215-220°C and quickly drops off after the solder paste is reflowed. The "Dip-and-Look" test described above does not simulate a typical reflow environment.

The Surface Mount Solderability Test Method (SMT test) is intended to simulate the actual environment which surface mount devices encounter during the solder reflow process. This test procedure begins with screening solder paste onto a ceramic plate (0.035" thick) by using a solder stencil (see Figure 7). The paste print must be equivalent to the pattern of the leads to be tested.

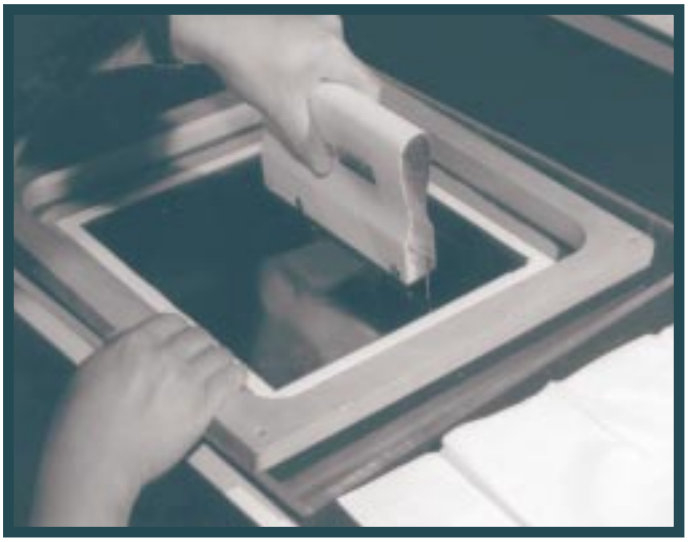


FIGURE 7 : Solder Paste is Screened onto the Ceramic Substrate

FIGURE 8 : Devices are Placed onto Solder Paste Print

The devices to be tested are then placed onto the solder paste print (see Figure 8).

The ceramic substrate is processed through a reflow cycle and then allowed to cool. After reflow, the units are removed from the ceramic and inspected. The beauty of this test method is the IC devices are subjected to the same reflow environment experienced in actual processing, and use of a ceramic substrate allows for inspection of the surface to be soldered. This test method has been adopted as an Electronics Industries Association (EIA) Interim Standard (EIA/IS-86, March 1993). EIA/IS-86 allows the user to select one of three types of reflow so equipment availability does not become an issue. The reflow options are Vapor Phase (VPR), Infrared/Convection (IR), and Convection (with a typical storage oven).

The Surface Mount Solderability Test has direct application to solving the problem of bridging encountered on fine pitch leads when using the Dip-and-Look test method. Additionally, the Surface Mount Test inspection focuses on the critical soldering area as compared with the MIL-Standards which require inspection of critical and non-critical lead areas.

Background

In 1990 a proposal was made to the Soldering Technology Committee (STC) of the EIA. The initial draft of the Surface Mount Solderability test was proposed as a new test method for adoption by the EIA. The committee was positive toward the idea of adopting a "use test" of this type. Over the following two years, several different experiments were performed by committee members to validate this type of test method. Results of three of the studies performed are discussed herein.

Experimental Procedure and Results

Correlation Between DNL and Surface Mount Test

This study was performed to correlate test results on various package /lead finish combinations between the Dip-and-Look and the SMT methods. Initial testing was performed on non-aged units using VPR reflow at 215-220°C for 60 seconds. The solder paste used was Kester type R-229-25 RMA with composition of 63Sn/37Pb. Results were identical with all units passing on either test method (Table 18, Figures 9 and 10). Also, Kester type NC-830 (No-clean) with composition of 63Sn/37Pb has been used successfully.

TABLE 18 : Correlation of DNL vs. SMT Method Results

Test Specimen	Lead Finish	Dip-and-Look Sample /3# Fails	SMT Test Sample /# Fails
120 Pin MQUAD®	Sn/Pb plated	5/0 {600/0 leads}	5/0 {600/0 leads}
28 Pin PLCC	Sn/Pb dipped	20/0 {560/0 leads}	20/0 {560/0 leads}
68 Pin PLCC	Sn/Pb dipped	20/0 {1860/0 leads}	20/0 {1860/0 leads}
20 Pin SOIC	Sn/Pb dipped	20/0 {400/0 leads}	20/0 {400/0 leads}
20 Pin SOIC	Pd plated	20/0 {400/0 leads}	20/0 {400/0 leads}

A follow-on study was performed to determine if the two test methods would give similar results with units which were expected to fail. In order to induce failures, samples of the 120 pin MQUAD®, units (0.8mm lead pitch) were degraded by baking at 150°C for 168 hours followed by 8 hours of steam aging. Results also correlated between the two test methods on degraded units (Table 19).

Figures 11 and 12 show the results seen when aged 120 pin MQUAD, packages were tested by each test method. Similar results indicated correlation between the two test methods. This was important because it was necessary to prove that degraded units would fail when tested with either method.

TABLE 19 : Correlation of DNL vs. SMT Method on Degraded Units

Test Specimen	Lead Finish	Dip-and-Look Sample /3# Fails	SMT Test Sample /# Fails
120 Pin MQUAD®	Sn/Pb plated	5/5 {600/248 leads}	5/4 {600/16 leads}

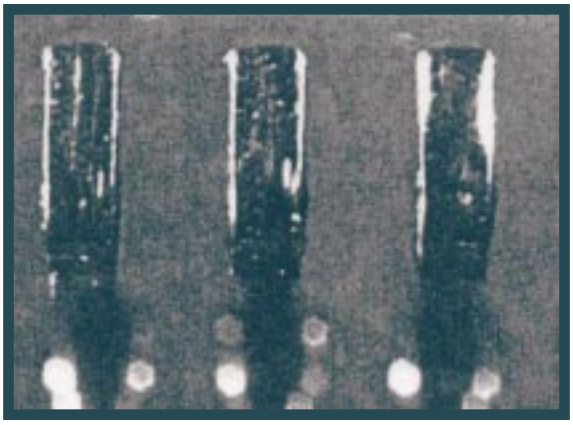


FIGURE 9 : 120 pin MQUAD®, Dip-and-Look Test Results

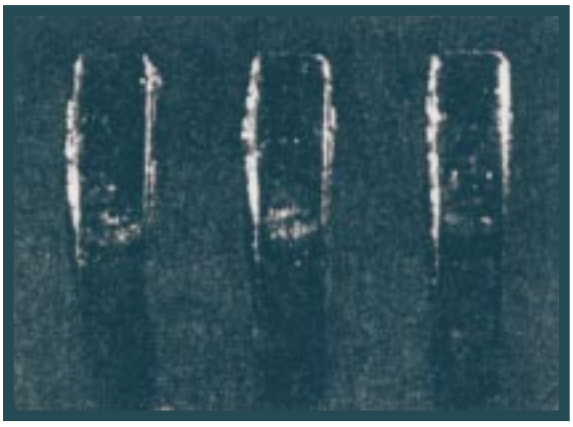


FIGURE 10 : 120 pin MQUAD®, SMT Test Results

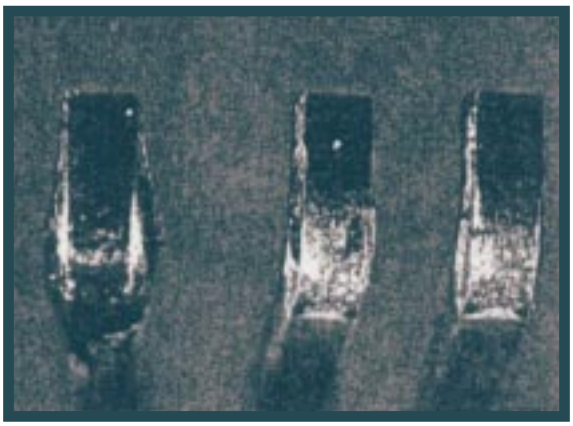


FIGURE 11 :
Degraded 120 Pin MQUAD® units, Dip-and-Look Test Results

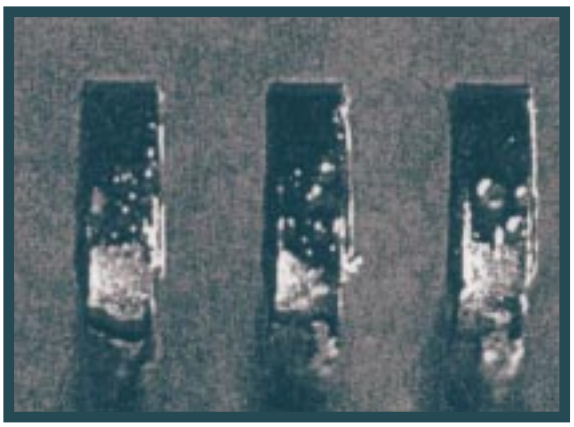


FIGURE 12 :
Degraded 120 Pin MQUAD® units, SMT Method Results

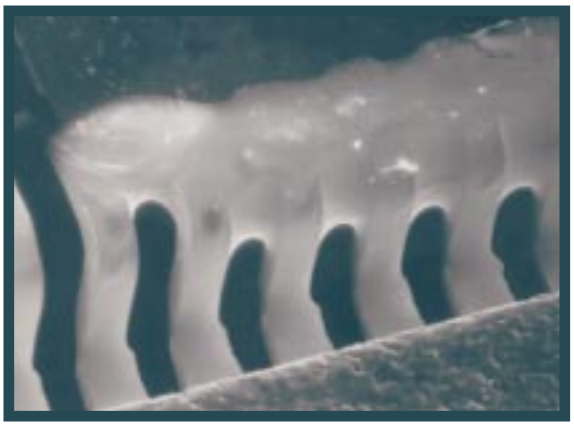


FIGURE 13 : Bridging on 120 pin TQFP Package (0.4mm lead pitch} After Dip-and-Look Testing

FIGURE 14 : Good Solderability Results With no Bridging on 120 pin TQFP Package Tested With SMT Method

Bridging on Fine Pitch Devices

As integrated circuit packaging evolves toward extremely fine lead pitch designs, solderability testing has become a more difficult task. The traditional Dip-and-Look test method often results in bridging between the leads on fine pitch surface mount packages. The Surface Mount Test eliminates this deficiency because the units are not immersed in a molten solder bath. Instead, the devices contact the same volume of solder paste as in the production operation and the reflow cycle is the same.

An actual device qualification demonstrated the need for use of the SMT method with fine pitch devices. Package qualification of the 120 pin TQFP with 0.4mm lead pitch included Dip-and-Look testing for solderability evaluation. Dip-and-Look tests on a 22-piece sample resulted in excessive bridging between the leads (see Figure 13).

The decision was made to use the EIA IS-86 Surface Mount Solderability Test method to eliminate the bridging and provide a good solder coat for visual inspection purposes. The results were excellent with zero failures on 22 packages (2640 leads). Results are seen in Figure 14.

Palladium Plated SOIC Devices

In the future, solderability test procedures must encompass both conventional, pre-tinned and palladium plated leads. The Surface Mount Solderability Test method has been found to be applicable for solderability testing of palladium plated surface mount devices.

In a typical solder reflow operation the palladium will be completely dissolved into the solder allowing the joint to be made to the nickel underlayer. The concern in solderability testing of palladium devices is that with low solder temperatures and/or low solder immersion times, the palladium may not completely dissolve and non-wet areas can result. Steam aging of IC packages prior to solderability testing has also been found to contribute to the frequency of non-wet areas. Particulates from the plastic mold compound can become entrained in the steam age water vapor and be redeposited on the surface of the IC leads. These mold compound particulates can hinder the dissolution of the palladium. The critical issue is that failures to the pass/fail criteria may occur which are actually a result of the influence of the test method and parameters rather than an actual failure of the surface to be soldered.

Typically, non-wet areas on palladium plated devices will appear in the shape of circular holes on the bottom side of the foot (see Figure 16). Experimentation has shown that the location and size of the non-wet holes can be varied by changing the orientation of the device during solder immersion. During inspection, the diameter of any non-wet holes is measured and recorded. For reference, the lead width on a SOIC lead is 16 mils (0.016”). Calculation of the permissible non-wet area with 95% solder coverage criteria indicates that the maximum allowable diameter of non-wet area is 11mils for a Wide Body SOIC device (this value assumes all of the non-wet area is concentrated in one spot).

The intention of the solderability test is to test the surface to be soldered, in this case, the nickel layer. If the palladium does not completely dissolve, a fail-

ure to the 95% solder coverage criteria may occur. In actuality, the underlying nickel never contacts the solder and the test parameters have hindered the goal of the test method.

The Surface Mount Solderability Test method was used to determine if the non-wet phenomenon experienced in DNL testing of palladium devices was indicative of actual board mount performance of these devices. The test vehicle used was a JEDEC 20 Pin Small Outline Integrated Circuit (SOIC) package (Figure 15).

Previous work has shown that steam aging, solder temperature, and solder immersion time are test parameters which all have a significant impact on the size of palladium non-wet holes during Dip-and-Look. Finished units in palladium lead finish were steam aged at various levels. Units were then tested using both test methods (DNL and SMT).

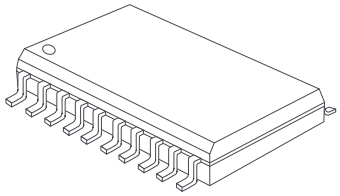


FIGURE 15 :
20 Pin Small Outline Integrated Circuit

Result of SMT vs. DNL with Palladium SOIC Devices

When using the DNL test method, non-wet holes were noted on the steam aged devices (see Figure 16). When units from the same groups were tested using the SMT method, no non-wet holes were noted on any of the various steam age levels (see Figure 17). The results indicate that by using the SMT method any contaminants which hinder palladium dissolution are removed and the palladium coating is completely dissolved. When using the DNL test method, short solder immersion time and low solder temperature with no pre-heat hinder the dissolution of the palladium from the lead surface. The results seen using the SMT test method indicate how the units would actually perform in an IR or VP reflow process.

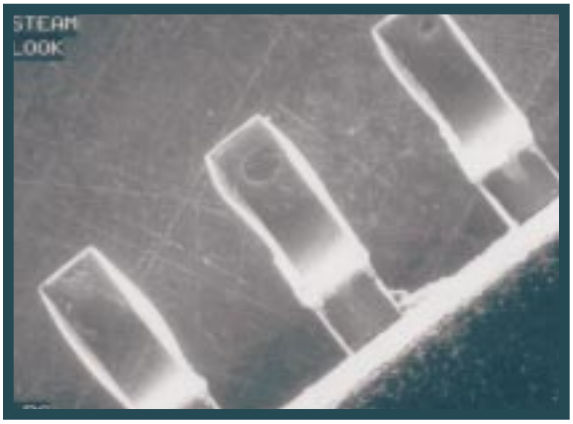


FIGURE 16 :
Non-wet Holes on a Palladium SOIC After Dip-and-Look Testing

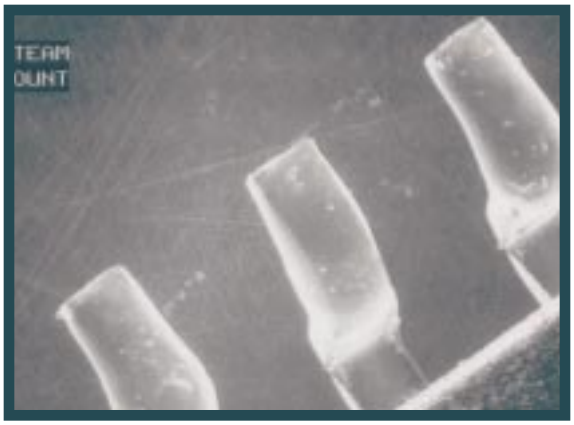
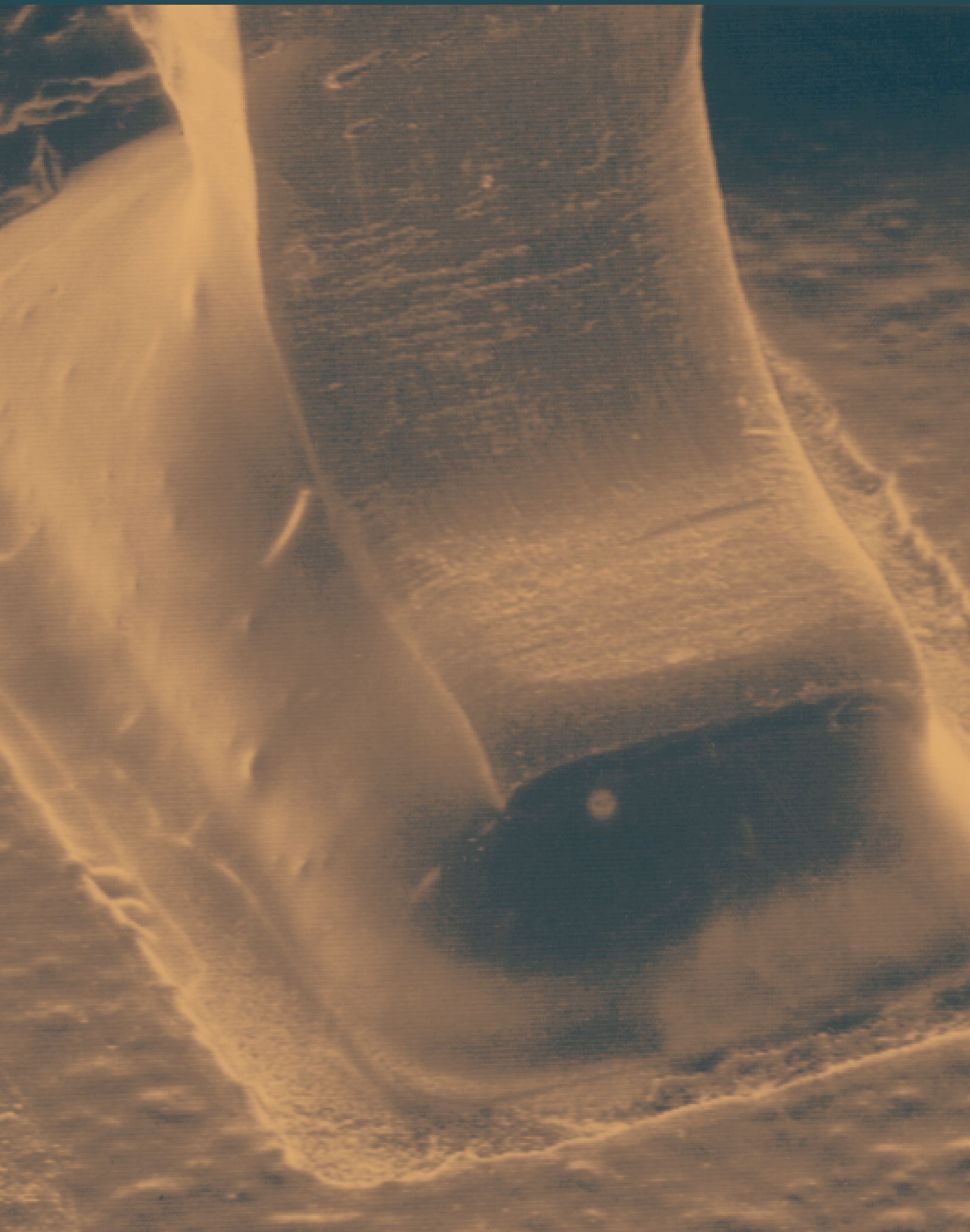


FIGURE 17 :
Palladium Units, 16 hrs Steam Age, Surface Mount Test

Summary

The Surface Mount Solderability Test method has proven to correlate with the Dip-and-Look method with both passing units and failing units. This test method can be used when testing fine pitch surface mount devices where solder bridging is an issue. Also, the SMT test method is recommended for palladium lead finish surface mount devices because false non-wets can be eliminated.

The SMT method is used by several major corporations that have recognized the need for this type of “use test”. The Surface Mount Solderability Test has been adopted by the Soldering Technology Committee of the Electronics Industries Association (EIA/IS-86, March 1993).



Visual Appearance

An issue for most users has been the visual appearance difference between Sn/Pb devices and palladium plated devices after board mount. Sn/Pb plated or dipped devices will usually have solder covering the top of the IC foot after reflow. Also, there is typically no noticeable transition between the IC lead and the solder itself with the Sn/Pb devices (Figure 18).

This occurs because the solder plated or dipped device is coated in solder which reflows off of the lead and onto the board. The solder on the lead mixes with the solder screened onto the board to give coverage of the top of the lead and smooth transition from the solder to the lead itself.

With palladium plated devices, the only solder available to form the joint is the solder which is screened onto the board prior to board mount. The typical solder joint with a palladium plated device will have little or no solder on the top of the foot. Also, the transition line from the solder to the lead may be noticeable (Figure 19).

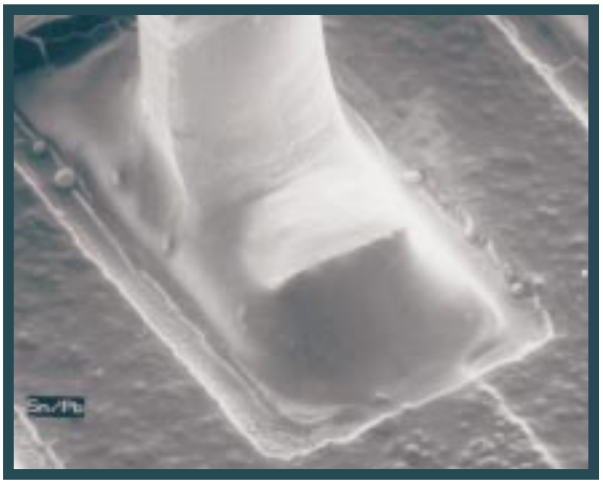


FIGURE 18 :
Sn/Pb Plated SOIC Lead After Reflow

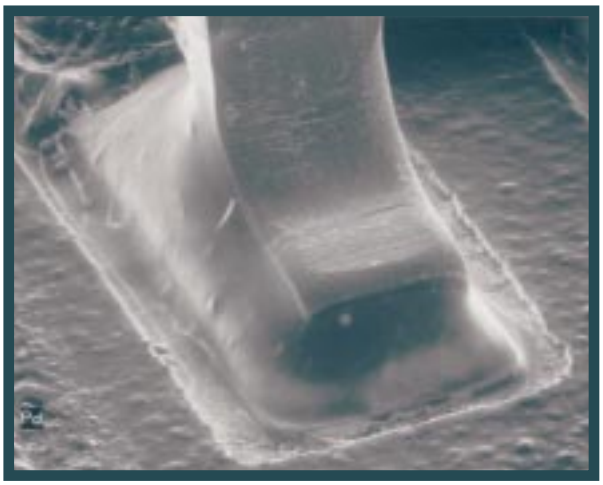


FIGURE 19 :
Pd Plated SOIC Lead After Reflow

This visual difference is logical when the user realizes there is no Sn/Pb on the lead to flow down into the joint. Many IC users were concerned with this visual difference when first encountered.

Mechanical strength tests were performed on the board mounted units shown in Figures 18 and 19 to compare the mechanical strength of the palladium joints versus the Sn/Pb joints. The mechanical strength of the solder joint for each unit was determined by shearing the component off of the printed circuit board. A die shear tester was used to shear the components from the PCB. The force was applied in the longitudinal direction of the IC device, along the center line. Shear values were recorded from the different devices and are listed in Table 20.

TABLE 20 : Mechanical Shear Data

Device	Board 1	Board 2	Board 3
Pd1	8.0 kg	8.0	7.0
Pd2	7.7	8.3	8.5
Sn/Pb	7.9	8.0	7.5

The data in Table 20 indicates the palladium and Sn/Pb devices are equivalent in shear strength.

Texas Instruments has performed numerous tests to verify that solder joints made with palladium plated devices are mechanically equivalent or stronger than joints made to Sn/Pb devices. Several major customers have performed independent verification of the mechanical strength of palladium joints.

One study was performed to determine the quality of palladium solder joints on the basis of mechanical strength. In this test, joint strength was measured by isolating the soldered lead and then pulling it from the printed circuit board with a force test chuck. The samples were heat aged prior to pull strength testing. Results are shown in Table 21.

TABLE 21 : Average Lead Pull Results After Heat Aging

Sample	0 hrs	8 hrs	16 hrs	24 hrs
3µ" Pd	5.17 lbf	5.95	5.85	4.71
Solder Dip	5.07	4.51	5.55	5.50

These results demonstrate equal performance for solder dip and palladium solder joint strengths. Minimum pull strengths for all groups were >3.0lbs.

The user of palladium devices must understand that the strength of the joint is determined by the Sn/Pb interface to the lead and is not dependent upon the solder flowing over the top of the IC foot. This is a fact that has become accepted within the industry and is now reflected by the visual inspection criteria given in industry standards ANSI/J-STD-001 and ANSI/J-STD-002.

One customer of TI was interested in determining strength of the solder joint versus fillet height up the side of the lead on palladium devices. The customer board mounted TI palladium plated devices and categorized the solder joints by fillet height. Then the customer performed lead pull tests on individual leads to determine mechanical strength. The results showed no difference in mechanical strength of the solder joint independent of the height of the fillet up the side of the lead (see Figure 19). This confirms the fact that the strength of the solder joint is determined by the solder in contact with the lead bottom.

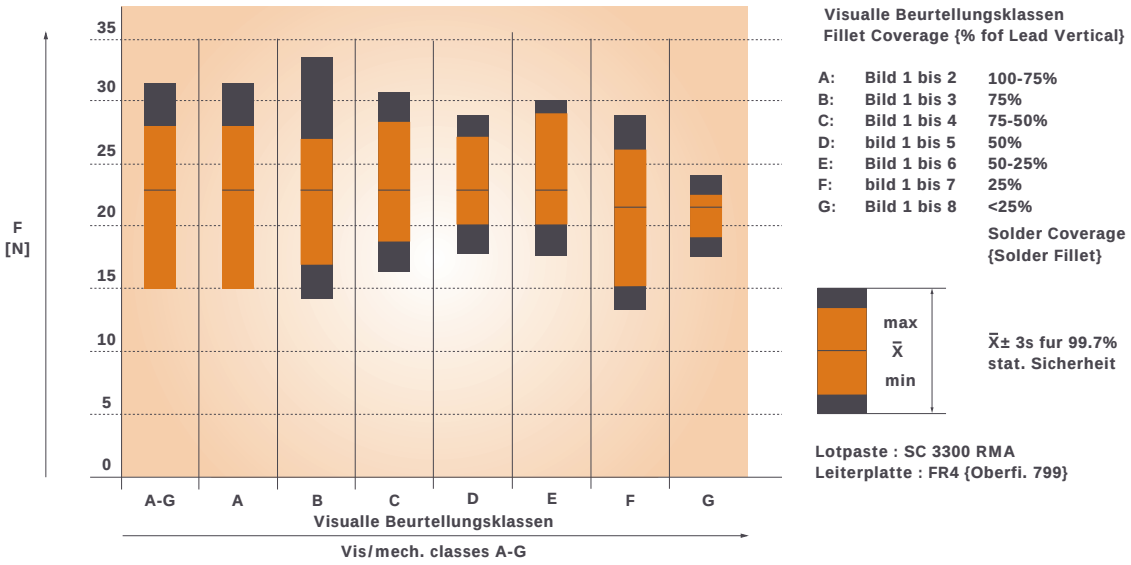


FIGURE 19 : Customer Lead Pull Results

In many cases palladium users have performed mechanical lead shear or lead pull tests and have verified the strength of the palladium solder joint in comparison to solder coated devices. In each case the user has been satisfied when he is assured of mechanical strength and he understands the reason for the visual difference.

Cracks at the Lead Bend and Exposed Copper

Microcracks can be seen with high magnification on the lead bends of palladium plated leadframes (Figure 20). The cracks are caused by discontinuous yielding of the base material. The plating cannot "stretch" over the gaps that appear in the base material so they crack as well. Cracking can be minimized by forming the material over a radius larger than the material thickness. For example, forming 8 mil thick material over a 10 mil radius will almost completely eliminate the cracks while forming the same material over a 6 mil radius will give worse results.

Although we are continuously looking for more "forgiving" SMT alloys, we have yet to find any better than the ones currently used. TI's materials people in Attleboro, Massachusetts, have ongoing programs with Olin, Kobe, and others but have yet to see any materials that show improved performance in this area.

To minimize the cracks, TI has enlarged both the upper and lower radii on its parts. On Wide-Body parts for example, TI enlarged the forming radii, growing the top radius from 5 - 8 mils and the lower radius from 8 to 12 mils. To enlarge

FIGURE 20 : Surface Cracks on SOIC Shoulder (77X)

the radii further is not possible without exceeding JEDEC package outlines.

On the subject of exposed copper, palladium plated parts are similar to solder plated components. Solder plated components can have copper exposed at the tips, the dam bars, and in some cases, up near the package body. Palladium plated leads will not have copper exposed up near the package but will have it on the cracks. TI believes the package body is the least attractive location for unprotected Cu to exist as any reaction products can be supported along the plastic body and eventually lead to shorts between leads.

Water-soluble and No-clean Solder Paste Study

In response to increasing environmental concern over the use of chlorofluorocarbons (CFCs) to clean printed circuit assemblies, most surface mount operations have now converted to water soluble or no-clean type solder pastes. This conversion began in mid-'92 and has progressed rapidly.

With the introduction of water soluble and no-clean solder pastes, many users saw a need to understand which factors influenced performance of these new generation pastes in their reflow process. In early 1992, TI began receiving feedback from its customers using palladium lead finish devices with these new-generation solder pastes. Board mount shops attempting to convert to these pastes were experiencing variability in wetting performance between the solder paste and the palladium lead finish devices. These palladium users were interested in determining how to optimize their board mount process to achieve the optimum performance with these new generation pastes.

Designed experiments were performed to determine to what degree the

solder paste, reflow profile, and component shelf storage time impacted solder joint quality for both palladium and solder plated surface mount devices. Several water soluble and no-clean solder pastes were included in the evaluation. Identical test matrices were performed for both palladium and solder plated devices.

The critical performance measure was how well the pastes allowed for an effective surface mount solder joint under typical manufacturing conditions. Obviously the term “an effective joint” is subjective at best, so a quantitative measure of wetting performance was required. In this study, the force to shear a component off a printed circuit board and the contact angle of solder on the backside of the component lead were considered the best quantitative measures. These indices are good predictors of solder joint quality and yield performance in a manufacturing environment.

The definition of contact angle used herein is the angle formed by the tangent to the back side of the lead and the tangent to the solder fillet at the point of contact of the lead with the fillet (Figure 21). Contact angle is typically measured by performing a cross-section on the lead of interest. Once the cross-section is available, the contact angle measurement can be taken.

In general, lower contact angles are considered to indicate a soldering condition that has produced good results, and higher contact angles indicate either a situation where the wetting rate has been decreased or where the equilibrium wetting point has changed. Contact angle can also be affected by the geometries of the soldered surfaces (relevant to the surface tension of the solder) and by the volume of solder present.

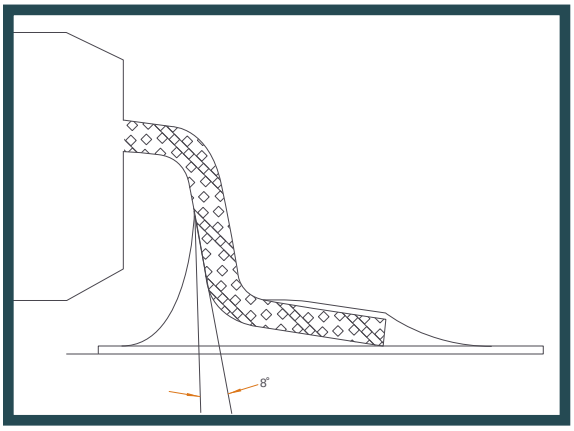


FIGURE 21 : Contact Angle to Back Side of Lead

One problem with this technique is it is subjective in the interpretation of how small the contact angle should be to indicate a good joint. Several values have been put forth. Howard Manko in “Solders and Soldering” states: “M, the marginal limit of the dihedral angle, is usually arbitrarily set at 75° or less in the case where extremely high quality is required”. This is confirmed by an electronic industry solderability test RS 178 of the EIA which contains the following statement: “Good wetting is characterized by a contact angle between the lead and the edge of the solder of 75° or less”.

Further constraints on this evaluation were put forth in the case of contact angles on surface mounted leads. In surface mounting, there is a limited volume of solder available, therefore the capillary wetting of solder up the lead can be limited. Surface mounting also deals with the reflow of a solder paste rather than the application of a liquid solder. The equilibrium shape of the solder fillet is very dependent on the heating rates of the leads relative to the solder and the solder pads. An example of this is thermally induced solder wicking where the lead heats up faster than the pad and the solder wets it preferentially reducing the solder in the fillet and possibly causing an open joint (Figure 22).

Such cases of solder wicking are common in surface mounting, and they result in a contact angle of zero or a negative contact angle. This condition is less than optimum in terms of assembly yield and board reliability. What then is an optimum range for a surface mount contact angle between the solder fillet and the back side of the lead? The answer to this question must consider both proper wetting and maintenance of sufficient solder in the fillet.

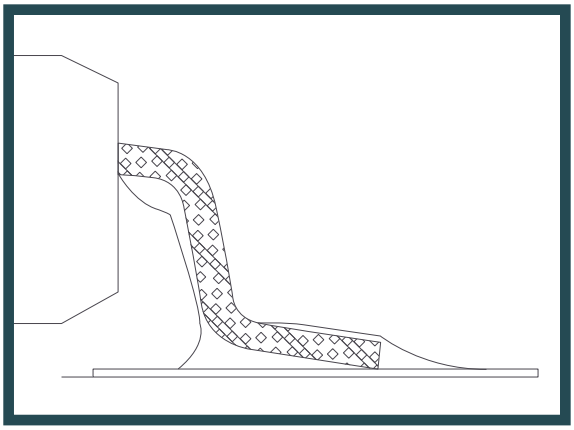


FIGURE 22 : Solder Wicking

Earlier references considered less-than 75° to be required for a good solder joint. This is probably a good measure for the high side, yet it must be considered that a surface mount board typically has a great many solder joints, and, for the whole board to be well soldered, the highest contact angle on the entire board should be less than 75 degrees. Given that contact angles for various soldering conditions can only be accurately measured by destructive techniques, only a sample will typically be available. Assuming the range of observed contact angles falls in a normal distribution, it is considered by the authors that an optimum soldering system will have the mean of the contact angle plus three standard deviations fall below 75°. This technique will assure a consistently low contact angle for the entire board and should be indicative of a soldering process that will not result in any non-wet or poorly wetted leads.

At the other end of the spectrum are the zero contact angle fillets. In many cases, these types of fillets are indicative of solder wicking to some degree. While it would be implausible to attempt to design a soldering system that did not display any zero contact angles, it is considered that a system that does not have its mean about the zero degree mark will exhibit less of the deleterious effects of solder wicking. It has been noted that solder wicking results not only in open solder joints, but also fillets with reduced solder which are more susceptible to stress induced fatigue cracking. The effects of solder wicking are reduced somewhat in IR reflow, compared to vapor phase reflow because of the lower heating rate. However effects of solder wicking are increased in fine pitch (.025” or less pitch) components due to the thinner stencils and corresponding lower volume of solder often used on these components.

Given the above discussions regarding the relevance of contact angle data, the optimum contact angle of a surface mount solder joint should be in the range of from 10° to 20° for a mean with a standard deviation of 10° or less. Minimum contact angle should be zero.

Shear Strength

The mechanical strength of the solder joint for each test run was determined by shearing the components off the printed circuit board. A die shear tester was used to shear the components from the PCB. The force was applied in the longitudinal direction of the device, along the center line (Figure 23).

Shear values were recorded from five devices per run. When comparing devices with a significant difference in foot length, the shear force per unit area should be normalized. This test was performed to determine any variation in mechanical strength of the solder joints between test runs.

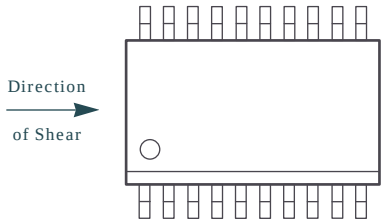


FIGURE 23 :
Direction of Shear During Mechanical Shear Test

Taguchi Designed Experiment

The goal of this study was to determine the effect of solder paste, reflow profile, and shelf life on board mount performance of surface mount devices. The test vehicle used was a 20 pin JEDEC Small Outline Integrated Circuit (SOIC) package. Two lead finishes were included, namely palladium plated devices and Sn/Pb solder plated devices. Each of the water soluble or no-clean pastes evaluated is commercially available and used industry-wide. The three reflow profiles used were intended to cover the spectrum of possible profiles seen in the field. Profile 1 (Figure 24) is a common profile used throughout the industry. The board encounters a pre-heat which raises the temperature to 150-170°C for approximately 4 minutes. Once pre-heated, the board temperature rises to 215-

220°C and quickly drops off after the solder paste is reflowed. This profile would be used by a customer with a large, complex board with non-uniform heating. Profile 2 (Figure 25) uses a 150-170°C pre-heat for approximately 2 minutes. The board temperature then rises to 215-220°C for reflow. This type of profile would be used with a small, uniform board. Profile 3 (Figure 26) slowly ramps up to the reflow temperature of the solder paste and then drops off as the board exits the oven. This profile would be used by the shop whose oven did not allow for much flexibility but whose boards were fairly complex and required a long pre-heat.

Steam age was chosen as a method which would simulate shelf storage.

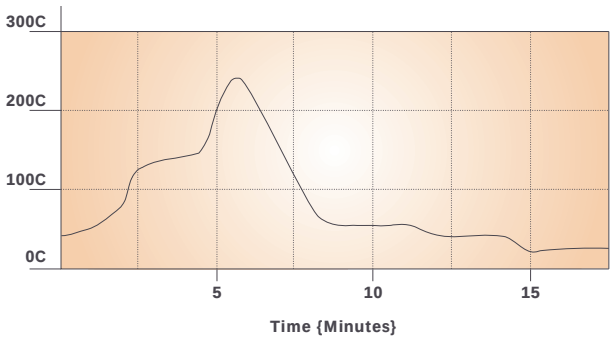


FIGURE 24 : Reflow Profile 1

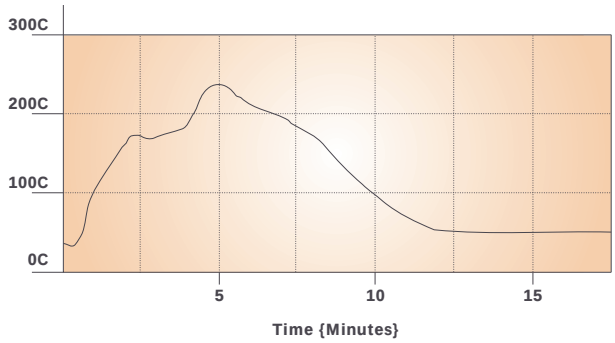


FIGURE 25 : Reflow Profile 2

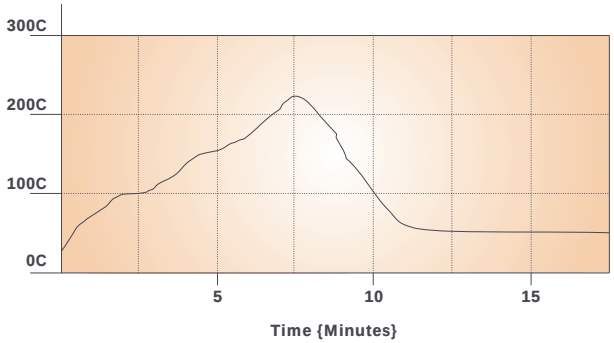


FIGURE 26 : Reflow Profile 3

Three levels (0, 12, and 24 hours) were used to determine the impact of extended shelf storage on board mount performance.

An L9 Taguchi designed experiment was chosen as the test matrix (Table 22). Runs 1-3 are occupied by a 63 Sn/37 Pb RMA solder paste used industry-wide. This paste is designated C1. A non-activated rosin-type paste was used for runs 7-9. This paste is designated C2. The intent in the choice of the control pastes was to "bracket" the expected performance of the evaluation pastes. C1 was expected to perform better than the evaluation pastes with regard to wetability and C2 was expected to perform worse. Replicate runs of rows 4-6 were performed for each of the water soluble or no-clean solder pastes evaluated. The evaluation pastes are designated E1, E2,...E5.

This matrix design allows for calculation of an Analysis of Variance (ANOVA) table for each evaluation paste. The ANOVA table calculations compute the variance seen between each evaluation paste and the two control solder pastes and assigns percent contributions of each factor to that variance.

TABLE 22 : L9 Taguchi Designed Experiment

Run	Solder Paste	Reflow	Steam Age {Hrs}
1	C1	1	0
2	C1	2	12
3	C1	3	24
4	EP*	1	24
5	EP*	2	0
6	EP*	3	12
7	C2	1	12
8	C2	2	24
9	C2	3	0

* Solder paste under evaluation.

Test Equipment And Procedure

The screen printer and pick-and-place machines used were Fuji GSP-II and Fuji IP-I, respectively. The reflow oven was a Vitronics 20 panel oven.

The printed circuit board used in this evaluation was a 6-1/2" x 7-1/2" FR4 board designed to accommodate 36 test devices (Figure 27). Each run of the test matrix was built on a single board. After reflow, the boards were disassembled so shear tests and cross-sections could be performed on the individual units.

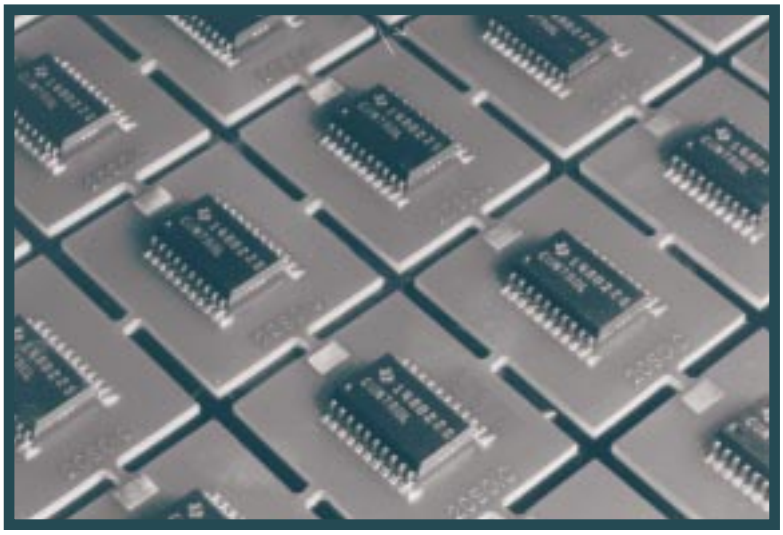


FIGURE 27 : FR4 Test Board With Mounted Devices

Results

The two responses used to measure and compare board mount performance were contact angle and the force necessary to shear the SOIC device from the board after mounting. ANOVA calculations were performed using contact angle and shear force measurements for each evaluation paste. These calculations were performed for both the palladium plated units and the solder plated units. As stated previously, the ANOVA calculations are used to determine the percent contribution of each factor to the total variance between the evaluation paste and the two control pastes. The error column indicates residual error inherent in the process. If the percent contribution assigned to a particular factor is greater than the residual error, then that factor can be considered to be a signif-

icant source of process variation.

Table 23 shows the ANOVA results for the response of contact angle for both palladium and solder plated units. For palladium plated devices, the solder paste had a significant contribution to the variance in four of the five cases evaluated (E2 through E5). For the solder plated devices, none of the three factors showed to be significant contributors to the variance, with the exception of the E5 paste case. For the E5 evaluation paste, the solder paste factor showed to be significant.

TABLE 23 : ANOVA Table for Contact Angle Response, Percent of Variance Attributable to Each Factor

	Solder Paste	Reflow Profile	Steam Age	Residual
Palladium Plate				
E1	49.3	0	0	50.7
E2	93.0	3.5	2.4	1.1
E3	63.1	13.2	15.1	8.6
E4	69.1	0	2.3	28.6
E5	73.9	8.8	6.5	10.8
Solder Plate				
E1	36.8	6.0	19.0	38.2
E2	0	9.3	0	90.7
E3	18.4	0	0	81.6
E4	25.8	0	8.2	66.0
E5	43.9	8.8	7.6	39.7

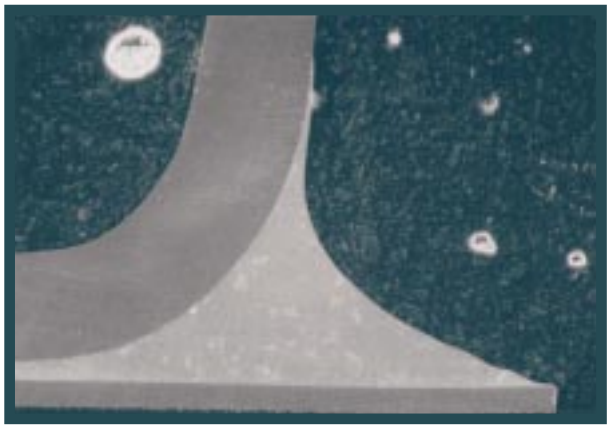


FIGURE 28 :
Palladium Plated SOIC Device, Water Solubles Paste E5

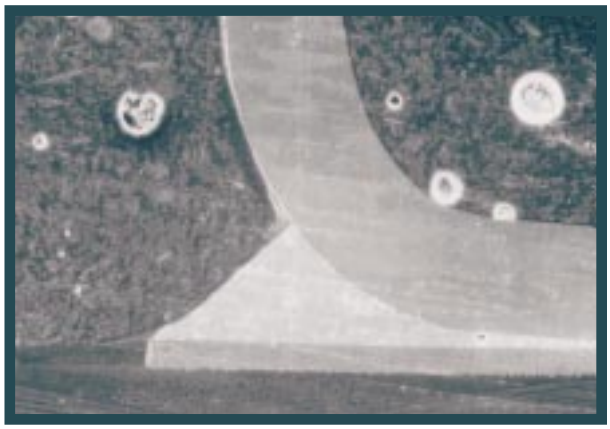


FIGURE 29 :
Palladium Plated SOIC Device, No-clean Paste E2

FIGURE 30 :
Palladium Plated SOIC Device, No-clean Solder Paste E4

Figures 28-30 show typical cross-section results for various evaluation pastes with palladium plated units.

Table 24 shows the ANOVA results for the response of shear for both palladium plated and solder plated units. During shear strength measurements it was noted that there was a slight difference in the lead contact area with the board between solder plated leads and palladium plated leads. This is due to a difference in lead length used between manufacturers. Because shear strength is a function of lead surface contact area with the board, the shear data was normalized. With palladium plated units, the contribution to the variance attributed to the solder paste and steam age were significant for evaluation paste E1. For E2 through E5, none of the three factors showed to have a significant contribution to the variance. With solder plated units, the solder paste factor alone was a significant contributor to the variance for evaluation pastes E2 through E5. For evaluation paste E1 none of the factors were significant.

In an effort to compare the performance of the evaluation pastes, the average and standard deviation were calculated for each paste using rows 4, 5, and 6

TABLE 24 : ANOVA Table for Shear Response, Percent of Variance Attributable to Each Factor

	Solder Paste	Reflow Profile	Steam Age	Residual
Palladium Plate				
E1	39.8	0	33.2	27.0
E2	10.0	0	0	90.0
E3	15.5	0	6.4	78.1
E4	0	0	0	100.0
E5	0	0	0	100.0
Solder Plate				
E1	39.2	3.6	3.5	53.7
E2	92.4	1.2	1.4	5.0
E3	96.8	0.4	0.5	2.3
E4	70.9	0	0	29.1
E5	54.4	0	0	45.6

of the matrix (Table 22). An average and standard deviation were also calculated for the control pastes in rows 1 through 3 and rows 7 through 9. Figures 31 and 32 graphically show the results of the contact angle measurements (average +/- one standard deviation) for palladium and solder plated leadframes, respectively. Figures 33 and 34 similarly show the shear force data. The horizontal lines in each graph indicate the limits for statistical significance at 95% and 99%. Basically, any mean value that falls outside of the limits can be considered statistically different from the group with either 95% or 99% confidence level.

Figures 31 and 32 show the variation in contact angle between the various solder pastes for each lead finish. The palladium plated devices exhibited greater sensitivity to changes in paste compared to the solder plated devices, however, the performance trend of the various pastes was similar for both lead finishes. It can be noted that at least one water soluble and one no-clean paste gave contact

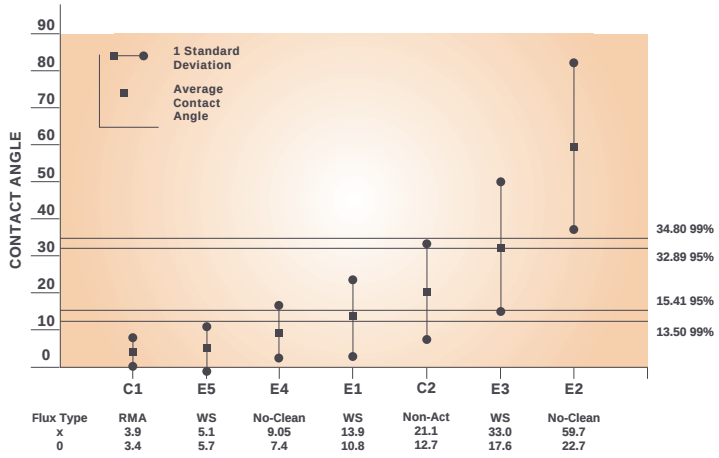


FIGURE 31 : Contact Angle for Palladium Plated Leads

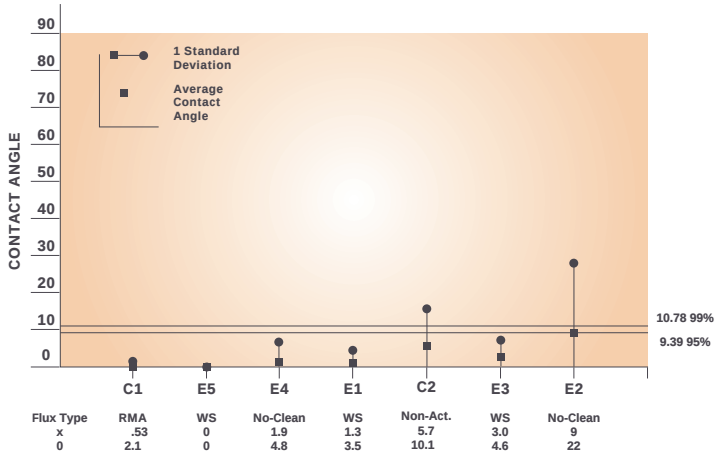


FIGURE 32 : Contact Angle for Solder Plated Leads

angle results comparable to paste C1 for both lead finishes. Figures 33 and 34 indicate shear force did not vary greatly when the paste was changed for either lead finish.

As described earlier, cases of solder wicking up the lead can contribute to assembly yield loss and degradation of long-term reliability. In several instances, the solder plated leads exhibited wicking up the lead to the point of interface with the package (Figure 35). This phenomenon of solder wicking was not seen to occur on any of the palladium plated devices.

The conclusions from this study are as follows:

- *The solder paste formulation has a strong impact on contact angle of the solder joint. Palladium plated devices exhibited a greater sensitivity to changes in solder paste, however the performance trend of the pastes was similar for both lead finishes. At least one no-clean paste*

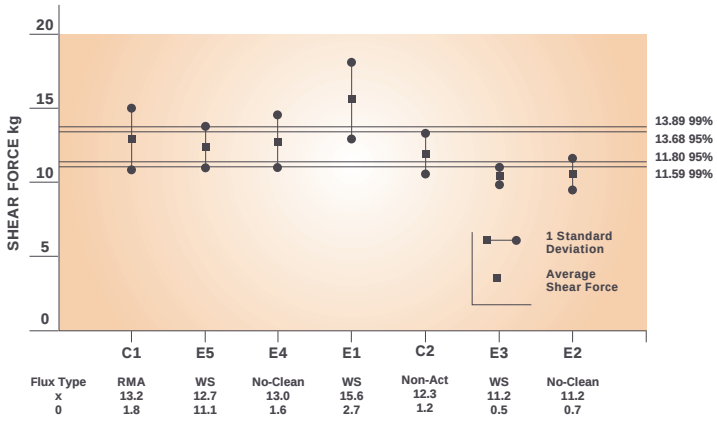


FIGURE 33 : Shear Force for Palladium Plated Leads

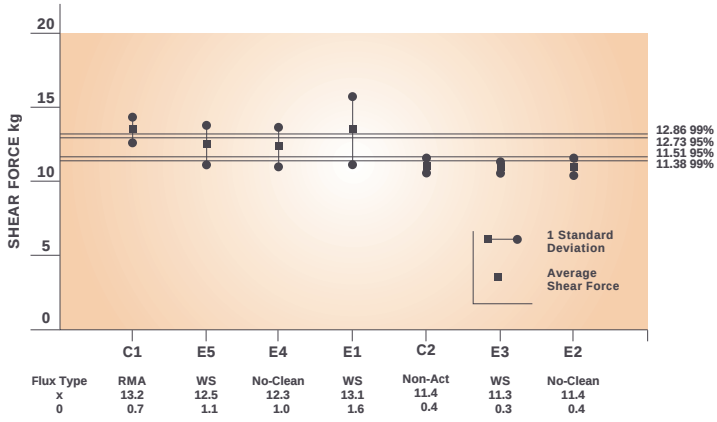


FIGURE 34 : Shear Force for Solder Plated Leads

and at least one water soluble paste performed well for both palladium plated and solder plated devices.

- *Variations in steam age time and reflow profile have minimal impact on the variance of the solder joint contact angle for either palladium plated or solder plated devices.*
- *Solder paste formulation has the greatest impact on shear strength of the solder joints for solder plated leads. For palladium leads, solder paste was a significant factor in shear strength variation in only one of five cases.*
- *Solder wicking was noted in several cases with the solder plated devices. Wicking was not noted on any of the palladium plated devices. Solder wicking can drastically reduce a solder joints resistance to thermal cycling and is an important concern.*

One point of interest is the above results have tracked exactly with customer feedback. Specifically, customer visual appearance results with the various pastes tested above correlate with the contact angle measurements in Figure 31. Customers using water soluble paste E5 are quite satisfied with the visual performance.

Once this evaluation was completed, attempts were made to work with the solder paste vendors to promote compatibility with palladium lead finish. A

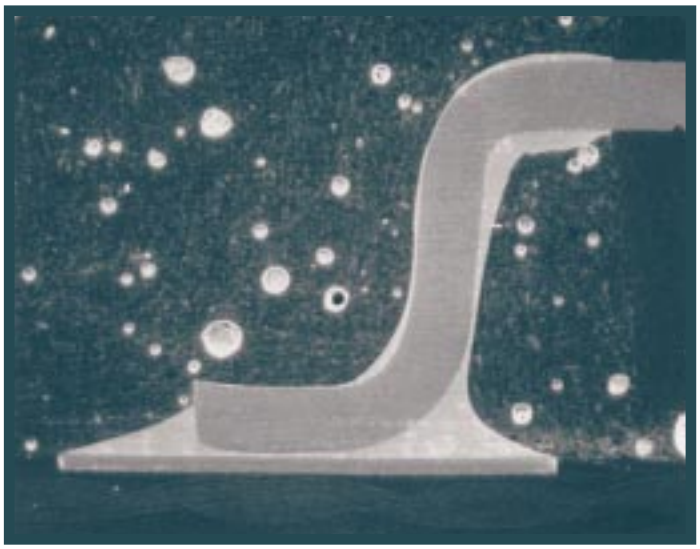


FIGURE 35 : Solder Wicking on Solder Plated Lead

meeting was held with each paste vendor to explain the performance of their paste(s) in the study and to offer palladium lead finish devices for solder paste evaluations. Several paste vendors have recognized the need for their pastes to perform well with palladium lead finish IC devices. TI is working closely with some of the paste vendors and has supplied finished devices for compatibility studies.

Degradation by Moisture Pre-conditioning

Solder joints made to palladium lead finish devices have been found to be mechanically equal to or stronger than joints made to Sn/Pb coated devices. In an attempt to create palladium joints with poor mechanical strength, 20 pin palladium SOIC devices were exposed to various levels of pre-conditioning prior to board mount. The units were board mounted using a standard reflow profile and Alpha WS609 solder paste. After board mounting, the units were sheared from the circuit board to compare the mechanical shear strength. The different levels of pre-conditioning with resulting shear strengths are shown in Table 25.

The results show that group 2 average is statistically lower than the other averages with a 99% confidence level. Also, the control group (no pre-condition-

TABLE 25 : Pre-conditioning Levels with Mechanical Shear Force Results

Group	Pre-Conditioning	Exposure	Sample Size	Shear Force Average (kg)	Shear Force Std Dev
1	85°C / 85% RH	168 hours	5	16.6	1.46
2	85°C / 60% RH	168 hours	5	15.5**	1.03
3	30°C / 60% RH	168 hours	5	18.5	1.33
4	30°C / 60% RH	72 hours	5	19.3	1.04
5	30°C / 60% RH	24 hours	5	18.0	1.7
6	30°C / 60% RH	6 hours	5	17.6	1.0
7	None	None	5	19.6*	1.1

* Indicates this group average is statistically different from all other group averages with 95% confidence level.
** Indicates this group average is statistically different from all other group averages with 99% confidence level.

ing) is statistically higher than all other group averages with a 95% confidence level. This shows that all pre-conditioned group averages are statistically similar with the exception of group 2. Also, the control group did perform slightly better than all other groups.

The purpose of this experiment was to intentionally degrade the palladium units and attempt to create a mechanical failure. By review of the data, the minimum shear value recorded was 14.5kg (in group 2). This minimum value converts to 32lbs. Even though there was a slight difference in the averages of the shear values, the fact that the minimum shear value was 32lbs indicates more than adequate strength for the palladium joints. The data is certainly meaningful, however this test did not yield a mechanical failure with the palladium plated SOIC devices.

PDIP Board Insertion Issues

Plastic Dual In-Line Packages (PDIPs) were introduced in palladium lead finish in 1990. Conversion of the PDIP package to palladium occurred with almost no interruptions. Just a few TI customers have experienced issues with board insertion of the PDIP package when using auto-insertion equipment manufactured by Universal Instruments. This issue has been addressed by both TI and Universal and is now understood.

On the Universal insertion equipment the actual insertion process consists of two steps: 1) gripping the PDIP unit and 2) alignment/insertion of the leads into the printed circuit board. The Universal equipment has two sets of steel combs to accomplish this process. Figure 36 shows the two combs which make up one side of the insertion jaws.

The inner jaws, or grippers, grab the PDIP unit and hold the individual leads just above the standoff. The gripper jaws have vertical grooves equal in width to the shoulder of the PDIP lead. The gripper jaws pick the unit and perform gross alignment of the lead with the outer jaws.

The second step in the PDIP insertion process is simultaneous alignment and insertion of the lead into the printed circuit board. The alignment guides extend below the gripper blades to make contact with the narrow lead tip. The alignment guides are designed with funnel shaped grooves to direct the lead tip into the PCB hole as the PDIP unit is forced through the jaws.

If the PDIP unit is not transferred to the head jaws properly, this misregistration may cause the PDIP unit to "hang up" on the alignment guides. Usually the PDIP unit will be forced through the jaws and into the printed circuit board. On occasion the leads will actually be bent and the unit will not insert into the board. On occasion the leads will actually be bent and the unit will not insert into the board. When the PDIP is not aligned with the alignment jaws a vertical scrape mark will be left on the wide area of the lead.

This issue was first reported by a major TI customer in Beaverton, Oregon. The customer was experiencing insertion errors on the Universal equipment with the TI palladium PDIP product. Upon investigation, the insertion jaws were found to be scraping the leads on both TI palladium product and solder plated product from other manufacturers. With the solder coated product however, the solder acts as a lubricant and allows the leads to slide through the jaws and into the board. The palladium lead finish devices do not have this Sn/Pb coating on the surface. If the jaws are misaligned and scrape the leads, the palladium prod-

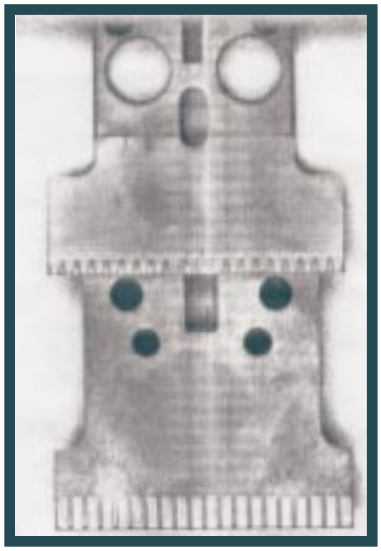


FIGURE 36 :
Gripper Blades (bottom) and Alignment Guides (top) from Universal Auto-Insertion Equipment

uct will exhibit the scraping problem first. When the problem was understood at the customer's site, Doug Romm of TI traveled to Universal Instruments in Binghamton, Oregon to run palladium product through Universals standard PDIP insertion equipment. Universal ran several hundred PDIP units with no scraping or misinsertion issues. A Universal technician visited the TI customer and made alignment corrections to the insertion heads. No PDIP insertion issues have been reported from this customer since that time.

The majority of TI customers using palladium PDIP devices use auto-insertion equipment manufactured by Universal. Only a few customers using TI palladium PDIP product have reported the same problem as described above. In each case Universal has made alignment adjustments and the problem has been corrected. This has not been an overwhelming problem for palladium PDIP users.

Flux Residue Issue on Palladium PDIPs

Since the introduction of palladium lead finish devices a few users have called to report problems with a discoloration on the lead surface or discoloration on the PCB near the device lead on palladium PDIP units. Typically this discoloration will be a chalky white or dark brown residue and will be seen after reflow and board wash. Initially the discoloration appears to the user to be present only on the leads of the TI devices. In each case TI will request a sample circuit board exhibiting the problem to be sent to TI for analysis. Also a sample of the flux in use is also requested.

In each case, the culprit has been flux residue not completely washed off during the wash process. This flux residue is most apparent on the TI palladium lead finish devices because of the shiny, almost mirror finish of the palladium devices. The customer usually reports seeing the residue only on the TI parts on the board, however upon close investigation the residue can be found on other devices on the board. Palladium product appears to be a good "barome-

ter" to show when the cleaning process is not performing correctly. TI has performed FTIR analysis of the residue and in every case has been able to identify flux left on the board after the wash process. The user must realize here that flux residue left on the board may pose a long-term reliability issue and every effort should be made to insure proper cleaning after board mount.

In one instance, a major TI customer in San Jose reported a problem with brown residue left on the TI palladium PDIP leads. On a visit to the site, the problem was found to exist in one process line only while nearby reflow lines did not exhibit a residue issue. A Megohm meter was used to test the cleanliness of the boards coming off of the line in question and compare to cleanliness of boards processed on other lines. Printed circuit boards tested from the problem line showed ionic contamination levels of 2-5 times greater than the levels on other production lines. When the wash problem was addressed the residue issue was resolved.

Palladium Lead Finish for Fine-Pitch Packages

As the electronic packaging industry moves toward finer lead pitch (0.025" or less) packages the advantages of the palladium leadframe become more apparent. Compared to Sn/Pb coated devices, the palladium finish has a more consistent plating thickness. Also, because there is no Sn/Pb to flow off the leads during reflow, the palladium user can more accurately control the solder volume in the joint. This feature is increasingly more important in controlling solder bridging with fine pitch devices. Component users are now experiencing one of the main advantages of the palladium lead finish as they mount greater numbers of fine pitch devices.

In 1989, TI converted the Small Outline Integrated Circuit (SOIC) package to bare palladium lead finish. The SOIC is a surface mount package with gull-wing leads and a lead pitch of 0.050". In 1990, TI converted the Plastic Dual In-line Package (PDIP) to palladium lead finish. The PDIP package is a through-hole component with lead spacing of 0.100". Also in 1990, TI introduced the 48 and 56 pin Shrink Small Outline Package (SSOP) into the market in palladium lead finish. This surface mount package has gull-wing leads with a lead spacing of 0.025".

Recently TI introduced a FIFO device in a 132 Bumpered Quad Flat Pack (BQFP) with palladium lead finish. This package has a lead pitch of 0.025". TI has also introduced 64, 80, and 100 pin Thin QFP with 0.5mm lead pitch (0.0197") and a 120 pin TQFP with 0.4mm (0.0157") lead pitch in palladium lead finish. Most recently TI introduced the low pin count (14-24 pin) SSOP and Thin SSOP packages with lead pitch of 0.65mm (0.0256").

TI's strategy is to introduce any new fine pitch packages into the market with palladium lead finish.

No-Lead Solder Paste Compatibility

Concern has grown recently over the amount of lead used in manufacturing environments. In response, leaders in the electronics industry have begun to investigate alternatives to traditional Sn/Pb solders. The National Center for Manufacturing Sciences (NCMS) has begun a project entitled "Alternatives to Lead (Pb) Based Solders". This study is composed of participants from across the electronics industry. The main objectives of this project are:

- *Identify and evaluate lead-free solder alloys for electrical/electronic assembly interconnections.*
- *Validate alternatives with manufacturing assessments, environmental stress screening, and reliability testing.*

TI palladium lead finish devices have been identified as a primary test vehicle for lead-free solders. Palladium components have no Sn/Pb on their surface to influence test results of lead-free solders. In order to accurately measure performance of the lead-free solder alternatives there should be no lead introduced into the solder joint. Traditional solder plated or dipped components can influence test results when evaluating no-lead solder alternatives.

TI has supplied palladium lead finish components to the NCMS in the 132 BQFP and the 20 SOIC packages. Studies are underway to evaluate no-lead solder paste alternatives with palladium lead finish devices.

Compatibility with lead-free processes is yet another advantage for the palladium lead finish.

Other Component Suppliers and Palladium

TI began the conversion to palladium leadframes in 1989. As this conversion has progressed other electronic component suppliers have seen the advantages to using palladium lead finish leadframes. The reduced cost and improved package integrity have appealed to several IC suppliers in the market.

Motorola began investigating the option of using the palladium lead finish leadframes in 1992. Motorola has built prototype samples of PDIP, SOIC, SIP, SOJ and QFP packages in palladium lead finish. Several of these packages are in qualification at present.

In late 1992, Doug Romm and Don Abbott of TI visited Motorola sites in Malaysia, Taiwan, and the Philippines. Don presented background on the palladium lead finish and discussed the palladium leadframe plating process. Doug worked with Motorola personnel on steam age solderability test issues.

Advanced Micro Devices (AMD) has also built IC packages using palladium leadframes. TI has worked closely with representatives of AMD to discuss packaging and solderability test issues. AMD has built a 44 pin SOIC package using palladium leadframes and is presently qualifying this package.

Acknowledgements

Development:

The author recognizes Don Abbott and Neil McLellan as the primary developers of the Ni/Pd lead finish in use by TI. Other major contributors to development work were Rich Brook, Larry Nye, and Jim Thomas.

Surface Mount Solderability Test:

The author recognizes Willie Reynolds as the co-author of this section. The author also recognizes the following employees of TI Dallas Environmental Test Laboratory for their professional assistance:

- *Steven Anderson for color photography of the test procedure.*
- *Somsack Vang for extensive evaluations using the SMT test method.*
- *Frances Allmon and Bill Frizzell for visual inspection and documentation of test results.*

The author recognizes Bill Ross and Paula Clark of TI Sherman Failure Analysis Laboratory for SEM photographs of soldered samples.

Water Soluble and No-Clean Paste Study

The author recognizes Neil McLellan as the co-author of this section. The author also recognizes Lynne Delp and Linden Halstead of TI Temple for their professional assistance with the board mount portion of this evaluation.

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