250 Watt Off-Line Forward Converter — Design Review

by Raoji Patel

Topic 4

250 WATT OFF-LINE FORWARD CONVERTER

DESIGN REVIEW

by

Raoj Patel

This paper gives a practical example of the design of an off-line switching power supply with forward converter topology. Topics include transformer and filter inductor design, proportional base drive, component selection, output filter design, and closing the control loop using the new Unitrode UC1524A control circuit.

POWER SUPPLY SPECIFICATIONS:

TOPOLOGY:	Forward Converter with Proportional Base Drive	
LINE INPUT:	117 Volts +/- 15% (99-135V), 60Hz	
	230 Volts +/- 15% (195-265V), 50Hz	
OUTPUT:	Voltage:	5 Volts
	Current:	5 to 50 Amperes
	Current Limit:	60 Amperes Short Circuit
	Ripple Voltage:	100mV p-p maximum
	Line Regulation:	+/- 1%
	Load Regulation:	+/- 1%
OTHER FEATURES:	Efficiency:	75%
	Line Isolation:	3750 Volts
	Switching Frequency:	40KHz

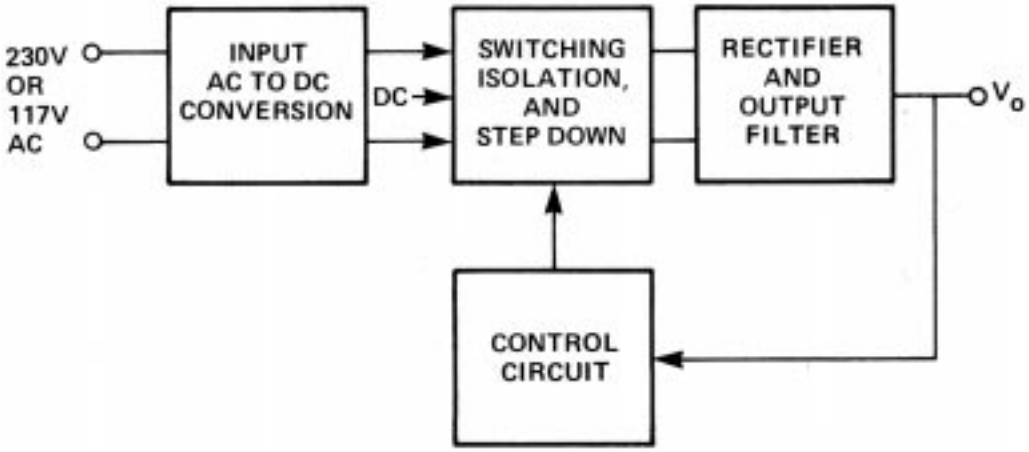

Figure 1. Block Diagram of the Switching Power Supply

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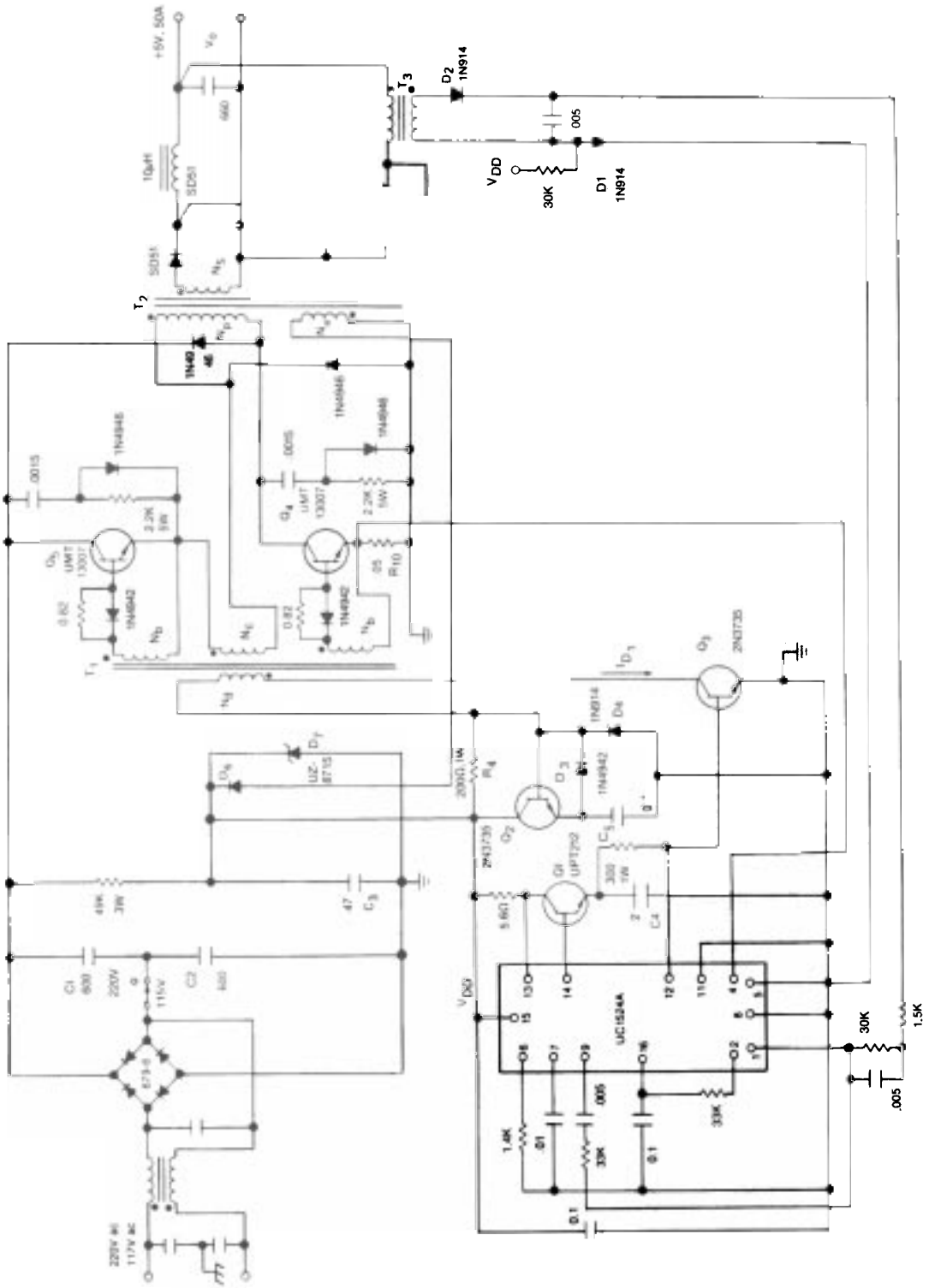

Figure 2. Complete 250 Watt Switching Power Supply

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THE COMPLETE POWER SUPPLY CIRCUIT

The complete 250 watt switching power supply schematic is given in Figure 2. This supply meets all of the specification requirements defined on page 1.

LINE INPUT AC TO DC CONVERSION

The input rectifier/filter section converts the AC line voltage into a crudely filtered and unregulated DC voltage, V_{in}, which powers the downstream switching regulator. The input section is configured as a full-wave bridge when operating from the 230 volt line, and as a voltage doubler when operated from 117 volts. This provides approximately the same V_{in} range (200-380 volts) for the switching regulator with either line voltage. Minimum input voltage, V_{min}, is 200 volts at low line.

The design of the input section is covered extensively in Section I1 of the Design Reference Addenda at the end of this book. The power input required in this application equals power output (250W) divided by efficiency (75%), or 333 watts. Circuit values for this application can be obtained by multiplying the 100 watt input values given in Table I of Section I1 by $P_{in}/100 = 3.33$, using the worst case voltage doubler configuration:

$$C_1 = C_2 = 3.33(160) = 533\ \mu F \quad \text{(use 600 } \mu F\text{)} \qquad (1$$

$$I_{chg} = 3.33(1.126) = 3.75 \text{ Amps RMS AC} \qquad (2)$$

The switching regulator draws 40 KHz rectangular current pulses which discharge the input capacitors. Peak discharge current, i_{dis}, occurs at Vmin when the duty cycle, D, is maximum (50%):

$$i_{dis} = Pin/(VminD) = 333/(200 \ .5) = 3.33 \text{ A peak} \qquad (3)$$

The RMS AC component of the discharge current, I_{dis}, which flows through the input capacitors at worst case 50% duty cycle is:

$$Idis = (idis)/2 = 3.33/2 = 1.67 \text{ Amps RMS AC} \qquad (4)$$

The total RMS AC current rating required for the input capacitors is calculated from Equation 8 of Section I1:

$$ICAP = \sqrt{Ichg^2 + Idis^2} = \sqrt{3.75^2 + 1.67^2} \qquad (5)$$

SWITCHING CIRCUIT TOPOLOGY

The two transistor forward converter configuration shown in Figure 3 was used in this 250 watt switching power supply for the following reasons:

1. Transistor voltage ratings are half the voltage required in a comparable single transistor circuit (400V vs. 800V). Only 1/4 the silicon chip area is required for the same current rating, and the switching speeds will be twice as fast.

2. The snubber networks are for load line shaping only and are not required to absorb all the energy stored in the transformer leakage reactance. Instead, clamp diodes D_5 and D_6 conserve most of this energy by returning it to the input, improving the efficiency.

3. Closed-loop stability is easier to achieve than with a flyback converter because there is no right half plane zero.

4. Filter capacitor requirements are much less severe than in boost or flyback converters because of the output filter inductor.

5. Transformer construction is simplified because there is no need for a clamp winding (N_a is used for the auxiliary supply).

6. Reliability is improved because faster transistors result in reduced switching losses, and each transistor dissipates only one half of these reduced losses.

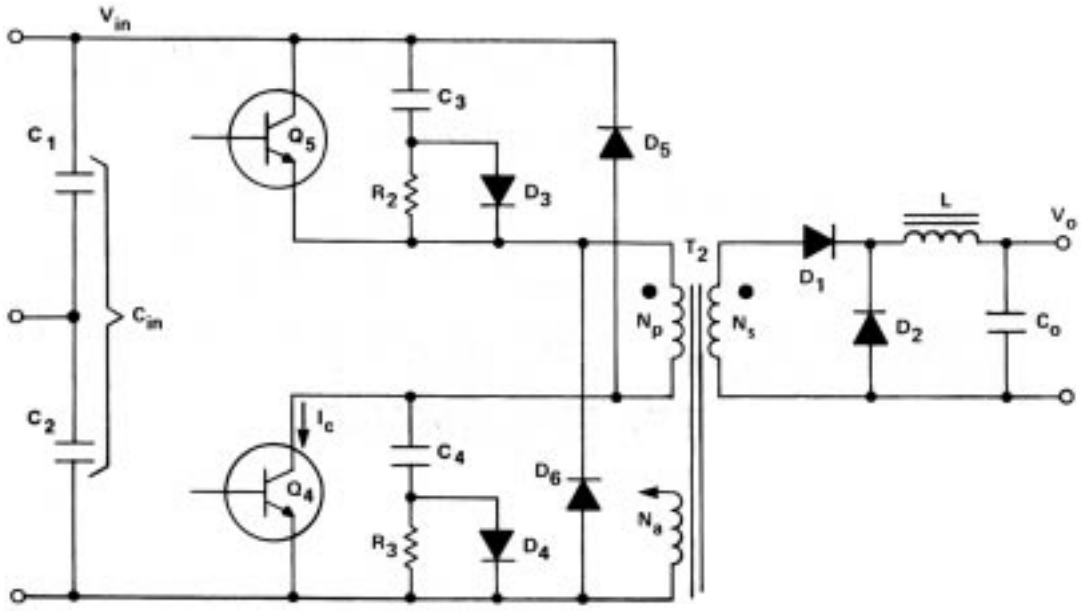

Figure 3. Two Transistor Forward Converter

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Disadvantages of this topology are:

1. Two transistors are required instead of one (but cost may be less).

2. Restricted to less than 50% duty cycle to permit core reset. This results in poorer transformer utilizetion.

3. Added cost of filter inductor, which is not required for the flyback converter.

SPECIFYING THE SWITCHING TRANSISTORS

Maximum peak primary current flowing through the transistors, I_{CM}, is the same as i_{dis} from Equation 3, or 3.33 A.

The transistors should have good VCE(sat) and switching speeds at a collector current of at least 4.0 amperes, which includes an allowance for unusual conditions such as short circuit current. (Disregard spec sheet "maximum current ratings" which are inflated for competitive marketing reasons, and focus on the specified test conditions.)

The collector voltage rating must be greater than maximum V_{in}, or 380 volts in this application. Conservatively, this should be the BV_{CEO} rating, but with careful load line shaping to make certain the transistor is completely off before voltage is applied, a less conservative designer might specify BV_{CEX} greater than $V_{in(max)}$.

The UMT13007 satisfies the above requirements, with BV_{CEO} of 400V, $V_{CE(sat)}$ less than 2.0V at 5A, and worst case fall time of 400ns under the proportional base drive conditions provided.

SNUBBER NETWORK DESIGN

The turn-off snubber networks shown across each transistor in Figure 3 provide shaping of the load line to ensure that it remains below the reverse bias safe operating area (RBSOA) of the transistors. Capacitors C_3 and C_4 accomplish this by holding the voltage across each transistor low during current turn-off. The snubber capacitors thus absorb the turn-off transition energy that otherwise would have been dissipated in the transistors (see Figure 4).

$$C_3 = C_4 = \frac{I_{CM}\, t_f}{2\, V_{in(max)}} \qquad (6)$$

$$\frac{3.33 \times .4 \times 10^{-6}}{2 \times 380} = .00175\ \mu F \qquad (\text{use } .0015\ \mu F)$$

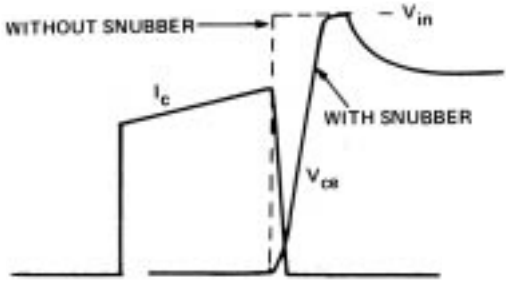

Figure 4. Effect of Snubber Network on Turn-Off Characteristic

Resistors R_2 and R_3 are designed to discharge the snubber capacitors with a discharge time constant of one-half the minimum on time, $t_{on(min)}$.

$$t_{on(min)} = \frac{D(max)}{f}\frac{V_{in(min)}}{V_{in(max)}} = \frac{0.5}{40,000}\frac{200}{380} = 6.58\ \mu s \qquad (7)$$

$$R2 = R3 = \frac{t_{on(min)}}{2C_3} = \frac{6.58 \times 10^{-6}}{2 \times 1.5 \times 10^{-9}} = 2.2K$$

Maximum power dissipation in each resistor:

$$P_{R2} = P_{R3} = \frac{1}{2} C2 V_{in(max)}^2 f \qquad (8)$$

$$= \frac{1.5 \times 10^{-9}}{2} \times 380^2 \times 40,000 = 4.3 \text{ watts}$$

POWER TRANSFORMER DESIGN

The design of the 40KHz inverter transformer is detailed in Appendix A. A primary to secondary turns ratio of 148/9, or 15.33, ensures that 5 volts output is provided with minimum Vin of 200 volts at 50% duty cycle, including voltage drops in rectifiers, transistors and windings.

Transformer winding N_a is used to provide an auxiliary supply to power the control and base drive circuits. This makes good use of the energy stored in the transformer primary inductance.

OUTPUT FILTER DESIGN

The output filter and its associated waveforms are shown in Figure 5. The filter inductor calculation is based on the maximum "off" time:

$$D(min) = D(max)\frac{Vin(min)}{Vin(max)} = 0.5\frac{200}{380} = .263 \qquad (9)$$

$$t_{off(max)} = \frac{1-D(min)}{f} = \frac{1-.263}{40,000} = 18.4\ \mu s \qquad (10)$$

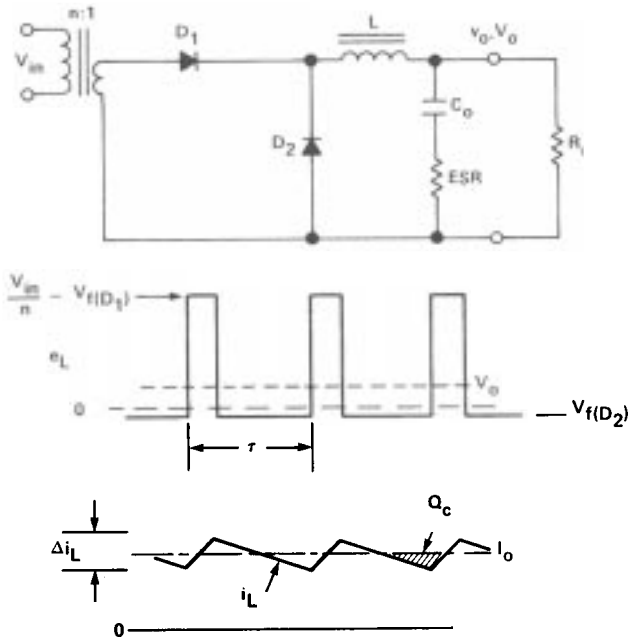

Figure 5. Output Power Filter Design

The inductance required to prevent discontinuous mode operation depends upon the minimum load current:

$$\Delta I_{L(max)} = 2I_{o(min)} = 2 \times 5 = 10A \qquad 11$$

$$L = \frac{(V_o + V_F)t_{off(max)}}{\Delta I_{L(max)}} = \frac{(5+0.6)18.35}{10} = 10\ \mu H$$

The capacitance required to achieve the output ripple voltage specification of 0.1 volts is:

$$C_o = \frac{1}{2}\frac{\Delta I_{L(max)}}{2}\frac{1}{2f\ v_o} = \frac{10}{8 \times 40{,}000 \times 0.1} = 312\ \mu F$$

The maximum ESR of the capacitor

$$ESR = v_o/\Delta I_{L(max)} = 0.1/10 = .01\ \Omega$$

To obtain the necessary ESR requires a capacitor much larger than the 312 microfarads calculated. This design will use three 220 microfarad solid tantalum capacitors, Mallory THF227M010P1G, in parallel. A single 14,000 microfarsd aluminum electrolytic capacitor, Mallory CG0143M10R2C3PL could also be used.

With the tantalum capacitor, the resonant frequency of the filter is 2KHz. With the aluminum electrolytic, the resonant frequency is reduced to 425Hz, changing the closed-loop design.

CLOSING THE CONTROL LOOP

The Unitrode UC1524A is used for the control circuit. It has additional features such as pulse by pulse current limiting and high current and voltage output capability (200mA, 60V) compared with the SG1524. The UC1524A reference is trimmed to +/- 1% which makes it possible to avoid using a voltage-setting potentiometer in many instances.

The control to output transfer function, dV_O/dV_C, shown in Figure 6, incudes the cascaded gain of the sawtooth modulator within the UC1524A control IC, the power switching circuit, and the output filter characteristic, $H_e(s)$.

In the control IC, a control voltage V_C is compared with sawtooth ramp voltage V_S (2.5 volts) to establish the drive pulse width to the power switches. For the forward converter, only one of the two alternating outputs of the UC1524A is used so as to limit the duty cycle to 50% maximum and allow for transformer core reset:

$$D = 0.5V_C/V_S = 0.5V_C/2.5 = V_C/5$$

The forward converter is a member of the buck regulator family Transformer turns ratio n = 16.44:

$$V_O = \frac{V_{in}}{n} D = \frac{V_{in}\, V_C}{n\, 2V_S}$$

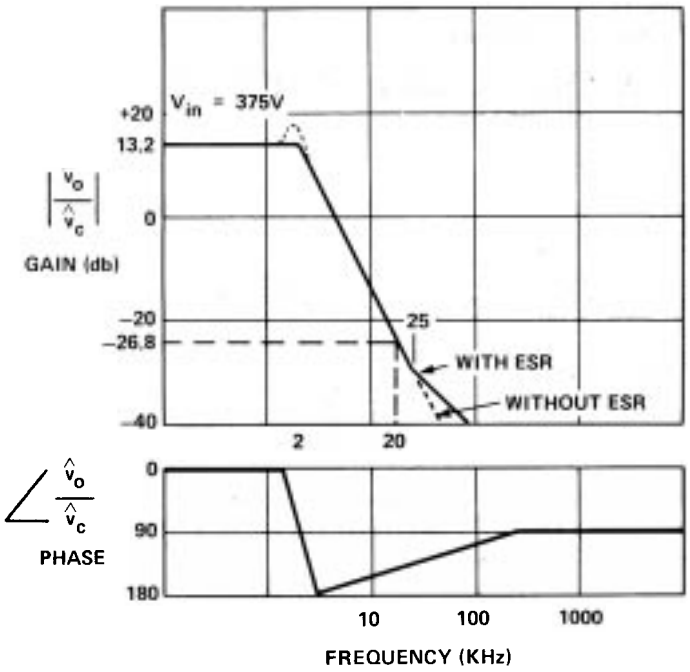

Figure 6. Control to Output Transfer Function LC Filter and Modulator

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The low frequency control to output transfer characteristic is obtained by differentiating with respect to Vc:

$$\frac{\partial V_O}{\partial V_C} = \frac{V_{in}}{n\ 2V_s} = \frac{380}{15.33 \times 5} = 4.95 = 13.2\ db \qquad (17)$$

Note that gain is greatest at maximum V_{in}. The overall control to output transfer characteristic including the filter is:

$$\frac{\partial V_O}{\partial V_C} = \frac{V_{in}}{n\ 2V_s} H_e(s) \qquad (18)$$

The filter introduces a two-pole characteristic at its resonant frequency (2 KHz). Above resonance, the gain drops 40db per decade, and the phase shift becomes -180 degrees. Combined with the -180 degree phase shift of the feedback network, this will cause instability and oscillations unless compensated.

Closing the loop involves feeding back the error voltage from the output terminal of the supply (⑦) to the IC control voltage port (②) through the UC1524A error amplifier. The approach taken is to make the gain of the feedback network such that the overall loop gain crosses zero db (with adequate phase margin) at one half the switching frequency.

As shown in Figure 6, control to output gain is 13.2db at low frequencies, rolling off above 2KHz at -40db per decade, so that at 20 KHz the control to output gain is 13.2 - 40, or -26.8db. For overall loop gain of zero,the feedback network gain must be made +26.8 db at 20 KHz.

From 20KHz down to 2Kz, there is a net single zero in the feedback network which cancels one of the two filter poles and reduces the phase shift in this region to -270 degrees.

Below the filter resonant frequency the two filter poles are gone. However, the resonant frequency may be less than 2KHz because of plus tolerances on the filter capacitor. The feedback network is therefore designed to transition from a net single zero to a single pole at 1KHz, half the resonant frequency.

Figure 7 shows the gain and phase plot of the error amplifier and the overall feedback loop. Figure 8 shows the specific feedback network used to achieve this result.

The high frequency error amplifier gain is set by R_2 and R_3. An R_3 value of 33K is chosen to minimize amplifier loading:

$$A_{v1} = R3/R2 = 26.8db = 21.9 \qquad (19)$$

$$R2 = R3/A_{v1} = 33000/21.9 = 1500\ \Omega$$

The required error amplifier gain at 1KHz is:

$$A_{v2} = A_{v1} \times 1KHz/20KHz = 21.9 \times 1/20 = 1.095\ (0.8db) \qquad (20)$$

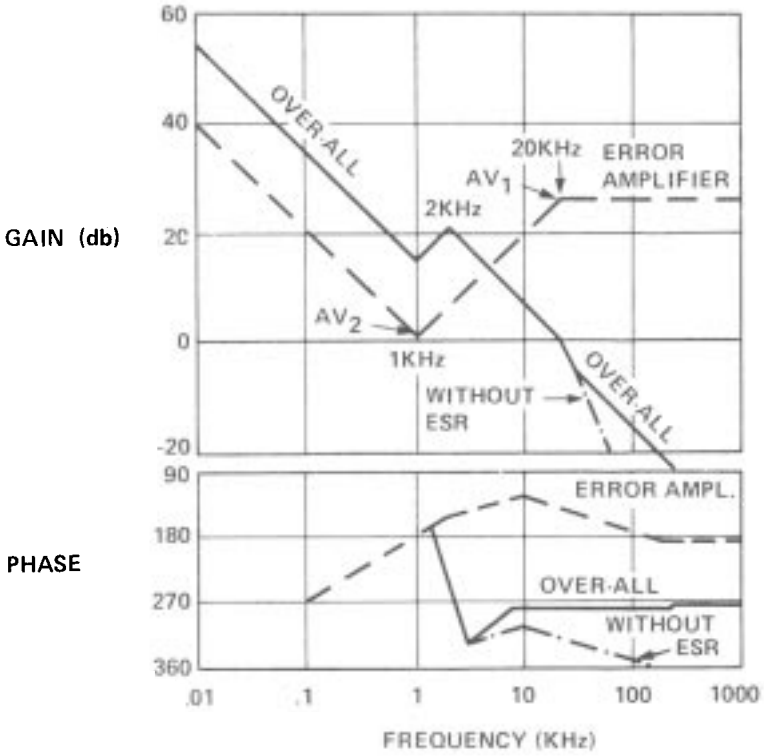

Figure 7. Open Loop Gain and Phase Plot

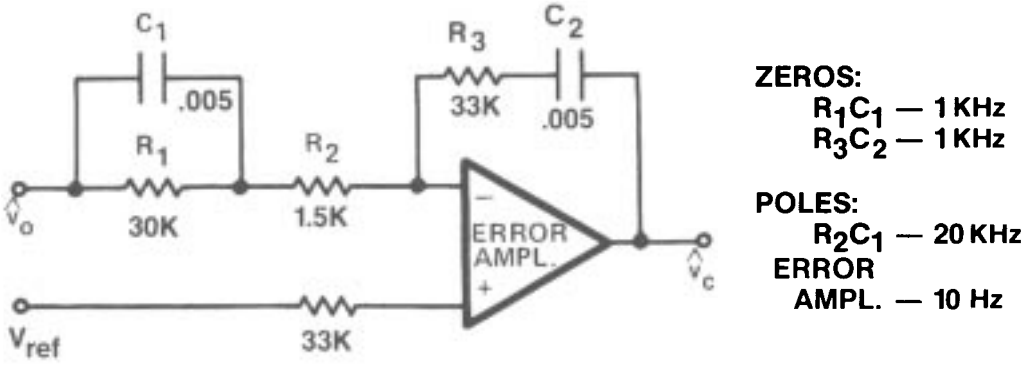

Figure 8. Error Amplifier with Compensation

The gain at 1KHz is determined by R_1, R_2 amd R_3:

$$Av2 = R3/(R1+R2) = 33K/(R1+1500) = 1.095 \quad [21]$$

$$R1 = 28.6K \quad \text{(use 30K)}$$

The two zeros at 1KHz which changes the feedback network from a net single zero to single pole are equal to:

$$f_1 = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_3 C_2} = 1 \text{ KHz} \qquad (22)$$

$$C_1 = .0053 \ \mu F, \qquad C_2 = .0048 \ \mu F$$

C_1 and R_1 in parallel with R_2 result in an additional pole at 20KHz. This flattens the error amplifier gain above 20 KHz. The overall phase shift will gradually increase toward 360 degrees, but it doesn't matter because the overall gain is less than one.

An additional pole occurs below 10 Hz. This is the inherent single-pole characteristic of the error amplifier's 5 megohm output impedance loaded by feedback capacitor C_2.

PROPORTIONAL BASE DRIVE

In Figure 2, transistors Q_2 and Q_3 and base drive transformer T_1 provide proportional drive to the bases of power switching transistors Q_4 and Q_5. The proportional base drive technique provides excellent performance from high voltage bipolar transistors. It provides large base current pulses for fast turn-on and turn-off, but with modest drive power requirements. Sustaining base drive is provided regeneratively from a collector current winding on the drive transformer. The transistors are never overdriven, even under light load conditions, since the sustaining base drive is proportional to the collector current. Design considerations for the proportional base drive technique are given in Section D1 in the design section at the back of this book.

Referring to the circuit of Figure 2, when Q_3 is on, R_4 establishes 75 mA magnetizing current in drive winding N_d of T_1. When Q_3 turns off, the energy stored in T_1 drives 150 mA into the base of each transistor. Collector current starting to flow in N_c provides sustaining base drive. With I_C of 3.33 A under full load conditions, an additional 667 mA of drive is provided to each base.

While Q_3 is off, capacitor C_5 charges through Q_2 in less than 1 microsecond. Then, when Q_3 turns back on, C_5 provides a negative base drive pulse of −1.5 A to each transistor, achieving turn-off in less than 1 microsecond.

Drive transformer T_1 has a drive winding inductance of 0.7 mH and is designed to saturate at 75 mA. High voltage insulation is not required because all windings are on the line side of the supply.

Core: Ferroxcube 1107P-L00-3B7 Pot Core
N_d: 20 turns AWG34
N_b: 5 turns AWG28x2 (2 wires, one for each base)
N_c: 2 turns 5xAWG28 (5 wires paralleled)

AUXILIARY POWER SUPPLY

A 15 volt auxiliary supply powers the control and driver circuits, obtaining its energy from capacitor C_3. Flyback energy is normally provided by T_2 through winding N_a and D_6 to maintain the charge on C_3 every switching cycle. However, at initial power-up it is neccessary to provide separate means to activate the V_{dd} supply. Otherwise, the control and driver circuits could not become functional and the supply could not start to switch.

The unique under-voltage lockout feature of the UC1524A facilitates this technique. All of its internal circuits are disabled (except the reference) until the Vdd voltage reaches 8 volts. This holds the standby current to less than 4mA until the 8 volt threshold is reached, and permits C3 to be initially charged through R1 from the unregulated input. Enough energy is stored in C3 to operate the control/drive circuits for several switching cycles, until flyback energy from winding N_a can take over and maintain the voltage on C_3.

It is also necessary to eliminate base drive to Q_3 during initial power-up, otherwise Q_3 will draw current through R_4 which will prevent C_3 from initially charging. This is accomplished by transistor Q_1 which disconnects base drive source capacitor C_4. When the UC1524A becomes active, its second output turns Q_1 on periodically to charge C_4.

The amount of energy stored in the power transformer is twice the drive/control circuit requirements. Excess energy is dumped into 15 volt zener diode D_7 which establishes the V_{dd} supply voltage at that level. This also provides a constant clamp voltage across the switching transistors, regardless of line voltage. With good coupling between N_a and primary winding N_p, it may be possible to eliminate clamp diodes D_{12} and D_{13}.

OUTPUT VOLTAGE SENSE AND OVERCURRENT SENSE

A small, inexpensive transformer, T_3, couples the output voltage to the line side control circuit with high voltage isolation. The transformer is wound on a Ferroxcube 204-T250-3E2A ferrite toriodal core. Primary and secondary windings are both 14 turns AWG32.

During the time the power switching transistors are on, Q_6 is on, applying V_o to the primary of T_3. Through D_2, this provides a real-time feedback voltage to the control circuit across C_6. When Q_6 is off, D_5 clamps the flyback voltage to 15 volts. Core reset is accomplished well before the end of the "off" time, since the "off" time of the forward converter is always more than 50%. All transformer windings then go to zero volts, establishing a DC coupling level. D_1 in series with the ground return compensates for the forward voltage drop and temperature coefficient of D_2.

Pulse by pulse current limiting is set by sense resistor R_{10}. Primary current is limited to 4A, corresponding to 62A load current.

Transient response of the switching supply is shown in Figure 9 with changes in load from 20A to 60A and back to 20A. This behavior is a large signal phenomenon. It doesn't matter how fast the control loop is, it is temporarily driven into the bounds because the load change is much larger than the output filter inductor current can accomodate in one cycle. Nevertheless, recovery is smooth and there is no evidence of ringing or oscillations, demonstrating the stability of the control loop. Step changes in load current that are small enough for the control loop to remain functional are barely noticable at the output.

Transient response can be improved by reducing the filter inductor and increasing the filter capacitor size, but this will increase the minimum load current required to keep the inductor current from becoming discontinuous.

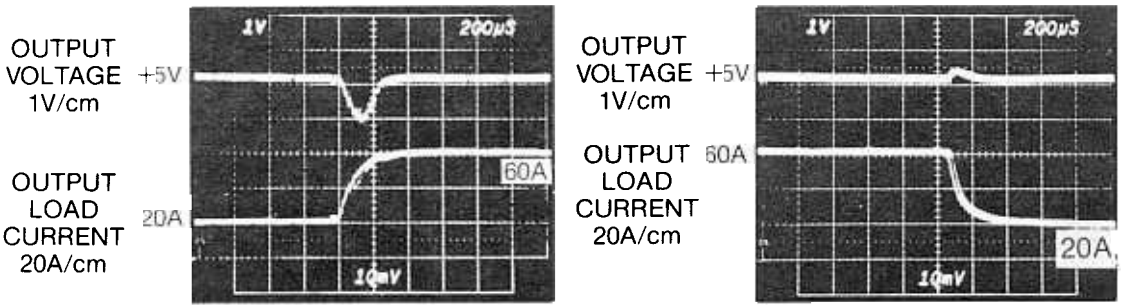

Figure 9. Step Change in Output Load

APPENDIX A

DESIGN OF THE POWER TRANSFORMER

AND FILTER INDUCTOR

The design procedure used herein is defined in Design Reference Section M5. Symbols, definitions and various core and wire data are given in Reference Sections M1, M2, and M3. Equation references are to Section M5.

Flux Density Excursion

In this forward converter application, the flux excursion is entirely within the first quadrant of the B-H characteristic, from zero flux density toward saturation. With simple duty cycle control, using the UC1524A control IC, it is possible to have nearly twice the normal volt-seconds, $V_{in(max)}t_{on(max)}$, during startup or after a large step increase in load current. This means that the flux density cannot be permitted to go more than half way toward saturation under normal conditions or the core will saturate under transient conditions.

Saturation flux density for 3C8 power ferrite material is greater than 0.3 Tesla (3000 Gauss), allowing a ΔB of 0.15 T (0 to 0.15 T) in this application. (With volt-second control, available in the UC1840 control IC, a ΔB of 0.3 T would be permissible, significantly reducing the transformer size.)

Core Selection

The core area product, AP, requirements in this application are calculated using Equation 1 and Table I of Section M5 with power input of 333 watts and frequency of 40 KHz.

$$AP = A_wA_e = \left(\frac{11.1\ P_{in}}{K\ \Delta B\ f}\right)^{1.143} = \left(\frac{11.1\ 333}{0.141\ 0.15\ 40{,}000}\right)^{1.143} = 5.4\ cm^4$$

This equation is based on the assumptions that the windings occupy 40% of the window area, the primary and secondary windings are of equal area, and the windings are operated at a current density that will result in a temperature rise of 30°C with natural convection cooling.

From Table I, Section M1, the EC52 core with an AP of 5.71 cm^4 is the obvious choice.

Designing the Windings

The minimum number of primary turns required to support the volt-seconds required for normal operation is calculated from Equation 2 of Section M5:

$$N_{p(min)} > \frac{5000\ V_{in(min)}}{\Delta B\ Ae\ f} > \frac{5000\ 200}{0.15\ 1.83\ 40{,}000} > 91 \text{ turns}$$

From Equation 3, the primary to secondary turns ratio is:

$$n = \frac{N_p}{N_s} = \frac{0.9\ D\ [V_{in(min)} - V_{CE(sat)}]}{V_O + V_F} = \frac{0.45(200-2)}{5+0.8} = 15.36$$

Secondary turns from Equation 4:

$$N_s = \text{Integer}(N_p/n) = \text{Integer}(91/15.36) = 6 \text{ turns}$$

Recalculate the primary turns:

$$N_p = 6 \times 15.36 = 92 \text{ turns}$$

RMS primary current from Equation 6

$$I_p = I_{in(max)}/K_t = \frac{P_{in(max)}}{V_{in(min)}\ K_t} = \frac{333}{200\ 0.71} = 2.34 \text{ A}$$

From Equation 7, the maximum current density for this size core is:

$$J_{max} = 450\ AP^{-.125} = 450(5.71)^{-.125} = 362 \quad \Omega/cm^2$$

The minimum primary wire area, A_{xp}, is:

$$A_{xp} = I_{p(max)}/J_{max} = 2.34/362 = .0065 \text{ cm}^2$$

From the Wire Table in Section M2 under 'AREA, Copper', AWG 19 is appropriate.

The maximum RMS secondary current, I_s, occurs at 50% duty cycle:

$$I_{s(max)} = I_{o(max)}/1.414 = 50/1.414 = 35.3 \text{ A}$$

Minimum secondary wire area, A_{xs}, is

$$A_{xs} = I_{s(max)}/J_{max} = 35.3/362 = .0975 \text{ cm}^2$$

From the Wire Table, this calls for AWG 7 to 8. Ten AWG 18 wires in parallel will carry the required secondary current and provide a smooth winding with less leakage inductance and acceptable eddy curent losses. Copper strip 4.5x.02 cm could also be used.

Th number of turns required for the auxiliary winding is:

$$N_a = \frac{V_{dd}\ N_p}{V_{in(min)}} = \frac{15\ 92}{200} = 7 \text{ turns}$$

This will provide enough volt-seconds during flyback to reset the core (back to zero flux density) at 50% maximum duty cycle. AWG 32 wire is adquate to carry the V_{dd} supply current. This winding should be tightly coupled to the primary.

Double-check the wire fit in the window (neglect N_a). The total copper area of all windings should be less than 40% of the total window area of the core (0.40x3.12 = 1.25 cm^2 max).

$$A_w' > N_p A_{xp} + N_s A_{xs} = 92(.0065) + 6x10(.00823) = 1.09\ cm^2$$

Calculate Losses and Temperature Rise

The total losses in the windings is calculated from Equation 12. The mean length per turn, l_t, for the EC52 core is 7.3 cm, and AWG 19 wire is .000353 Ω/cm from the Wire Table at 100°C.

$$P_w = 2\ I_p^2\ N_p\ l_t\ (\Omega/cm) = 2(2.34)^2x92x7.3x.000353 = 2.59\ watts$$

The total core losses for 3C8 ferrite are obtained from from Figure 1 in Section M3. The flux density axis of this graph assumes the transformer is operating with a symmetrical flux swing about the origin. The forward converter operates asymmetrically, so enter the graph with ΔB/2, or .075 T. The resulting 0.1 W/cm^3 must be multiplied by the core volume to obtain the total core loss, P_c.

$$P_c = .01x18.7 = .187\ watts$$

Total transformer losses are:

$$P_t = P_w + P_c = 2.59 + .187 = 2.78\ watts$$

The temperature rise of the core for natural convection cooling is calulated from Equation 14:

$$\Delta\theta = \frac{850\ P_t}{A_s} = \frac{850(2.78)}{91} = 25.9^{\circ}C$$

Summarizing the transformer design:

Core: Ferroxcube EC52, 3C8 Ferrite E-E core
Np: 92 turns AWG19
Na: 7 turns AWG32
Ns: 6 turns 10xAWG18 (10 wires paralleled)

The primary and auxiliary windings are tightly coupled. The secondary is insulated with 2mil mylar tape to provide 3750 volt line isolation capability.

Filter Inductor Design

The design of the filter inductor is covered extensively in Unitrode Application Note U68A, in the Unitrode Databook. Using this approach, the inductor design is summarized as follows:

Core: Ferroxcube 4229-3C8 Ferrite Pot Core
Winding: 7 turns 10xAWG17 (10 wires paralleled)
Losses: 2.2 watts
Temperature Rise: 35°C