

TEXAS INSTRUMENTS

Title DM355 Power Reference Design		
Size B	Number PMP3779	Rev A
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Filename: DM355\_bom.xls

Date: 12/10/2008

## DM355 Reference Design BOM

Count	RefDes	Value	Description	Size	Part Number	MFR
2	Q1	2N2222	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild
	Q2	2N2222	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild
3	C2	0.1uF	Capacitor, Ceramic, 50V, C0G, 5%	603	C1608C0G1H220J	TDK
3	C1, C4, C10	10uF	Capacitor, Ceramic, 6.3V, X5R, 20%	603	GRM188R60J106ME47D	muRata
1	C3	180nF	Capacitor, Ceramic, 50V, C0G, 5%	603	C1608C0G1H220J	TDK
2	C5, C7	0.1uF	Capacitor, Ceramic, 50V, C0G, 5%	603	C1608C0G1H220J	TDK
3	C6, C8, C9	1uF	Capacitor, Ceramic, 6.3V, X5R, 20%	603	GRM188R60J106ME47D	muRata
1	R1	1.8k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R2	30.1k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R3	47.5k	Resistor, Chip, 1/10W, yy%	805	Std	Std
1	R4	100k	Resistor, Chip, 1/10W, yy%	805	Std	Std
1	R5	475k	Resistor, Chip, 1/10W, yy%	805	Std	Std
1	R6	28k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R7	56.2k	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	U1	TPS79501DCQ	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF, 500mA, xxV	SOT223-6	TPS79501DCQ	TI
1	U2	TPS79533DCQ	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF, 500mA, 3.3V	SOT223-6	TPS79533DCQ	TI
1	U3	TPS73101DBV	IC, Cap-Free NMOS, 150mA LDO Regulator With Reverse Current Protection	SOT23-5	TPS73101DBV	TI

# 1 Block Diagram

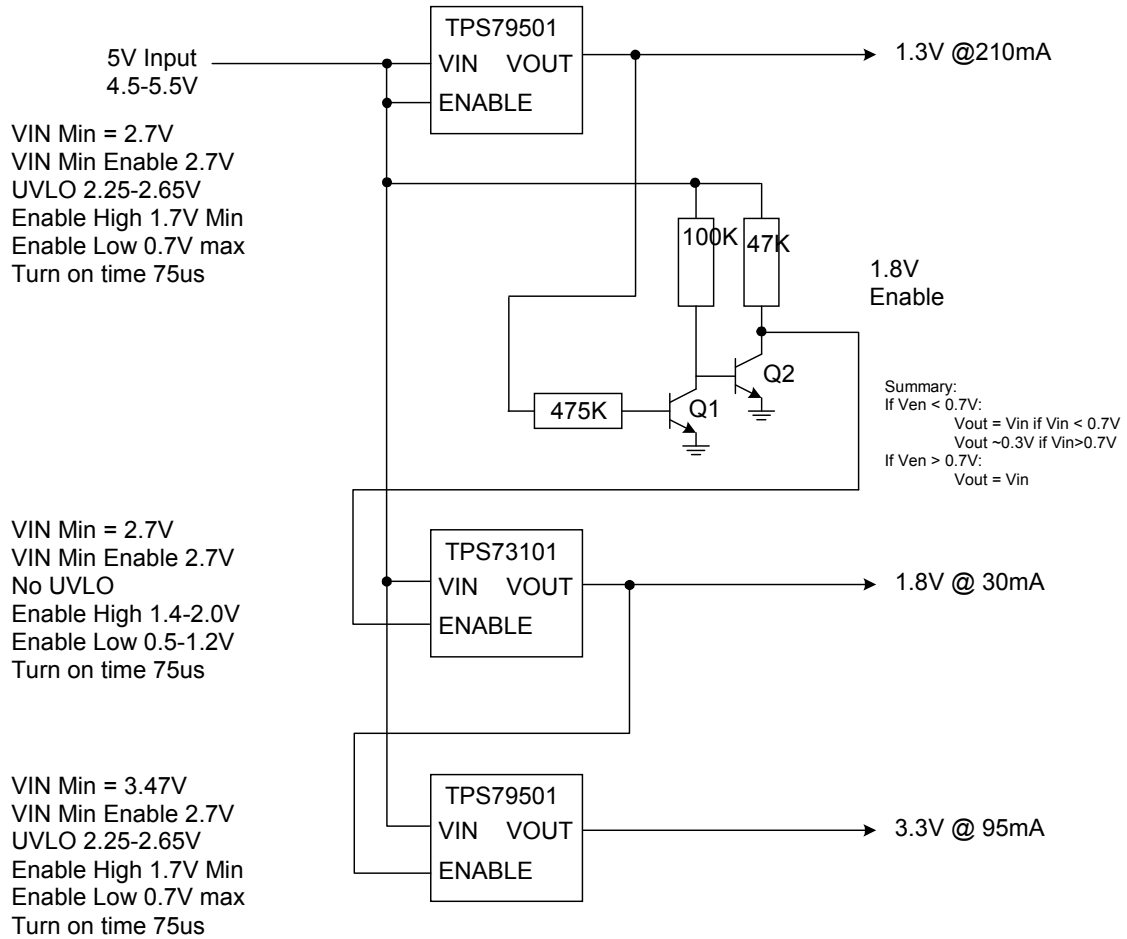
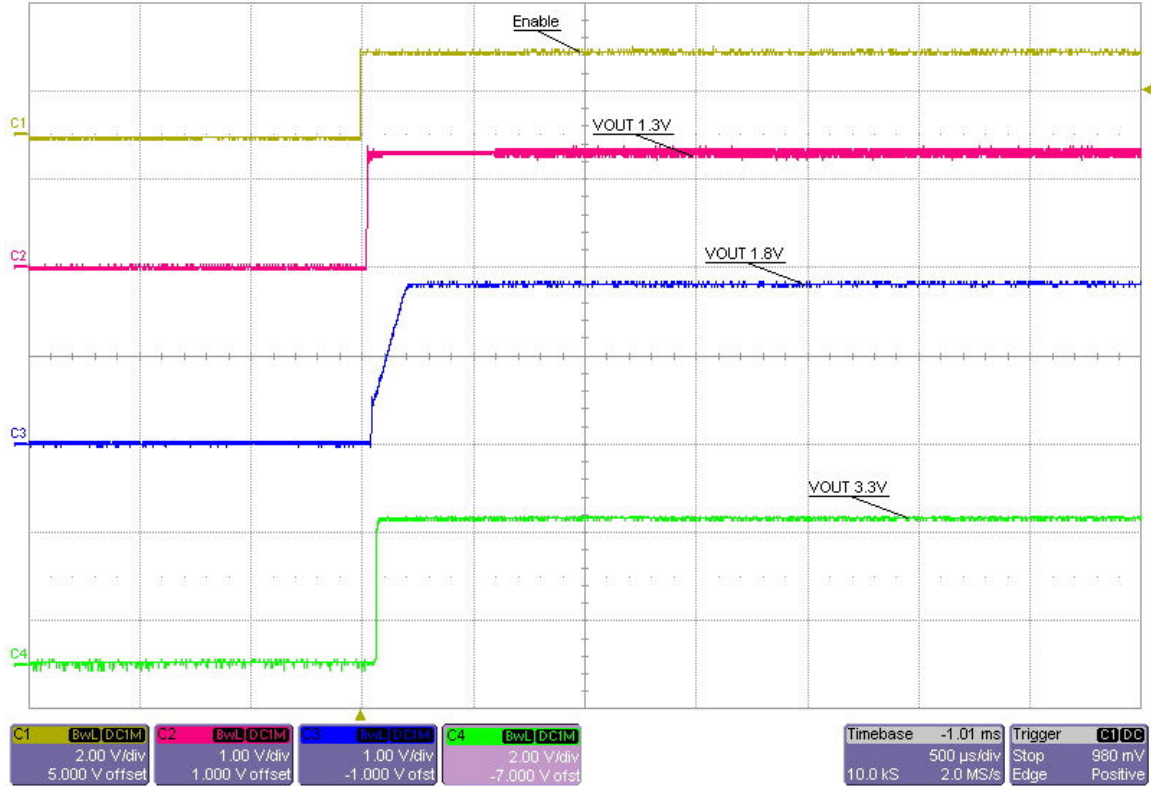


Figure 1. Block Diagram of Power Design

## 2 Power Up

The figure below shows the startup waveforms after ENABLE is applied. The outputs voltages shown are at full load. (Enable=2.00V/div, 1.3-V=1.00V/div, 1.8-V=1.00V/div, 3.3-V=2.00V/div, 500us/div)

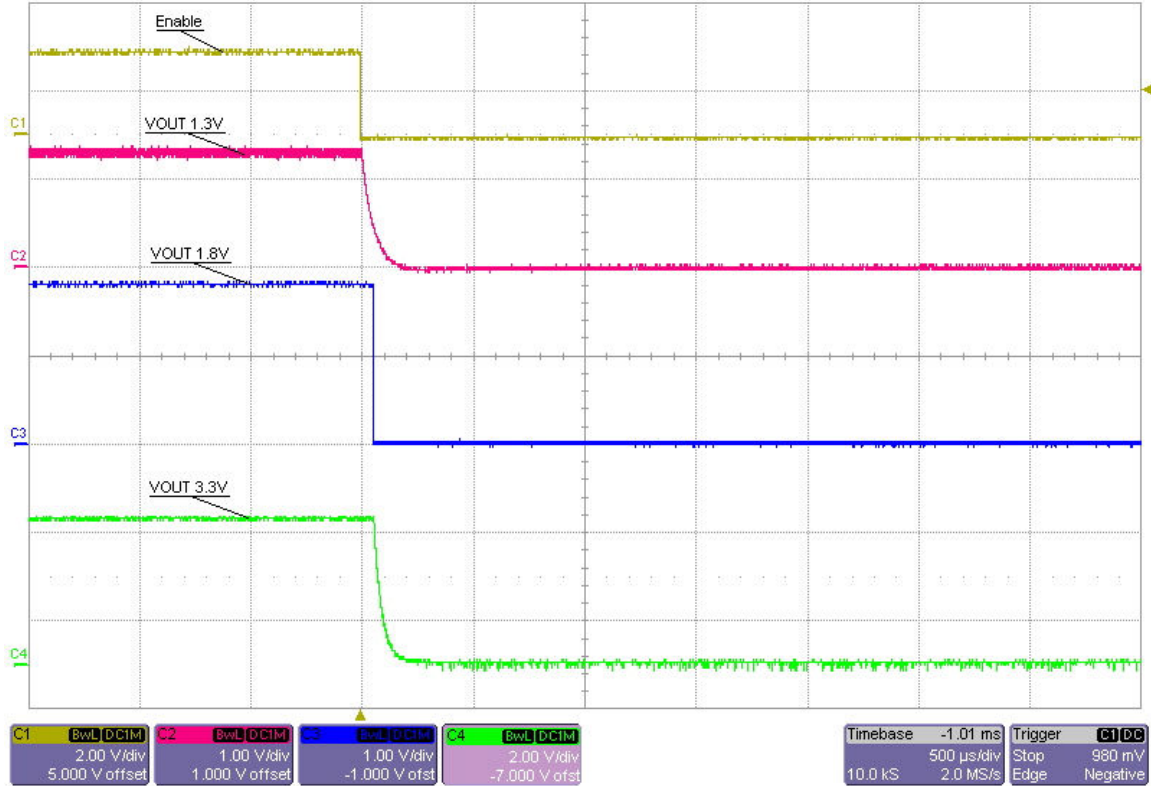


**Figure 2. Power Up with 5-V Input and ENABLE Voltage**

Once ENABLE is pulled high, the 1.3-V rail comes up and the 1.8V and 3.3V come up together later.

### 3 Power Down

The figure below shows the power down waveforms after ENABLE is pulled low. The outputs voltages shown are at full load. (Enable=2.00V/div, 1.3-V=1.00V/div, 1.8-V=1.00V/div, 3.3-V=2.00V/div, 500us/div)



**Figure 3. Power Down with 5-V Input and ENABLE Voltage**

Once ENABLE is pulled low, the 1.3-V rail starts to come down first, and 1.8V and 3.3V come down after 50us.

### Thermal Considerations:

TPS79501: (from page 11 of TPS79501 datasheet)

$$V_{in}=5V, V_{out}=1.3V, I_{out}=210mA$$

$$P_D = (5 - 1.3) * (210) = 780mW$$

For Ambient temperature of 85C

$$R_{\theta JA} = \frac{(125 - 85)C}{780mW} = 51.3 \frac{C}{W}$$

Using Figure 26 of TPS79501 datasheet, with no airflow, the ground plane needs to be approximately 1.5 in<sup>2</sup> to dissipate 780mW.

<http://focus.ti.com/lit/ds/symlink/tps79501.pdf>

TPS79533: (from page 11 of TPS79501 datasheet)

$$V_{in}=5V, V_{out}=3.3V, I_{out}=95mA$$

$$P_D = (5 - 3.3) * (95) = 162mW$$

For Ambient temperature of 85C

$$R_{\theta JA} = \frac{(125 - 85)C}{162mW} = 247 \frac{C}{W}$$

Using Figure 26 of TPS79501 datasheet, with no airflow, the ground plane needs to be approximately 0.1 in<sup>2</sup> to dissipate 247mW.

<http://focus.ti.com/lit/ds/symlink/tps79533.pdf>

TPS73101: (from page 11 of TPS79501 datasheet)

$$V_{in}=5V, V_{out}=1.8, I_{out}=30mA$$

$$P_D = (5 - 1.8) * (30) = 96mW$$

For Ambient temperature of 85C, TPS73101 can dissipate 155mW. (page 2 of TPS73101 datasheet power dissipation ratings for Low-K JEDEC board).

<http://focus.ti.com/lit/ds/symlink/tps73101.pdf>

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