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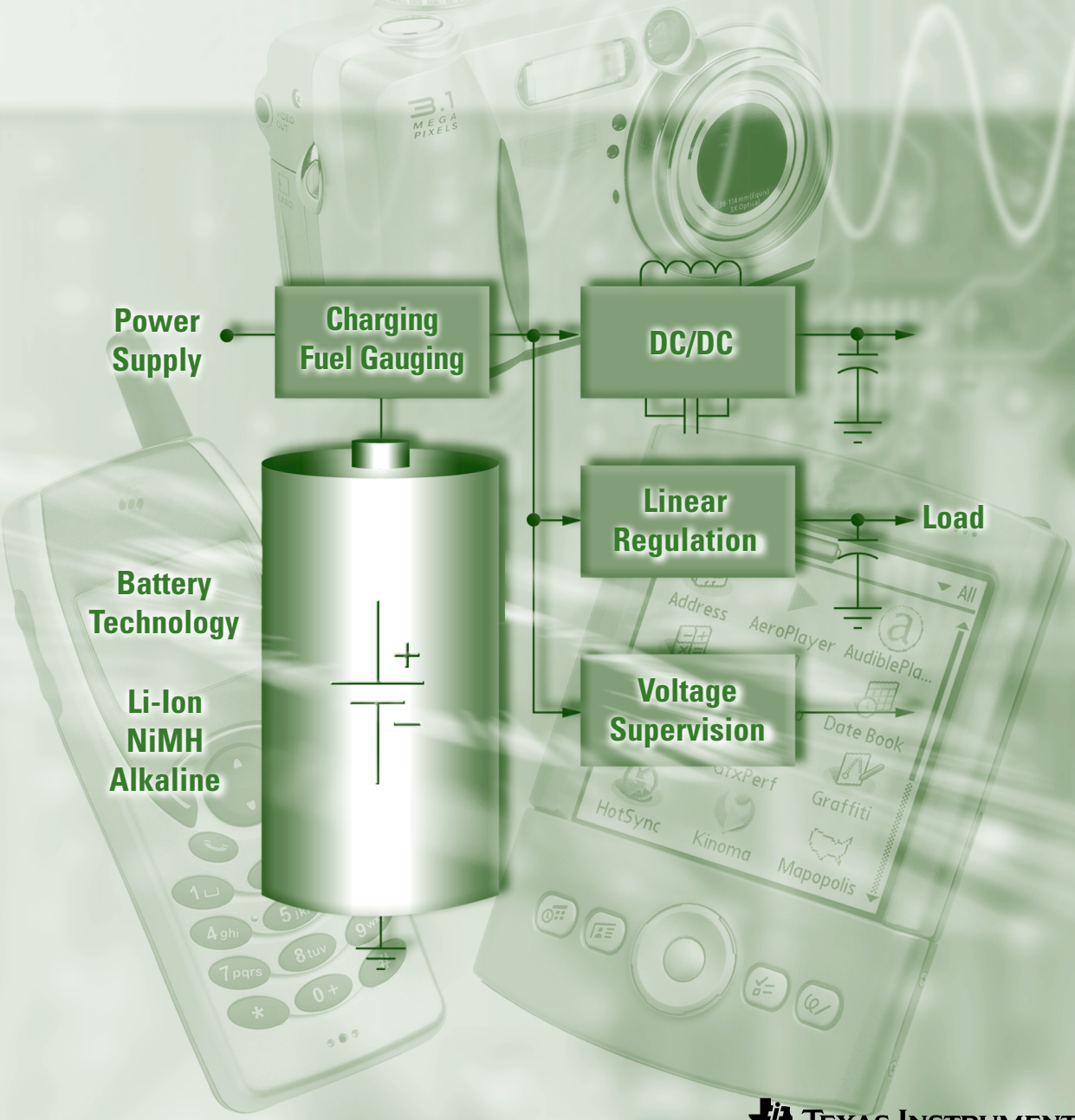

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Challenges and Solutions in Battery Fuel Gauging

Yevgen Barsukov

Abstract

In recent years, the purpose of battery gas gauging has changed from providing warnings of low state of charge (SOC) to servicing applications with information needed to make critical decisions. These increasing demands have been met with improvements in measurement precision and incremental correction of existing run-time calculation methods. However, the need to provide some applications with run-time information with an error below 1% for all operational conditions calls for a radical new solution based on deep understanding of the physics governing battery response to load and its dependence on parameters such as battery age, temperature, load profile, and others.

In addition, rapidly changing battery models and designs of battery-interfacing electronics favor solutions that require minimal testing, calibration, and collection of device-specific data. This topic gives an overview of the advantages and disadvantages of existing fuel-gauging solutions and details radical new methods that increase portability and simplify implementation.

I. Introduction

In recent years a clear change has become evident in the requirements of battery-capacity (C) indicators. The purpose of the first gas gauges was to give the end user some qualitative idea about battery state of charge (SOC) that would warn of impending power loss. Usually four to five levels were used to indicate the relative remaining capacity. Since operation-critical decisions based on these remaining-capacity estimates were very limited, sensitivity to their imprecision was low. However, with increasing use of battery-capacity gauges, systems within digital mobile devices such as notebook computers, PDAs, and hand phones have begun to make actual operation decisions based on battery-capacity data. For example, notebooks give warnings at predefined levels of remaining capacity and even force a sleep mode. Today, capacity-estimation error is not only misleading but typically results in reduced usable run time because the estimate must provide enough margin to compensate for possible errors. This can make the accuracy of the gas gauge as important as the capacity of the battery.

Methods of achieving higher levels of accuracy are not obvious. Superficially, accurate gas gauging might sound like a hardware requirement – the precision of voltage and current measurements and the resolution of the ADCs used. In this sense, modern battery-monitoring ICs have achieved remarkable improvements. Tiny battery monitors have achieved accuracies much better than 1% for voltage and current measurements. These measurements rival many research-grade battery testers. However, it turns out that complications like battery-operated devices with highly variable loads, or peculiarities of battery voltage response, require sophisticated analysis of collected data so that accurate predictions of usable capacity can be made. That means that significant on-board processing capability and new generations of firmware are needed to satisfy market needs for a reliable battery monitor. This paper gives an overview of existing battery gas-gauging methods and discusses the principles of the new generation of self-adapting methods.

II. Existing Battery-Capacity Monitoring Methods

Currently two general methods are used to monitor battery capacity. One is based on current integration and the second is based on voltage

measurements. In most cases these methods are combined in a simplistic manner.

The first method relies on the robust idea that if we integrate all battery charge and discharge currents, we will always know how much coulometric capacity remains. Integrating the current works particularly well when the initial battery capacity is known and the coulometric efficiency is 100%. In other words, during charging, all the coulombs that go into the battery stay in the battery and all decreases in battery capacity are due to an external discharge current.

This seemingly bulletproof approach is modified by predicting self-discharge and battery-charging efficiencies. After these modifications, the current integration method is successfully used in the most recently employed battery gas gauges. However, these modifications to the charge integration methods are principally estimates that may produce errors in particular usage patterns, such as those with long periods of inactivity or highly variable discharge current.

If the battery is charged and left unused for several days, or is just never fully charged for several charge and discharge cycles, the self-discharge due to internal chemical reactions becomes noticeable. Since there is no way the self-discharge current can be measured, it has to be corrected with a predefined equation. And, because different battery models have different self-discharge rates (which also depend on SOC, temperature, and cycling history of the battery), the exact modeling of the self-discharge requires time-consuming effort in data collection and still remains quite imprecise.

Although not restricted to coulomb counting, another problem is that the value of total capacity is updated only if a nearly full discharge occurs soon after full charge. If full discharge events are comparatively rare, considerable decreases of actual available capacity can commence before their values are updated by the gas gauge. This will result in overestimation of available capacity during these periods.

The second method of monitoring battery capacity is based on the known correlation between battery voltage and remaining capacity. This method was one of the earliest to be applied because it used only voltage measurement across battery terminals. It seems to be straightforward, but the catch is that the battery voltage correlates in a simple way with capacity only if no, or a very light, load is applied during measurement. When a load is applied (as it is in most cases when the user is interested in the capacity), battery voltage is distorted by the voltage drop due to internal impedance (R) of the battery. Moreover, even when the load is removed, relaxation processes inside the battery continue to change the voltage for hours. Correction of the voltage drop based on the knowledge of battery impedance is problematic for multiple reasons, which will be discussed further.

III. Battery Chemistry and Voltage Response

The reason for transient voltage response of batteries is in their complex electrochemistry. Fig. 1a depicts basic steps of charge transfer from the electrode of a Li-ion battery (other batteries

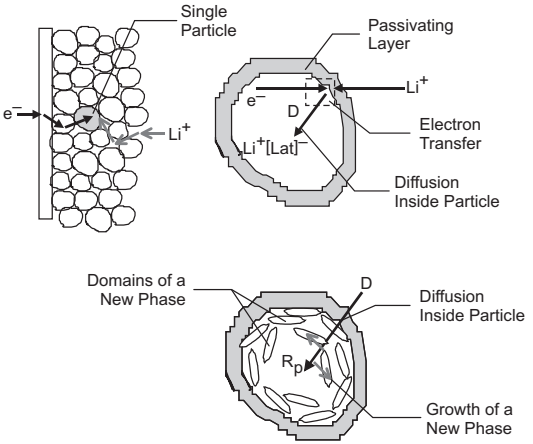


Fig. 1a. Simple steps of Li-ion battery-discharge kinetics.

have similar steps). The charge has to travel through multiple layers of electrochemically active material, storing the energy (anode or cathode) first in the form of electrons until the surface of the particle is reached, and then in the form of ions in the electrolyte. These chemical steps can be associated with time constants in battery voltage response. This is shown in Fig. 1b with the impedance spectrum of the battery. (These time constants range from milliseconds to hours.)

After a load is applied, the voltage will gradually decrease with time at a varying rate and gradually exhibit a recovery after the load is removed. Fig. 2 shows such voltage relaxation after a load is applied to a Li-ion battery at different states of charge.

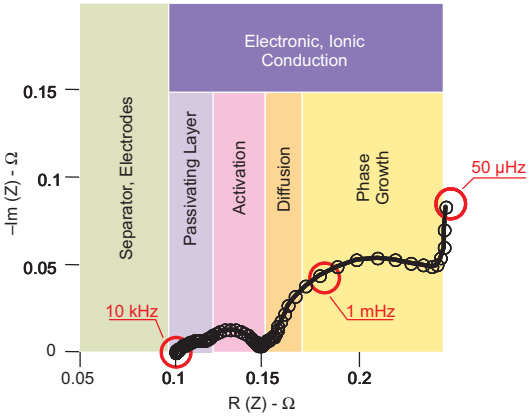
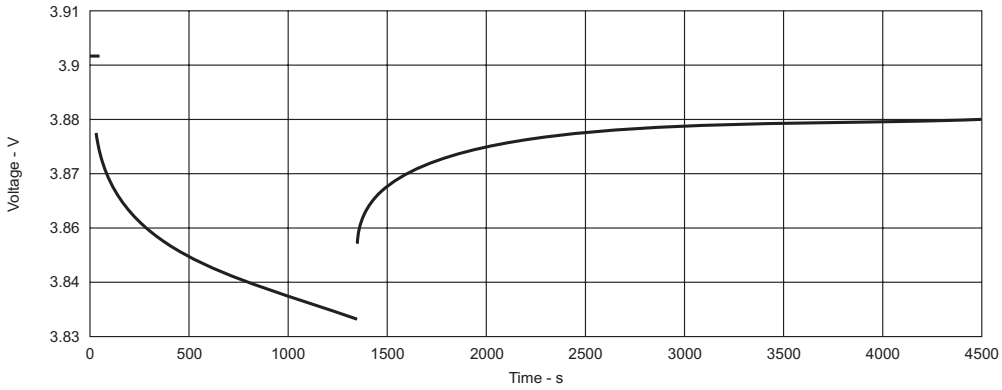
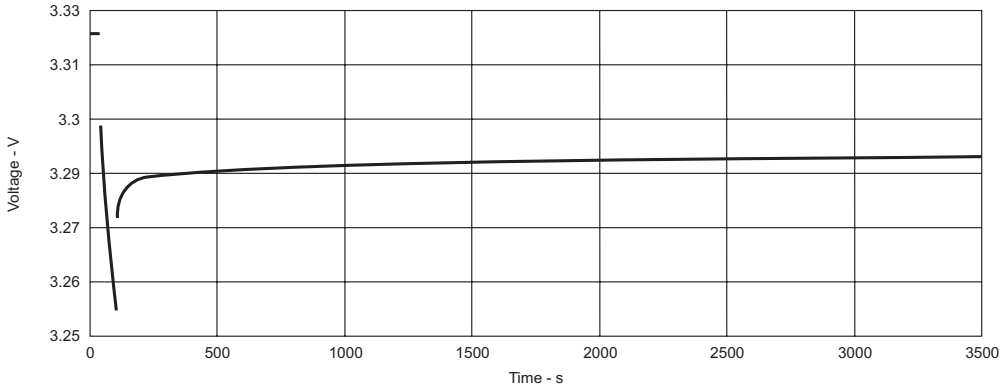


Fig. 1b. Impedance spectra of Li-ion battery with designated areas corresponding to each kinetic step.



a. Battery in fully charged state.



b. Battery in discharged state.

Fig. 2. Voltage drop and relaxation after a C/3-rate load is applied to a Li-ion battery.

IV. Contributions to Error of Voltage-Based Gas Gauging

Let's assume that we are going to correct voltage under load by subtracting IR drop from it and then using a corrected voltage to obtain the current SOC. The first problem we will encounter is that R depends on SOC. If we use an average value, it will introduce an error in SOC estimation of up to 7% for C/2-rate, as can be seen in Fig. 3. A solution for this would be to use a multi-dimensional table of voltages at different loads depending on the SOC. The resistance also strongly depends on temperature, increasing about 1.5 times with every 10ºC of temperature decrease, as can be seen in Fig. 4. If this dependence is also added to the table, then the table becomes larger and more computationally expensive. Gathering the data for an accurate table such as this is also demanding.

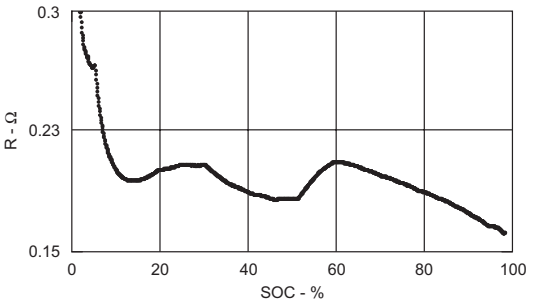


Fig. 3a. DC internal resistance vs. SOC.

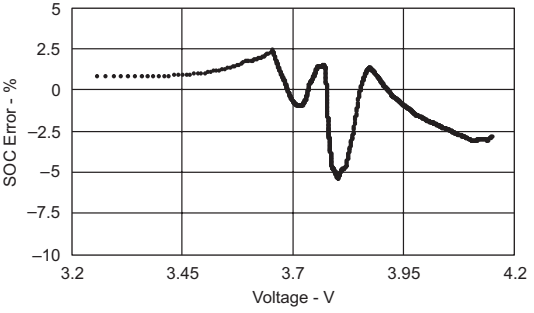


Fig. 3b. Error in SOC estimation performed for C/2-rate discharge when IR drop is corrected, assuming constant internal resistance (using average value).

Considering the transient behavior of battery voltage response, the effective R will depend on the duration of the load application. This means that treating internal impedance as simple ohmic resistance without considering time will lead to

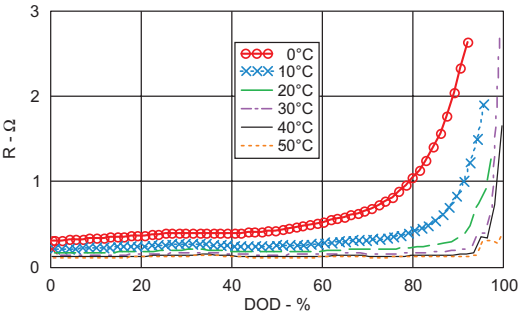


Fig. 4. DC internal resistance vs. depth of discharge (DOD) for temperatures from 0 to 50ºC (DOD = 1 – SOC).

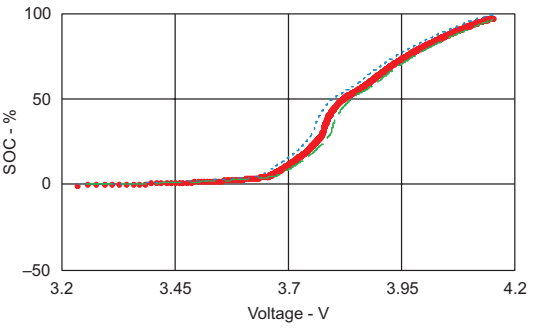


Fig. 5a. SOC vs. voltage with indicated confidence interval resulting from transient error.

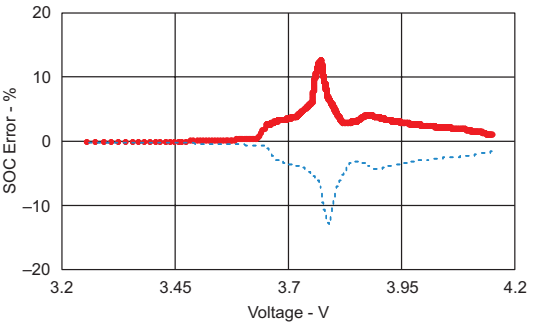


Fig. 5b. Error in SOC estimation depending on voltage where estimation was performed.

significant errors, even if we consider the dependence of R on SOC taken from a table. Because the slope of the SOC voltage function depends on SOC, transient error will range from 0.5% at the end of the discharge state to 14% in the middle-charged state (Fig. 5).

An additional complication is the impedance variation between different cells. Even unused cells are known to have low-frequency (DC) impedance variations of ±15%. That makes a significant difference in voltage correction at high loads. For example, a common discharge C/2-rate and a typical DC impedance (for 2-Ah cells) of about 0.15 Ω results in a worst case of 45-mV differences between cells. This may result in an SOC estimation error of 20%. Fig. 6, which shows impedance spectra of 50 new cells from two different manufacturers, indicates the usual impedance variations between cells. Note that high-frequency impedance (on the right side of the Nyquist plot) is very similar for all cells; however, low-frequency impedance, which actually defines DC performance, shows substantial variation.

Finally, the single biggest impedance-related problem comes when a cell ages. It is known that an increase of impedance is much more significant than a decrease in cell charge capacity. A typical Li-ion battery doubles its DC impedance in 70 cycles, while its no-load capacity decreases in the same period by only 2 to 3%, as can be seen in Fig. 7. If this effect is not considered, a voltage-based algorithm, which seems to work for new battery packs, will fail miserably (with a 50% error) when the pack reaches only 15% of its life estimation of 500 cycles.

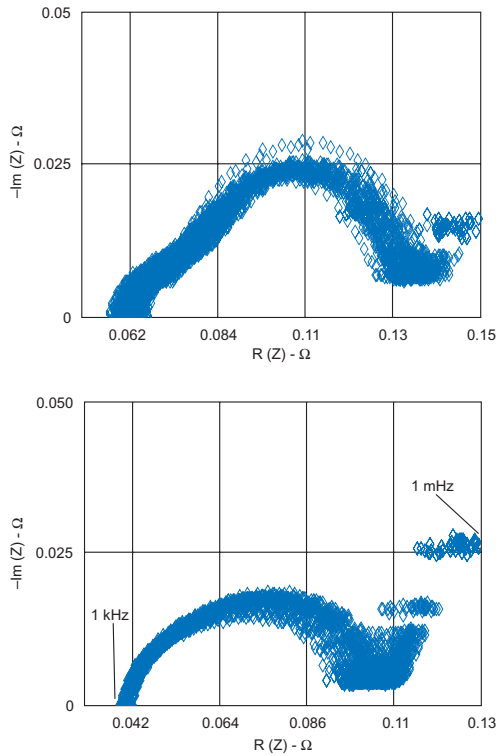


Fig. 6. Impedance spectra measured at 3.750 V from 1 kHz to 1 mHz for 50 new cells from one batch for two manufacturers.

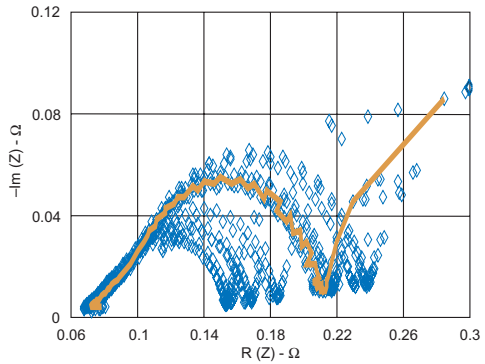


Fig. 7a. Impedance spectra measured in fully charged state from 1 kHz to 1 mHz after each 10th cycle during 100-cycle charge/discharge test of Li-ion battery. Continuous line corresponds to 70th cycle.

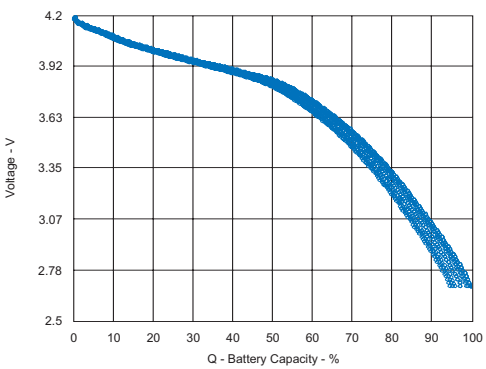


Fig. 7b. Voltage profiles measured at C/10-rate at each 10th cycle during 100 cycles.

V. Using the Best of Both Worlds

In order to improve the prediction of remaining battery capacity, a combination of voltage measurement and current integration can be used. Although many of today's methods use this combination near the end of discharge, the application of these two methods at higher SOCs provides important benefits, especially for those batteries whose capacities vary greatly with discharge rate and temperature.

Due to very precise correlations between open-circuit voltage (OCV) and SOC, the voltage method allows for a precise SOC estimation when no load is applied and the battery is in a relaxed state. Periods of inactivity (which are present in any battery-powered device) can be exploited to get an exact "starting position" for SOC, as indicated in Fig. 8.

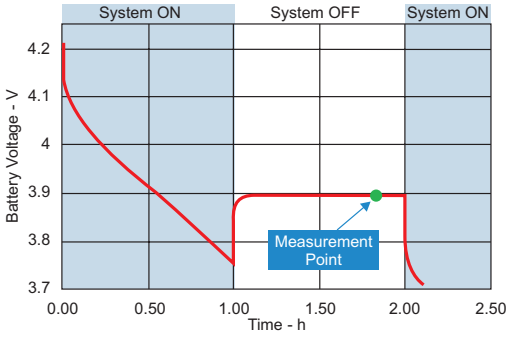
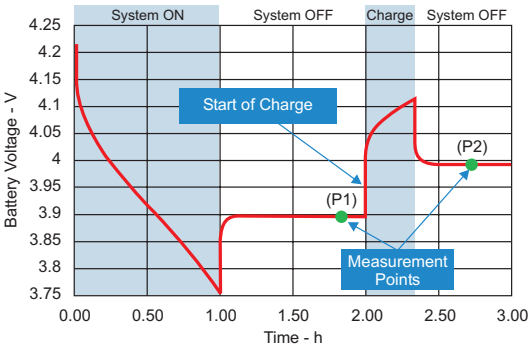


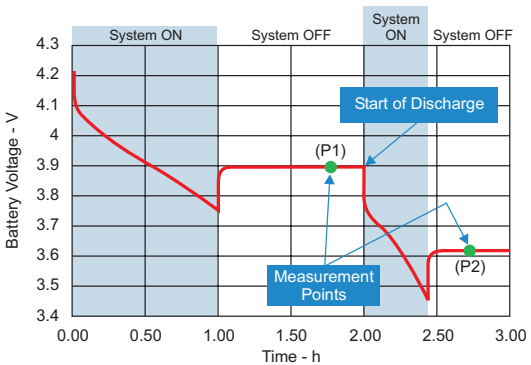
Fig. 8. Determining the starting SOC for the next active period using OCV measurement. Measurement is taken during inactive period as shown.

In this manner, the need for self-discharge estimation for periods of inactivity is eliminated, as are the inaccuracies from measuring very light loads (such as those of battery-pack electronic devices and system leakage paths). Before the device is switched on, a precise SOC can be determined. This requires that periodic measurements of voltage be made while the device is off. These voltage measurements are used to determine the most recent SOC. When the device is switched to the active state and a load is applied to the battery, current integration takes over. This method can reduce the idle current of the device by making only periodic measurements and otherwise allowing it to stay in a lower-power state.

Can this also be used to update full-charge capacity? Yes. When we know the SOC before and after applying the load, and we have precise measurements of the capacity removed, we can easily determine total capacity by knowing the amount of capacity removed and the corresponding change in SOC (see Fig. 9). This method can be used whenever the determination of the SOC and measured capacity removed is known to be accurate. Small changes in SOC or capacity may lead to errors, but limits can be used to disqualify them. While the question regarding SOC is solved by this approach, the effect of cell impedance is still an important parameter for other purposes.



a. After charging.



b. After discharging.

Fig. 9. Estimating total battery capacity by determining the starting SOC for the next active period and the final SOC after (a) charging or (b) discharging a known amount of charge through the battery using OCV measurement. Measurements are taken during inactive period as shown.

The total capacity we determine by this method corresponds to "no-load" conditions; e.g., the maximum possible capacity that can be extracted. Under a non-zero load, capacity will be less due to IR_e drop, which causes the termination voltage to be reached earlier. If the cell impedance dependencies on SOC and temperature are known, it is possible to employ simple modeling to determine when termination voltage will be reached at the load and temperature currently observed. However, as mentioned before, impedance is cell-dependent and increases rapidly with cell aging and cycling, so it would not be useful just to store it in a database.

To solve this problem, one approach is real-time impedance measurements, which can keep a database continuously updated. To avoid distortion of impedance measurement by those transient effects mentioned earlier, a level-detection algorithm can continuously monitor load change and disqualify measurements that happened during, or shortly after, load change. An example of such level detection is given in Fig. 10.

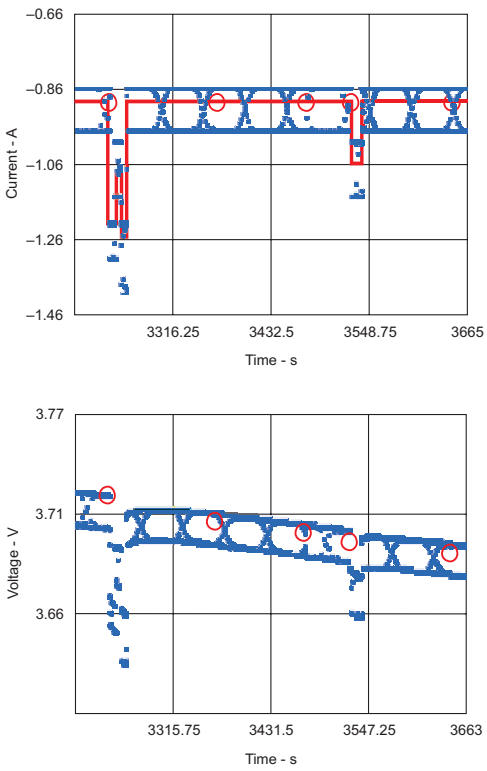


Fig. 10. Current level detection in variable load during notebook operation. Circles indicate qualified impedance measurement points.

Such real-time impedance updates greatly reduce the problem with impedance variations between cells and cell aging. As can be seen in Fig. 11, live updates of impedance data enable remarkable precision of voltage-profile prediction at a given load.

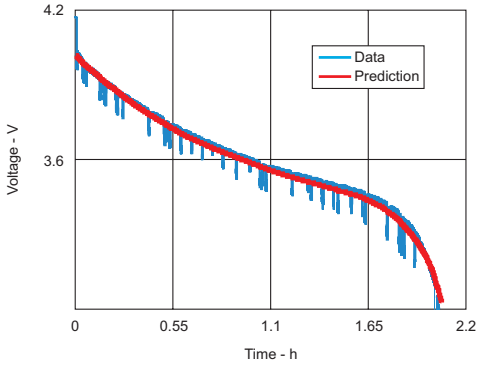


Fig. 11. Voltage profile predicted by fuel-gauging algorithm on the basis of real-time cell-impedance updates vs. profile subsequently measured using typical notebook-load experimental data.

In most cases, an error below 1% in estimating usable capacity can be achieved; and, most importantly, high accuracy is sustained throughout the entire life of the battery pack.

VI. Plug-and-Play Implementation as Free Bonus of Self-Adapting Algorithm

Implementation of the algorithm just discussed removes the need for a preloaded database describing impedance dependencies on SOC and temperature because this data will be obtained by real-time measurements. An initial, simple database can be used while real-time data is collected for the actual battery pack. The need to correct for self-discharge is also eliminated. What is still needed is a database defining the correlation between OCV and SOC (including temperature). The character of this correlation is defined by chemical properties of the anode/cathode system and not by battery model design specifics such as

electrolyte, separator, thickness of active material, additives, etc. Because most cells are manufactured with the same chemistry for active materials ($LiCoO_2$ and graphite), the dependence of voltage on SOC and temperature is common among them. Experiments support this assertion.

Fig. 12 shows a comparison of no-load voltage profiles for cells made by different manufacturers. It can be seen that they are very close, with the largest deviations amounting to only 5 mV, resulting in a worst-case SOC error of 1.5%. If a new chemistry is developed, just one new database will be needed as opposed to the hundreds of different databases currently used for different battery models. This simplifies the implementation of gas-gauge solutions in a variety of end equipment. No reprogramming or data collection is necessary if cells with similar chemistry are used, even if the manufacturer is changed. This will practically enable plug-and-play implementation of battery-monitoring circuits without compromising on acceptable accuracy.

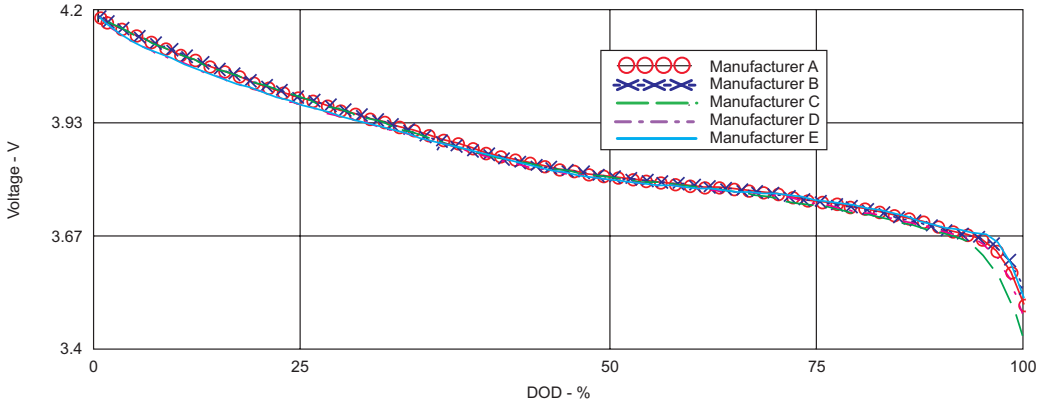


Fig. 12a. Voltage dependence on DOD for Li-ion batteries of five different manufacturers (DOD = 1 – SOC).

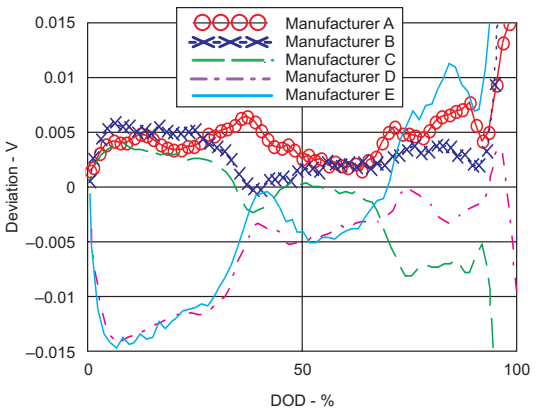


Fig. 12b. Voltage deviation from average.

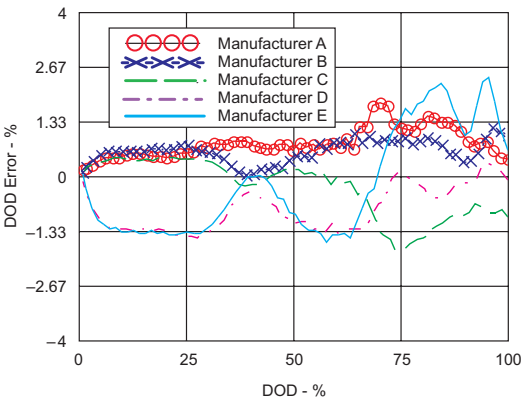


Fig. 12c. DOD error calculated if averaged database is used.

VII. Conclusion

An analysis of battery response to load makes it evident that voltage-based methods of fuel gauging cannot achieve today's required accuracy of SOC estimation. Further, correction for internal impedance of the battery suffers from transient effects and variability of impedance with aging and from cell to cell. Radical new solutions to this problem use voltage-based methods where no correction is needed. OCV dependence on SOC is defined only by battery chemistry and not by cell design, a bonus that allows a generic database to be used for a variety of different models.

Current integration during periods of activity allows precise estimation of the change in SOC from the last voltage-based estimation. Impedance information is still needed for calculating the usable capacity under a particular load and can be acquired by real-time measurement. Apart from always providing up-to-date and cell-specific impedance information, such an approach removes the need for a preloaded impedance database. This makes implementation of a fuel-gauge IC that applies a combined voltage/current-based algorithm much simpler, as no cell-specific data needs to be collected. An additional benefit is that the same fuel-gauging solution can be used with cells made by different manufacturers without reprogramming the IC and retesting the solution.

Battery Circuit Architecture

Bill Jackson

ABSTRACT

Battery-pack requirements have gone through a major evolution in the past several years, and today's designs have considerable electronic content. The requirements for these batteries include high discharge rates, low insertion loss from components in series with the cells, high-precision measurements, redundant safety protection, and no upset with very high electrostatic discharge (ESD) transients. Virtually all Li-ion protector circuits for one- and two-cell applications have protector FETs in the low (negative) side of the battery. Key issues particular to a low-side Li-ion protector circuit are discussed. The transients produced when the Li-ion protector opens during a momentary short or when the battery is unplugged while under load may exceed the voltage rating of semiconductors in the battery pack. This topic describes a number of design issues and proposes solutions to resolve or improve them. Resolution of these issues requires attention to both the circuit design and the printed circuit board (PCB) layout.

I. Typical Battery Circuitry for a Li-ion Battery Pack

Fig. 1 is a block diagram of circuitry in a typical Li-ion battery pack. It shows an example of a safety protection circuit for the Li-ion cells and a gas gauge (capacity measuring device). The safety circuitry includes a Li-ion protector that controls back-to-back FET switches. These switches can be opened to protect the pack against fault conditions such as overvoltage, undervoltage, and overcurrent. The diagram also includes a temperature-sensitive three-terminal fuse that will open due to prolonged overcurrent or overtemperature, or it can be forced to open by redundant protection circuitry in case there is a fault where the primary protection circuitry fails to respond. Opening this

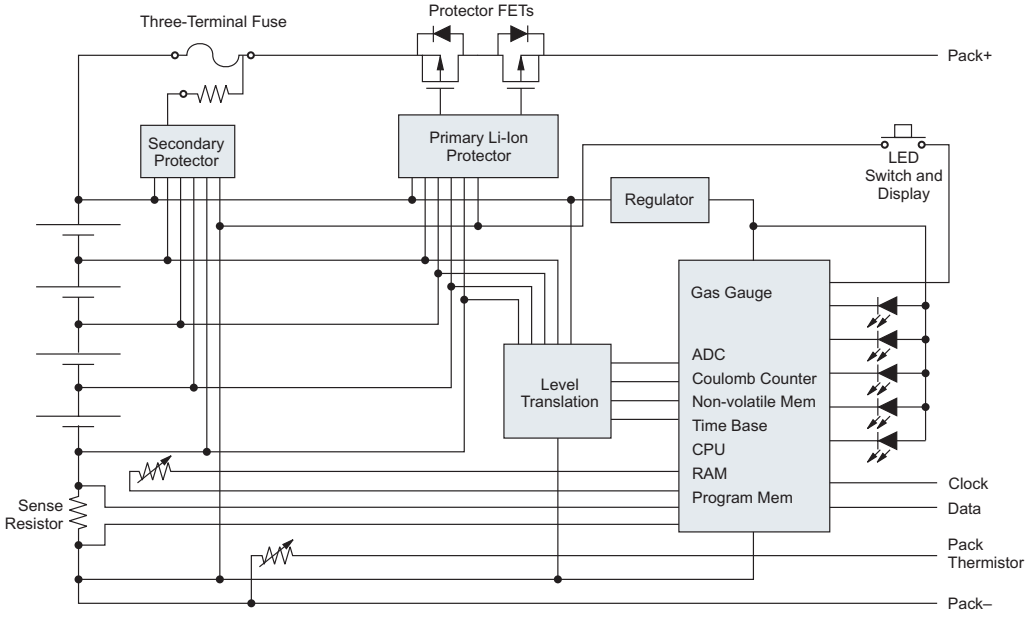


Fig. 1. Block diagram of circuitry in a typical Li-ion battery pack.

fuse is a last resort, as it will render the pack permanently disabled. The gas-gauge circuitry measures the charge and discharge current by measuring the voltage across a low-value sense resistor with low-offset measurement circuitry. The current measurement is integrated to determine the change in coulometric capacity. In addition, the gauge measures temperature and voltage, evaluates gas-gauging algorithms to determine the available capacity in the battery, and computes time-to-empty and other values required by the host. The available capacity as well as other measurements and computational results are communicated to the host over a serial communication line. A visual indication of available capacity can be displayed by the LEDs when activated by a push-button switch.

II. Optimizing the Design for Measurement Accuracy

Measurement accuracy requires an accurate measurement data acquisition system and measurement sensor and also requires a careful board layout. If the designer does not pay attention to all these items, the resulting system performance may not deliver the expected results.

The sense resistor and how it is connected to the data acquisition system are critical design decisions. The sense resistor may see changes in temperature that are much larger than the ambient variations of the battery pack due to power dissipation in the resistor. Use of a low-temperature coefficient resistor will improve available capacity and current-measurement accuracy. The effective sense resistance seen by the measurement circuitry may depend on how the printed circuit board (PCB) etch is connected to the sense resistor. If the sense resistor is connected in such a manner as to include some of the PCB etch resistance in the actual sense resistance seen by the measurement circuitry, the effective resistance is increased. In addition to having a larger resistance than intended, the portion of the effective sense resistance that is due to copper etch will have a very high temperature coefficient (0.39%/ºC). The best practice is to connect the sense resistor into the circuitry at the location that includes the least amount of copper trace in the current path. If this method is followed, there will be very little error due to the voltage drop across the connection, and the connection resistance will not add to the effective sense resistor value.

If single-ended measurements are made on the voltage across the sense resistor, it is critical that the V_{SS} of the measuring device be connected to the sense resistor with much care. In the single-ended system, the measurement system ground provides one of the inputs for the measurement. The value that is measured is the difference between the single-ended input and the measuring system ground. If the measuring system ground path has a voltage difference between the on-chip ground and the ground end of the voltage measurement desired, this difference will create an error. The measurement system ground should tie to a low-current ground etch. The low-current ground should be separated from the high-current ground, and the ground end of the sense resistor should be the tie point where the low-current ground is tied to the high-current ground. This will also provide a more robust design for electrostatic discharge (ESD), as discussed later.

Voltage measurements of the battery stack are also affected by PCB layout and connection drops. Some battery-pack designs may use nickel straps from the PCB connection to the battery stack. Nickel is used because it is easy to weld to the battery cells, but its resistance is five times as much as that of copper. When current flows through these straps, the voltage measured by the circuitry on the PCB connected to these straps will not measure the true cell voltage. To measure the true cell voltage, separate voltage measurement connections should be made with wiring that does not carry the load current. This drop may not be significant, but if the circuitry measures each cell voltage, such drops will cause the top and/or bottom cells to measure lower or higher (with discharge or charge currents) than the other cells. The same issue exists for copper etch routing on the PCB. A high-current-carrying conductor on the PCB will have a voltage drop across it. In general, the voltage measurement connections need to be made so that these connections have very little current flowing through them between the desired measurement point and the input to the

measurement IC. If the gas-gauge algorithm uses the lowest cell voltage for determining when the battery is empty, a small voltage drop may represent a significant capacity error and cause the gauge to report a smaller available capacity from the battery. If single-ended measurements are made of the voltage across the sense resistor and also of the voltage, accuracy considerations dictate that the sense resistor ground connection should be very close to the cell stack ground connection.

III. Thermal Issues

There can be a lot of power dissipation in the battery pack. There will be some temperature rise due to power dissipation in the cells. High currents can also produce appreciable heat from the protector FETs, sense resistor, and even etch and wiring resistance. Make sure that intended temperature measurements are not elevated due to proximity of the thermal sensor to various heat sources. For example, if the substrate temperature of an integrated circuit (IC) mounted to the PCB is being measured, a narrow etch that runs under the IC may raise the reported temperature by at least 6º with as little as 2 A flowing through the etch. This is disastrous if the design is a NiMH or NiCd pack and the temperature measurement is used to determine full charge by a dT/dt charge termination. An increase of charge current can cause a false detection of a fully charged condition due to an increased dT/dt value. Excessive temperatures may also degrade the measurement accuracy of the gas gauge by causing drift in the on-chip reference. A good design practice is to avoid placing any measurement component close to the heat sources – for example, the protector FETs and sense resistor.

IV. Transient Protection

Most designers will recognize the need to add transient protection across the pack output terminals if the battery is used to drive a motor or highly inductive load. However, many designs with non-inductive loads do not have any transient-limiting devices and depend only on some small capacitors to attenuate the transients. Li-ion cells have a relatively high inductance for their size due to construction techniques. If a battery pack is removed from the system while under load, there is an opportunity for a damaging transient to occur. The battery pack should have sufficient capacitance to reduce transients or have something to clamp them. An even greater danger exists if there is a momentary short across the battery pack. The Li-ion safety protector may open to protect the cells from this short. If the FET switch in the protector opens quickly, the $L \times dI/dt$ transient may be very large. Capacitance or transient-limiting devices on the output of the pack will not see this transient. The transient will appear on the cell side of the protector. There is a potential to damage any components tied to the cell side of the protector if there is not sufficient capacitance or other means to attenuate the transient across the cell stack.

V. Low-side Protector Issues

Virtually all one- and two-cell Li-ion protectors are low-side protectors, where the protector FETs are located between the negative lead of the battery cell stack and the battery negative terminal. There are several issues that can result depending on where the designer chooses to insert the protector FETs with respect to the battery-pack electronics.

The Li-ion protectors typically use p-channel FETs for high-side protectors and n-channel FETs for low-side protectors. The available voltage to turn on the FETs is lower for a one- and two-cell protector, and a low-threshold n-channel FET is cheaper and has better performance than a low-threshold p-channel FET.

Circuitry in a battery pack, such as a gas gauge, needs to measure the battery-cell stack voltage at all times. This drives the decision to place the Li-ion protector FETs between the ground connection of the battery electronics and the negative pack terminal. This decision creates two design issues that can exist when the Li-ion protector FETs are open. Any communication between the host and the battery electronics may be disrupted when the protector FET opens. The more serious issue involves safety. There is a sneak path for continued charging of the Li-ion cell stack. If the protection FETs are opened due to an overvoltage condition, this path allows the

cells to continue charging – the very condition that the protector is attempting to prevent.

Virtually all ICs will have an internal substrate diode from communication lines to the V_{SS} ground connection. This diode is part of the ESD protection structure in the device. A typical device will be protected to 1.5 to 2 kV by this internal structure. Typical end-equipment specifications will have an ESD requirement of 15 kV, requiring additional ESD protection components. The internal substrate diode and the external ESD protection components may both provide a return path for sneak charging currents from a charger that fails in a high-voltage fault condition. Fig. 2 shows the path where the charge current may flow. If the charger voltage exceeds the high-voltage trip threshold of the protector by more than one diode drop, the IC substrate diode will be forward-biased, and charge current can flow whenever the host drives the communication line to a logic zero. Resistance in the communication line will limit the peak current flow, and the duty cycle of a logic low on the communication line will affect the average current flow.

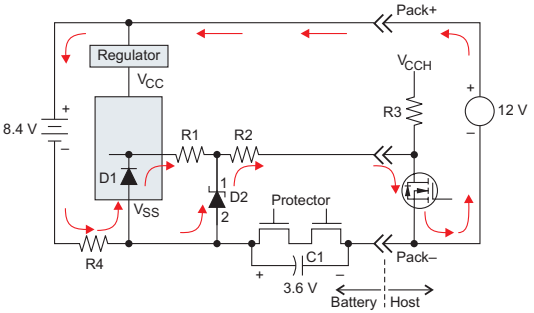


Fig. 2. Sneak charge-current path from a high-voltage charger failure.

There are basically three ways to prevent the sneak charging from a high-voltage charger when low-side protectors are used. The most popular way is to add a blocking diode in the communication line. A second way is to detect a high-voltage condition and gate the communication driver so that it cannot pull low when the high-voltage condition exists. The third way is to add a high-side FET in series with the charger and to turn it off if a high-voltage condition exists. These methods are shown in Fig. 3. To implement the first method, a diode is placed in the communication line with a parallel capacitor and high-value pull-down resistance on the battery side of the diode. The diode is typically a Schottky diode to reduce the impact on the communication noise margin. The capacitor provides AC coupling of the communication waveform around the diode and also protects the diode from ESD damage. The pull-down resistance provides a DC restoration path for the charge on the added capacitor.

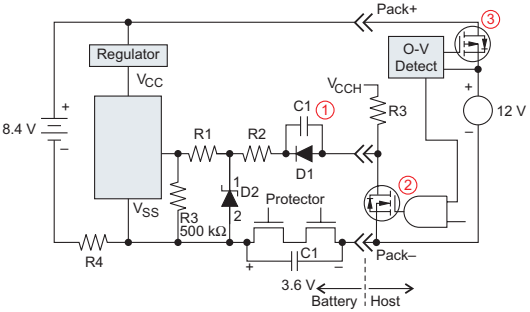


Fig. 3. Preventing the sneak charge-current path from a high-voltage charger failure.

VI. ESD Considerations

Most battery-pack requirements include surviving multiple ESD hits from both direct connection and air-gap spark discharges. The equipment must generally withstand both positive and negative discharges of at least 15 kV to all connector pins as well as to the case of the battery pack. Most requirements go further than just requiring survival, insisting that there be no observable disruption in performance. Since the component ratings are generally much lower than 15 kV (2 kV or less), the electronics must include protection components and design countermeasures to reduce the ESD damage and upset potential.

ESD damage control is generally provided by shunt zener diodes, transient suppressors, and capacitors. Series resistors may be used to limit the peak current flow. It is noteworthy that 15 kV may arc across the body of some small resistors, reducing or eliminating their effectiveness for

limiting current flow and for decoupling. The key to designing circuitry that meets ESD requirements is an understanding of where the peak current from the ESD event will flow, the potential for both capacitive and magnetic coupling onto other signal lines, and the possibility for secondary arcing from the input that received the discharge.

Where the Current Flows – The ESD event will result in a very fast-rising voltage and current pulse on the line that receives the discharge. The discharge will seek the lowest-impedance path to earth ground. In a battery pack, the largest capacitance to earth ground is from the battery cells through the case to a hand or other surface adjacent to the pack. If ESD is applied to the Pack+ or Pack– connector terminals, the current path is obvious. If ESD is applied to a communication or other interface signal, the current will find the lowest-impedance path to the cells.

The Effect of the Discharge – The ESD event may cause a 1-ns rise-time voltage pulse of several thousand volts and/or over 30 A of momentary current flow. The fast-rising voltage spike can capacitively couple onto any etch and components adjacent to the affected line. The fast-rising current flow from the discharge will create a large inductive voltage drop along the path of the current flow. It will also create a magnetic field from the current flow that can induce transients into other circuitry through the nearby components and etch runs.

VII. ESD Design Hardening

Start the hardening process at the connector. One popular technique for improving ESD susceptibility is to build a spark-gap structure in the outside etch layer behind the battery-pack connector. This is a low-inductance (wide) ground etch that runs close to the etch-pad connections for the other connector pins. The etch structure provides a small clearance between points, or corners, in the etch to encourage a breakdown from a high voltage across the clearance. The clearance must be kept free from solder mask, as the solder mask would increase the voltage breakdown of the gap enormously. A 10-mil gap has a voltage breakdown at sea level of about 1500 V. This breakdown voltage is typically less than the damage threshold of IC inputs. The spark gap will tend to clamp the peak voltage on the connector pins other than ground and divert much of the charge to the ground etch. If the ground etch is handled carefully, this approach can significantly improve the ESD susceptibility of a design. Fig. 4 shows a typical ESD spark-gap structure in the etch pattern around the pack connector.

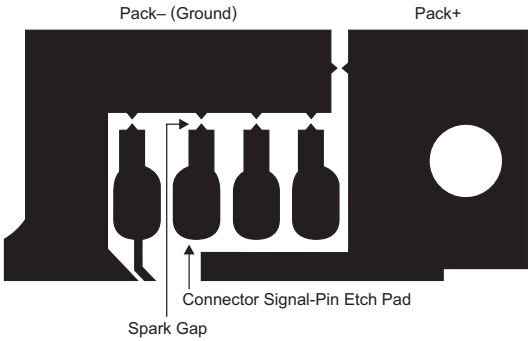


Fig. 4. Typical ESD spark-gap structure at pack connector.

Keep the etch connecting to the top and bottom of the cell stack away from all sensitive components. If the connections to the cell stack run the full length of the PCB, upset from an ESD event is much more likely due to the capacitive and magnetic coupling to nearby components and etch runs. If the Pack+ and Pack– connections can route through the protector FETs and sense resistor and then immediately leave the PCB and connect to the cell stack, a large portion of the PCB may be relatively free from coupling from an ESD event. Fig. 5 shows a sketch of component placement and etch routing that may yield a design with very high ESD susceptibility limits.

The recommended design practice is to separate the high-current ground etch from the low-current ground etch. Even a small inductance on the high-current ground etch will develop a large potential across the length of the connection due to the extremely fast dI/dt from the ESD event. If sensitive circuitry has connections to ground at different points along the high-current ground path, there may be a large differential voltage between these connections during an ESD

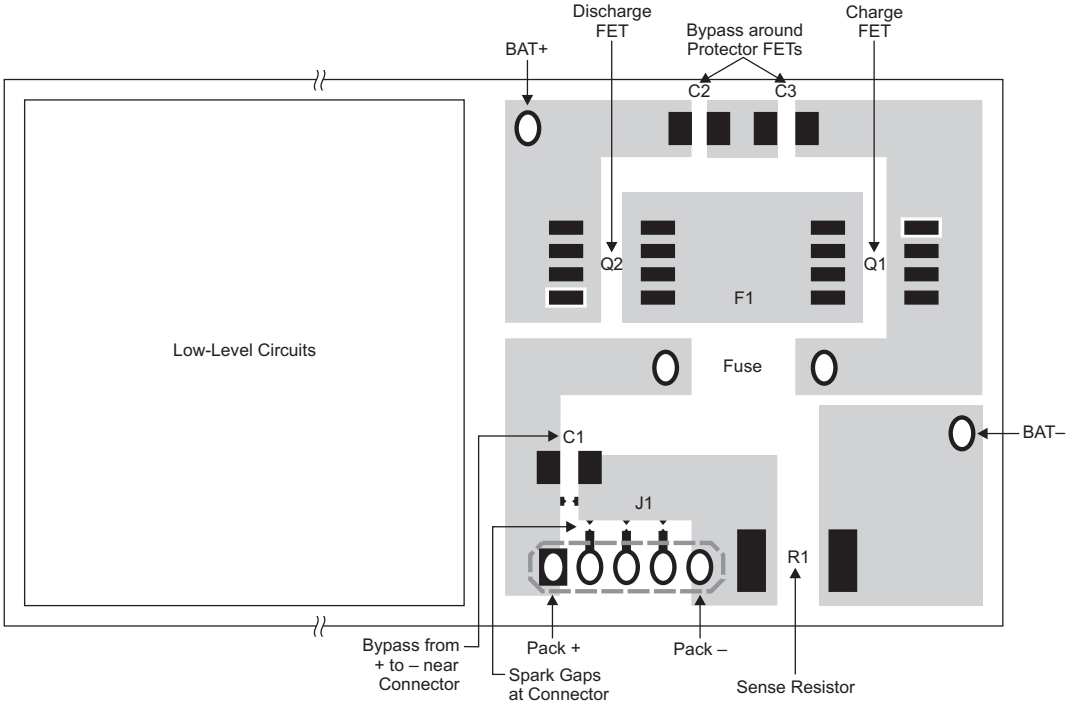


Fig. 5. Component placement and routing to achieve good ESD performance.

event. This differential voltage may allow some inputs to be momentarily pulled lower than V_{SS}, and the resulting substrate current flow can cause upset of the circuit performance. The best way to handle this issue is to connect all the low-current grounds together and then tie the low-current ground to the high-current ground at a single point. Make sure that none of the ESD protection components, such as shunt zener diodes or transient suppressors, tie to the low-current ground but tie to the high-current ground instead. This greatly reduces the possibility for ESD to cause current flow through the low-current ground and to create differential voltages between different ground connections.

Keep bypass capacitor leads short. It is very important to keep from canceling the high-frequency capability of a good ceramic capacitor by adding an inductor in series with it. This is what happens when care is not taken to keep *both* connections to the bypass capacitor short and wide. A long connection on the ground side of the capacitor is just as bad as a long connection to the signal side. Use of a ground plane, where practical, makes this a lot easier. If an electrolytic capacitor is required to obtain the needed bulk capacitance, add an additional ceramic capacitor in parallel to take care of the high-frequency bypass requirement. The frequency components in an ESD pulse are so high that even ceramic capacitors will seem inductive. Some critical circuits may benefit from a small-value (68- to 100-pF) ceramic capacitor in parallel with a larger (0.1-µF) bypass ceramic capacitor because the impedance of the small-value capacitor may be much less at the higher frequency due to much lower series inductance. Long connections to series components may not be a problem and, in fact, may add some inductance that will aid in decoupling. For example, some designs use small inductors in series with V_{CC} connections to aid in decoupling an ESD transient from a sensitive circuit.

Placing a capacitor across the Pack+ and Pack– connector pins very close to the connector and using short and wide etch runs can reduce the ESD susceptibility. This placement will provide

an alternate path for a portion of the current pulse from a Pack+ or Pack– ESD hit and reduce the peak current amplitude through the etch runs to the battery cells. This may provide some improvement in the peak ESD voltage transient level that the pack can withstand.

The Li-ion protector FETs will be in either the positive or negative high-current path from the connector to the battery cells. A capacitor around the protector FETs will provide a current path for ESD as well as help to minimize peak transient amplitudes when the protector FETs are switched off. The shunt capacitor will help limit the voltage transient across the FETs during an ESD event. Most designs have two capacitors in series for redundancy, so that shorting of a single capacitor won't disable the safety protection.

Protecting communication or other interface signals with zener diodes and/or transient suppressors is mandatory. The shunt suppression component should tie to the high-current ground as mentioned previously. It is very important to insure that the impedance of the path intended to shunt the transient to ground be significantly lower than the series impedance to the device input being protected. A long, thin connection to the transient suppressor may severely reduce the effectiveness of the protection components. It is generally helpful to add some series impedance both before and after the shunt zener diode or transient suppressor. Resistance between the pack connector and a shunt zener diode may reduce the peak current through the latter and keep it from failing. The zener diode normally fails as a short and will render the interface signal useless. The series resistance may need to be a larger package style that will withstand a larger voltage without arcing. This resistance may also protect the zener diode from failing due to a momentary short from the interface signal to Pack+. The larger resistor package will also withstand a momentary overload for a longer time. Resistance between a shunt zener diode and the IC input is also effective to reduce the potential for upset. The IC input will generally have an ESD protection structure that has a diode to V_{SS}. If a negative ESD transient is applied to the input, the shunt zener diode and ESD protection diode in the IC will share the current. A little resistance between the zener diode and IC input will force most transient current to flow through the zener diode instead of sharing it with the IC. Current flow through the substrate of the IC is very likely to cause an upset condition in the IC, so removing that possibility is a big help.

Another design approach to enhance performance is to implement a reset strategy that does not always upset the information displayed to the user. If critical data is maintained even with a reset, an upset due to an ESD event may not cause any significant disruption to the user. This strategy may employ redundant copies of critical information or checkbyte values that may be used to determine if the critical data is still useful after a device reset.

VIII. Pack Insertion Issues

Some designs have communication and/or interface signal lines to circuitry in the battery pack. In many cases the ESD protection on these lines does not clamp a positive transient to less than the V_{CC} of the battery electronics. If the circuitry in the battery pack contains a substrate diode from the communication line to V_{CC}, it is possible to disrupt the V_{CC} supply when plugging in the battery pack. This disruption may cause improper operation of the battery-pack electronics. If the host system is not applying a charging potential to the host-side pack connector, the capacitance across the battery connections will be discharged before the battery pack is inserted. Most battery connectors do not have any provision to insure that the Pack– or ground connector pin mates first. If the Pack– pin connects last when the battery pack is plugged in, there is a path to pull up the V_{CC} in the battery electronics temporarily until it almost reaches the Pack+ terminal potential. The electrical path to pull up the battery pack V_{CC} passes through the host capacitance from Pack+ to Pack–, through a substrate diode in the host interface driver from V_{SS} to the communication or interface line, and through a substrate diode from this line to V_{CC} in the battery-pack circuitry. The complete path is shown in Fig. 6. The best design practice is to use circuitry in the battery pack that does not have an internal substrate diode to V_{CC}. This has a side benefit of preventing the battery-pack electronics from

being able to clamp the communication line to a low V_{CC} value resulting from a depleted battery. The ESD protection circuitry on the communication line should also clamp the voltage on the line to less than the maximum allowable voltage. This will limit the peak transient voltage and prevent damage to the battery electronics if the ground pin makes the last connection during pack insertion.

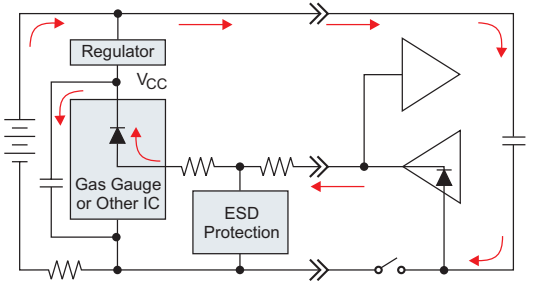


Fig. 6. Pack insertion issue when ground pin makes last connection.

IX. Conclusion

Battery-circuit design and layout are considerably more critical than might be expected. The combination of battery requirements includes: high-amplitude ESD to connector pins and exposed surfaces, coupling from an ESD event to nearby etch and components, heavy load currents, plugging and unplugging with power on the connector pins, multiple circuit ground references including high-current grounds, measurement of very small signals, and thermal management. Meeting these requirements and implementing the design on a circuit board that may be almost too small to hold the required components provides an extremely difficult challenge. The key to a successful design is the recognition of the various issues prior to starting the design and a close control of the PCB layout by the design engineer. A good design is a layered approach; removing any one layer will reduce the effectiveness of the others.

Design Considerations and Advances in Portable Power Battery Chargers

Charles Mauney

ABSTRACT

Battery-charger demands have changed from a simple stand-alone charger to an embedded charger and power source for the system. This topic provides some insight into the many new issues the designer should consider when designing either a linear or a switching regulator. Common transient issues caused by hot plugging/unplugging the adapter or system load during operation are presented. Problems and solutions surrounding use of a stand-alone charger to charge a battery with a system load in parallel are discussed along with the optimal solution for powering system loads.

I. INTRODUCTION

Providing power to a system is often regarded as a last-minute task, delegated to a systems person or an engineer with little power-supply design experience. This paper attempts to help the inexperienced power designer avoid many of the common mistakes made in portable power product design. Section II discusses the pros and cons of linear and switcher power conversion for a given application. A general theory of operation is followed by an explanation of a FET driver circuit, a current mirror circuit, and design considerations for component selection and layout. Section III highlights the potential hazards that may be caused by connecting and disconnecting active charger sources and loads. Typical application scenarios are modeled, simulated, and presented. Section IV explains the issues introduced when a system load is connected in parallel with a battery under charge. Several application "work-around" solutions are presented. Section V explores an alternative solution that avoids many of the pitfalls introduced when the system is connected in parallel with the battery.

II. CHOOSING BETWEEN A LINEAR AND SWITCHER BATTERY CHARGER

There are two basic types of power conversions – a linear regulator and a switching regulator.

A linear regulator is similar to a resistor divider where the regulator drops the input voltage down to a usable "charging" voltage (see Fig. 1a). The

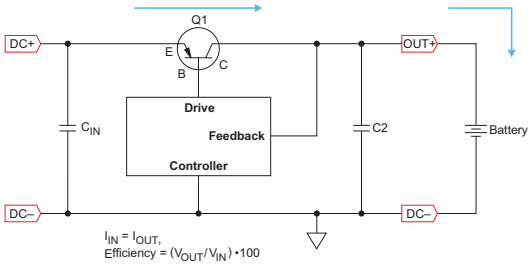


Fig. 1a. Linear regulator.

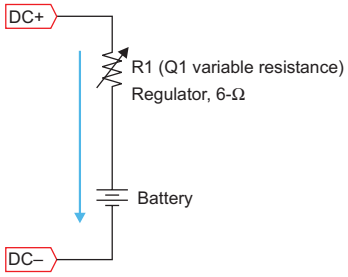


Fig. 1b. Equivalent DC circuit.

current is the same through both resistors (see Fig. 1b, where the top resistor represents the regulator and the bottom resistor represents the load). From the following equation one can see that, if 10 V is applied to a series 6-Ω regulator and a 4-Ω system load resistor, the system voltage will be 4 V and the current will be 1 A.

$I = V_{SYS}/R = 10\ V/(6\ \Omega + 4\ \Omega) = 1\ A$

$V_{SYS} = V_{IN} \cdot R2/(R1 + R2)$
$= 10\ V \cdot 4\ \Omega/(6\ \Omega + 4\ \Omega) = 4\ V$

$P = IV$

$P_{R1} = 1\ A \cdot 6\ V = 6\ W$

$P_{R2} = 1\ A \cdot 4\ V = 4\ W$

R1 (Q1, the linear pass element) will dissipate 6 W and R2 (R_{System} or battery) will use 4 W. One can see that, for a linear charger with a 10-V input and 4-V output, only 40% of the energy will be delivered to the system or battery. The linear design does not require an inductor or diode and is generally less expensive than a switcher for low-power, low-dissipation designs. As power demand

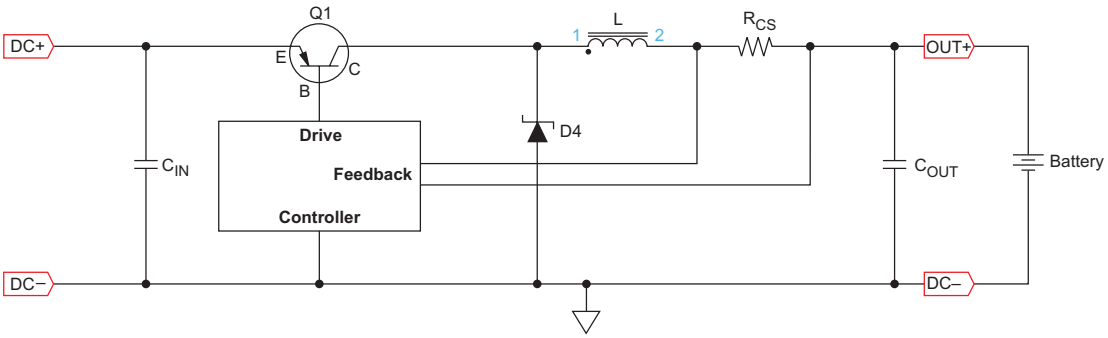


Fig. 2a. Buck power stage.

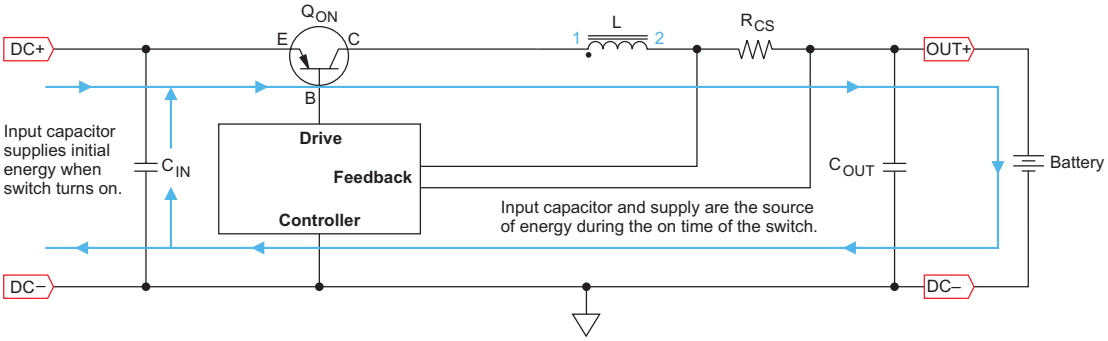


Fig. 2b. Current flow when switch is on.

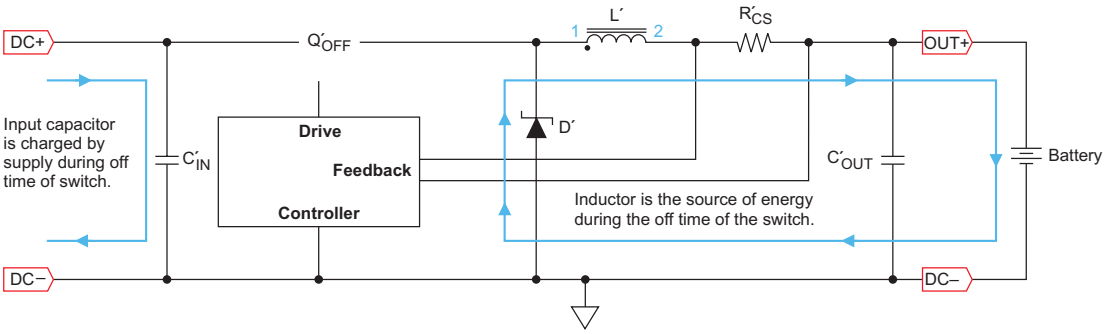


Fig. 2c. Current flow when switch is off.

increases or as linear efficiencies decrease, the cost or the ability to manage excessive power dissipation will make the linear topology a less desirable choice.

Switching regulators can boost or buck the input voltage. The buck switcher design converts (bucks) the input voltage down to a lower desired output voltage. The buck switcher (see Fig. 2a) is connected between the input supply voltage and the output load (battery or system load). Q1, the power switch, is turned on and off at a high frequency (> 50 kHz) by the controller for a controlled on time (t_{ON}). This results in a square wave with amplitudes between V_{IN} and ground, with a duty cycle proportional to V_{OUT}/V_{IN} (see Fig. 3). This square wave is applied to a low-pass LC filter that averages (filters) the signal, producing a DC output waveform. The controller monitors the feedback from the output and makes the necessary adjustments to the duty cycle to maintain the desired regulation. This power conversion method is more efficient than the linear because it stores excess energy in the inductor during the on time of the switch and delivers it to the load during the off time of the switch.

A. The Power Stage

In Fig. 2a, the power stage that converts the power from the input to the output consists of C3 (the input capacitor), Q1 (the power switch), D4 (the free-wheeling diode), L2 (the output filter inductor), R20 (the current sense resistor), C12 (the output capacitor), and the load (battery or system). The reference designators are the same ones used in the power stage of the bq2954 IC EVM schematic in Reference [1].

There are two stages to the power conversion, one with the switch on and one with the switch off (see Figs. 2b and 2c).* The control loop operates

*Note that, when the switching regulator switch is on, it provides a low resistive path and, when off, it has a very high resistance. In either state, the transistor is dissipating very little power (P = IV; i.e., low voltage times load current or input voltage times approximately zero current). For a bipolar switch, the power dissipation is approximately:

$$P = I_C \cdot V_{EC} + I_B \cdot V_{EB} \cdot \delta$$

where δ is the duty cycle. A MOSFET has three main types of power dissipation: The dissipation to drive the capacitances of the FET (switch FET on and off), the dissipation during the transition times from off to on and on to off (linear region of the FET), and the dissipation due to the switch current during its on time.

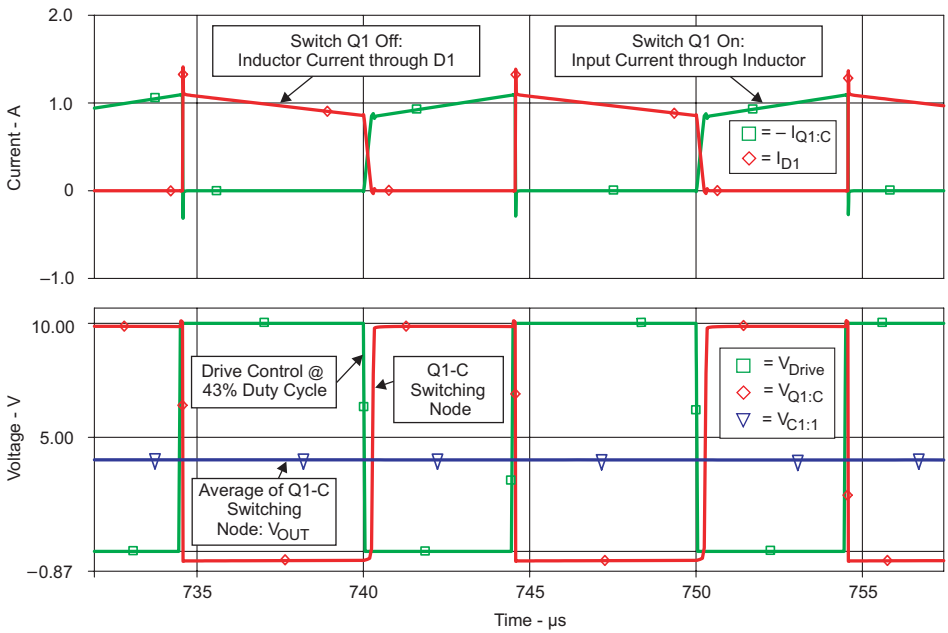


Fig. 3. Buck switcher waveforms.

on a fixed pulse-width modulation (PWM) that turns on the switch at a set time each cycle. If the switching frequency (f) was set to 100 kHz, the switch would turn on every 10 µs (1/f). The control loop, in steady-state operation, would turn off the switch after the current or voltage conditions were met. (The switch is usually on between 1 and 9 µs, depending on the input and output conditions.) For Li-ion battery chargers, there are usually two control loops, one for maximum constant current regulation and one for voltage regulation. Both loops control switch Q1 via an "or" operation. The current loop is in control until the cell voltage reaches 4.2 V, and then the voltage loop takes over as the current tapers off. When the switch is on, the current flows from the input capacitor through the switch, inductor, and sense resistor to the output capacitor/battery/system; then it returns through the ground plane to the input capacitor. The source is charging the battery and at the same time charging the output inductor. During the switch on time, the inductor's current ramps up at the rate of:

$$di/dt = V_{Inductor}/L$$
$$= (V_{IN} - V_{SW} - V_{SNS} - V_{OUT})/L$$

When the control loop turns the switch off, the input current through the switch goes to zero (the source replenishes the input capacitor's energy during the off time). The output inductor's current cannot change instantly; so after the switch is turned off, it has to become the source by flipping polarity. Now the current flows from the inductor through the output capacitor/battery/system, through the return ground plane, through D4, and back to the inductor. While it is the source of the current, the inductor's current ramps down at a rate of:

$$di/dt = (V_{Inductor} + V_{Diode})/L$$

The cycle repeats with the switch turning back on. The power stage components should be placed in sequence in the layout as the current flows from input to output. The routing should be heavy etch or mini-complex planes that connect the components, with the return path being routed on an adjacent layer underneath the path on the top layer. For this topology, a ground plane can be used as a good return path. The intent is to have all currents return to their source along the same path they initially followed, which will minimize the path length and keep them clear of sensitive components. It will also minimize the noise by reducing the inductive loop (antenna).

B. The Drive for the Switch Q1

The switch Q1 dissipates large amounts of energy in its active region during its transition between the off and on states. The faster this transition occurs, the lower the transition power loss. Linear regulators continually operate in their linear state and usually have poor efficiencies unless the overhead voltage is minimized. A low-impedance drive circuit, shown in Fig. 4, is required for turning off the bipolar switch to decrease switching losses. The bipolar switch, when fully on, is in saturation and requires a high-current drive to remove charge stored in the base quickly for a fast turn-off transition. A high signal (~4.7 V) from the MOD pin turns on Q4 and provides a constant current programmed by R16 [(4.7 V – 0.7 V)/220 = 18 mA]. This provides an 18-mA drive to turn on Q1 via D3. To provide fast turn-on of Q1, D3 shunts L1 initially until L1 ramps up to 18 mA, and then D3 turns off. When the MOD pin goes low, Q4 turns off; and the inductor flips polarity and becomes the source to drive its current into the base of Q2. This will turn on Q2 and drive the base of Q1 to its emitter's voltage, which will turn off Q1. R1 insures that any Q4 leakage will not pull on Q1. A similar

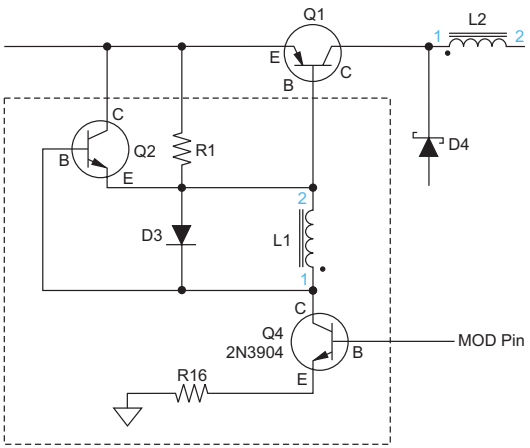


Fig. 4. Driver for the power-stage bipolar switch.

(capacitive) drive circuit is used to turn on and off a P-channel FET. The larger the C_{ISS} of the FET, the better the drive (the lower the impedance) has to be to switch the FET quickly on and off. A 75 ± 50-ns transition time is a good target for which to aim for a 100- to 200-kHz switching frequency. If the FET's input capacitance is small (as in a low-power application), a pull-up resistor may be good enough for turn-off.

C. Current Mirror

The current mirror is a method of converting a low-side to a high-side current-sensing design. The main advantage is that the battery current returns at the same potential as the system return, effectively removing the sense resistor from the battery discharge path and thus improving overall system efficiency. The current mirror monitors the voltage across the high-side current sense resistor and translates this information to the ground side as a reference (see Fig. 5). Current mirrors made from discrete components often cost less than ones produced on one silicon die but can't match the accuracy of the integrated circuit with its matched transistors and uniform die temperature.

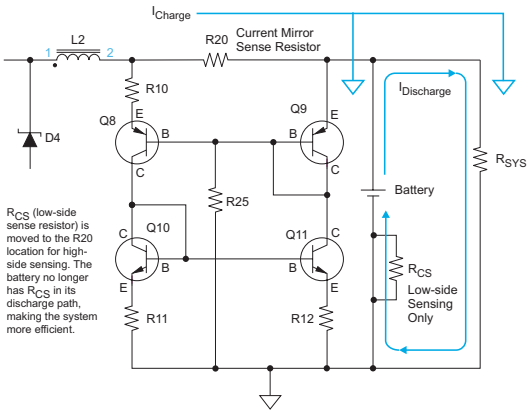


Fig. 5. Current mirror.

Notice the symmetry of the circuit: On the left are R10, Q8, Q10, and R11, which all have the same "collector" current running through them. On the right-hand side are R20, Q9, Q11, and R12, which also all have the same collector current running through them (R20 also has the output current). If these currents are the same magnitude, they will have the same V_{BE} drops, which are the key to the accuracy of the circuit. Note that R10 and Q8 are in series and also in parallel with R20 and Q9. R10 and R20 connect at the same node, and Q8-B connects to Q9-B. Since the V_{BE}'s are matched, the drops across R10 and R20 have to be the same. The current through R10 and R11 is the same; and if the values are the same, then the voltage drop across R11 is equal to the voltage drop across R10. Thus the voltage drop across R20, the sense resistor, is the same as the drop across R11. Note that if R11 and R12 remain the same value, the current through each leg will be the same with the same V_{BE} drops. The designer could scale R10 to change the gain of the current mirror. If the resistance was reduced by half, it would have twice the collector current and twice the sense voltage; and the controller would cut the current in half to get back to the desired regulation. Thus, reducing the value of R10 by half would cut the programmed current in half:

$$I_{OUT} = (V_{SNS}/R20) \cdot R10/R11$$

D. Switcher Design Considerations

The input should be of low impedance so that it can provide the necessary current when the switch turns on. The primary current jumps up to the inductor's current level when the switch is turned on. Therefore, since the source leads are inductive, a good input capacitor with low equivalent series resistance (ESR) (such as from the Panasonic Al Elect. FK series) is needed to supply the desired pulsed (switched) current. If the output impedance of the input filter matches the switcher's impedance, the system will oscillate. The resonance frequency of a capacitor and an inductor occurs when their impedances match each other. If the converter's input voltage drops, the input current increases to deliver the same amount of power. This negative change in voltage divided by the increase in current makes the switcher appear as if it is dropping in impedance like a negative-impedance device. For the system to remain stable, the impedance the switcher sees at the input capacitor has to be lower than the lowest impedance the switcher achieves.

The drive circuit should be designed with enough current to drive the bipolar switch into

saturation for worst-case conditions (h_{fe} gain when V_{EC} is at its minimum and at a minimum temperature, $I_{Drive} \geq I_C/h_{fe}$).

The output inductor should be able to deliver the peak programmed current without saturating. The inductor's ripple current should be no more than 60% of the programmed current:

$$di = V_{IND} \bullet dt/L \text{ or}$$

$$L = [V_{OUT(min)} + V_{Diode}] \bullet [1 - V_{OUT(min)}/V_{IN(max)}] \bullet T/(0.6 \bullet I_{PROG})$$

$$T = 1/f = 10\ \mu s \text{ for } f = 100\ kHz$$

The larger the ripple current, the larger the difference is between average current and peak current. If the current feedback signal is not filtered, the current will be regulated off of the peak. This often is the reason that the actual average charge current is less than the programmed current. The larger the ratio between input and output voltage, the larger the ripple current will be. As the battery increases in voltage, the ripple current decreases. If the control loop regulates off the peak current, the average current will rise as the ripple current is reduced.

The output capacitor's capacitance is small compared to the battery capacitance. The amount of ripple current through the capacitor is determined by the ratio of impedances between the capacitor and battery. The output capacitor should be placed across the battery terminals in a low-side sense configuration. This allows all of the ripple current through the output inductor to be regulated via the sense resistor. Changing the path of the AC current component does not change the average charge into the battery. The output capacitance is chosen mainly for desired operation in case the battery is absent. For a PWM converter, the output capacitance and its load produce a pole in the loop response, which affects the crossover frequency and loop stability. If the capacitance is too small, the pole will be at too high a frequency, the phase margin will be too low, and there will be stability problems. A hysteretic converter's switching is controlled by a hysteresis window and not by a fixed switching frequency and controlled duty cycle. The output low-pass filter, input/output voltages, and sense filters are the main factors that set the switching frequency.

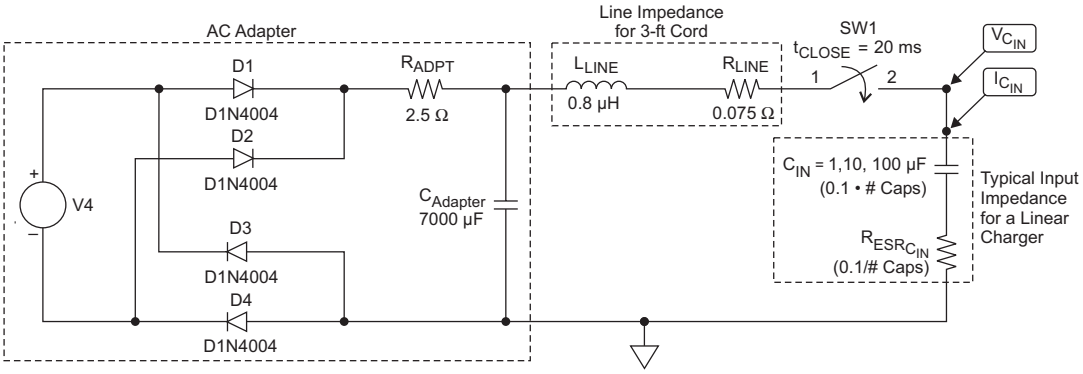
III. Effects of Connecting/ Disconnecting Sources and Loads for a Battery Charger

There are four components of a battery charger configuration: the power source, the charger/ battery management circuit, the battery pack, and the system load. The method by which these circuit blocks are connected/disconnected, their sequencing, and their state of charge can greatly affect the response. Some of the responses could result in damage to the circuitry if not accounted for during the design phase. Four design configurations will be reviewed along with their potential problems and solutions. Many of the issues presented may not result in problems due to the damping effects of circuit parasitics (mostly contact, line, and component resistances) and contact bounce, but the designer should be aware of the possible failure mechanisms.

The ideal battery charger configuration is a stand-alone unit that has the source always connected to the charger. The discharged battery is installed in the charger, and then the wall adapter is plugged into the outlet. This method minimizes any potential problems but also limits the number of applications and the flexibility of the charger.

Problem 1

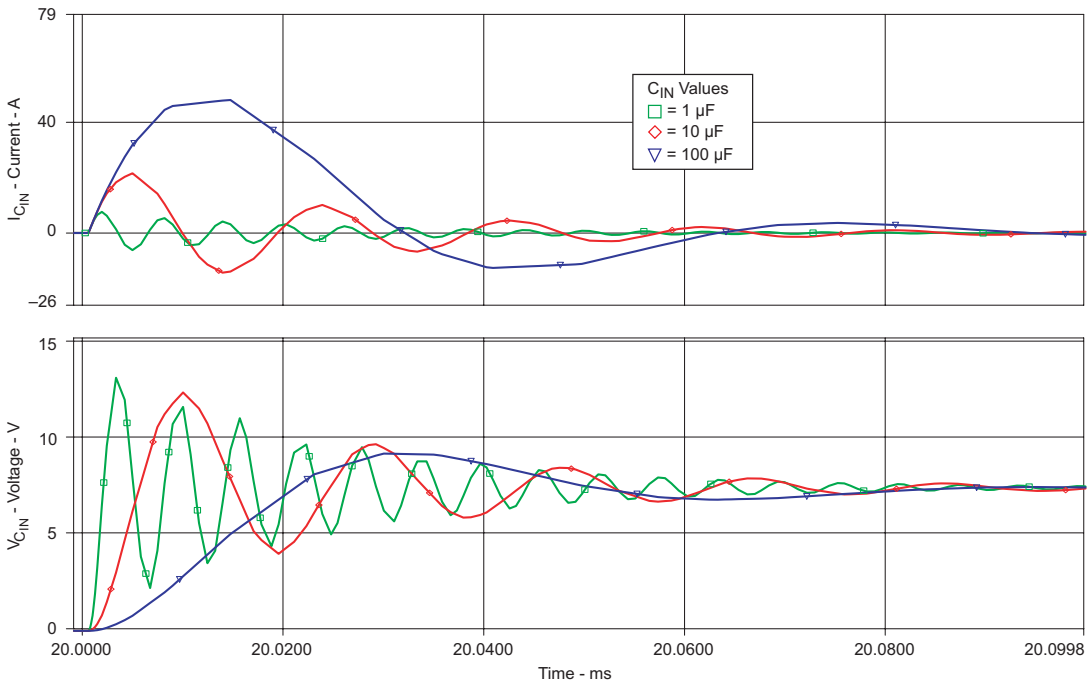
The first potential problem arises when the output of a charged wall adapter (plugged into an outlet) is connected to the input of the charger. The large capacitor in the output of the adapter is charged and is the source for quickly charging the input capacitance to the charger via the adapter's line inductance. This was modeled and simulated as shown in Fig. 6 and is similar to a step response on an LC filter. Typical adapter values were used for a 5-V (~7-V with no load at the output of the adapter), 1-A, 7000-µF output capacitance wall adapter with 36 inches of 21-AWG wire. The simulation was run with five different battery charger input capacitance values ranging from 0.1 to 1000 µF. In the top plot of Fig. 6b, the current peaks in the line inductance when the charger's input voltage reaches the adapter's output voltage (V_L = 0 V). The inductor then flips polarity, becoming the source, and delivers its energy into the charger's input capacitor, resulting in a voltage



Adapter (120 VAC to 5 VDC unregulated) is plugged into wall source and then hot plugged into charger's input capacitance.

Note that a DC source is used to represent the voltage at the peak of an AC waveform.
The adapter's output capacitor will be charged to this peak value prior to hot plugging into the charger circuit.
C1 will stay charged to its full value during this time of interest (80 µs).

a. Schematic.



b. Plot of current and voltage waveforms for C_{IN} = 1, 10 and 100 µF.

Fig. 6. Hot plugging an adapter into a charger circuit as a function of charger capacitance.

of ~2 • V_{OUT}. This would have the potential to damage any parts that are not rated for this 2× voltage. There are several solutions to this problem:

- Reduce line inductance by reducing the adapter's cable length.
- Increase damping resistance.
- Increase the input capacitance to the charger.
- Clamp the input of the charger with a zener diode.
- Increase the voltage rating on input components to ≥ 2× the hot-plug voltage.
- Avoid hot plugging the adapter into the charger.

The simulation shows that adding input capacitance to the charger can reduce the peak voltage. For a series RLC circuit, critical damping occurs at $R = 2\sqrt{L/C}$. Adding capacitance reduces the impedance of the LC circuit, increasing the damping ability of the 75-mΩ line resistance. As capacitance is added, the peak current rises. If the current gets too large the contacts may arc, causing damage due to the poor connection during the plugging action.

In this situation, it is better to increase the damping resistance along with moderate increases in charger capacitance. It is equally effective to increase the damping resistance without increasing the input capacitance. Note that for a switching charger, the input capacitance has to be a low impedance to avoid matching the switcher impedance and becoming unstable; so any resistive damping should be in series with the inductor (see Fig. 7). One can see from Fig. 7b that as the damping resistance is increased to critical damping, the ringing and overshoot are filtered. The one side effect is that 250 mW of line resistance now dissipates power and takes away from the drive. A parallel damping RC could be added in parallel with the charger capacitance, but it would have to be three to four times the capacitance of C_{IN} and have a resistance close to the resonance impedance of the LC circuit to be filtered. This would be the most costly solution. A zener in parallel with C_{IN} would cost slightly more than the R_{LINE} resistor but would avoid the IR drop. The zener's knee is selected at 1.5 • $V_{IN(nom)}$ for an unregulated supply. The peak voltage will be just below the knee, and any inductive voltage spike will be clamped. Since the inductive spikes are not repetitive, a low-power zener may be used.

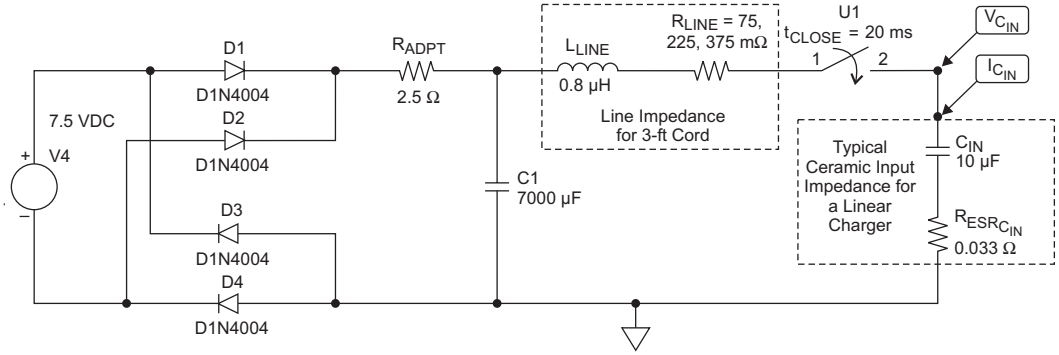
Problem 2

The second potential problem can occur when the adapter is unplugged from the charger while the charger is delivering the programmed fast-charge current (1 A in the simulation) near the regulation voltage of the battery (see Fig. 8). The charged inductance of the adapter's line cord flips polarity to continue to drive the line current. The switch is modeled to open the connection (go from a short to an open) in 1 µs, which leaves little time to discharge the inductor's energy. The waveforms in the top plot of Fig. 8b are the current in the load, the C_{IN} capacitor, and the line inductance. The waveform in the bottom plot is the voltage at the adapter's connector.

In reality a connector can't be unplugged very fast (maybe in 10 ms); and the contact resistance during this time slowly increases, allowing the inductor's current to decrease while keeping the inductor's voltage low. A mechanical switch may be able to open fast enough to cause an inductive voltage spike. One potential effect is arcing, which may degrade the contacts. A more likely failure is damage to a FET switch – which, if turned off quickly, would see a large inductive voltage spike. There are four basic solutions to this type of problem:

- Slow down the FET switch time by adding gate resistance.
- Put an RC series "snubber" across the switch.
- Clamp the inductive voltage spike with a zener upstream of the switch.
- Don't unplug the adapter from the charger during charging.

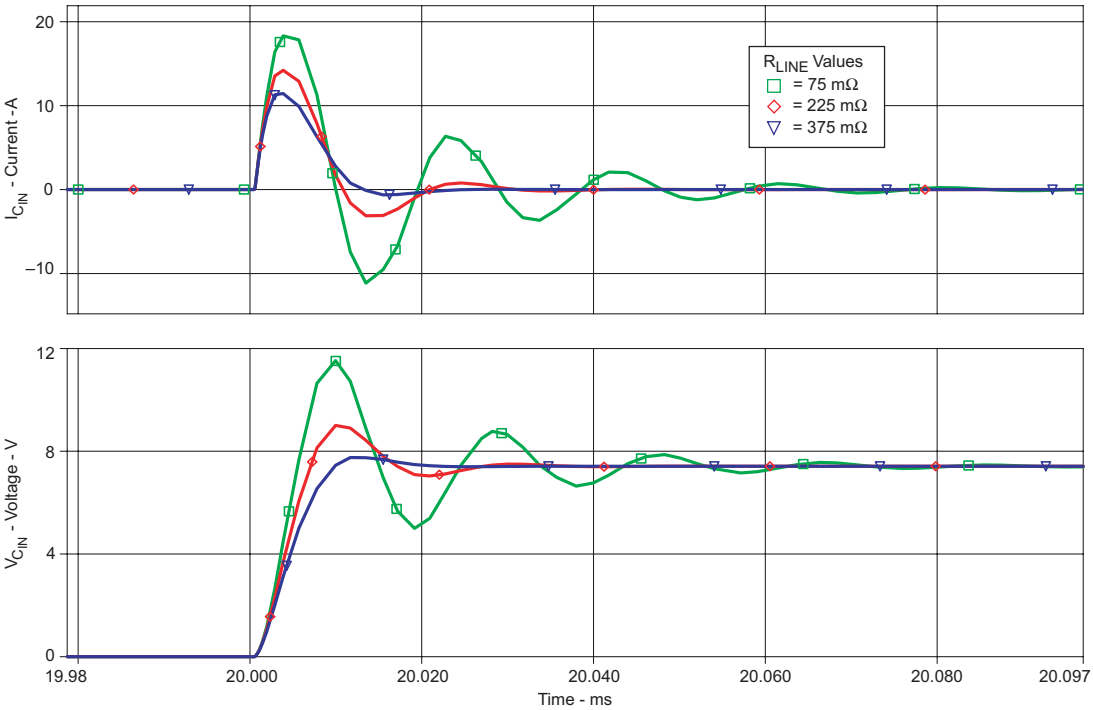
The typical application is unplugging a connector, which probably won't be a problem due to the relative slow speed of breaking the contact. Breaking the contact between the adapter and charger with a mechanical or semiconductor switch is rarely implemented, but this discussion is presented here to help the designer reach a complete understanding.



Adapter (120 VAC to 5 VDC unregulated) is plugged into wall source and then hot plugged into charger's input capacitance.

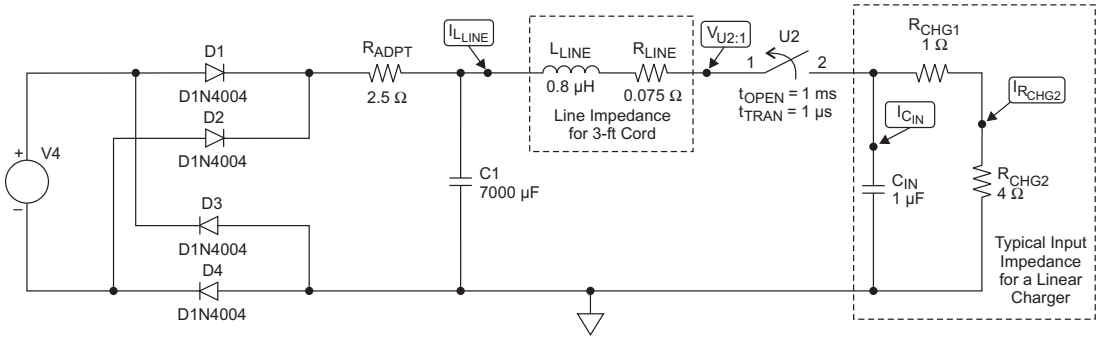
Note that a DC source is used to represent the voltage at the peak of an AC waveform.
The adapter's output capacitor will be charged to this peak value prior to hot plugging into the charger circuit.
C1 will stay charged to its full value during this time of interest (80 µs).

a. Schematic.



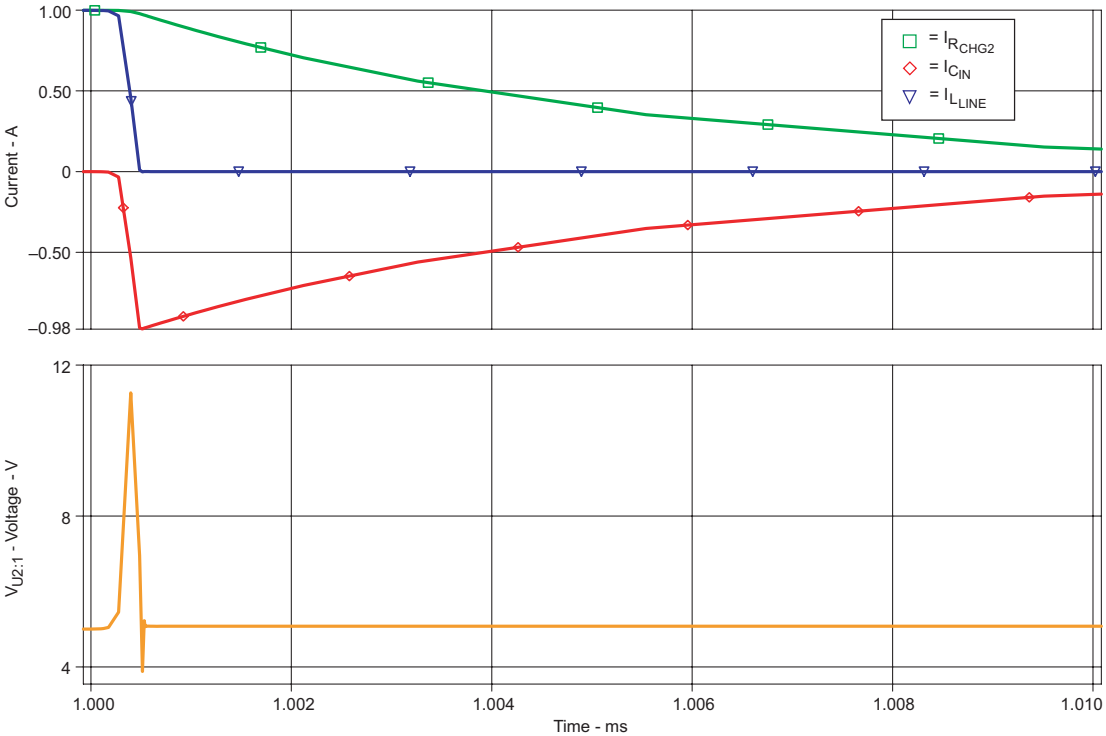
b. Plot of current and voltage waveforms for R_{LINE} = 75, 225, and 375 mΩ.

Fig. 7. Hot plugging an adapter into a charger circuit as a function of damping resistance.



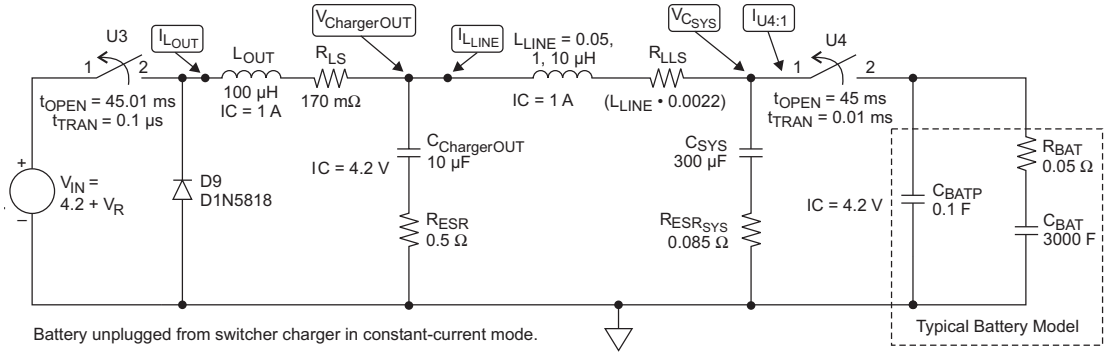
Adapter (120 VAC to 5 VDC, 1 ADC, unregulated) is charging battery pack, and then adapter is unplugged from the charger.

a. Schematic.

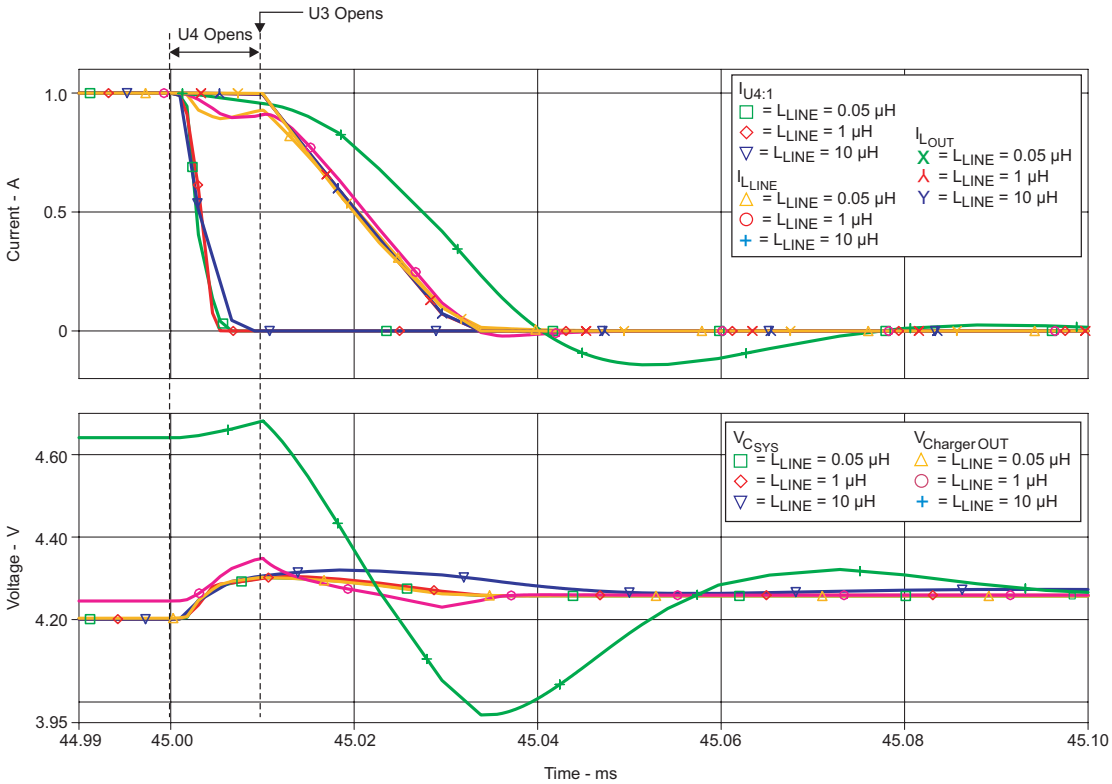


b. Plot of current and voltage waveforms for L_{LINE} = 0.8 µH.

Fig. 8. Effects of unplugging an adapter from a charging circuit.



a. Schematic.



b. Plots of current (top) and voltage (bottom).

Fig. 9. Battery removal during fast charge for a switcher charger, with the system in low-power mode.

Plugging a battery or system load into the charger seldom causes issues due to the fast current loop limiting the current to the programmed level. There may be some system issues with detecting a system load (at 0 V) and supplying a regulation voltage, but this is not within the scope of this topic.

Problem 3

The third potential problem can occur when a charger's load (battery, system, or both) is unplugged while charge current is being supplied.

Unplugging the system load while a battery is connected does not present a hazard, since the battery can momentarily absorb any inductive kick from the line inductance until the controller makes necessary adjustments. If the output is in regulation, the additional pulse in the current could cause a slight voltage overshoot across the battery's impedance, causing the controller to turn off the pass element and then terminate. Discharging the battery to the refresh voltage will start a charge cycle.

Unplugging a charging battery while the system is at heavy load will limit the overshoot due to the damping effect of the system load (capacitive and resistive).

The most likely worst-case condition results from removing a load when there is little or no system load and the battery is removed during a fast charge near voltage regulation, or when the pack protector opens. A model of a switching charger is shown in Fig. 9, and a model of a linear charger is shown in Fig. 10. For both simulations, the battery switch was opened over a period of 10 µs, from 45 to 45.01 ms.

The switcher has a large output inductor that is driven by a voltage source equivalent to the output regulation voltage (4.2 V) plus the line drops. This explains the higher charger output voltages as R_{LLS} is increased. This source is disconnected (the high-side switch is opened) immediately after the battery is fully disconnected. Note that as soon as switch U3 is opened, the output and line inductor currents, L_{OUT} and L_{LINE}, start to decay along with all of the charger and system voltages. The free-wheeling diode provides a low-impedance return path for the discharging inductor. Typically the high-side switch will open as soon as the regulation voltage is exceeded (within a few microseconds) and before the battery is fully disconnected. Therefore there should be much less overshoot than that shown in the figures.

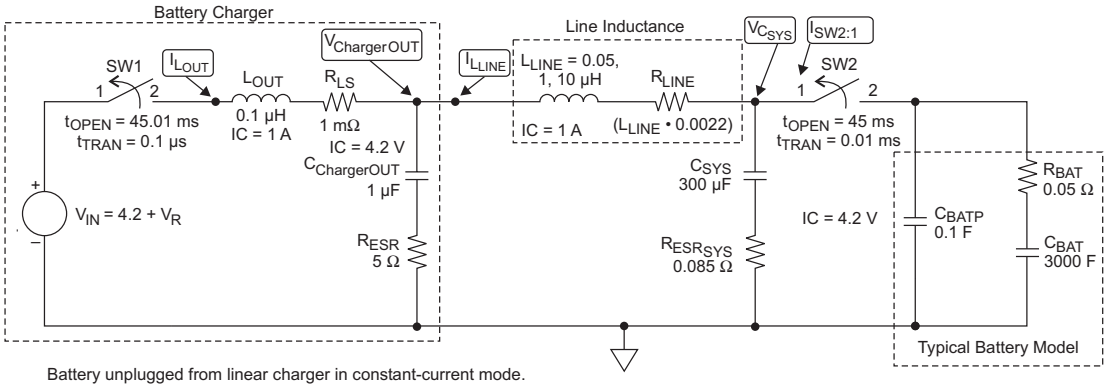
The battery removal for the linear charger simulation has results similar to those of the switcher. The inductor currents, along with the charger and system voltages, start to decay once the pass element is disconnected. The notable difference is that the linear design does not have a free-wheeling diode and therefore results in a discharge of the charger capacitance while the line inductance is discharging.

In all cases, it has been shown that as long as the control loop for the PWM or pass element is sufficiently fast (< 10 µs), the overshoot is negligible.

Problem 4

The fourth and last problem to consider is when the system is powered from the input. If the system is operating under heavy load and is disconnected, the line inductance between the input and the systems will flip its polarity and become the source. The voltage across the inductance will be used to continue to drive this current. There is typically an input charger capacitance and a system capacitance. During the discharge of the line inductance, the current will flow from the charger capacitance to the system capacitance. The smaller-value capacitor will change voltage the fastest. Typically, the input charger capacitance is much smaller and thus will discharge quickly. A large charge in the inductor can drive the charger capacitor negative, causing potential damage to the charger circuit. A Schottky diode, with cathode to the input and anode to ground, will protect the charging circuit. If the system capacitance is small or is disconnected with the load, the system voltage can spike high along with the charger capacitance voltage going negative. Adding a zener clamp can be effective in controlling this voltage. As always, reducing the line inductance or avoiding disconnection of the load is the best approach.

Overall, most of the issues that result in component damage or the necessity for resets are due to voltage spikes from hot plugging/unplugging components. The two most problematic cases are hot plugging a charged adapter into a charger and removing the adapter when directly powering a



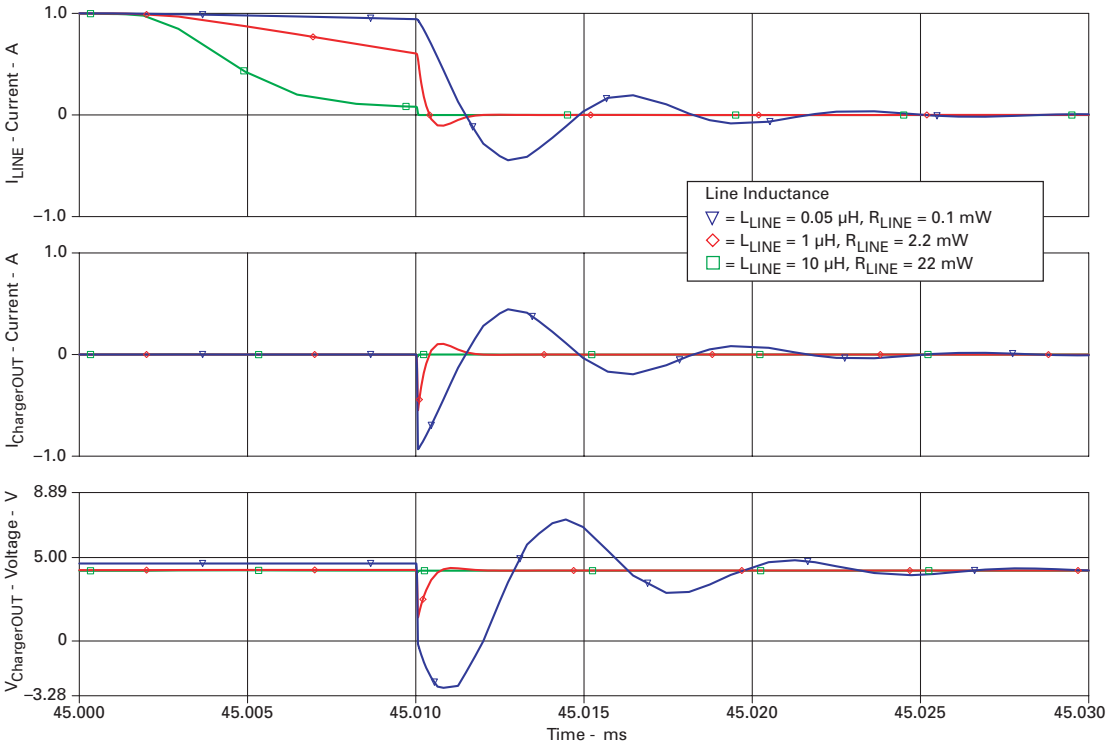
Battery unplugged from linear charger in constant-current mode.

The line inductance is equivalent to 2.5" (0.05 µH), 50" (1 µH), or 500" (10 µH) of line cable. If the line conductors form a large loop, the inductance may be in the microhenry range with a much shorter length (<100").

V_R = Voltage drop from V_{IN} to V_{BAT}.

IC = Initial condition.

a. Schematic.



b. Plots of current and voltage.

Fig. 10. Battery removal during fast charge for a linear charger, with the system in low-power mode.

heavy system load. This is because charged inductors can't change current instantly and will go to whatever voltage is needed to keep the current flowing. These inductive voltage transients often find the breakdown voltage of the lowest-rated component. The best solution is to reduce the line inductance by minimizing the length of the cables. This alone should eliminate the problems. If there is a need for long cables, the design should account for the potential problems presented. The typical solutions to consider are damping by series resistance or RC snubbing; clamping voltages with zeners; or increasing component ratings. Twisted pairs have the lowest inductance per length. To calculate wire inductance (signal and return) for twisted or parallel pairs, use 10 to 20 nH per inch of cable as an estimate. For a series RLC circuit, critical damping takes place when alpha and omega are equal and $R = 2\sqrt{L/C}$. For a parallel RLC circuit, $R = 0.5\sqrt{L/C}$.

Hopefully this discussion will help the designer consider, during the design phase, the potential field application problems that can arise from voltage/current transient failures.

IV. Effects of Charging a Battery with a System Load

In portable power, integration is paramount; and the trend is to use the battery charger also as a power source for the system. This seems like a logical progression, but several new issues arise that the charger controller has to handle. These problems are mainly associated with the system load profile. Understanding the system load profile is the key to finding system design solutions. The main problems occur during startup and termination.

In portable power the trend is to use high-energy, high-density batteries that give the longest run time for the smallest package size. The 4.2-VDC Li-ion battery has become increasingly popular among manufacturers; it fits well with the typical load/charge usage patterns of the consumer, since it is not susceptible to memory effects. For this reason, this section of the paper deals mainly with 4.2-V Li-ion batteries, with a few comments about the other chemistries along the way.

In the past, there were no start-up issues for stand-alone chargers. If a discharged battery was installed, the charger would start with a precharge current if the battery voltage was below ~3 V; with a constant current charge if between 3 and 4.2 V; and with voltage regulation if at 4.2 VDC. When the charger current dropped to ~C/10, the charge cycle would terminate. If the protector was open and the output was 0 V, a precharge current would attempt to close the protector. With the integration of a system load in parallel with the battery came start-up and termination issues.

The start-up issues occur when the stand-alone charger is used as a building block in the system design. If the charger powers up into precharge mode ($V_{BAT} < 3$ V), the power delivered will be

$$P = IV = (C/10) \cdot V = (I_{CHG}/10) \cdot V_{BAT}$$

and the system's average load (in watts) most likely will be greater than the power delivered. The system will have to go into a low-power mode so the precharge current can do its job and bring the battery into fast charge. If the charger enters fast-charge, constant-current mode, the system load (in watts) will still have to be considerably less than the charger output (in watts) for the battery to charge in a timely manner. The maximum available power deliverable by the charger occurs during voltage regulation:

$$P = IV = I_{CHG} \cdot 4.2 \text{ VDC}$$

The lower the output voltage, the less power a constant-current charge delivers:

$$P = I_{Fixed} \cdot V$$

Many constant-power loads (such as switching converters) require more current as the voltage drops. Therefore, the best way to avoid depleting the battery during charge is to keep the average system load (in watts) lower than the lowest charger output (in watts) in fast-charge mode:

$$P = I_{CHG} \cdot V_{BAT} = I_{CHG} \cdot 3 \text{ V}$$

Considering these issues during the design phase will insure a more robust product. Once fast charge enters voltage regulation, the concerns focus on proper termination.

Termination issues arise when the charger controller is designed with the assumption that all output current will go to the battery. With a system load connected across the battery, the charger can't determine the destination of the current. Battery manufacturers recommend terminating charge when the battery is full. Charging can be resumed after the battery is partially discharged. Leaving the pack connected to a voltage source (LDO) is not recommended. Termination is typically based on $I_{CHG}/10$, which is not likely to occur if there is a system load in addition to the battery charge current. If the termination is delayed, the safety timer may expire, terminate charging, and enter fault mode. Disabling the safety timer solves this problem but creates others. The purpose of the safety timer is to protect against a bad cell that is not taking a charge. The root problem of proper termination is that the charger can't accurately determine the actual minimum current of the battery. For these reasons, it is critical that the designer fully understand the system load profile and how it relates to the charger functions.

There are four controller thresholds that should be analyzed when the dynamic load profile is considered: precharge/fast-charge, taper, termination, and refresh. Transients near these thresholds may cause a change in charging states. Deglitch filters often take care of many transients, but some load profiles require additional application circuits for the product to operate as desired. Setting the duration of the safety timer requires understanding of the average system load current. A discussion of the external solutions for the different thresholds follows.

A. Precharge Threshold

Problem

Entering precharge from fast charge due to a pulsed load will reduce the charge current to a level that may not charge the battery or supply sufficient power to the system.

Solution

1. Identify the amplitude of the load pulse and the circuit and battery impedances to determine at what threshold the system needs to enter a lower-power mode to avoid dropping out of fast charge. Add more low-impedance filtering on the output if necessary. If there is a deglitch (filter) time before a mode change and the average power load is less than the output of the charger, there should not be an issue unless the load step is longer than the deglitch time.

2. Add an RC filter to the battery feedback voltage to filter the transient. This is equivalent to a deglitch circuit for load transients.

3. Have a microprocessor monitor the battery voltage and control the system load to avoid getting near this threshold. Keep in mind the diminishing returns: As the pack voltage drops, the power delivered by the charger drops, while the system load typically remains at constant power. A safe design will have an average system load (in watts) that is less than the minimum charger power output in fast-charge mode. In precharge mode, the system should be in sleep mode.

B. Taper Threshold

Problem

At the taper threshold the battery is considered full, but often a timer is set to give a little more charging time before termination. If there is a dynamic load or a slow-stepping system load, the threshold is exceeded and the timer is reset, avoiding normal termination.

Solution

1. For a transient load where the average current is below the taper threshold, the feedback sense current can be filtered to remove any transients. Average-current-mode chargers that use a current mirror to program the output current with an external high-value resistor are excellent candidates for filtering. Applying a small capacitor across the programming resistor to average the waveform prevents transients from affecting the taper timer.

2. For stepping loads with long durations (in seconds) that are not practical to filter, a circuit to detect a preset valley can be implemented to terminate the charge as shown in Fig. 11. This circuit was designed to interface with a charger that terminates instantly if the charger's current drops near zero. Switch Q4, controlled by a status output pin, disables the circuit during a no-charge condition to prevent battery discharge. Q22's emitter is preset just below the normal current

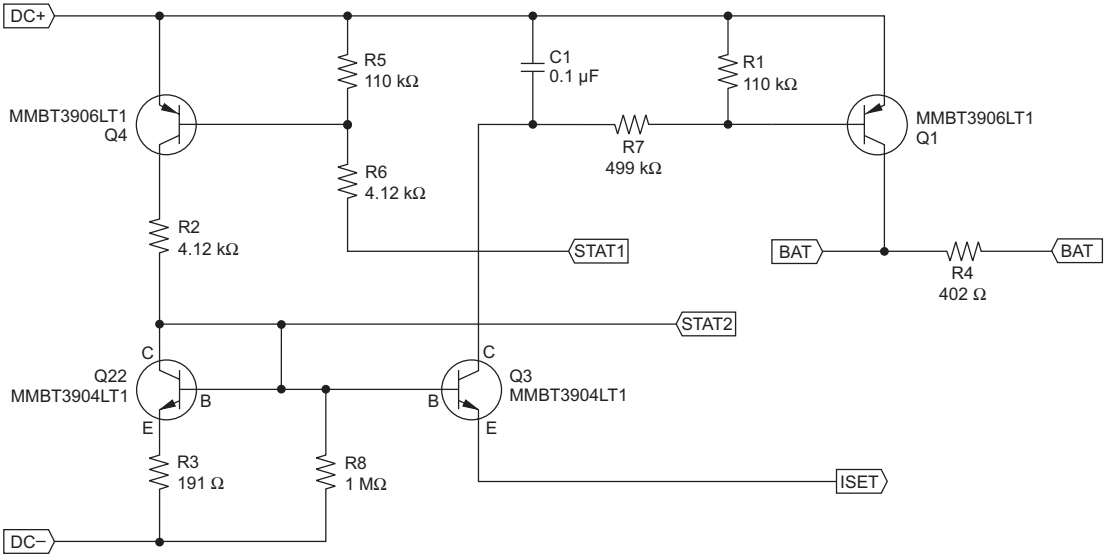


Fig. 11. Termination circuit triggered by minimum sense current.

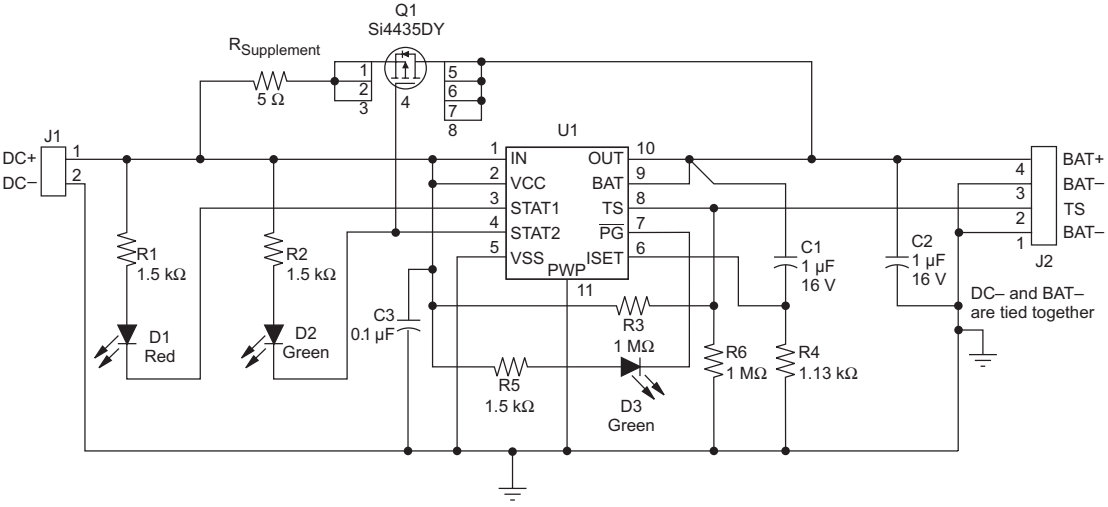


Fig. 12. Supplemental 160-mA charging current from input through Q1 to output offsets system minimum load. If system load current is 150 mA, all of the charger current will go into the battery and will terminate properly.

taper-threshold voltage by dividers R2 and R3. If Q3's emitter's voltage, which is tied to the sense current signal, drops below the voltage on Q22-E, Q3 turns on and pulls on Q1. This applies a current to the battery feedback signal at the IC's error amp and produces a small voltage on top of the battery pack voltage, thereby making the controller "believe" that the battery is slightly above voltage regulation. The charge current is reduced, which further reduces the sense voltage. This positive feedback drives the charge current to zero, and the controller terminates due to zero current. The battery then has to be discharged down to the refresh threshold for the charge to continue.

3. Another possibility for a fixed minimum system load is to supplement this current from the input source through a resistor and P-channel FET to the system (see $R_{Supplement}$ and Q1 in Fig. 12). The charger will no longer be delivering this current, and the battery can terminate normally. The gate of the FET is tied to the status pin that goes high when charging is terminating. This disconnects the supplemental current, which prevents overcharging of the battery.

C. Termination Threshold

There are several notable problems in dealing with termination.

If a system load is removed quickly during voltage regulation, it is possible for the battery to overshoot voltage momentarily due to the energy stored in the line inductance, which would drive the pass FET off and terminate the charge. This may result in termination with a battery at less than full capacity. The solution is to reduce the line inductance, reduce the amplitude or speed of the transient, or filter the battery sense feedback signal.

There are other conceptual problems with termination. Often designers use the C/10, C/5, or C/15 termination threshold as a figure of merit. One problem is that this is relevant only at a 1C programmed charge rate. In reality, if a fast charge is set to C/2, the termination threshold is actually at $I_{PGM}/10 = (C/2)/10 = C/20$. Thus the "C/10" termination threshold actually results in a termination of 1/20 the C-rate of the battery.

There are other problems associated with full capacity. The accuracy of termination affects capacity. The desire to have low power dissipation at fast charge necessitates having a small-current sense resistor. At termination the charge currents are very small. A small current multiplied by a small resistance is a small control signal that is very susceptible to noise. This problem is compounded if the battery is charging at less than 1C, since the termination then would be < C/10. To overcome these accuracy issues, a taper threshold (the point at which the battery is deemed full) can be created to set a 30-min timer for termination. The charge current tapers at an exponential rate, so accurately detecting the taper threshold makes little difference at the end of 30 min.

Other methods of current sensing and regulation use matched transistors that have the same biasing and are scaled to different current levels. For example, the current sense matched transistor in TI/Benchmarq products is typically 1/320 of the larger charge-pass transistor and delivers 1/320 of the current to the charge current program pin. The current is regulated by connecting a large resistance (0.7 to 8 kΩ) to this current source and driving the pass FET (on/off) to regulate the resistor voltage to 2.5 V. This allows one to program the output current by changing the program resistance:

$$R = 2.5\ VDC \bullet 320/I_{PGM}$$

Chargers with nickel chemistries shouldn't have any transient load in parallel with the battery, since any increase in load would produce an IR drop. This drop would be detected as a peak voltage detect (PVD), which terminates charge. The solution for dynamic loads is to monitor the temperature change in the battery pack via a thermistor. When the rate of change of ~1ºC/min is reached, termination occurs. This method of termination is not affected by load transients.

D. Refresh Threshold

Problem

If the battery is full, the charge has terminated, a system load is applied, and the battery is removed, the charger often will not start charging without going through a battery-detect cycle or a deglitch filter. This may cause the system to crash before the charger supplies sufficient power.

Solution

Add enough system capacitance to hold up the output for the deglitch and/or battery-detect routine time. An alternative is to detect the battery removal and toggle the charge enable pin to restart a charge. This still will require significant holdup capacitance.

One can see that there are many issues with adding a system load in parallel with the battery; and most of these issues have work-around solutions involving additional circuitry, provided the load profile is understood. Many manufacturers cannot predict all the load scenarios that may happen in the field. The next section presents one optimal solution that eliminates many of the problems with connecting the system across a battery while it is charging.

V. The Proper Way to Power a System Load from a Battery Charger Circuit

The recommended solution is to power the system directly from the input source, when it is available, and at the same time to charge the battery from the input via the charger. This allows the charger to be dedicated exclusively to the battery without any external disturbances. The overall efficiency is also greater, since the power to the system is not regulated down to a lower voltage by a linear regulator. This recommended solution does have some issues that are discussed next.

The transition timing of the FETs is the primary issue to consider when power to the system is switched from an input source to the battery pack. There are two types of switching transitions: "make-before-break" and "break-before-make." The former will connect the secondary source before disconnecting the primary source to make sure the system never loses power. The problem with this type of power transfer is that, if the sources are at different potentials, the sources may interact and cause damage or potentially high shoot-through currents.

Break-before-make switching will disconnect the primary source before connecting the secondary source, which solves the interaction between the supplies but momentarily causes the system to lose power. This method requires enough system capacitance to hold up the voltage for a specified amount of time.

Fig. 13 shows an example of how to implement switching between the source and the battery. When the input voltage is greater than the battery voltage, the power good ($\overline{PG}$) signal pulls low, turns on Q1/Q4, and turns off Q3 and Q2. If the input source drops below the battery voltage, the $\overline{PG}$ signal goes high, which turns off Q1/Q4 and turns on Q3 and Q2. The threshold of Q1 and Q3 overlaps such that when their gates are at 2.5 V, they are both nearly off (> 1 kΩ from source to drain). The partial overlap of the FET's turn-on thresholds emulates a break-before-make circuit.

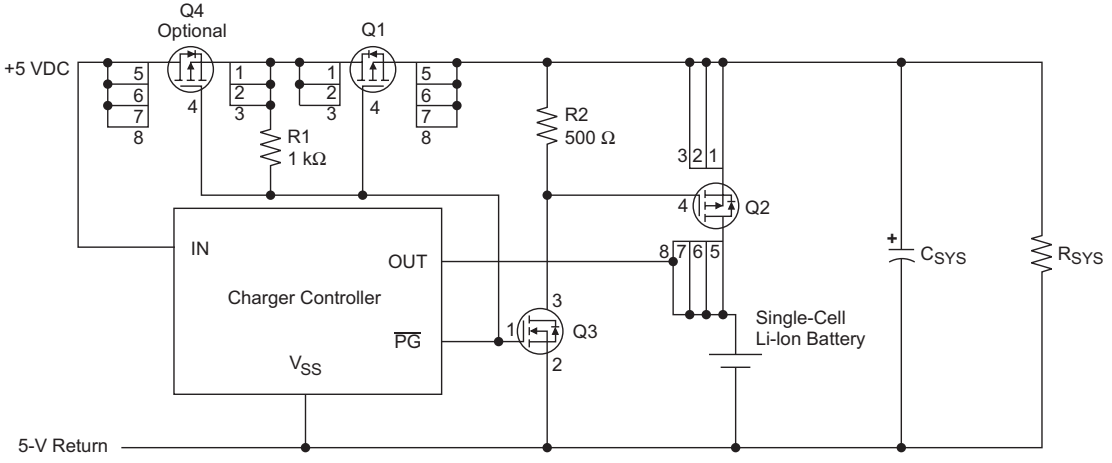


Fig. 13. Stand-alone battery charger controls power to system and battery.

The system capacitance should be large enough to hold up the system voltage for this 10- to 50-µs time period. Q2 has its body diode such that the battery can supply the current to the system if the system voltage falls a diode drop below the battery voltage. Q4 is optional and is needed only if there is something hanging on the input that will load the battery via the body diode of Q1. The charger controller selected for the design should have a $\overline{PG}$ pin to control the switching. (A status pin that shows sleep mode could be used as well.)

Placing the system load in parallel with the battery complicates the task of a smart charger. It is impossible for the charger to determine where the current is going or the condition of the battery. Designing a charger for a known DC system load across the battery requires some additional design, but designing for transient loads immensely complicates the task. The long-term solution for putting the system load in parallel with the battery is to emulate the circuit design in Fig. 13. This design powers the system from the input and switches the battery to the system only when input power is lost. This approach can be extended for multiple Li-ion cells with a little more attention to both timing and cross-conduction issues. Keeping the system current separate from the battery current during charging will also simplify the task of managing the battery pack.

VI. Summary/Conclusion

This paper has attempted to cover many issues that typically arise during the design and testing phase of a battery charger. Circuit design, thermal and layout issues, and other design concerns were discussed for power conversions. Product testing and return current issues dealing with connecting and disconnecting charging components during charging were presented. The paper concluded with issues surrounding charging a battery with a system load across the battery. Even though many types of work-around solutions were examined, the best is to power the system from the input, let the charger be only a battery charger, and connect the battery to the system only when input power is lost.

VII. Reference

[1] *DV2954S1H Li-Ion Charger Development System*, User Manual, TI Literature No. SLUU053

Design Trade-offs for Switch-Mode Battery Chargers

Jose Formenti and Robert Martinez

ABSTRACT

The design of switching converters as a standalone block is a well-known topic. However, very specific challenges arise when a DC/DC converter is used to charge a battery pack. Understanding the impact of using a battery as a load, and other charger-related system-level details up-front, is a requirement when designing a DC/DC converter targeted at battery-pack charging. Up-front consideration of those issues will enable the designer to incorporate features and functions during the design phase that are not present in common DC/DC converters but that should be included in DC/DC converters targeted at battery charging. This article discusses the most common benefits and challenges faced when using switching converter topologies to charge battery packs, including specific challenges and design tradeoffs faced when using the battery pack as a load.

I. Introduction

Methods for designing stand-alone switching converters are well-known. However, specific challenges arise when a DC/DC converter is used to charge a battery pack. Understanding up-front the impact of using a battery as a load and other charger-related system-level details enables the designer to incorporate features and functions not present in common DC/DC converters.

This paper discusses the most common benefits and challenges of using switching-converter topologies to charge battery packs. A comparison of distinct switching topologies identifies when each is most advantageous. Subsequent sections focus on buck switching charger design; synchronous versus nonsynchronous operation; power dissipation and switching frequency; the impact of AC adapter voltage range on converter design; MOSFET selection; loop-compensation requirements for battery-pack loads; and safety and fault-protection circuits.

II. Converter Topology

A. Overview

There are currently two major topologies used to implement buck converters targeted at battery-pack-charging applications: synchronous and nonsynchronous rectification. These topologies can be implemented with integrated or discrete switching MOSFET devices. The switching devices can be NMOS, PMOS, or a combination of both.

The selection of a specific topology will be dictated by the design boundaries set by the following system requirements:

- Charge-current level
- AC adapter voltage range
- Ambient temperature range
- Converter switching frequency
- Target PCB area
- Availability of system resources dedicated to power-management functions

Sections B and C discuss the most common synchronous and nonsynchronous topologies.

B. Basic Buck-Converter Topologies and High-Side FET Selection

Nonsynchronous buck converters represent one of the earliest implementations of switching regulators; a simplified circuit for a nonsynchronous buck converter is shown in Fig. 1. A single switch (S1) is

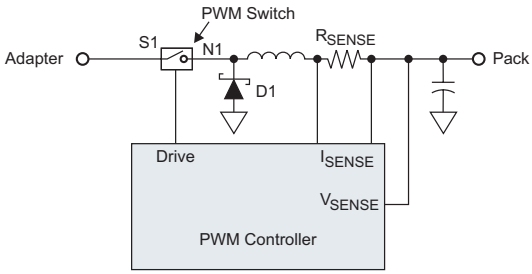


Fig. 1. Simplified nonsynchronous topology.

closed during a time (t_{ON}) connecting the AC adapter voltage to the inductor. When the switch opens during the off time (t_{OFF}), a free-wheeling diode (D1) holds the voltage at a node (N1) while providing a path for inductor (charge) current. The duty cycle is set by internal control circuits and regulation loops that monitor the pack voltage and pack charge current.

The control loops are configured to limit either the charge current or the charge voltage to a programmed value. This scheme enables control of the charge current when the battery voltage is below the target charge voltage, or control of the charge voltage when the battery voltage reaches the regulation voltage (see Fig. 2).

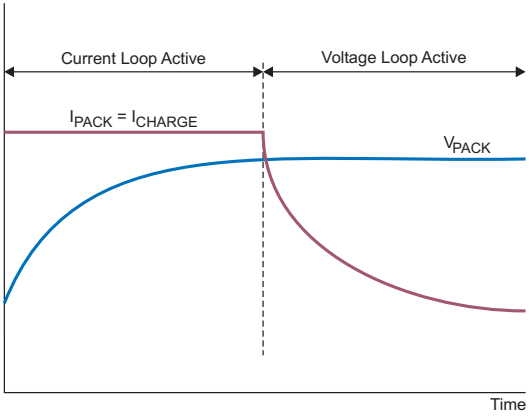


Fig. 2. Typical charge cycle.

The high-side power MOSFET selection will influence and sometimes dictate key charging parameters such as the maximum possible charge current, maximum frequency, minimum number of output filter components, and cost. The two obvious choices are either NMOS or PMOS FETs (see Fig. 3). Each has its own advantages, disadvantages, and proper application.

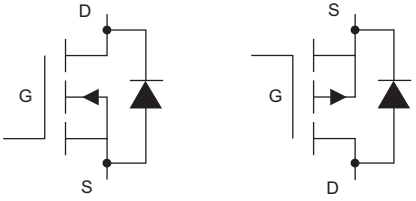


Fig. 3. NMOS FET (left) and PMOS FET.

Typically the NMOS devices have the advantage of a lower $R_{DS(ON)}$ for the same package; thus either more load current can be used or the cost can be lower. Another way to look at it is that, for the same $R_{DS(ON)}$, the die size can be smaller; thus the total gate charge of a discrete NMOS typically can be lower than that of a discrete PMOS. The lower gate charge lowers the switching losses, allowing a higher switching frequency and lowering the output filter inductor and capacitor requirements. The disadvantage of an NMOS on the high side is that turning it on requires a method to drive the gate with a voltage higher than the input voltage. The voltage also must be maintained below the maximum gate-to-source voltage rating of the device. For PMOS high-side FETs, turn-on of the FETs is simplified because the gate voltage needs to be lower than the input voltage by at least 5 V instead of higher. Devices with a lower voltage rating can be used, and the only requirement is that the lower voltage rail be provided.

For most implementations where the power MOSFETS are discrete parts external to the control IC, the preferred MOSFET to use is the NMOS to lower system cost and to have high performance with high efficiency.

For implementations where the power MOSFETs are integrated within the control IC, the PMOS is usually preferred over the NMOS because of its ease of implementation and also because the PMOS/NMOS area trade-off favors the PMOS in integrated MOSFETs (see Fig. 4). Discrete devices typically have a 2:1 trade-off,

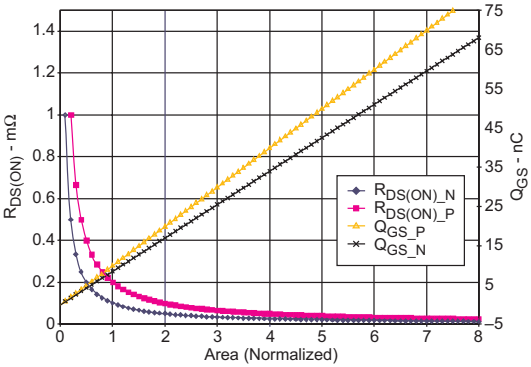


Fig. 4. $R_{DS(ON)}$ and Q_{GS} versus area for NMOS and PMOS FETs.

whereas integrated lateral devices may have a 1.4:1 trade-off. This is typically offset by the gate-drive requirements of the NMOS implementation. Total gate charge also is typically much smaller in an integrated lateral device, allowing the increase in gate charge for the larger-area PMOS implementation with little effect on total power losses.

C. Nonsynchronous and Synchronous Topologies

Nonsynchronous Topologies

Nonsynchronous topologies enable designs that simplify controller architecture and system-side power-management functions. To minimize system cost, less complex controllers designed to drive external PMOS devices are the preferred choice for nonsynchronous buck-charger stages. The selection of PMOS switching devices enables the use of a very simple driver architecture for the power stage on the controller, switching gate-voltage levels between adapter voltage and ground. More sophisticated designs that require higher efficiency or operation at higher voltages have dedicated circuits to clamp the gate-driver low level to a fixed value as shown in Fig. 5, minimizing switching losses and preventing MOSFET device damage from gate-oxide breakdown. The clamp circuit is usually a low-accuracy regulator that uses an external tank capacitor to handle the current peak pulses that occur during MOSFET switching. Another advantage of the PMOS is that the duty cycle can be kept indefinitely at 100%.

The use of a free-wheeling diode implements a topology that intrinsically has no problems with cross-conduction on the power stage during switching; it also eliminates any stray paths from battery pack to ground when the high-side switch is off (see Fig. 6). As a result there is no need for the complex system power-management functions usually required when cross-conduction and battery-pack leakage paths are present.

The downside of nonsynchronous topologies is their power dissipation. With proper PCB thermal design and proper selection of PWM power-stage components, nonsynchronous topologies typically can be used to charge battery packs with maximum

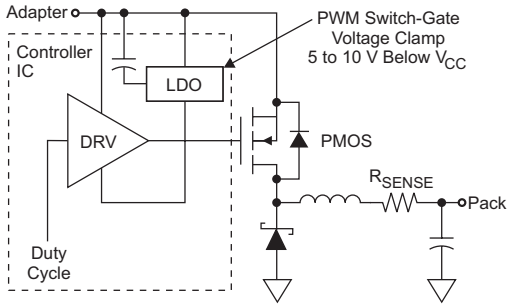


Fig. 5. High-side-driver voltage clamp.

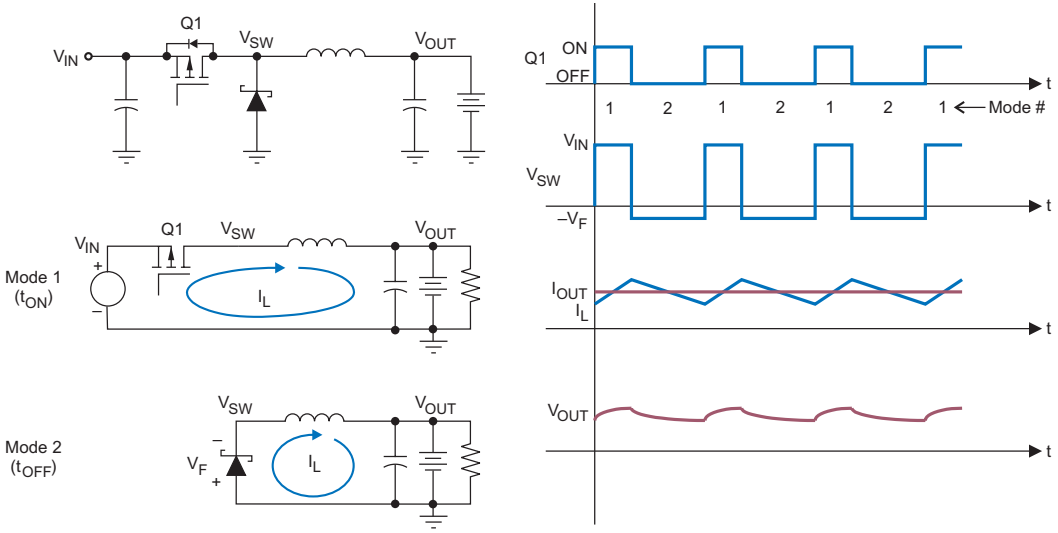


Fig. 6. Modes of operation and waveforms for an nonsynchronous buck converter.

charge-current rates in the 3- to 4-A range. The power dissipation for nonsynchronous topologies occurs in the switching device, the free-wheeling diode, and the driver. Power losses on the free-wheeling diode effectively limit the maximum charge current to values significantly lower than those in synchronous topologies.

Synchronous Topologies

Synchronous DC/DC converters are a logical choice for application conditions where the nonsynchronous topologies do not meet power dissipation and efficiency requirements. Synchronous converters typically cost more because additional components are required and the controller is more complex. There are two basic topologies commonly used for synchronous DC/DC converters; both of them use a low-side NMOS switch to minimize losses on the free-wheeling diode. The high-side switch can be either PMOS or NMOS.

Fig. 7 shows a simplified diagram for a synchronous converter with a PMOS high-side switch. This configuration improves the overall efficiency as compared to the nonsynchronous solution, while still enabling use of a simple gate driver for the high-side switch.

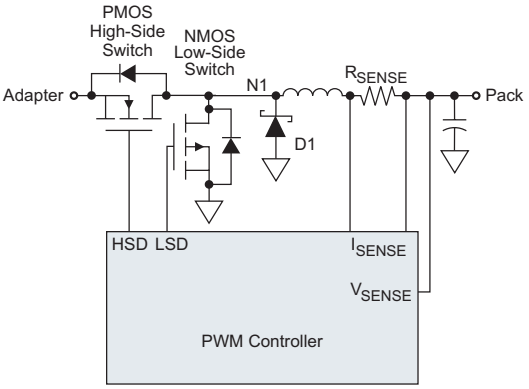


Fig. 7. Synchronous topology with a PMOS high-side switch.

The synchronous operation of the high/low-side switches impacts controller complexity. To avoid shoot-through currents during switching, a break-before-make logic function must be added to ensure that the switches are never on at the same time. Usually a dead time is built in to guarantee that no cross-conduction happens; a Schottky free-wheeling diode is required to hold the node N1 voltage during the dead time (see Fig. 8).

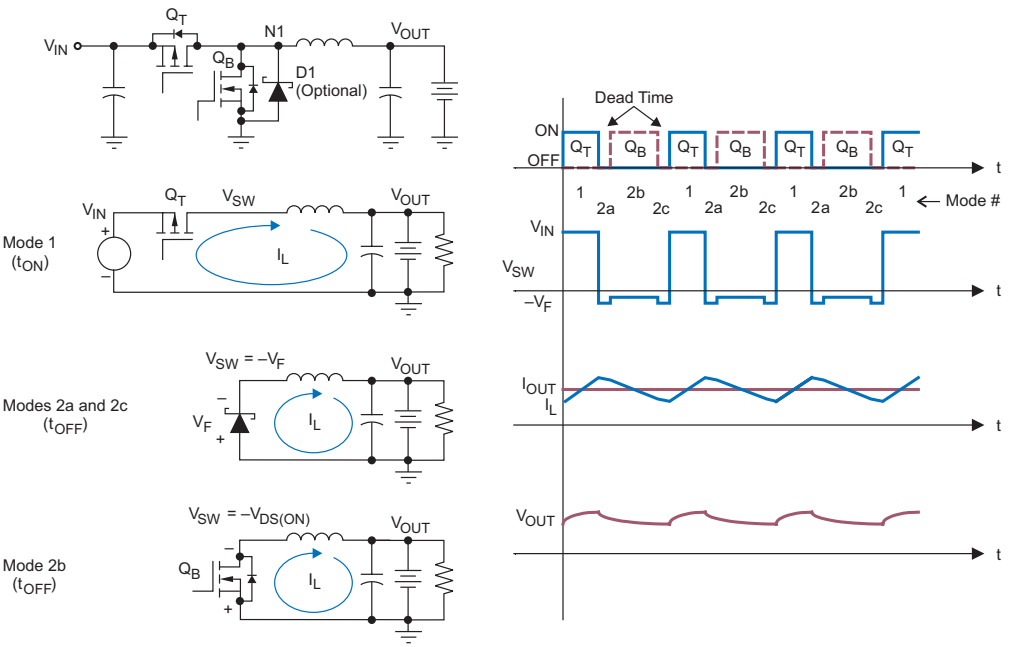


Fig. 8. Modes of operation and waveforms for a synchronous buck converter.

The main impact of implementing a synchronous topology is that additional functionality must be added to the PWM controller. In addition to the break-before-make circuit, a new gate driver for the low-side switch is needed; this in turn requires a new LDO and tank capacitor to enable operation of the low-side switch driver at high voltages with minimal switching losses (see Fig. 9).

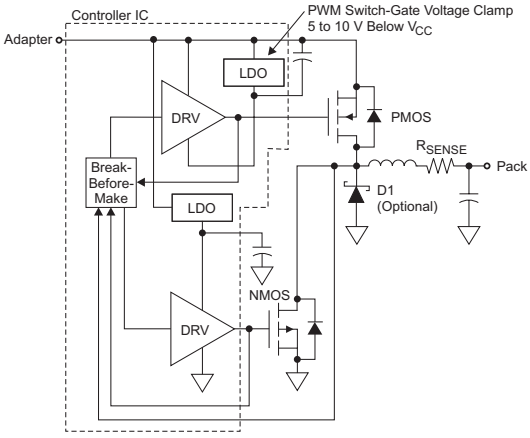


Fig. 9. Driver topology for synchronous PMOS/NMOS topology.

To avoid shoot-through currents during PMOS switch activation (the PMOS drain goes from ground to adapter voltage), the low-side driver must be dimensioned to hold the low-side switch gate close to ground while the drain/gate capacitor for the low-side switch is being charged. This can be accomplished by designing the low-side switch driver so that the off-state $R_{DS(ON)}$ is lower than the high-side switch on-state $R_{DS(ON)}$.

Even though the PMOS/NMOS synchronous topology represents an improvement over the nonsynchronous topology, a few limitations still are present. The most important is that the synchronous PWM can't be run at very high frequencies due to the typically high gate-charge values for PMOS devices and the power-dissipation constraints on the PWM controller IC. This prevents the use of a smaller inductor. Also note that PMOS switches cost more than NMOS switches with the same voltage/current ratings.

This limitation can be overcome by using an NMOS/NMOS topology. Similar to the non-synchronous/synchronous transition previously discussed, new circuitry must be added to the controller because an NMOS/NMOS synchronous converter requires driving the high-side switch gate to voltage levels above the adapter voltage. This can be done in any of three ways:

1. Use a separate, external gate-drive supply rail that is higher than the input voltage rail by at least 5 V.
2. Use a charge pump to generate the higher gate-drive supply rail. This requires three capacitors and four high-frequency switching FETs, or two high-frequency switching FETs and two Schottky diodes.
3. Use a bootstrap circuit to provide the required gate-drive voltage from a 5-V external rail every cycle. This requires the 5-V supply, a Schottky diode, and a capacitor.

The preferred method is usually the bootstrap circuit because it does not require a higher voltage rail and is usually the simplest to implement. The disadvantage is that it requires extra components, and they need to be rated at higher voltage than the input voltage. Another disadvantage is that the bootstrap capacitor needs to replenish its charge loss due to switching and leakage currents within the IC and the Schottky diode. This prevents leaving the high-side FET fully on at a 100% duty cycle for long periods of time. A periodic recharge pulse providing a 99.9x% duty cycle is required.

The other two methods, using a higher voltage rail or a charge pump, do allow an indefinite 100% duty cycle to be maintained; but in most cases, durations of < 1% are not required when traded off with the expense of more complex circuitry, more components, bigger size, and more internal noise.

A simplified schematic for an NMOS/NMOS topology is shown in Fig. 10. This commonly used solution implements a bootstrap circuit with an external capacitor and a regulated voltage generated by the controller IC.

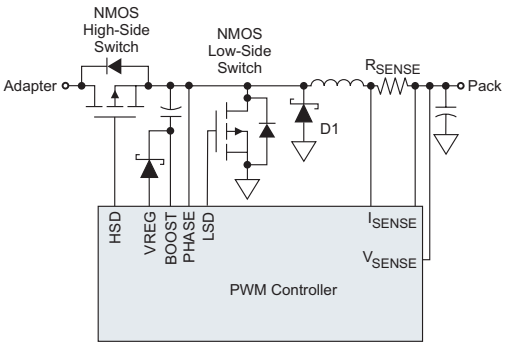


Fig. 10. NMOS/NMOS synchronous topology.

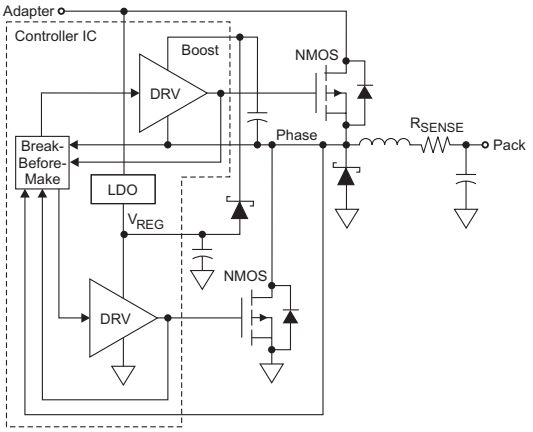


Fig. 11. Driver topology for synchronous NMOS/NMOS topology.

The controller drivers also have to be modified to enable use of an NMOS/NMOS topology; Fig. 11 is a simplified diagram of commonly used driver topologies. Note that in this configuration the high-side switch driver is driven between boost and phase nodes; the bootstrap capacitor is recharged with the low-side driver supply regulator to optimize controller design. The break-before-make circuit also needs to be modified to sense the high-side voltage gate levels accordingly.

III. Power Dissipation and Size versus Switching Frequency

For most chargers the input supply is off the AC adapter; thus low-load efficiency as a battery input supply is not a key concern. Instead, high current efficiency is important for lower thermal dissipation and to obtain maximum charge current. With this in mind, it is common to target an increase in switching frequency to decrease the output inductor and output capacitor values and sizes. The output inductor and output capacitor can be calculated from the following equation:

$$L = \frac{V_L \bullet \Delta t_{ON}}{\Delta I_L} = \frac{\left(V_{IN} - V_{OUT}\right) \bullet \left(\frac{V_{OUT}}{V_{IN} \bullet f_S}\right)}{\Delta I_L}$$

where ΔI_L is the inductor current ripple. This is plotted in Fig. 12 for a one-cell Li-ion battery charger (V_{OUT} = 4.2 V) with a 2-A charge current, an input voltage of 10 V and 20 V, ΔI_L = 600 mA, and sweeping switching frequency from 100 kHz to 1.5 MHz.

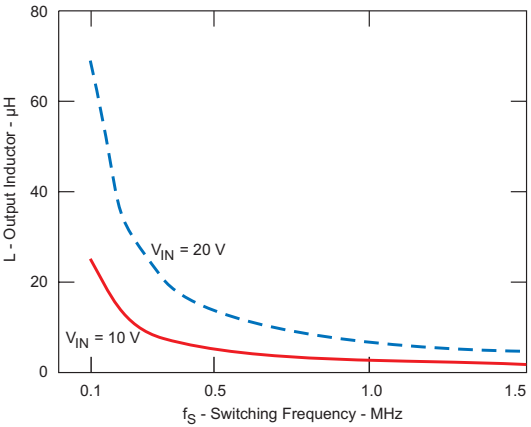


Fig. 12. Output inductor versus switching frequency at V_{IN} = 10 V and V_{IN} = 20 V.

The output capacitor is determined with the following formula:

$$C = \frac{\Delta I_L \bullet \left(\frac{V_{OUT}}{V_{IN} \bullet f_S}\right)}{\Delta V_C}$$

where ΔV_C is the capacitor output voltage ripple. This is plotted in Fig. 13 for a one-cell Li-ion battery charger (V_{OUT} = 4.2 V) with a 2-A charge current, an input voltage of 10 V and 20 V, ΔI_L = 600 mA, and ΔV_C = 0.5% of V_{OUT} = 21 mV.

The formula for C also shows that a higher switching frequency can decrease the ripple current and voltage proportionately for the same output inductor and capacitor. If the frequency is kept constant and the output inductor or capacitor

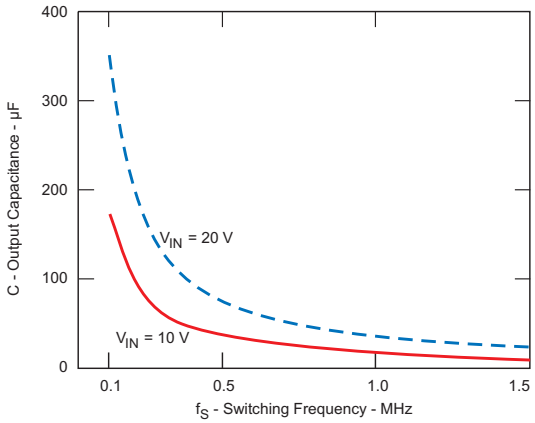


Fig. 13. Output capacitor versus switching frequency at V_{IN} = 10 V and V_{IN} = 20 V.

is decreased, the output ripple current and voltage will proportionately increase.

The simplified first-order power-loss equations are composed of conduction-loss components and switching-loss components.

Total power losses are

$$P_{TOT} = P_{CON} + P_{SW}$$

The conduction losses are composed of five main contributors. Conduction losses are

$$P_{CON} = P_{ON\_T} + P_{ON\_B} + P_{R_{SENSE}} + P_L + P_C$$

given by

$$P_{ON\_T} = R_{DS(ON)\_T} \bullet \left(\sqrt{D} \bullet I_{OUT}\right)^2$$

where $R_{DS(ON)\_T}$ is for the *top* control MOSFET.

$$P_{ON\_B} = R_{DS(ON)\_B} \bullet \left\{\sqrt{(1-D) - \left[f_S \bullet \left(t_{d1} + t_{d2}\right)\right]} \bullet I_{OUT}\right\}^2$$

where $R_{DS(ON)\_B}$ is for the *bottom* synchronous MOSFET, and t_{d1} and t_{d2} are the dead times.

$$P_{R_{SENSE}} = R_{R_{SENSE}} \bullet {I_{OUT}}^2$$

where R_{SENSE} is the current sense resistor.

P_L inductor power loss, excluding AC losses, is

$$P_L = R_{DCR} \bullet {I_{OUT}}^2$$

where R_{DCR} is the series resistance of the output inductor.

P_C capacitor power loss is

$$P_C = R_{ESR} \times \left(\sqrt{D} \bullet I_{OUT}\right)^2$$

where R_{ESR} is the equivalent series resistance (ESR) of the input capacitor.

The switching losses are primarily dependent on the gate charge of the power FETs and the dead time. Switching losses are

$$P_{SW} = P_{SW\_T} + P_{SW\_B} + P_{SCH} + P_{GD}$$

The top high-side power FET switching losses are

$$P_{SW\_T} = \frac{Q_{GSI\_T} + Q_{GD\_T}}{I_G} \bullet \frac{V_{IN} \bullet I_{OUT}}{2} \bullet f_S$$

where Q_{GSI} is the gate-to-source charge, and Q_{GD} is the gate-to-drain Miller gate charge of the *top* control MOSFET.

$$P_{SW\_B} = \left[\left(Q_{RR\_B} \bullet V_{IN}\right) + \frac{C_{OSS} \bullet {V_{IN}}^2}{2}\right] \bullet f_S$$

including the reverse recovery, Q_{RR}, losses and output capacitance, C_{OSS}, of the lower synchronous MOSFET.

$$P_{SCH} = V_F \bullet I_{OUT} \bullet \left(t_{d1} + t_{d2}\right) \bullet f_S$$

where V_F is the forward voltage of the Schottky diode in parallel with the low-side synchronous FET, and t_{d1} and t_{d2} are the dead times.

$$P_{GD} = V_{IN} \bullet \left(Q_{GSTOT\_T} + Q_{GSTOT\_B}\right) \bullet f_S$$

where Q_{GSTOT_T} and Q_{GSTOT_B} are the total gate charge at the gate drive regulator voltage for the top and bottom FETs, respectively.

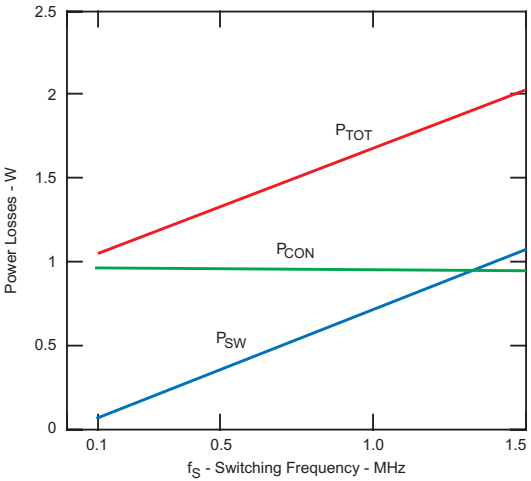


Fig. 14. Total power losses, switching losses, and conduction losses for a typical single-cell, Li-ion battery charger.

As shown in Fig. 14, the total power dissipation is dependent on the switching frequency; however, the values of the output inductor and capacitor are inversely proportional to the switching frequency. For battery chargers, this trade-off is usually optimized to minimize the size and cost of the components while keeping the system power dissipation below the thermal limit. Thus switching frequency is increased primarily to improve the power density (size) of the charger until a thermal limit is reached. Also keep in mind that off-the-shelf capacitors and inductors are available in only a handful of values and sizes; thus they must change as a step function instead of linearly with frequency.

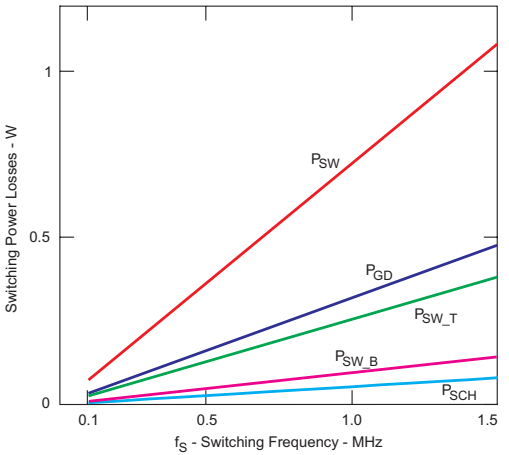


Fig. 15. Switching losses during dead time for the single-cell, Li-ion battery charger: Total, gate drive, top FET, bottom FET, and Schottky.

The total input gate charge of the power MOSFETs contributes to gate-drive losses that dissipate within the control IC and raise its temperature. As shown in Fig. 15, the gate-drive losses could be significant. This needs to be considered when the charger ICs are operated at higher switching frequencies such as 500 kHz for high-current applications, or 1 MHz for lower-current applications. The junction temperature should be calculated to ensure that the data sheet specification is not being exceeded. To reduce the temperature, the designer can either decrease the switching frequency or select power MOSFETs with lower gate charge. Some charger control ICs have an integrated thermal-limit comparator that automatically shuts off if the junction temperature exceeds a maximum threshold. The maximum power loss for a package can be calculated from the maximum junction temperature of the silicon ($T_{J(max)}$), the ambient temperature (T_A), and the package thermal junction-to-ambient resistance ($R_{\theta JA}$).

$$P_{LOSS(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

IV. Switching Regulator Trade-offs for Battery-Charging Applications

A. Can Standard Converters Be Used in a Battery-Charging Environment?

The standard topologies discussed in section II can be implemented with a wide array of DC/DC controllers available on the market today. However, using standard controllers for a synchronous conversion potentially can cause various problems when a battery load is used, unless additional circuits are designed into the overall solution.

Traditional stand-alone controllers are designed to handle loads that have only sink capability; a battery load can both source and sink currents. Using traditional converters can lead to premature battery discharge; pack protector activation; or converter malfunction.

Following are a few problems that can happen:

- The pack is shorted to the AC adapter output if the pack is above the adapter voltage.
- The PWM converter does not start when the charger is enabled and a pack is connected.
- Battery reverse current flows through the low-side switch during the charge-current taper phase.
- The bootstrap circuit can't be recharged when the adapter voltage is too close to the battery-pack voltage.

The discussion up to this point has focused on the major topologies used in synchronous converters targeted at battery-pack-charging applications. For the sake of simplicity, only the trade-offs related to controller complexity, cost, and power dissipation have been covered. The next section provides an overview of common challenges that arise when those topologies are used in a battery-pack-charging environment and practical solutions that can be used to implement a robust design.

B. Avoiding Undesirable Reverse Discharge

A battery is a two-quadrant device in that it has a positive voltage but could allow both positive and negative current to flow. When the current is positive, the battery sources the current; when the current is negative, it sinks the current (see Fig. 16). Because of this, battery chargers need to avoid reverse discharge, which can drain the battery and reduce expected run-time capacity. There are two probable paths for reverse discharge within a synchronous buck regulator: from battery to input and from battery to power ground.

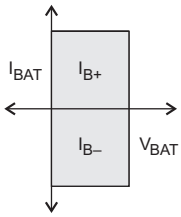


Fig. 16. A battery is a two-quadrant device that sources and sinks current.

The first path is from the battery, through the output inductor, and through the back diode of the high-side power MOSFET to the input (see Fig. 17). This occurs when the battery is higher than the input voltage. Connecting a series Schottky diode at the input with the cathode connected to the drain of the high-side power FET prevents the reverse-discharge current (see Fig. 18). This protection is the simplest to implement for discrete solutions. The penalty of using the Schottky diode, however, is that the added forward voltage drop, V_F, increases conduction power losses and the size of the diode as the charge current increases. A power MOSFET can be used instead of the Schottky diode to reduce the conduction losses and the area as shown in Fig. 19. A gate signal needs to be generated in which the FET is kept on only during charging. Also, the input voltage and battery voltage must be monitored during charging to ensure that the blocking FET is turned off quickly if the input voltage ever falls below the battery voltage. This is easier to implement with integrated solutions. Keep in mind that both Schottky-diode and FET reverse-blocking implementation still have reverse leakage currents to consider. Schottky diodes typically have higher leakage current (up to the milliamps), especially at high junction temperatures; whereas the MOSFET leakage is typically in the microamps.

The second path for reverse discharge within a synchronous buck regulator is from the battery, through the output inductor, and through the low-side FET to ground, as shown in Fig. 20. This occurs through the channel of the FET when the power MOSFET is on and the current reverses

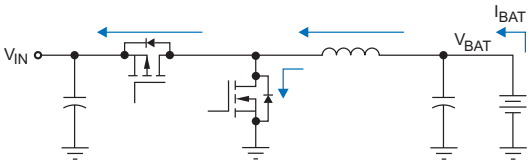


Fig. 17. Reverse battery leakage path from battery to input when $V_{IN} < V_{BAT}$.

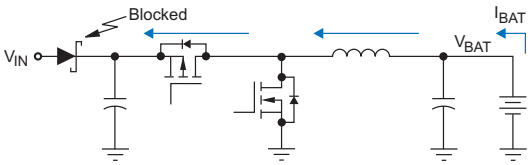


Fig. 18. Protecting reverse leakage from battery to input with a Schottky diode.

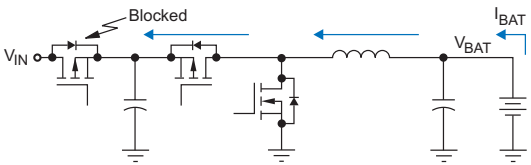


Fig. 19. Protecting reverse leakage from battery to input with a synchronous PMOS FET.

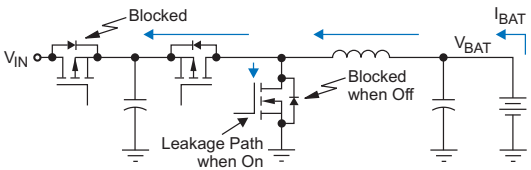


Fig. 20. The NMOS low-side FET provides a leakage path to ground when on but blocks reverse conduction when off. A circuit that detects a near-zero current is needed to shut off the FET before the current reverses.

through the inductor. To prevent this, the inductor current or low-side MOSFET current must be monitored, and the low-side power MOSFET must be turned off before the inductor current reverses (goes negative). It is better to turn off the low-side FET before the current reverses than to let even a small current reverse. If the inductor current is allowed to reverse and then the low-side FET is turned off, the inductor will try to force current through the high-side power MOSFET into the input supply. If there is an input reverse-blocking Schottky diode or MOSFET, it will avalanche and possibly could be damaged if the energy is high enough. Thus it is always preferable to avoid reverse conduction of synchronous buck chargers. Keep the low-side FET off when the circuit is not charging; turn on the low-side FET when the circuit is charging and the inductor current is positive; and then turn off the FET before the inductor current reverses. This is very important, especially during power-up or whenever the duty cycle is very low, during which the low-side FET will attempt to be on most of the time.

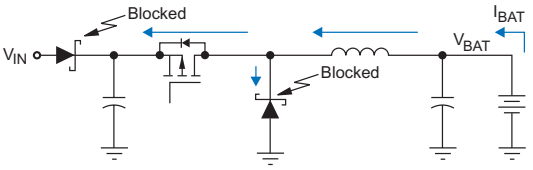


Fig. 21. A nonsynchronous buck regulator blocks large reverse-discharge currents to ground, but it also has higher conduction losses.

Nonsynchronous buck regulators use the Schottky diode instead of a power MOSFET to prevent reverse discharge (see Fig. 21). The diode prevents reverse conduction at the expense of increased forward-conduction power dissipation and size. Again, keep in mind that there will be some reverse leakage current for both the Schottky diode and the power MOSFET. The leakage of a Schottky diode is usually a magnitude higher than that for a power NMOS FET. Both Schottky diodes and NMOS FETs have a higher leakage as their junction temperature increases.

Preventing reverse discharge to ground is also important when a charger is started up with a battery connected at the output. If the converter is allowed to conduct negative current through the low-side FET, the current will go negative and will not be able to charge the inductor with positive current, either indefinitely or for a significant amount of time. Fig. 22 shows an oscilloscope plot of a charger with no reverse-current protection. The current is allowed to go to –1.5 A. Fig. 23 shows the same charger with the reverse-current protection enabled. The NMOS low-side FET is turned off before the current is allowed to reverse and discharge to ground. There is no negative current, and the charger more quickly powers up the output.

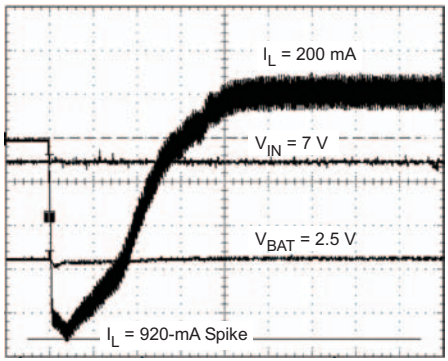


Fig. 22. Inductor current during startup with no reverse-current protection, causing large 920-mA discharge-current spikes. Inductor current goes negative and settles to a charge current of 200 mA.

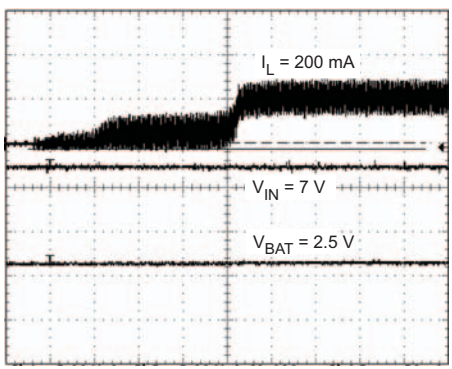


Fig. 23. Inductor current during startup with reverse-current protection enabled so there are no discharge-current spikes. The low-side FET is turned off before the inductor current reverses and goes discontinuous, which then settles to a charge current of 200 mA.

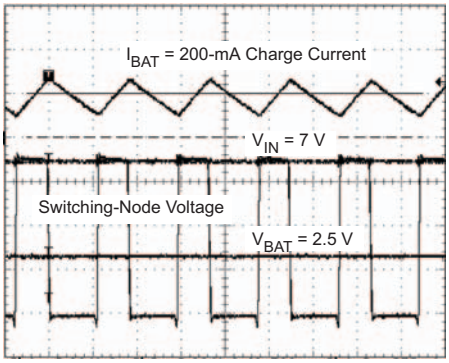


Fig. 24. Switching-node voltage with continuous inductor-current conduction when current is always positive.

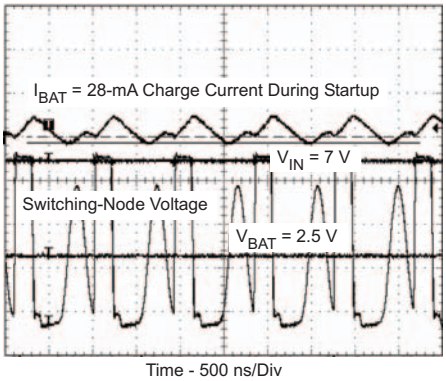


Fig. 25. Switching-node voltage with discontinuous inductor-current conduction to prevent reverse conduction.

C. Unique-Load Behavior

Battery chargers have a few unique requirements that stand-alone voltage converters don't. Besides regulating the output voltage, battery chargers have the additional task of regulating output current when the battery voltage is below the voltage-regulation value. Another difference with battery chargers is that the loads are not always the same as in a simple voltage converter. Voltage converters typically have a resistive load, or a constant power load with very low input impedance. For a constant output voltage, the load could be simplified to a constant current source. Expected loads for a typical stand-alone voltage converter are shown in Fig. 26. Constant power loads are usually due to any combination of linear and switching regulators that distribute the power to the various blocks of the application. Constant power loads can be represented by a voltage-dependent current source.

Battery chargers, on the other hand, are expected to have various load combinations depending on the application. Cradle chargers usually have only a battery load (see Fig. 27). If the battery is removed, the cradle charger is expected to detect removal and then stop charger operation.

For embedded-charger applications, the charger could have a battery load and a constant-power system load at the same time (see Fig. 28). The combined load behaves more like a constant-power operation than a constant-current operation

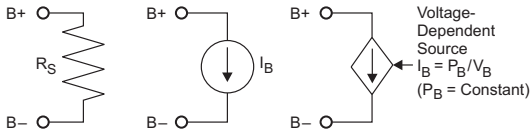


Fig. 26. Expected loads for a typical stand-alone voltage converter.

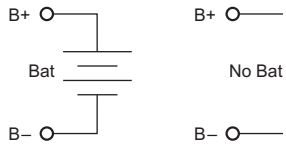


Fig. 27. Expected loads for a cradle battery charger.

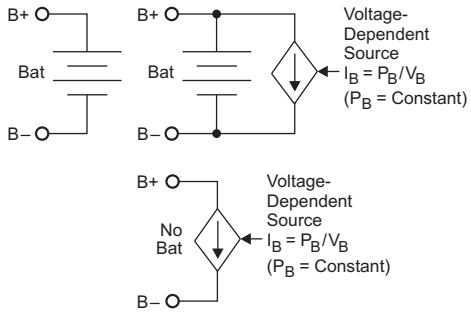


Fig. 28. Expected loads for an embedded battery charger.

when the battery voltage is below the voltage-regulation threshold. In some embedded applications, the charger is also expected to regulate the main system rail if the battery is removed or is being changed. Dual-pack embedded applications require power-management handling to switch from one pack to another.

Special attention should be paid to compensation when a battery is connected as a load. The battery behaves as an energy source or an energy sink, since current can flow in both directions. The battery protection described earlier can take care of the reverse-discharge concerns; however, it introduces a discontinuous-current mode when the current is low. The converter needs to ensure stable operation for both continuous- and discontinuous-current modes. Chargers go discontinuous when in precharge and during tapering when nearing charge termination. Fast charge is typically in continuous-current mode. Operation in continuous-current mode has a double pole due to the output inductor and capacitor. During discontinuous-current mode, the poles split and the dominant pole frequency is a function of the load.

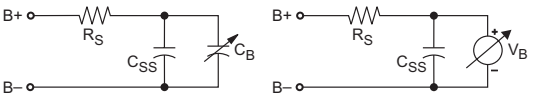


Fig. 29. Large-signal model of a battery.

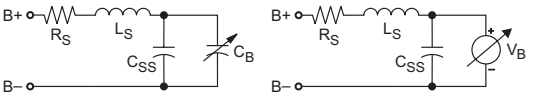


Fig. 30. Small-signal model of a battery.

Another requirement is that the battery behave as a unique load whose small-signal behavior is not always taken into consideration. As shown in Fig. 29, the battery looks like a very large capacitor that plays a key role in large-signal behavior; but, contrary to intuition, the small-signal behavior is different in that it is dominated by the series inductance and resistance of the pack (see Fig. 30). The large capacitor is modeled as an ideal voltage source during the small-signal analysis and plays a minor role in the response. The voltage on the ideal (large-capacitance) voltage source may vary depending on its state, but the series resistance and inductor are relatively constant. This inductive behavior needs to be accounted for in compensation design, as it has a tendency to improve phase margin but reduce gain margin as the output behaves more like a current source. The low gain margin can allow excessive ringing at frequencies above the crossover frequency.

As in voltage converters, the output capacitor and its associated ESR need to be considered in battery chargers. A key goal in portable equipment is to reduce the size of converters by increasing the switching frequency, which enables small ceramic capacitors to be used at the input and the output. The result is that the converter could have large swings in resonant frequency due to the wide capacitance tolerance over temperature. Ceramic capacitors also have very low ESR values that push out the zero frequency to a value too high to assist in canceling a pole. ESR zeros for ceramics are typically at or above the switching frequency.

D. Control Scheme Affecting Frequency

Various control schemes can be used to regulate the converter current and voltage. Control schemes can be divided into two groups: one that maintains constant switching frequency and another that varies the switching frequency. In all control schemes the output is regulated by varying the duty cycle, which is equal to the on time divided by the period.

$$D = \frac{t_{ON}}{T_S} \approx \frac{V_{OUT}}{V_{IN}}$$

The constant-frequency control schemes regulate the duty cycle by varying the on time while keeping the frequency constant (f_{S_Fixed}).

The variable-frequency control schemes can be divided into three types: constant on time, constant off time, and hysteretic. Following are the equations for the first-order frequency of each:

- The constant-on-time method keeps the on time constant and varies the off time to get the necessary duty cycle, thus varying the frequency.

$$f_{S\_t_{ON}} = \frac{D}{t_{ON}}$$

- The constant-off-time method keeps the off time constant and varies the on time to get the necessary duty cycle, thus varying the frequency.

$$f_{S\_t_{OFF}} = \frac{1-D}{t_{OFF}}$$

- The hysteretic method varies both on time and off time, thus varying the frequency.

$$f_{S\_HYS} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{L \bullet \Delta I_C \bullet \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{OUT}} \right)}$$

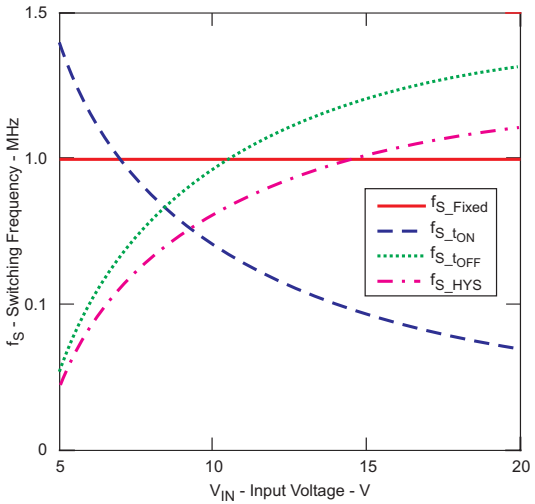


Fig. 31. Frequency variation versus input voltage of converters with fixed-frequency, constant-on-time, constant-off-time, and hysteretic control schemes.

The possible frequency variations for a 4.2-V, single-cell output charger with a 10-µH inductor, a 100-µF output capacitor, and an input varying from 5 to 20 V are plotted in Fig. 31. A 1-MHz constant-frequency converter is compared to a 500-ns constant-on-time converter, a 500-ns constant-off-time converter, and a 15% current ripple hysteretic converter.

Constant-frequency control schemes have the benefit of keeping the frequency above critical frequency bands such as the audible noise region (300 Hz to 3 kHz) or the ADSL carrier frequency (900 kHz), which are important design constraints in many portable applications. Lower efficiency due to higher switching frequency is not an issue for chargers as long as the thermal limits are not reached.

Variable-frequency schemes have the disadvantage that the frequency could vary depending on the adapter input voltage, output (battery) voltage, and load-current (charge) conditions. The frequency could drop into or below a critical frequency range, causing noise issues; or it could go up so high that the switching losses are excessive, causing thermal concerns.

Also, worst-case minimum frequencies could occur at minimum load (charge) current, such as when the charge cycle is tapering and nearing termination. This is due to the slow rate at which the output capacitor is discharged. Frequencies could easily fall into the audible frequency range. Sometimes a "dummy" load is required to bleed the minimum-current limit and avoid falling into low-frequency operation. Care must be taken, as this "bleed" resistor is a leakage source that drains the battery when it is not being charged.

V. Overall System-Design Considerations

A. Preventing AC-Adapter-Induced Failure Modes

The use of an AC adapter to power a converter requires consideration of the following items:

- The DC/DC controller must survive an adapter hot-plug event.
- The DC/DC converter application circuit must not affect AC adapter insertion/removal detection.

An adapter hot-plug event can have catastrophic results for the controller IC, depending on the input capacitor used on the system. When an already powered adapter is connected to the system, the input voltage at the adapter connector terminal rises very fast; the adapter cable inductance and series resistance interact with the input filter capacitor and generate an overshoot pulse. For small input-capacitor values, it is not uncommon to see overshoots in excess of 50% of the adapter regulation voltage, as shown in Fig. 32. Increasing

the input capacitor to large values to obtain an underdamped response is not a viable solution, as cost will increase and sparks on the adapter system connector will occur upon connector insertion, causing long-term reliability effects.

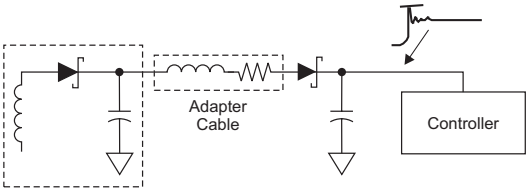


Fig. 32. Supply-line overshoot upon adapter hot-plug insertion.

The only practical solution is to dimension the input capacitor to limit the pulse to reasonable values, below the converter maximum ratings for input voltage. Selecting controllers with high input-voltage ratings will minimize system cost while still enabling design of a robust system.

The simplified topologies shown in section II have the potential problem of biasing the adapter terminal with the battery-pack voltage through the high-side switch back-gate diode when the battery voltage exceeds the adapter voltage. This situation can occur during adapter removal or when DC voltages lower than the pack voltage are used to bias the end equipment (such as car battery lines, airline adapters, etc.).

This parasitic path can hold the voltage at the adapter terminal above the threshold for AC adapter detection, preventing the detection of AC adapter removal and creating the potential for unexpected system behavior.

The condition that has the highest damage potential, however, occurs when one of the simplified circuits in section II is used on systems where the positive terminal of the adapter connector is mechanically shorted to ground upon adapter removal. This will generate a hard short from battery to ground with the current path being provided by the high-side switch back-gate diode, potentially damaging the high-side switch.

The solution discussed in section IV to prevent reverse conduction from the battery to the adapter also takes care of these additional issues.

B. AC Adapter Power Considerations

Most end equipment must maintain normal operation while charging a battery pack. Usually the cost of the AC adapter is directly proportional to the rms current supplied to the system. One of the design targets for the system is to lower the power dissipation of the AC adapter; to do that, usually the adapter voltage is kept as close as possible to the target charge voltage. This approach has an adverse impact on the rms current, as the converter duty cycle will increase as the battery-pack voltage increases. To harmonize these requirements, a new topology was developed with the addition of a third dynamic-power-management (DPM) loop to the standard converter (see Fig. 33). This third loop effectively reduces the charge current when the adapter current limit is reached, effectively adapting the charge-current value to the system load conditions and AC-adapter limits

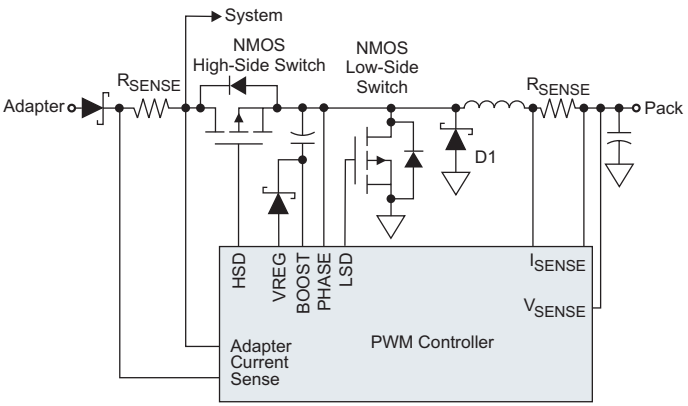


Fig 33. Additional DPM loop.

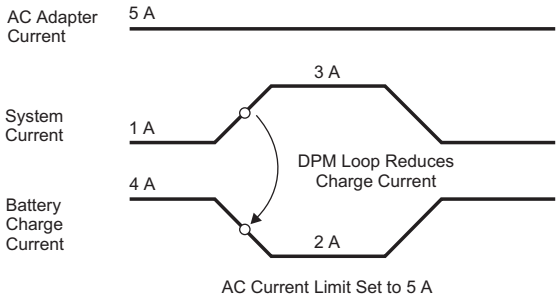


Fig 34. Example of charge-current reduction to accommodate a system load increase.

(see Fig. 34). As a result, the AC adapter cost can be reduced, and simultaneous pack charging and system operation can be achieved.

C. Additional Charger-Startup Issues

Upon initial startup, the error signal generated by the error amplifiers will try to increase the ramp voltage. Some amount of overshoot for the charge current or charge voltage can be expected during power-up if the ramp voltage increases faster than the feedback loop response. To avoid overshoot conditions, a soft-start circuit is usually implemented to decrease the slew rate for the error signal used by the PWM ramp comparator. This methodology guarantees an orderly startup for the system and avoids undesirable ringing or overshoots (see Fig. 35).

The most common topologies use an external capacitor that is charged by a current source; the voltage at the capacitor clamps the PWM ramp-comparator input if it is below the desired regulation point. When the error voltage reaches the regulation point, the soft-start circuit is disabled.

As a general rule, to guarantee that the soft-start circuit is always active when the converter is initially enabled, all the soft-start capacitors must be discharged by a fast-discharge circuit when the converter is disabled.

Another soft-start method is to step up the internal voltage reference that the charge-current regulation loop uses to set the battery charge current.

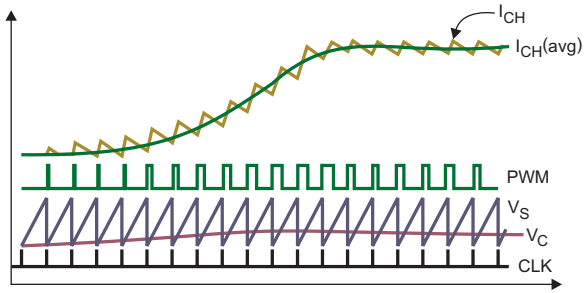


Fig. 35. Soft start ramping up the charge current.

D. Preventing Other Battery-Charger Failure Mechanisms

Failure mechanisms are of special concern when Li-ion packs are being charged. Li-ion packs have internal safety devices to protect against overcurrent and overvoltage conditions; however, it is a recommended practice to include secondary fault-protection functions in Li-ion charging systems for increased reliability and safety. Those functions should end the charge if abnormal conditions are detected; and they can be implemented on either the charge controller or in a power-management IC that monitors the charge process (see Table 1).

TABLE 1. FAULT-PROTECTION FUNCTIONS IN LI-ION CHARGING SYSTEMS

Event	Detection/Action
Charge time exceeds normal charging time	Monitor converter on time; End charge
Battery-pack temperature is out of range	Monitor pack thermistor; End charge
Converter-IC temperature exceeds safe operating range	Monitor converter-IC junction temperature (thermal shutdown); End charge
Charge current exceeds target value while pack is connected	Monitor charge current; End charge
Voltage overshoot occurs at pack removal when charger is on (due to loop delay)	Detect pack removal; End charge
Pack cell or pack terminal is short-circuited; or pack opens, resulting in low pack visible voltage	None; Design PWM loop with ground-compatible common-mode range
High-side switch is damaged due to thermal overload and shorts adapter to pack	Monitor charge current; Add additional on/off switch in series with high-side device to isolate pack from adapter
Overvoltage condition occurs	Detect output voltage above target voltage; End charge

MUST HAVE **OPTIONAL**

Optimizing Low-Power DC/DC Designs – External versus Internal Compensation

Michael Day

ABSTRACT

This topic is a broad discussion of internal and external compensation in switch-mode power supplies. It first explains why compensation is needed, then examines two power-supply designs: one externally compensated and one internally compensated. The differences between external and internal compensation are explained and compared to show which type is appropriate under given conditions. The focus then shifts to the limitations imposed upon an internally compensated power-supply design. Practical considerations of power-supply design are discussed along with ways to optimize the design for specific conditions.

I. INTRODUCTION

Power-supply design has always been considered something of an art, probably because it typically has involved loop compensation and magnetic design. An engineer who specialized in and typically spent most of his time designing power supplies usually also was assigned the task of generating the system power supply. For the most part, this is still true for high-power, offline supplies. However, for lower-power DC/DC converters that run from regulated inputs or batteries, this mode of operation is quickly coming to an end. With fast-paced design schedules and leaner staffing, power-supply design now often is assigned to nonspecialists.

Although power-supply design by nonspecialists is certainly attainable, it becomes more and more difficult as product complexity grows and consumers (and management) demand reduced design-cycle times. The product engineer receives the brunt of these demands. Fortunately, IC manufacturers are making power-supply design quicker and easier for the designer by providing power-supply parts with integrated FETs and internal compensation. The data sheets for these parts provide recommended external components and layout guidelines. In many cases, designing the power supply is reduced to selecting an IC with the appropriate ratings, then picking the external components from a table in the data sheet. While this is often a valid procedure, the power-supply engineer still needs to understand how these ICs operate and what effect the external-component selection has on the operation of the supply.

II. WHY COMPENSATE?

This paper focuses on the synchronous-buck topology, which is the easiest topology to explain and to understand. Fig. 1 shows a simplified block diagram of the voltage-mode-controlled synchronous buck. The designer should consider three

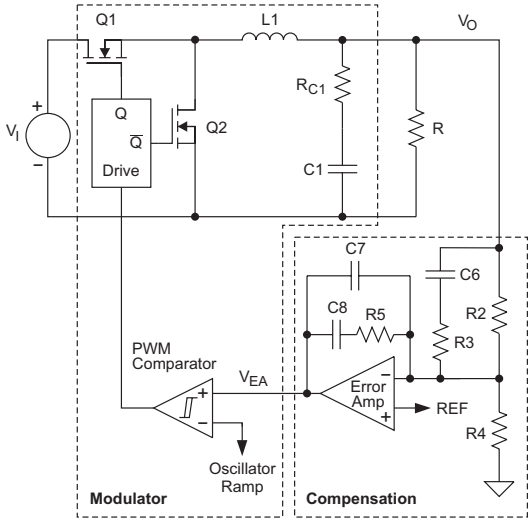


Fig. 1. Voltage-mode control implementation for synchronous buck converter with external pole-zero compensation.

main elements when compensating a power supply: the modulator, the compensation, and the overall response. The modulator gain is a function of the external filter components (C1, RC1, and L1), the input voltage, and the peak-to-peak ramp voltage. The DC portion of the modulator gain, G_{MOD_DC}, is defined as the change in output voltage divided by the change in the error-amplifier voltage. This is clearly demonstrated in Fig. 2. When the output of the error amplifier is below the minimum ramp voltage, the duty cycle is 0%; therefore, the output voltage is 0 V. When the error amplifier is above the peak of the ramp voltage, the duty cycle is 100%; therefore, the output voltage is V_{IN}. Expressed mathematically:

$$G_{MOD\_DC} = \frac{V_{IN}}{\Delta V_{RAMP}}$$

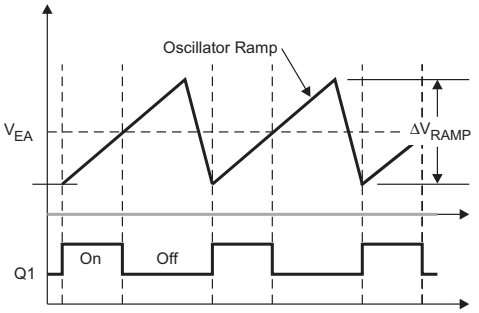


Fig. 2. Modulator operation waveforms.

Ideally, G_{MOD_DC} is independent of frequency or output current.

The AC portion of the modulator gain, G_{MOD_AC}, is simply the transfer function of the LC output filter. This is expressed as:

$$G_{MOD\_AC} = \frac{1 + j \bullet \omega \bullet C1 \bullet R_{C1}}{1 + j \bullet \omega \bullet C1 \bullet R_{C1} + (j \bullet \omega)^2 \bullet L1 \bullet C1}$$

The overall modulator gain, G_{MOD}, is the product of these two terms. Typically, the designer places little thought into the design of the modulator gain. The modulator gain is simply a function of the input voltage and the value of the external filter components that the designer picked in order to meet other system requirements.

Choosing the external filter components to meet the electrical and physical requirements of the supply is only the first step in the design process. Once the power stage is complete, the designer must compensate the power supply to ensure that the overall loop response is stable. Since a typical power supply is not inherently stable, the designer must examine the modulator response carefully and then properly modify this response in order to make the supply stable. The following terms help to define the stability criteria of a power supply:

Gain Margin – The difference between unity gain and the actual power-supply gain at the frequency where the phase reaches 180º.

Phase Margin – The difference between 180º and the actual power-supply phase when the gain reaches 0 dB.

Stability Criteria – A minimum value for both the gain and phase margin of a power supply. In power-supply design, a power supply is typically defined to be stable if the gain margin is greater than 6 dB and the phase margin is greater than 45º. The requirement for stability typically is met if the overall gain crosses 0 dB with a slope of –20 dB/decade.

Fig. 3 shows the gain and phase margin of the modulator response for a typical power supply. Note that this response must be modified, or compensated, in order to make the supply stable. The following power-supply parameters are assumed for this figure:

V_{IN} = 6 V L_{OUT} = 10 µH R_{ESR} = 25 mΩ
V_{RAMP} = 1 V C_{OUT} = 10 µH

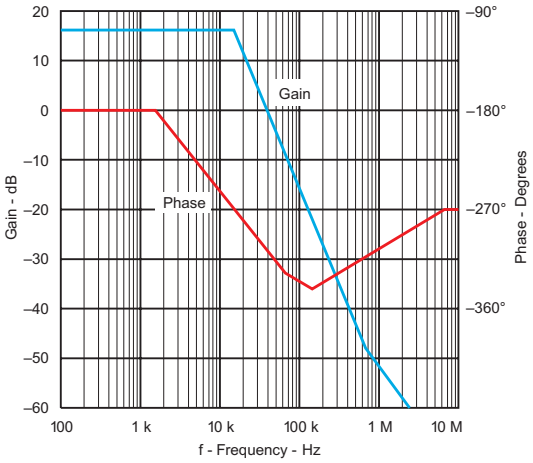


Fig. 3. Bode plot of G_{MOD} showing the gain and phase.

$$G_{MOD\_DC} = \frac{V_{IN}}{\Delta V_{RAMP}} = 6 = 15.5\ dB$$

The pole, f_P of LC, is

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \bullet C_{OUT}}} = 15.9\ kHz$$

The zero, f_Z of the equivalent series resistance (ESR), is

$$f_Z = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} = 636\ kHz$$

Note that the phase margin is only 22º.

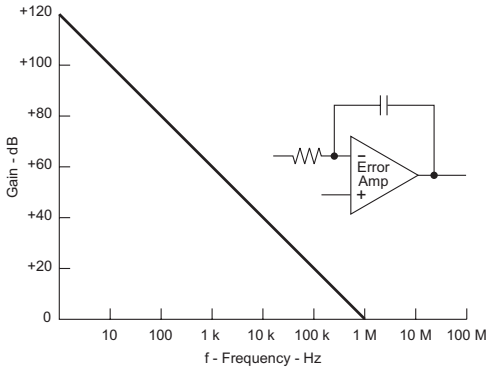
III. Compensation Design Options

We now understand why compensating a power supply is necessary. The next concern is how to do it. Many books have been written that discuss how to compensate a power supply. The focus of this paper is to provide an overview of important compensation factors. In general terms, compensating a power supply can be simplified into graphically adding and subtracting waveforms on a semilog graph. The overall power-supply response is simply the sum of the modulator, G_{MOD}, and the error-amplifier gain, H_{Error_amp}. The sum of the modulator gain and the error-amplifier gain must meet the requirement for stability. Three different types of error-amplifier responses, shown in Fig. 4, are commonly used to compensate power supplies: Type 1, Type 2, and Type 3. A detailed discussion of each can be found in Reference [1].

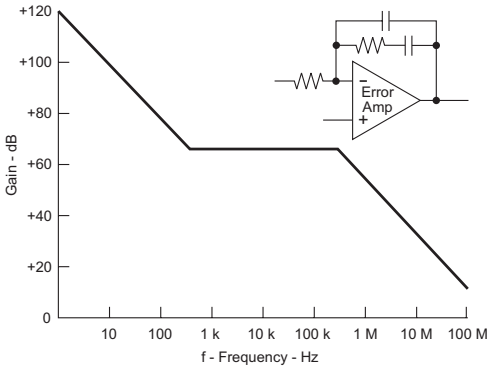
To compensate a power supply, the first step is to graph the response of the modulator, G_{MOD} (shown in Fig. 3). The next step is to draw the desired response of the power supply, G_{Supply}. If the difference between the overall supply gain and the modulator gain ($G_{Supply} - G_{MOD}$) can be made to match either a Type 1, 2, or 3 error-amplifier gain, the supply can be easily compensated.

The following two examples show the design steps for a single power supply used in a typical portable or wall-powered application. The first example is a power-supply controller with external FETs and compensation. The second example uses a fully integrated power-supply IC. The supply requirements for both examples are as follows:

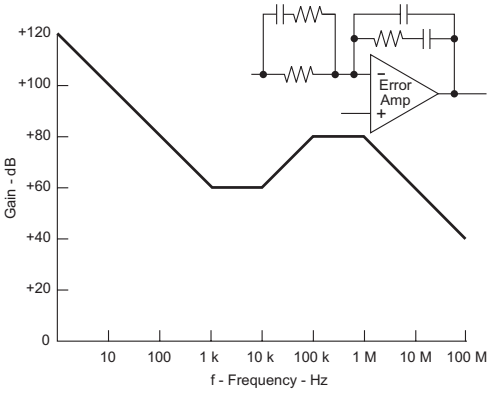
V_{IN} = 3 to 8 V I_{OUT} = 600 mA
V_{OUT} = 1.8 V V_{Ripple} = 25 mV



a. Type 1 compensation.



b. Type 2 compensation.



c. Type 3 compensation.

Fig. 4. Three power-supply compensation schemes.

A. Example 1 – External Compensation Design

- Choose an IC that can meet these requirements.
- Choose an initial switching frequency of 500 kHz. A higher frequency usually results in a smaller power supply with a lower efficiency. A lower frequency usually results in a larger power supply with a higher efficiency.
- Choose an inductor value that sets the maximum ripple current to 20% of the maximum output current. The ripple current can be higher or lower than 20%, but this is a good starting point for a power-supply design. When calculating the output inductor, don't forget to use the lower tolerance of the switching frequency for the chosen IC as well as the maximum input voltage. A larger inductance requires fewer output capacitors to meet the output-voltage-ripple requirements, whereas a smaller inductor may require more capacitors or capacitors with less ESR. Smaller inductors typically provide a better transient response.
- L = 15.6 µH for this example.
- Choose an inductor that meets both the inductance and current requirements.
- Calculate the maximum ESR to meet the 25-mV ripple-voltage requirement.
- R_{ESR} = 30 mΩ maximum for this example.
- Choose an appropriate output capacitor such as a 10-µF ceramic with < 30-mΩ ESR.
- Calculate the voltage ripple due to the output capacitance.
- Repeat the preceding steps until an acceptable design is reached. Several iterations may be needed to optimize the design for size, efficiency, cost, etc.
- With the external filter components defined, calculate the modulator gain.
- Determine the desired overall supply response.
- Calculate the appropriate error-amplifier response, H_{Error_amp}.

When designing for gain and phase margin, the designer has several additional requirements to consider:

- Ensure that variations in input voltage do not cause instability.
- Ensure that the crossover frequency is less than 1/10 of the switching frequency.
- Allow for variations in the peak-to-peak oscillator voltage.
- Ensure that the error amplifier has sufficient attenuation at the switching frequency so it does not amplify the output voltage ripple and cause subharmonic oscillations.
- Ensure that the midfrequency gain is greater than zero to prevent a large overshoot at turn-on and during transient conditions.
- Ensure that the error amplifier has the drive capability to drive the feedback network properly.

Fig. 5 shows a schematic of the final solution with a TPS5103.

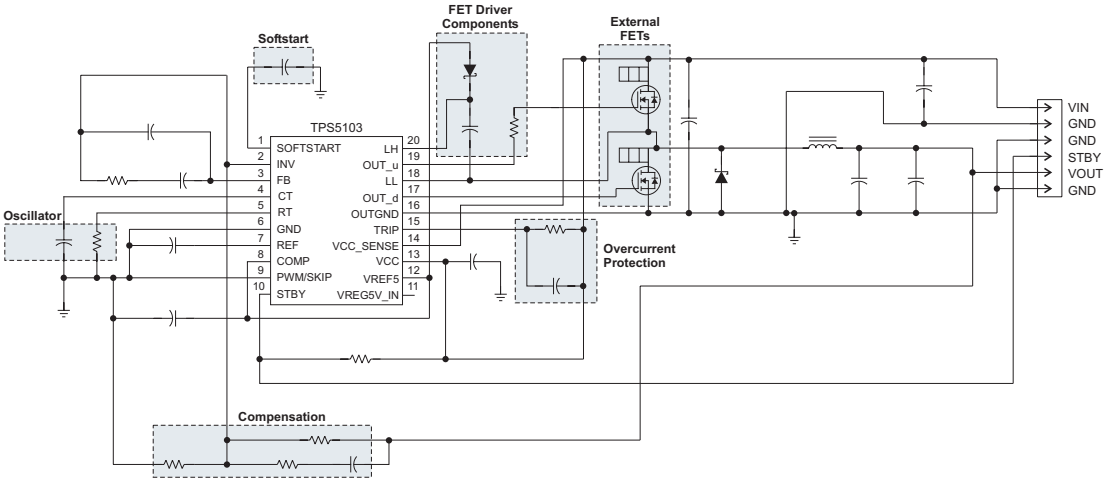


Fig. 5. Schematic of TPS5103 solution.

B. Example 2 – Internal Compensation Design

The design procedure for an internally compensated power supply with integrated FETs is significantly different. It flows as follows.

- Choose an IC that meets the V_{IN}, V_{OUT}, and I_{OUT} requirements.
- Choose an external inductor and capacitor from the list of recommended components in the data sheet.
- Verify that the design meets the ripple requirements.

Fig. 6 shows a schematic of the final solution with an internally compensated power supply.

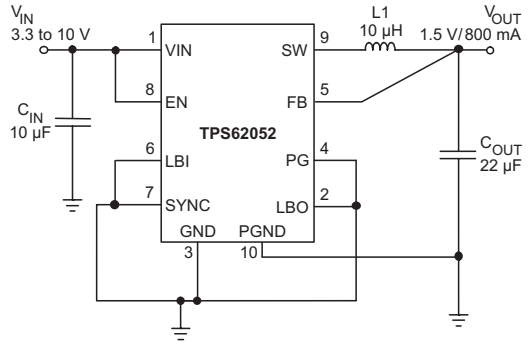


Fig. 6. Integrated TPS62050 solution.

These examples clearly demonstrate that designing a power supply with an internally compensated IC requires less time and power-supply knowledge than designing a power-supply controller with external FETs and compensation.

IV. Limitations on External Components for an Internally Compensated Power Supply

A. Practical Considerations

The foregoing examples show that the designer has full control over all aspects of the power-supply design. Freedom to optimize the supply for size, efficiency, transient response, etc., permits free choice of component values, types, and sizes. With external compensation, the designer chooses the external filter components first and then tailors the compensation around these components. The design procedure is reversed with internal compensation. The compensation is fixed first, so the designer must choose external filter components that result in a stable design. The range of external filter components is limited, and choosing components outside the recommended data sheet range can lead to an unstable design.

The cause for this limitation begins in the IC design phase. The IC design process typically follows the same procedure as that of an externally designed power supply. The designer begins with a target specification and then designs the IC to meet it. This process involves choosing appropriate values for the switching frequency, internal FET characteristics, and external filter components. At this point, just as with a standard power-supply design, the designer shapes the error-amplifier response to compensate the supply properly with the choice of external components. The error-amplifier response becomes a fixed, integral part of the IC. Because of this, the choice of external filter component values is limited to those that are compensated properly by the error amplifier. The IC data sheet provides acceptable component values that result in an optimal power-supply response.

In most cases, choosing the recommended component values for an internally compensated power supply provides an acceptable solution. However, there are times when the solution may need to be optimized. With an internally compensated power supply with integrated FETs, the designer has control over only the external filter, which severely restricts freedom to optimize the supply. Even with this restriction, the savvy power-supply designer can stray from the recommended component values in an attempt to optimize critical system parameters such as transient response, size, and efficiency. The key to accomplishing this safely is to understand the limitations and implications of the choices.

B. Stability

Obviously, the first and main consideration for modifying the external filter components is stability. The filter values and sizes can be made larger or smaller, but they must still meet the criteria for stability. Since most data sheets do not provide detailed information on the poles and zeroes of an internally compensated device, the designer is left with the question, “What component values guarantee stability?” In the

absence of any other information, the designer can simply keep the LC filter pole equal to that of the recommended components.

As an example, let's look at the TPS62200. This IC was designed for and the data sheet recommends a 10-µH and 10-µF output filter combination. This LC filter provides a double pole at 15.9 kHz. Clearly, the small signal response of the overall supply remains constant as long as the LC filter pole is fixed at 15.9 kHz. This means the inductor value can be reduced by a factor of two as long as the capacitance is increased by a factor of two. The designer has even more flexibility if he knows the response of the IC. Fig. 7 shows an idealized Bode plot of the internal compensation along with the response of the recommended filter components.

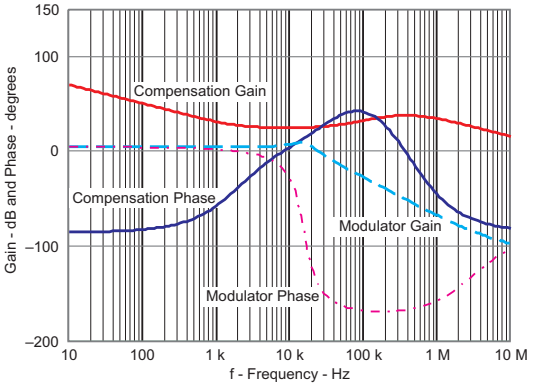


Fig. 7a. Compensation and filter response of an internally compensated power-supply IC.

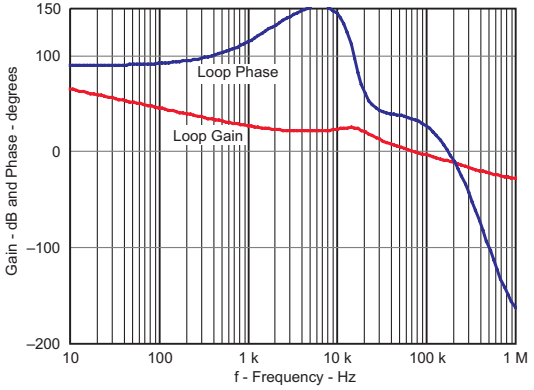


Fig. 7b. Overall power-supply response with the recommended 10-µH and 10-µF output filter.

Careful examination of Fig. 7 reveals that the criterion for stability is met if the resonant pole of the external filter components is kept less than 24 kHz. Don't forget to take the component tolerance into account when calculating the resonant pole. Table 1 shows several acceptable and unacceptable output filter combinations. Note that although a 10-µH and 4.7-µF pole is an acceptable 23.2 kHz, this combination is not acceptable when you include a 20% tolerance on these values. The transient response of a *stable* design with a 10-µH and 10-µF output filter is shown in Fig. 8. The transient response of an *unstable* design with a 4.7-µH and 10-µF output filter is shown in Fig. 9. These two figures confirm our analysis of Fig. 7.

TABLE 1. OUTPUT FILTER COMBINATIONS

L (µH)	C (µF)	Pole (kHz)	Pole with 20% Tolerance (kHz)	Result
10	4.7	23.2	29.0	Unstable
15	4.7	19.0	23.7	Marginally stable
22	4.7	15.7	19.6	Stable
10	10	15.9	19.9	Stable
6.8	10	19.3	24.1	Marginally stable
4.7	10	23.2	29.0	Unstable
2.2	22	22.9	28.6	Unstable
4.7	22	15.7	19.6	Stable
6.8	22	13.0	16.3	Stable

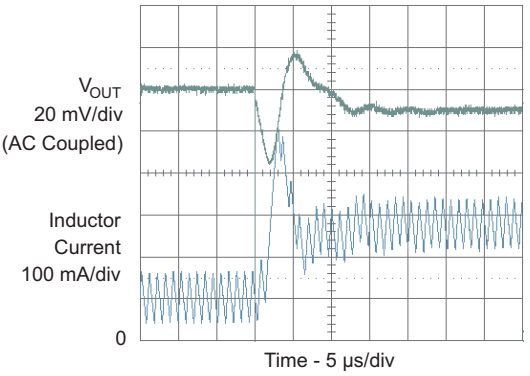


Fig. 8. Transient response of stable, internally compensated power supply with 10-µH and 10-µF output filter.

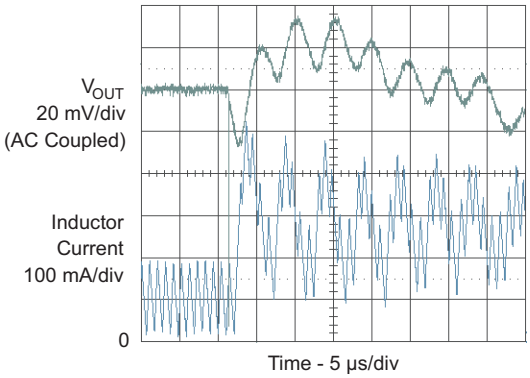


Fig. 9. Transient response of unstable, internally compensated power supply with 4.7-µH and 10-µF output filter.

C. Inductor Saturation

In portable power, size is often critical. Typical application circuits in a data sheet are often just that, typical. These circuits can be modified to optimize size. The filter inductor is often the first thing that designers consider to reduce size. If two inductors with equal inductance are compared, the physically smaller inductor usually has a higher winding resistance. The smaller inductor results in a smaller solution but also results in lower supply efficiency. Fig. 10 shows an example of the reduction in efficiency versus decreased inductor size.

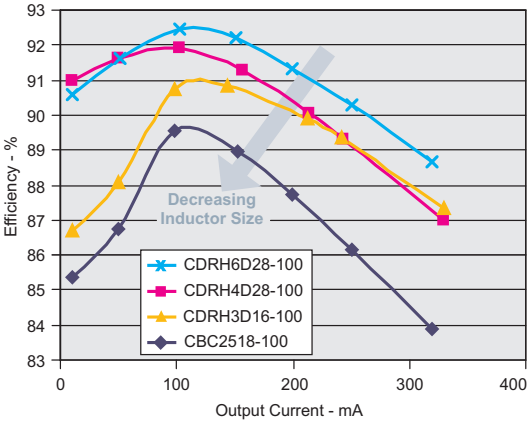


Fig. 10. Reduction in efficiency versus decreased inductor size.

Choosing a smaller inductor with the same inductance value is an easy way to reduce the supply area without having to worry about stability concerns. However, be aware that a smaller inductor has a lower saturation current. During load transients, the inductor current may reach the maximum current allowed by the IC. The inductor must be able to handle this current without saturating. Fig. 11 shows the inductor current during a transient condition. As the inductor current approaches the maximum switch current limit, it begins to enter saturation. Monitoring the inductor current is an easy way to determine whether or not it is saturating. If saturation starts to occur, the inductor current will become nonlinear and start to rise as shown in Fig. 11.

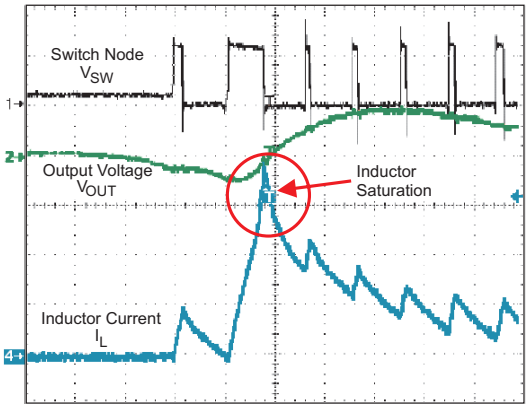


Fig. 11. Transient response with inductor current entering saturation.

D. Current Limit

In an attempt to reduce component size while maintaining high efficiency, many designers choose a lower inductor value when they move to a smaller footprint part. Table 1 shows that a smaller 4.7-µH output inductor is an acceptable choice as long as the output capacitance is increased to keep the resonant pole at an acceptable frequency. At first glance, this solution appears to work. However, keep in mind that the external filter components are limited by IC parameters other than stability. One IC parameter that limits component selection is the peak-current limit. In our example, the device is guaranteed to provide 300 mA of output current under all

conditions when the recommended components are used. A smaller inductor value actually reduces the maximum output current from the IC. Fig. 12 helps illustrate how the inductor value affects the maximum output current from a power supply. The triangular waveform is the inductor current. I_{SW_Limit} is the guaranteed minimum MOSFET current limit in the IC, 380 mA for the TPS62200. The supply's maximum output current is reached when the peak inductor current reaches the MOSFET current limit. Defined mathematically:

$$I_{OUT\_max} = I_{SW\_Limit} - \frac{\Delta I}{2}$$

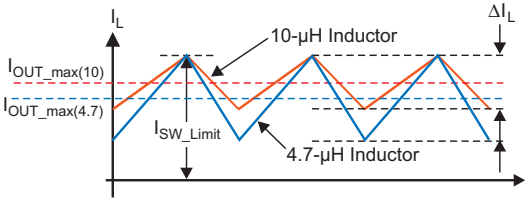


Fig. 12. Effects of inductor on output current.

A smaller inductance results in a larger ripple current, which reduces the maximum possible output current. For example, assuming the following operating parameters, the maximum output current of 300 mA is guaranteed: V_{IN} = 5 V, V_{OUT} = 1.5 V, f_{SW} = 1 MHz, I_{SW_Limit} = 380 mA, and L = 10 µH. Under these conditions, the inductor ripple current is 100 mA, so the maximum output current is 380 mA – 100 mA/2 = 330 mA. If a 4.7-µH inductor is used, the ripple current increases to 224 mA, and the guaranteed output current drops to 268 mA. Likewise, a larger inductor can be used to increase the guaranteed output current of a supply.

E. Transient Response

The output filter also can be modified to improve transient response. The impedance of the output filter is given by:

$$Z_{Filter} = \sqrt{\frac{L}{C}}$$

The lower the filter output impedance, the better the transient response. Reducing the inductance or increasing the capacitance lowers the filter impedance. Fig. 13 shows the transient response with a 10-µH and 10-µF filter. Fig. 14 shows the transient response with a 10-µH and 22-µF filter. Fig. 15 shows the transient response to reducing the impedance even further with a 4.7-µH and 22-µF filter.

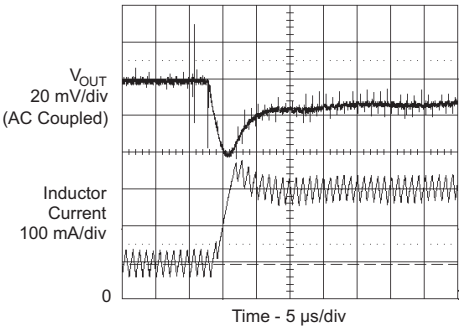


Fig. 13. Transient response with a 10-µH and 10-µF filter.

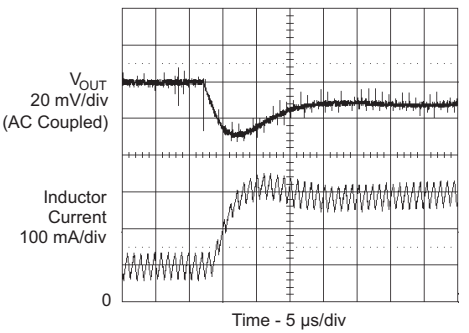


Fig. 14. Transient response with a 10-µH and 22-µF filter.

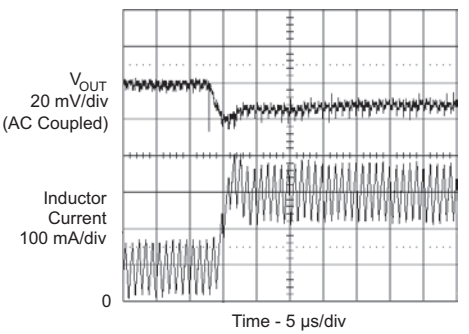


Fig. 15. Transient response with a 4.7-µH and 22-µF filter.

F. Total Solution Size

Internal compensation integrates the discrete components required to shape the error amplifier. With lower-power outputs, this integration provides a smaller overall power-supply solution by eliminating the discrete resistors and capacitors required for compensation. With low-power outputs, the board area required for the three resistors and three capacitors necessary for a Type 3 compensation network easily can be as large as, or larger than, the output filter. For portable applications, integrating these components provides a sizable reduction in supply area; however, this reduction diminishes with larger-power outputs.

As output currents exceed 3, 4, and even 5 A, the size of the compensation network becomes insignificant compared to the supply's increased filter area. Under these conditions, an internally compensated supply actually can result in a larger solution when the compensation is not designed for the minimum filter size. The selection of filter components is restricted and the filter cannot be optimized. Internally compensated supplies in the 5-A range typically are designed for large tantalum or aluminum output capacitors. The ESR of these capacitors is used to help compensate the power supply. Migrating to an externally compensated design actually can provide a smaller overall solution under these conditions. The external compensation allows the designer to optimize the filter inductor and possibly to use smaller ceramic output capacitors.

Let's compare the solution sizes of two power supplies designed to meet the same specifications. The requirements are V_{IN} = 5 V and V_{OUT} = 3.3 V at 5 A. The first supply is designed with an internally compensated IC. The second supply is designed with the externally compensated version of the same family of ICs. Figs. 16a and 16b show the two schematics. Fig. 17 compares the layout of these two designs. The externally compensated design is 20% smaller.

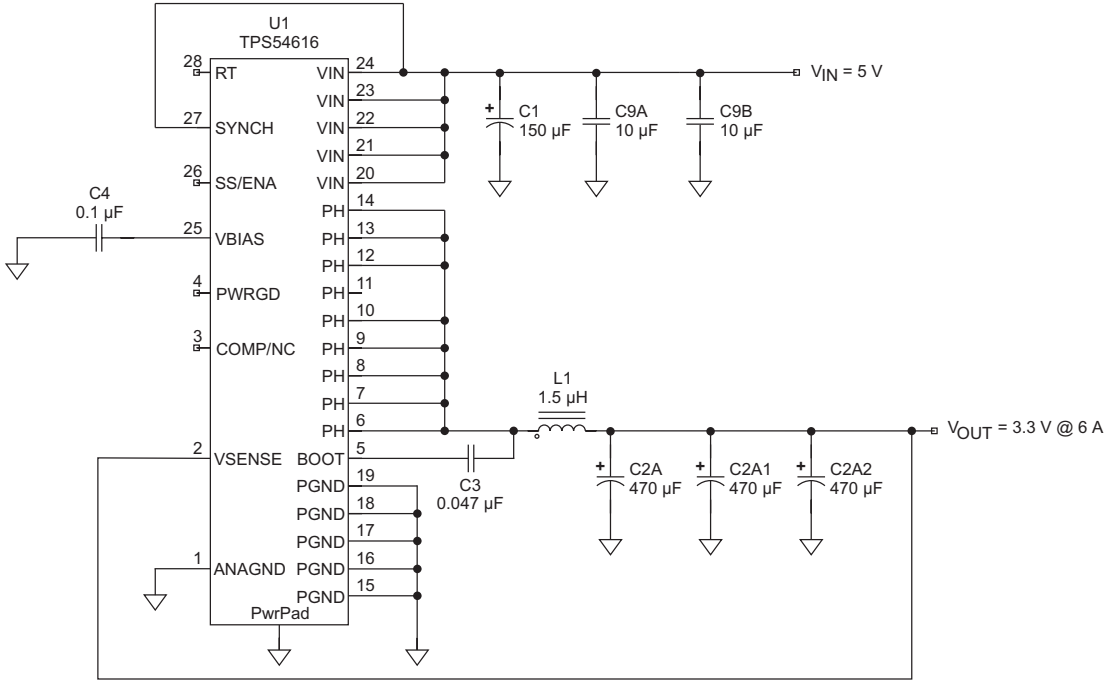


Fig. 16a. Typical supply with internal compensation.

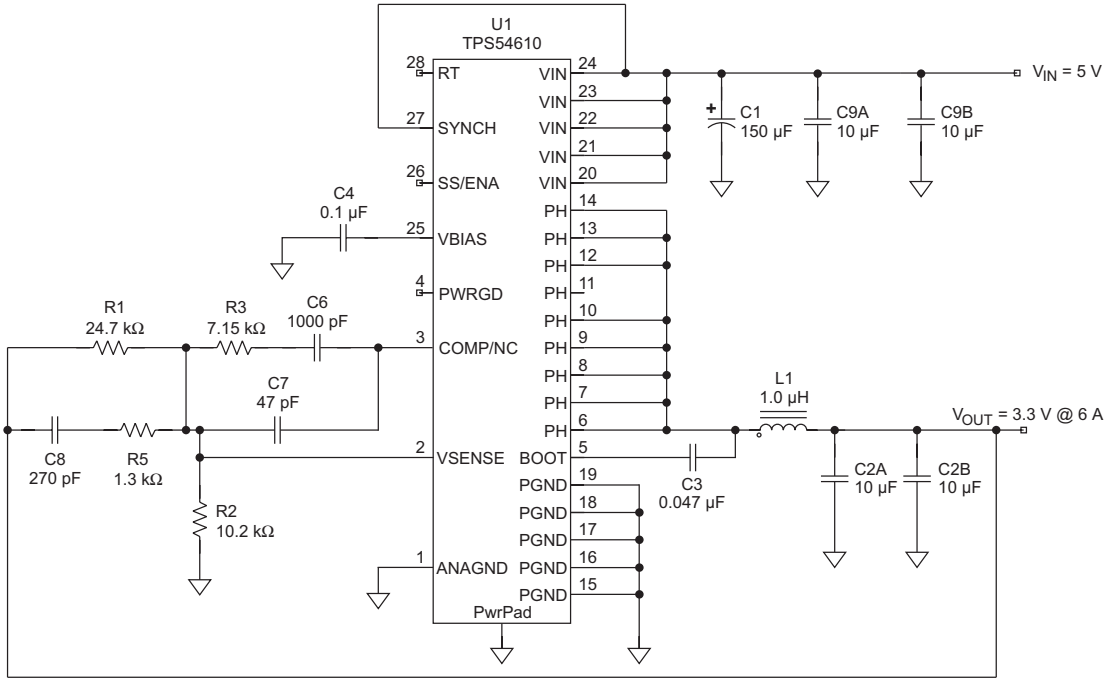
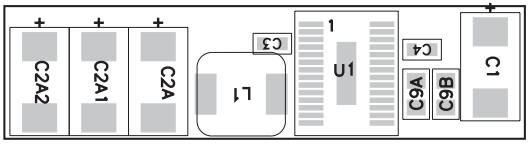
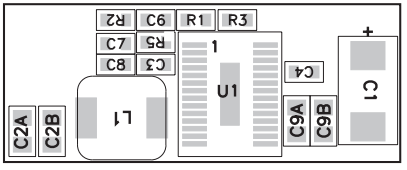


Fig. 16b. Typical supply with external compensation.



a. Internal compensation (1.750 × 0.45 in).



b. External compensation (1.200 × 0.525 in).

Fig. 17. Board layout example.

V. Summary

We have examined a basic buck-topology power supply and identified the need for some type of compensation. The example design steps for compensating a power supply showed that internal compensation reduces design time and complexity. With internally compensated ICs, designing the power supply often is reduced to selecting external filter components from tables in the data sheet. The range of external filter components in these tables is restricted because the filter response must match the compensation in the IC. However, with an understanding of the limitations and restrictions that the IC places on the filter, one can stray from the recommended components in the data sheet to optimize the supply for size, efficiency, or transient response.

We have also examined how low-power output supplies typically require less board space when internally compensated, while higher-power output supplies are typically smaller when externally compensated because the filter can be optimized before the compensation is designed. The benefits of internal compensation for low-power, portable supply design is evident.

VI. Reference

[1] Abraham Pressman, *Switching Power Supply Design* (McGraw-Hill Inc., 1991)

Noise Management in Portable RF Systems

Ray Crampton, Dennis Hudgins, and Dave Heisley

ABSTRACT

The evolution of battery-powered, handheld RF equipment has demanded ever-increasing battery life, which translates into higher efficiency requirements in the power supply. In some designs these efficiency improvements have been achieved by migrating from linear to switching supplies. Highly efficient state-of-the-art modulation schemes place stringent requirements on distortion and adjacent channel interference, which mandates that careful attention be paid to all noise sources, particularly those that are conducted throughout the power-supply system. This topic discusses noise generation and suppression in switched-mode and linear regulators as well as techniques to manage noise in portable battery-powered RF systems.

I. INTRODUCTION

A representative block diagram of a portable, battery-powered RF system is shown in Fig. 1. A number of potential noise sources are present: switched-mode power supplies; an AC power source; baseband and RF oscillators, amplifiers, and modulators; linear regulators; and interference from external sources. There are three ways that noise couples into other circuitry: electromagnetic coupling through the air and circuit-board dielectric, conduction through circuit-board traces and components, and conduction through the ground plane. If these noise sources sufficiently couple into the signal chain, they can cause unwanted interference, possibly enough to fail FCC regulations.

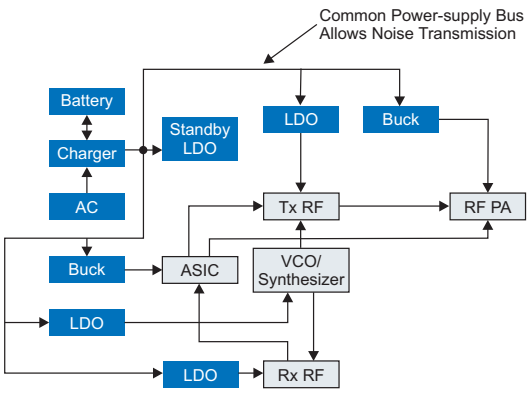


Fig. 1. Typical battery-powered RF system block diagram.

II. SOURCE IMPEDANCE

The source impedance of a freshly charged battery is typically very low. Some other power sources such as a partially discharged battery, a wall adapter, or a battery charger can result in higher source impedances. Long circuit-board traces, vias, and interconnecting wires also increase source impedance. The resistive part of source impedance causes ripple at its output due to the effective degradation of load regulation of the supply. The inductive part of source impedance causes voltage spikes on the power-supply line when load transients occur. This inductance can cause high voltage spikes at the input to power-supply integrated circuits (ICs), possibly exceeding safe operating levels. Due to these effects, source impedance can be a source of unwanted supply noise to the entire system. Voltage ripple (V_{RIPPLE}) due to a series trace resistance (R_{TRACE}) and a switched-supply current ripple (I_{RIPPLE}) is easily calculated as:

$$V_{RIPPLE} = R_{TRACE} \cdot I_{RIPPLE} \quad (1)$$

The input current (I_{RIPPLE}) waveform to a buck converter looks like a square wave from zero current to I_{LOAD} plus half of the small-inductor current ripple (I_L):

$$I_{RIPPLE} = I_{LOAD} + (1/2)I_L \approx I_{LOAD} \quad (2)$$

A series R_{TRACE} of 100 mΩ and an I_{LOAD} of 500 mA results in a 50-mV peak-to-peak ripple. Switching noise on the input power supply can be

greatly reduced by placing bypass capacitors at the input of switching regulators.

III. Buck and Boost Converter Topology Review

Switched-mode regulators are very efficient at converting one DC voltage to another because they use "lossless" components to achieve voltage conversion. These regulators also have several sources of noise that can be radiated and conducted throughout other circuitry. The buck regulator shown in Fig. 2 has several such sources: a ripple current in the inductor L, a current waveform at the input to the switch, equivalent series inductance (ESL) and equivalent series resistance (ESR) of C_{IN} and C_{OUT}, and the switching waveforms driving the gate of the switch. An understanding of these noise sources and design techniques to mitigate them are essential to good power-supply design for noise-sensitive applications.

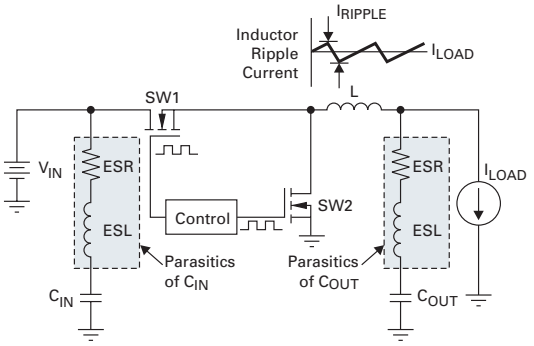


Fig. 2. Buck converter schematic.

A. Charge/Discharge of Switch Gates

Voltage and current waveforms that are present when the gates of the switches are being charged and discharged can be a significant source of noise. Peak-to-peak amplitudes can be multiple volts with sharp rising and falling edges and with ringing present after each switch transition. The current and voltage waveforms depend primarily on gate drive capability, gate parasitic capacitance and resistance, and control-loop methodology and compensation. If external switches are employed, lower C_{GS} and higher R_G reduce noise at the expense of $R_{DS(ON)}$ and efficiency.

B. Ringing at the Switch Node

For both integrated and external switches, ringing can be seen at the node common to the switches and inductor due to the tank circuit formed by the inductor and stray capacitances on this node. A snubber circuit (shown in Fig. 3) can be used to absorb this energy and reduces ringing at the expense of efficiency.

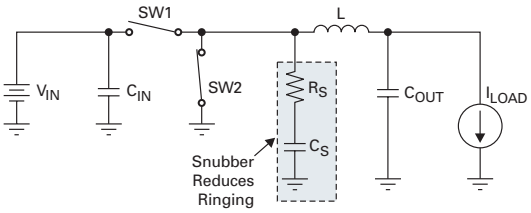


Fig. 3. Snubber used to reduce ringing at the switch node.

C. Switched Inductor Current

The AC current waveform in the inductor causes a changing electromagnetic field in its vicinity. This field can be coupled to nearby traces, components, and the ground plane, causing small voltage perturbations that appear as noise at the switching frequency and its harmonics. The amplitude of coupled voltage in a buck converter is dependent on inductor construction, peak-to-peak inductor current ripple, frequency components of the inductor current slope, and physical layout design. Shielded inductors are manufactured for switching converters to contain the inductor fields, possibly at the expense of efficiency, cost, and component size. Attention should be paid to these fields during board-layout design to prevent the fields from coupling to critical nearby lines. If layout constraints require that traces be run very near traces or inductors with these switching currents, it is generally preferred to make these DC traces so that bypass capacitors can be added to the coupled lines to reduce noise voltage. In addition, surrounding the inductor and switch nodes with ground planes is good practice.

D. Output Capacitor Selection and Load Transients

Load transients can cause output voltage ripple that can be a source of noise to loads that share a common supply bus. If the output of each converter

is treated as a source with some impedance connected to a supply bus, placing bypass capacitors near each load can greatly reduce this noise on the supply bus. Fig. 4 shows the behavior of a typical buck converter during a load transient. The top part of the figure shows the load-current transient and the resultant inductor-current waveform. The bottom waveform is the output voltage response.

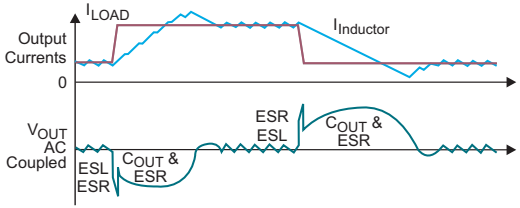


Fig. 4. Load-transient response in a typical buck converter.[1]

The initial undershoot spike is dependent on the load-transient magnitude, slew rate, and the ESL and ESR of the output capacitor. This undershoot can be minimized by use of large-value, low-ESL and low-ESR output capacitors.

The undershoot after the initial spike results from the time it takes for the inductor average current to catch up to the new load current. The amount and duration of this undershoot depend on the inductor value being used and on the IC switching frequency and feedback control loop characteristics. The current increase per switching cycle is inversely proportional to the inductor value, so small inductors improve load-transient response.

When this undershoot has been overcome, the inductor current may have overshot the average load current, resulting in a slight output-voltage overshoot. A negative-going load transient has very similar characteristics. While the undershoot in the positive transient is dependent on both the input and output voltage, the negative transient overshoot is dependent only on output voltage. A bulk-storage tantalum capacitor is needed when load transient di/dt can be large compared to the slope of inductor current $[(V_{IN}/V_{OUT})/L]$.

The filter formed by the inductor and output capacitor of a buck converter filters noise conducted from the input supply rail or resulting from switching waveforms in the regulator. A high-quality ceramic capacitor can be effective in bypassing both switching and broadband noise, while a bulk tantalum capacitor helps with the relatively slower load transients.

E. Frequency-Synchronized and Phase-Offset Supplies

When multiple switching supplies are used in a system, they can be synchronized to a common clock frequency to avoid filtering multiple clock frequencies. Clocks can be phase-offset so that only one switcher draws current from the supply at a time. This reduces the peak load currents and therefore the voltage ripple on the common supply; it also reduces the capacitance needed on the supply source for a given ripple.

F. Power-Savings Modes

Many modern switching regulators offer power-savings modes, typically pulse-skipping or frequency-reduction modes for when light load currents are present. In pulse-skipping mode, the inductor current is allowed to decay and remain at zero until the output voltage falls below tolerance. Then a number of switching cycles are performed to bring the output voltage to its upper tolerance. This cycle repeats and results in the waveforms shown in Fig. 5. One benefit of this power-savings approach is that switching noise frequency is constant; although a new, lower switching frequency is introduced due to pulse skipping.

In frequency-reduction mode, the switching frequency is reduced significantly to improve efficiency. This has the disadvantage of creating a wide spectrum of noise that is more difficult to filter.

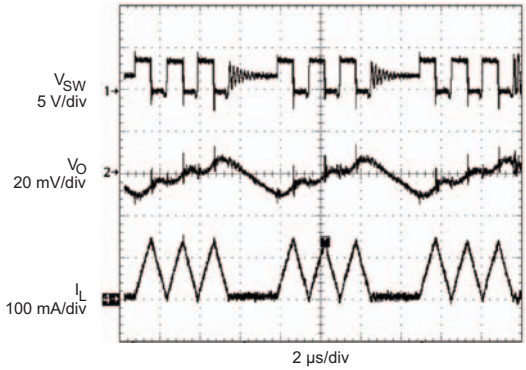


Fig. 5. Ringing at switch node in buck converter without a snubber.[2]

G. *Layout Considerations*

The schematic of a buck converter is shown in Fig. 6. Connections that are sensitive to layout are highlighted with bold lines. The following guidelines apply to the layout of this circuit and are illustrated by the layout shown in Fig. 7:

- **C_{IN}** – A low-ESR and low-ESL capacitor of high value is desired for C_{IN}. Effective ESR and ESL include traces and vias connecting the capacitor to the supply line and to ground, which includes the ground return current path. C_{IN} should be located physically close to the IC to provide the lowest source impedance possible.
- **L1** – Long traces connecting to L1 increase the amount of radiated energy. These traces should be kept as short as is practical.
- **C_{OUT}** – As with C_{IN}, trace and via impedances to the source and ground add to the ESR and ESL of this capacitor. Low ESR and ESL minimize output voltage ripple from charge being injected and removed from this capacitor. Higher values for C_{OUT} also improve output voltage ripple by minimizing changes in output voltage that are due to increasing or decreasing stored charge in the capacitor.

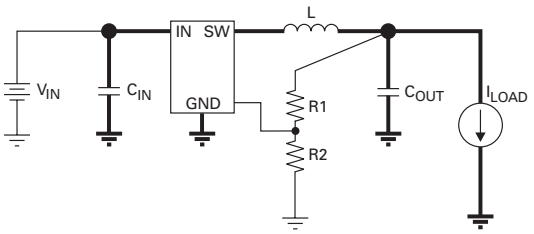


Fig. 6. Buck converter schematic. Bold lines show critical layout areas.

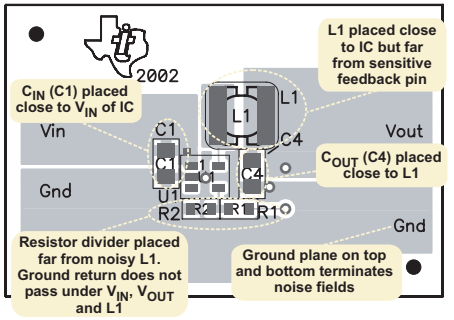


Fig. 7. Compact buck converter layout optimized for performance and noise.[3]

- **Tap point** – The tap for the feedback pin should be taken close to the load rather than closer to the inductor L1. This improves load regulation by taking into account trace resistance between L1 and the load. The tap point is also isolated from switching noise by physical location and the ground plane.
- **IC ground connection** – The ground connection for the IC should have a very low impedance. This is accomplished by having a short return path to the input supply of the device.
- **Tight layout** – In general, tighter layouts that reduce any line lengths that carry AC voltage or current waveforms will reduce radiated noise.

IV. Low-Dropout (LDO) Linear Regulator Overview

LDO linear voltage regulators, while generally being less efficient than switching supplies, have significant advantages in noise suppression and generation. A typical block diagram of an LDO is shown in Fig. 8. The bandgap provides a voltage reference that is stable with supply, temperature, and process variations. This voltage is compared with a sample of the output voltage, and the error amplifier modulates the series resistance of the pass transistor to maintain a constant output voltage under all conditions. A noise-reduction (NR) or bypass pin is typically included on low-noise LDOs to suppress noise generated by the on-chip bandgap. Due to the improved noise suppression properties of LDOs, power-supply designers often use them to filter noise from switching supplies or other noisy

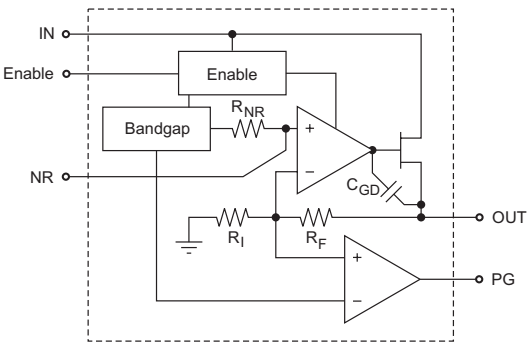


Fig. 8. Simplified LDO block diagram.

supply sources. LDOs also may be preferred for applications that need fast load-transient response.

A. Noise Generation by LDO Regulators

The dominant noise source in LDOs results from shot noise in the bandgap and is related to $V_T \bullet \ln(N)$, where V_T is the thermal voltage and N is the ratio of the area of two transistors used in a bandgap. This is a broadband white-noise source roughly proportional to $1/\sqrt{I_C}$, so LDO designers can reduce the amount of noise by increasing the current consumed by the bandgap. Bandgap noise also can be reduced if an NR (bypass) pin is present on the LDO as shown in Fig. 8. An external capacitor connected to this pin creates a pole in the broadband noise spectrum of the reference. The time constant of this pole is determined by $Z_{NR} \bullet C_{NR}$, where Z_{NR} is R_{NR} plus the output impedance of the bandgap; and C_{NR} is the bypass capacitor value.

Power-supply designers should pay careful attention to the effects of C_{NR} on start-up time. Low-current bandgaps are often used in LDOs designed for battery-powered equipment, so it may take several milliseconds to charge an external capacitor, significantly slowing start-up time. Some LDO regulators mitigate this effect by using a quick-start circuit to increase the current drive of the bandgap output. The output capacitor is also an important factor in bypassing output noise. Fig. 9 shows the effects of C_{OUT} and C_{NR} on output noise.

The following relationship shows the impact of output voltage on output noise:

$$V_{N(OUT)} \cong V_{N(BG)} \bullet (V_{OUT}/V_{BG}) \quad (3)$$

where $V_{N(OUT)}$ is the output noise voltage, $V_{N(BG)}$ is the bandgap noise voltage, V_{OUT} is the regulator output voltage, and V_{BG} is the bandgap voltage. It is easily seen that, when output noise specifications on LDO data sheets are compared, they should be scaled to a common output voltage for proper comparison.

Designers must be careful when comparing output noise on LDO data sheets. Few data sheets present noise characterization under identical conditions. The conditions for output voltage, output current, output capacitance, C_{NR}, input voltage, and frequency range must all be the same in order to compare the noise of one LDO to another. To emphasize the importance of frequency range, for pure white noise the amount of noise between 10 Hz and 50 kHz is the same as between 50.01 kHz to 100 kHz.

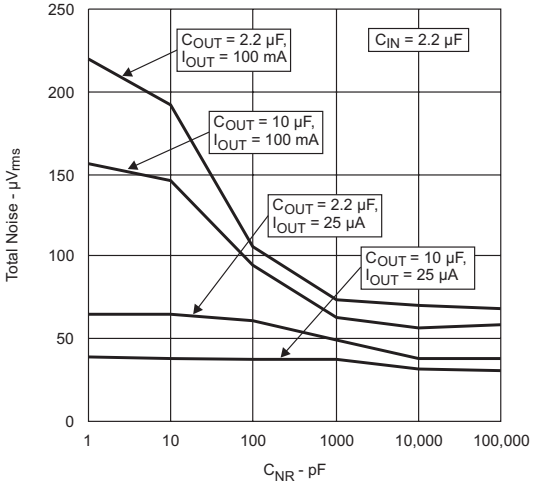


Fig. 9. Output noise as a function of C_{NR}.[4]

It is also important to study the noise spectral curves to determine if noise in critical bands is within acceptable limits. For example, noise within the bandwidth of a PLL is rejected by the effective PLL gain. Noise outside this band will show up at the output.

Designing low-noise power supplies with LDO regulators is not difficult as long as careful attention is paid to characterization conditions, the noise spectrum as it pertains to a specific design, and the choice of C_{OUT} and C_{NR}.

B. LDO Power-Supply Rejection

A relatively high power-supply rejection ratio (PSRR) is often the most important attribute of LDO regulators. PSRR at low frequencies is determined almost solely by the error amplifier loop gain. This is also demonstrated as better DC accuracy over input-voltage and load-current variations. Rejection of typical switching-supply frequencies (50 to 100 kHz) up to 50 dB can be achieved with an LDO if good design practices are followed. This higher-frequency PSRR can be

thought of as a function of the low-pass filter action of Z_{OUT} (output impedance) and Z_{IO} (input to output impedance) as shown in Fig. 10.

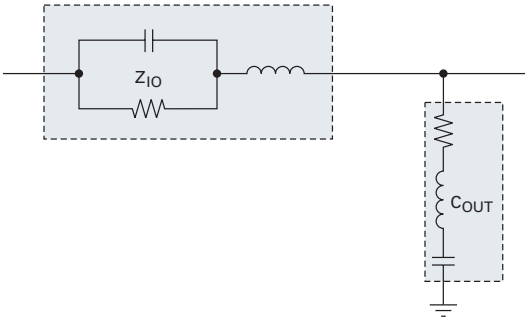


Fig. 10. Schematic of low-pass filter composed of Z_{OUT} and Z_{IO}.

To increase PSRR, Z_{OUT} can be reduced and Z_{IO} can be increased. Z_{OUT} is determined by:

$$Z_{OUT} = Z_{C_{OUT}} // Z_{O(LDO)} \quad (4)$$

where $Z_{O(LDO)}$ is the output impedance of the LDO and C_{OUT} is the output capacitor or combination of capacitors. $Z_{O(LDO)}$ and Z_{IO} are determined by the internal IC design if the pass transistor is integrated, and they are affected by the external pass transistor of LDO controllers. The following effects can be seen in LDOs whether the pass transistor is integrated or external:

- **Effective resistance of the pass element** – At light load currents the pass transistor resistance is relatively high, increasing Z_{IO} and improving PSRR. At high load currents the resistance is lower, decreasing PSRR.
- **Configuration of the pass element** – The common source topology of P-type pass transistors causes an out-of-phase relationship between the control node and the regulator output. In this case, parasitic capacitance from the regulator input to the control node can work in favor of PSRR due to the canceling effect of the control-to-output phase relationship if the transistor gain is > 1.0. In an N-type configuration, the common-collector topology gives a gain of about 1 from the control node to the output, so noise coupled from the regulator input to the control node passes directly to the regulator output.
- **Parasitic C_{GD} of the pass element** – In both P- and N-type topologies, the voltage gain from gate to source is unity, so the parasitic capacitance from gate to drain passes ripple voltage from the input to the output.
- **Parasitic C_{DS} of the pass element** – In both P- and N-type topologies, C_{DS} can be an important part of the Z_{IO} impedance. This parasitic capacitance passes ripple voltage from the input to the output.
- **PSRR as a function of $V_{IN} - V_{OUT}$** – Since $V_{DS} = V_{IN} - V_{OUT}$, the pass element has higher gain at higher $V_{IN} - V_{OUT}$, giving better supply rejection as shown in Fig. 11. If the LDO is to be used in or near dropout (usually at low battery voltages), this effect should be considered.

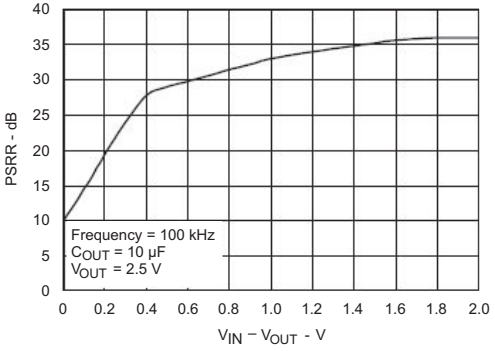


Fig. 11. PSRR vs. $V_{IN} - V_{OUT}$.[5]

Output capacitor selection is also critical to high-frequency power-supply rejection. Low-ESR, low-ESL capacitors give optimal results. Higher-value capacitors also improve PSRR if ESR and ESL are not significantly compromised. High-frequency rejection can be significantly affected by the resonant frequency of C_{OUT}. In Fig. 12 the peaks in rejection at 500 kHz are caused by the 10-µF output capacitor. Changing the output capacitor value can move these peaks up and down in frequency; but variations due to layout, capacitance, and ESL should be taken into account.

Using data sheets to compare the PSRR of two LDOs is often not possible since there is no standard for measurement conditions. PSRR can be significantly affected by $V_{IN} - V_{OUT}$, I_{OUT}, C_{OUT},

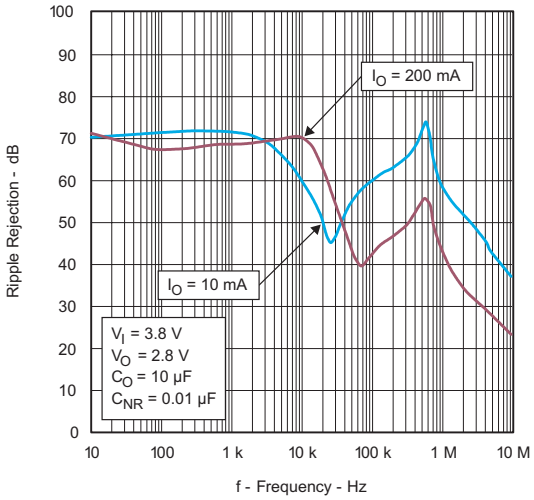


Fig. 12. Ripple rejection vs. frequency, showing peaks due to C_{OUT} resonance.[4]

C_{NR}, and I_{OUT}, so care must be made when specifications from different data sheets are compared.

C. LDO Load-Transient Response

Load-transient response of LDOs is typically very good compared to switching regulators. This improved transient response results in lower output-voltage ripple propagating through the output bus. In pulsed applications or applications requiring fast start-up times, LDOs can provide an excellent solution.

When load current changes rapidly, the pass transistor must change its resistance quickly to prevent the output voltage from changing. The transistor resistance is changed by the error amplifier that drives its gate. The speed at which this occurs is dependent on several factors in the IC design:

- **Control-loop bandwidth** – The regulator can respond only as quickly as the control loop can respond. The higher the loop bandwidth, the faster the regulator will respond to load changes.
- **Dynamic range** – At very low current levels, some control loops are at the low end of their dynamic range and have lower loop gain. This results in degraded transient response on positive-going transients starting from low current. Higher output-voltage undershoot may occur from transients starting near zero output current than from those with, say, a few milliamps of output current.
- **Open-loop output impedance** – Newer N-type LDOs have inherently lower open-loop output impedance, improving load transient response. The load-transient response of an N-type LDO with various C_{OUT} values is shown in Fig. 13. The difference between no capacitor and a typical-value output capacitor is relatively small.
- **Error-amplifier output capability** – The speed at which the error amplifier can charge or discharge the pass transistor gate is determined by its frequency response and its output-drive capability. Increased drive capability usually requires increased supply current, another important specification in many applications.

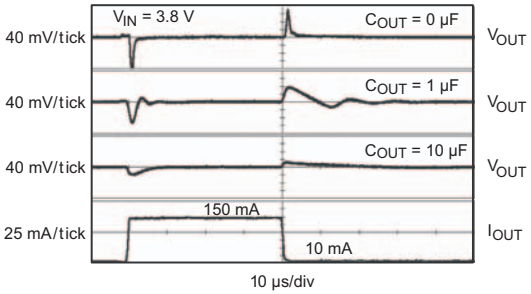


Fig. 13. Transient response of an N-type LDO vs. C_{OUT}.[5]

Load-transient response also can be heavily dependent on $V_{IN} - V_{OUT}$ and the absolute value of the pre- and post-transient load currents. As $V_{IN} - V_{OUT}$ approaches dropout, error-amplifier dynamic range and drive capability are usually compromised, limiting how quickly the regulator can respond to load changes. This can result in over- and undershoot of the output voltage. A good example of this can be seen during certain sequential decreases, then increases, in load current as shown in Fig. 14. A negative-going load transient near zero current that is faster than the loop response will cause an overshoot of the output voltage due to the extra charge dumped into the output cap before the control loop catches up. This extra charge, referred to as a "hiccup," bleeds off at a rate typically determined by the

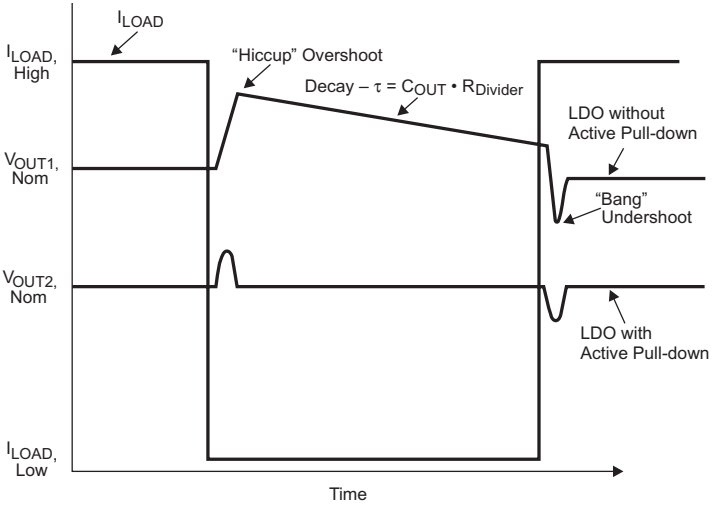


Fig. 14. Transient effects of active output pull-down.

resistor divider that sets the output voltage. If a fast, positive load-current transient (called a "bang") occurs before the control loop catches up, a severe undershoot can result. This hiccup-bang behavior is not a problem for most applications, but designers should be aware that it may occur. Some LDOs have active pull-down devices on the output that turn on when output overvoltage is detected. While this is desirable in some applications, it can be a problem if another supply is to be connected in parallel with the LDO.

Input and output capacitors can affect load-transient response. Low-ESR, high-value capacitors near the input of an LDO can minimize output-voltage droops due to source impedance. Low-ESR, high-value output capacitors also improve transient response by reducing over- and undershoot during fast positive and negative transients.

Ringing can occur under certain conditions at the unity-gain bandwidth of LDOs. This is caused by low phase margin at this frequency. Increased phase margin reduces ringing at the expense of slower transient response and degraded PSRR.

When the transient response of different LDOs is compared, test conditions must be similar. $V_{IN} - V_{OUT}$, load-transient slope, minimum I_{OUT}, and C_{OUT} all have significant effects on transient response.

V. Conclusion

Noise management in battery-powered portable RF systems demands careful trade-offs between noise and efficiency. Noise sources in switching and linear regulators have been discussed along with design principles to mitigate them. The use of linear regulators to suppress noise has also been discussed. The design techniques presented in this paper provide practical methods for addressing the noise management challenges faced by RF system designers.

VI. References

[1] Brian Lynch and Kurt Hesse, *Under the Hood of Low-Voltage DC/DC Converters*, TI Literature No. SLUP206

[2] *High-Efficiency, SOT23 Step-Down, DC-DC Converter*, TI Literature No. SLVS417B

[3] *TPS62203EVM-211, TPS62200EVM-211*, User's Guide, TI Literature No. SLVU069

[4] *200-mA Low-Noise, High-PSRR Negative Output Low-Dropout Linear Regulators*, TI Literature No. SLVS346

[5] *Cap-Free, NMOS, 150mA Low-Dropout Regulator with Reverse Current Protection*, TI Literature No. SBVS034

PRESENTATION

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Challenges and Solutions in Battery Fuel Gauging

Yevgen Barsukov

Outline

- Increased requirements to fuel-gauging solution
- Overview of existing fuel-gauging solutions and their problems
- New approach combines the best and avoids weaknesses

Reducing Design Time and Effort

- Current solutions require different settings for each new battery model
- With same battery model, a fuel-gauge needs different settings depending on particular application
- New settings have to be written into every chip using flash memory or configured using external components like resistor dividers
- Ideal for reduction of development time and cost would be a “plug-and-play” fuel-gauge

Increased Requirements to Precision of Determining Useable Remaining Capacity

- Hardware requirements
  - Precise measurement of current and voltage
    - Need for high resolution ADC
    - Calibration ability
  - Sufficient processing power and memory to implement improved algorithms

- Firmware requirements
  - Consideration of aging effects
    - Eliminating the need for full discharge for correction of full capacity
    - Providing continuous correction rather then periodic
    - Considering impedance change with aging
  - Considering self-discharge and low-current discharge

Improved Run-Time Prediction

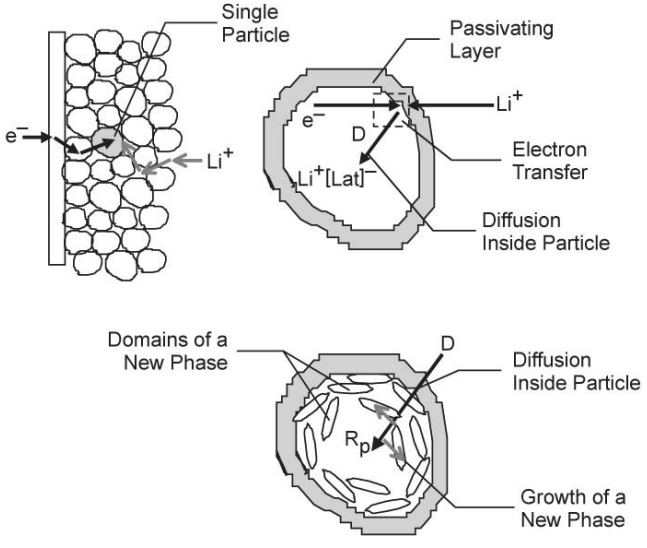
- Providing remaining runtime based on capacity, impedance, rate and temperature
- Power load based run-time prediction along with current based
- Information about run-time degradation

Issues With Currently Employed Algorithms

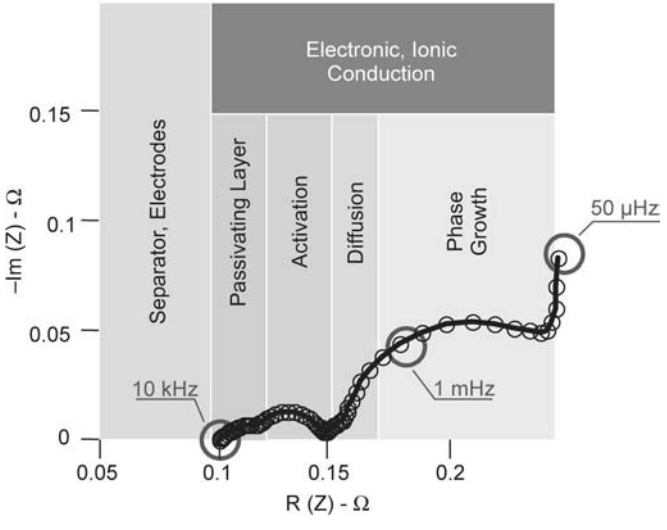
- Current integration based
  - If not immediately following charge, requires correction for battery self-discharge and low-rate discharge by electronics
  - Update of total capacity due to degradation only at full cycle discharge
- Voltage based
  - Relaxation properties of battery response make calculation of voltage drop dependent on both current and time
  - Time constants governing battery response are not fixed and depend on state of charge, temperature, battery age
  - Battery impedance defining voltage drop strongly depends on state of charge, temperature, battery age

Battery – Under the Hood

Kinetic Steps in Li-Ion Battery

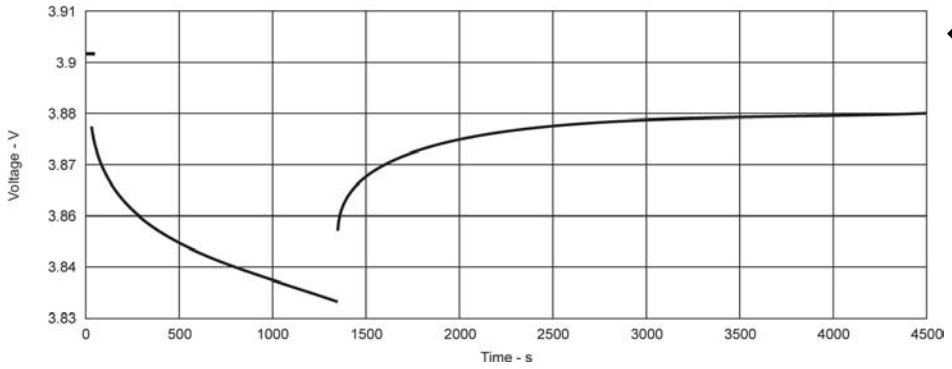


Corresponding Impedance Spectrum

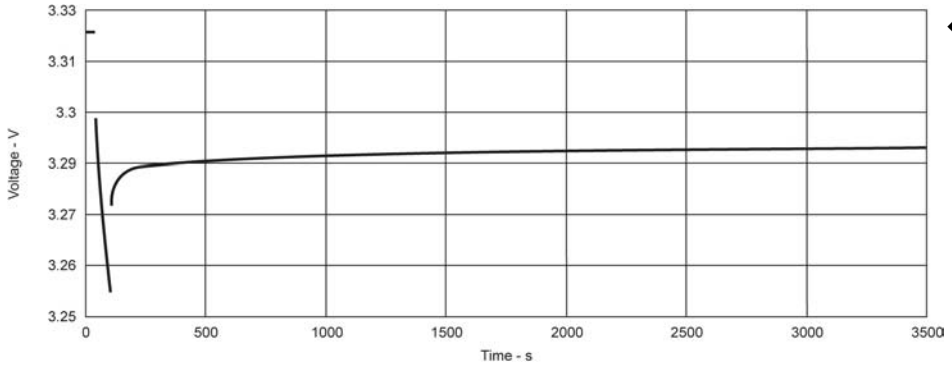


*E. Barsoukov et al., J. New Materials for Electrochem. Sys., 3, (2000) 301

Battery – Transient Response



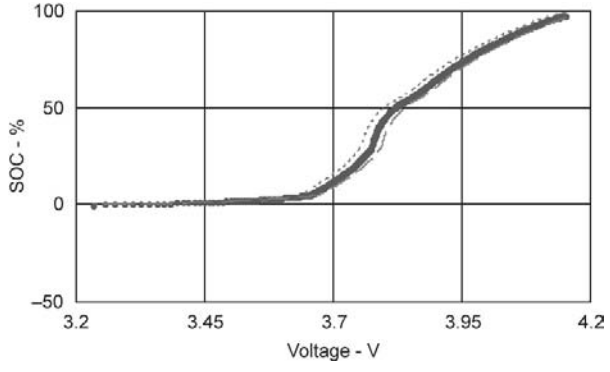
- Charged state
  - Complete relaxation takes about 3000 seconds
  - Voltage difference between 20 and 3000 seconds is 20 mV

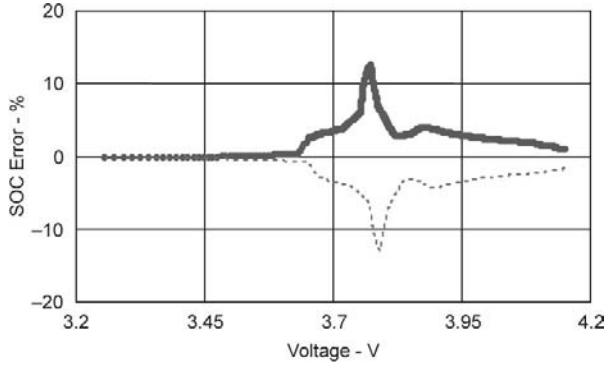


- Discharged state
  - Impedance is much higher, therefore fast drop
  - Despite small passed charge, complete relaxation takes about 3000 seconds
  - Voltage difference between 20 and 3000 seconds is 40 mV

***C/3 rate current used for both tests**

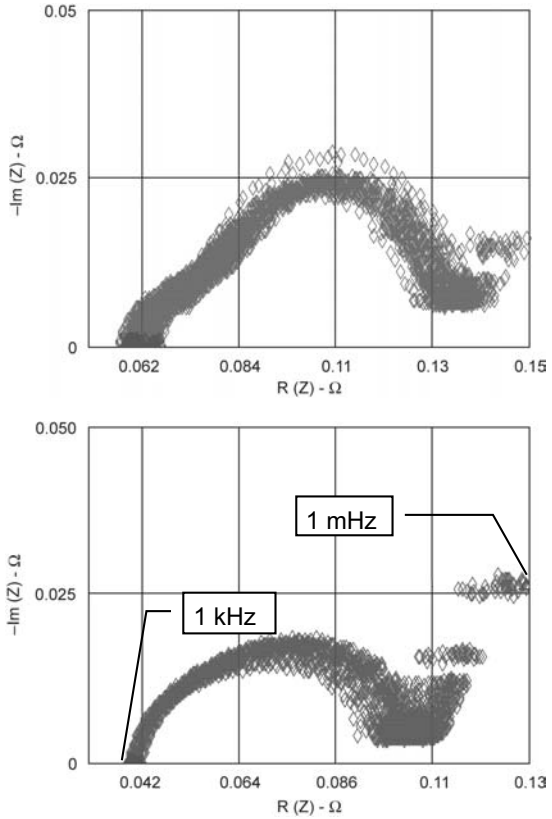
How Voltage Relaxation Error Transforms in State of Charge (SOC) Error?





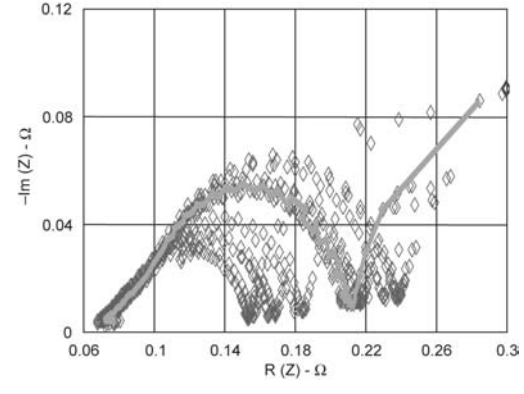
- Any algorithms which either make impedance correction or directly correlate voltage under load with SOC are subject to relaxation error
- Error depends on particular voltage at the moment of estimation
- Maximal error reaches 15%, average error 5%
- Difference in SOC prediction based on voltages measured during relaxation and excitation states reaches 30%
- In discharge state, impedance and relaxation error are about 10 times larger, proportionally increasing error in SOC estimation

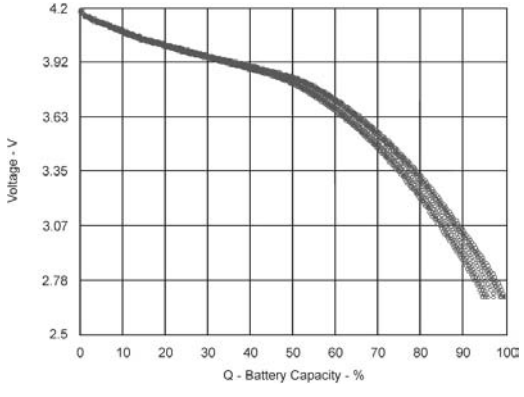
Effect of Impedance Differences of New Cells



- New cells made by same manufacturer (even in the same batch), and in same state of charge, have significant impedance differences
- Common industry impedance measurement at 1 kHz gives false feeling of security by being similar for different cells. However, only low-frequency impedance reflects DC performance
- 50 cells reviewed for 2 different manufacturers showed low-frequency (1 mHz) impedance variation ±15%
- At 1C rate discharge, this difference amounts to about 40-mV difference, which results in maximum SOC error of ±15% as shown in previous slide

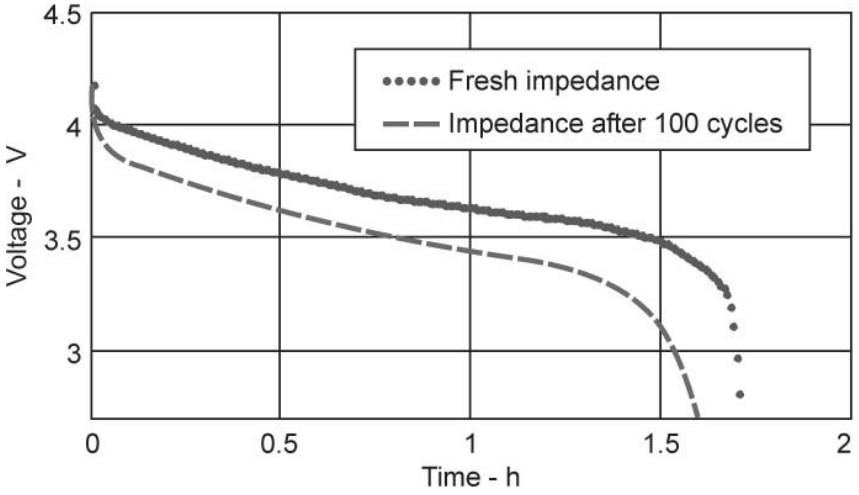
Voltage Error Due to Impedance Change During Aging





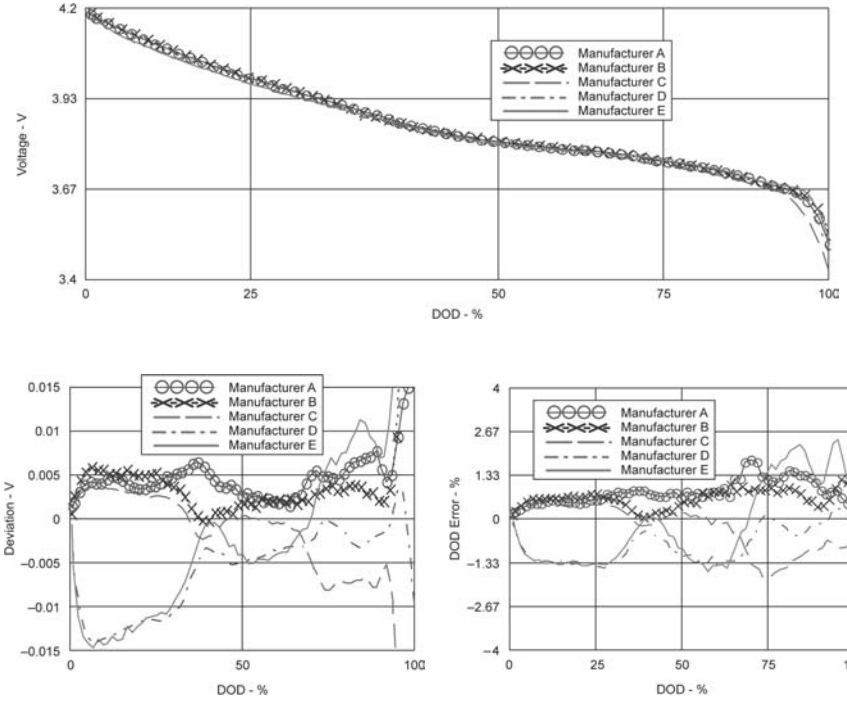
- Increase of battery impedance with aging is much faster than the decrease of capacity
- At 70 cycles, impedance typically doubles compared to original
- This change of impedance results in voltage-drop error of 75 mV at 1C rate in fully charged state, and much bigger one in discharged state
- Impedance increase widely depends on usage conditions such as temperature. Therefore, estimation of aging by cycle counting has limited precision

Effect of Impedance Increase on Runtime



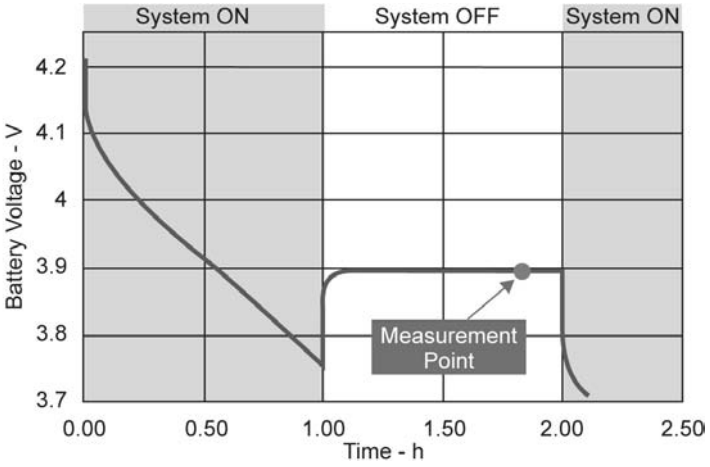
- Change of no-load capacity during 100 cycles is less then 1%
- During the same time, impedance doubles
- 2-times larger impedance results in 7% decrease of runtime at 4-W/cell rate

Comparison of OCV/DOD Profiles for 5 Manufacturers



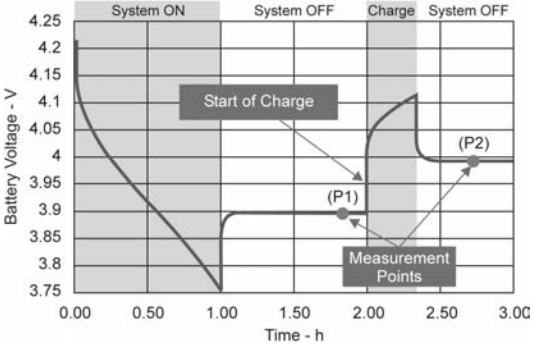
- OCV profiles similar for all tested manufacturers
- Most voltage deviations from average are below 5 mV
- Average DOD prediction error based on average voltage/DOD dependence is below 1.5%
- Same database can be used with batteries produced by different manufacturers as long as base chemistry is same
- Generic database allows significant simplification of fuel-gauge implementation at user side

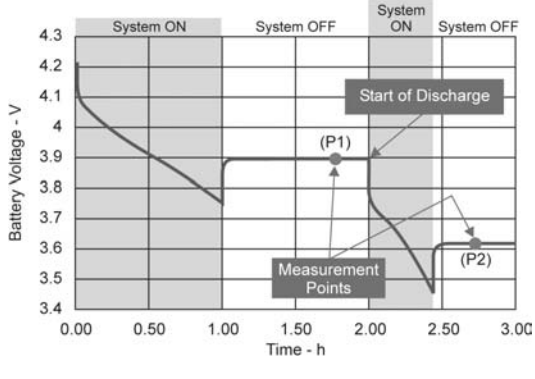
Improved Initial State Estimation Using OCV from Last Wake-up Measurement



- Precision of OCV measurement allows SOC with 0.1% max error
- 1000 seconds is sufficient relaxation time for all tested batteries
- If time between last termination and new start is less then 1000 seconds, previous SOC can be used because self-discharge is negligible
- Therefore, the need for self-discharge estimation is eliminated

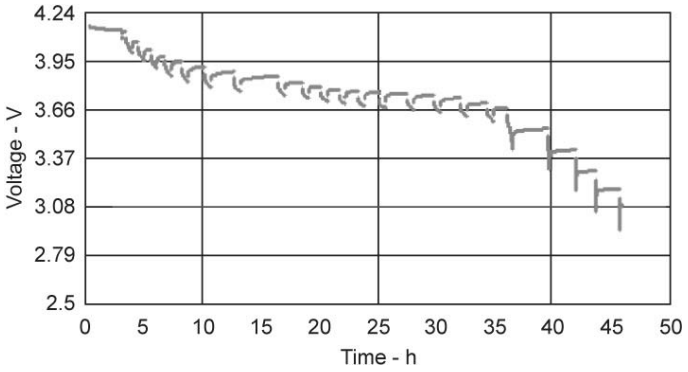
Removing the Need of Full Discharge to Account for Capacity Fade



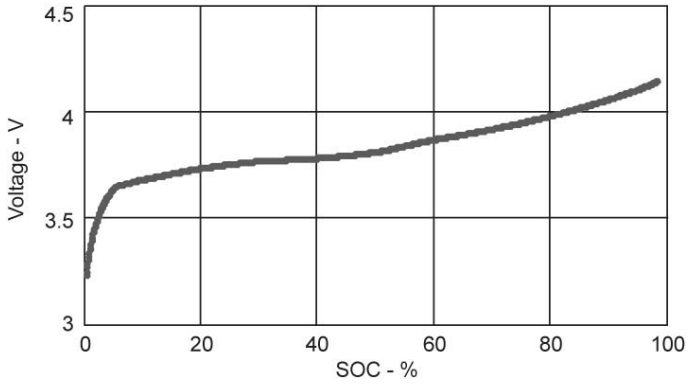


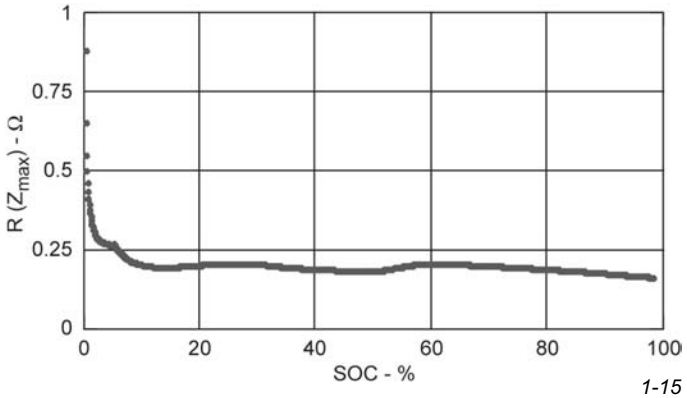
- Problems with full discharge
  - Takes long time, so rarely used if at all. Errors can accumulate between updates and cause erroneous values due to temperature dependence of termination or point load spike
- Solution
  - Full capacity can be detected by comparing SOC before and after exposure to load. SOC is obtained from OCV points (P1) and (P2)
  - Charge passed during exposure is determined by exact coulomb counting
  - Method works for both charge or discharge exposure

Pulse-relaxation Profile to Obtain OCV

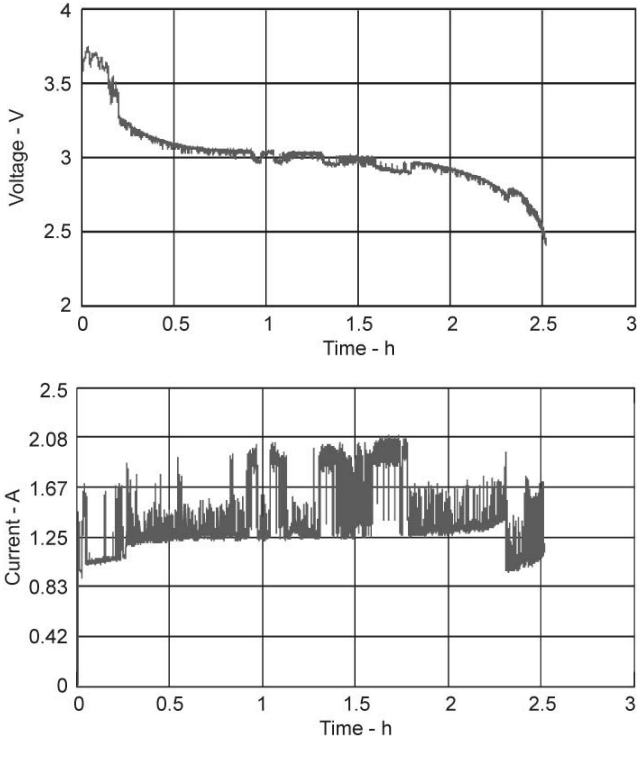


- Adaptive relaxation time used to assure full relaxation at all states of charge
- Both voltage (OCV) and limiting impedance profiles obtained in one measurement





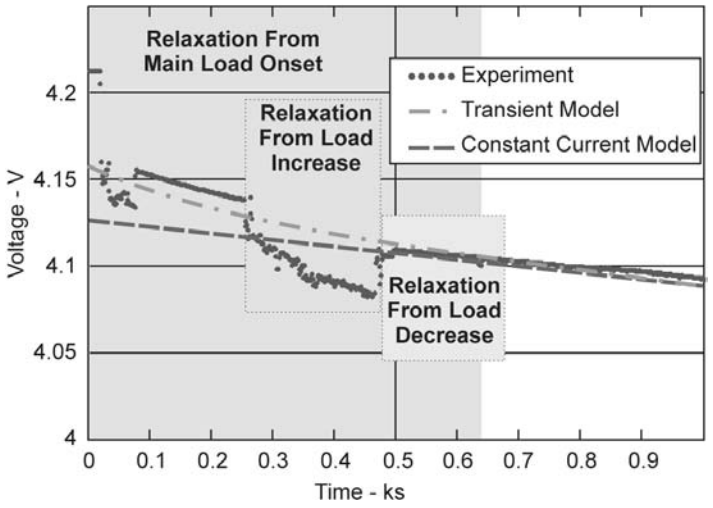
Operational Environment for Impedance Change Correction



- Notebook load environment is determined by
  - Main constant power load
  - High-frequency current pulses (above 50 Hz), about 20% of main load
  - Long duration transient loads (above 1 second), up to 100% of main load

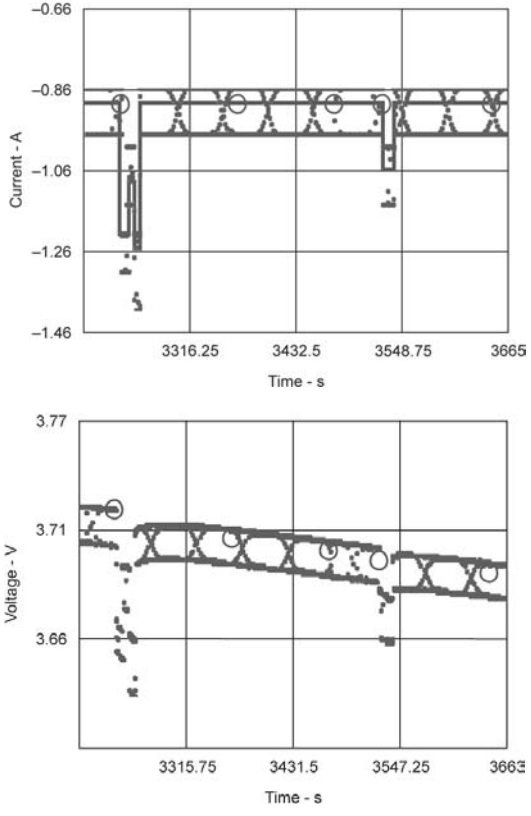
***Samsung notebook current load and battery voltage recorded in real time**

Voltage Response Analysis



- Complex load requires precise measurement of current to enable efficient voltage analysis
- Smoothing out high-frequency voltage noise possible by simple averaging
- Relaxation from primary load onset has duration of about 500 seconds
- Detecting relaxation periods after load changes requires precise current measurement with high sampling rate

Selection of Current Levels and Optimal Measurement Points



- Measurement of voltage for resistance estimation can be distorted by relaxation periods after load change
- Relaxation periods can be excluded in real-time by analyzing the current and detecting its changes
- When the start points of new current levels are found, data is taken after finishing the relaxation

Improved Consideration of Aging Effects

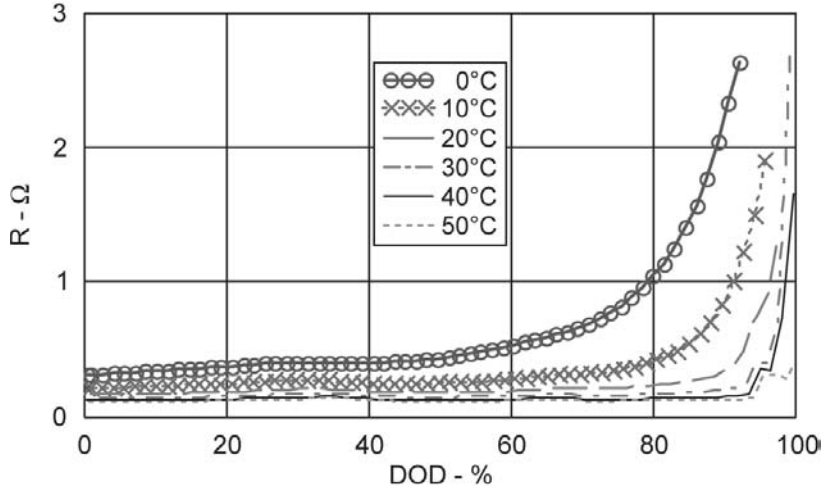
◆ Full charge capacity

- 2-point last wake-up OCV method updates total no-load capacity at every cycle
- 20% discharge or charge is enough for update
- No previous full-charge needed

◆ Impedance change

- Updated during every run
- Update requires analysis of load/response profile
- After first 500 seconds of operation, previous profile is rescaled
- Profile is updated along with discharge progress

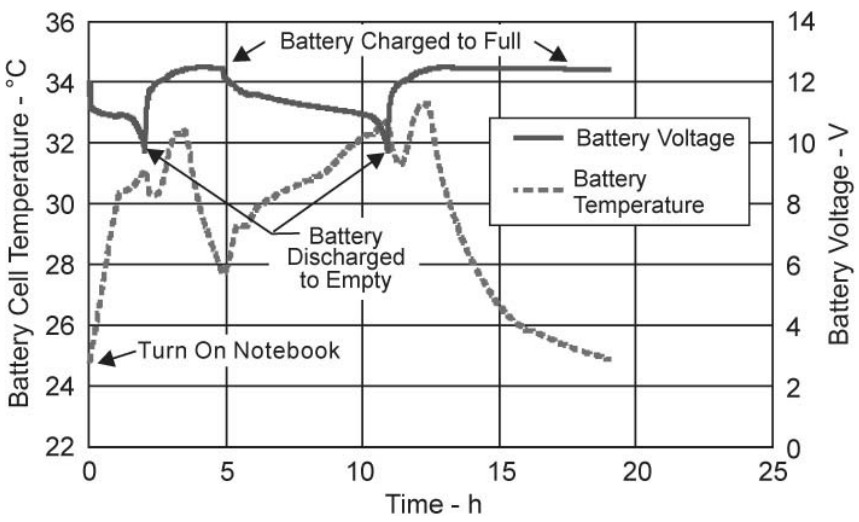
Impedance Dependent on Temperature and Depth of Discharge (DOD)



- Limiting impedance is strongly dependent on temperature in both value and profile shape
- Pulse-relaxation profiles are acquired at different temperatures to provide temperature dependence database

Knowledge of Temperature Profile Needed for Run-time Prediction

Battery cell temperature during notebook operation



***Measurement on IBM notebook**

- Significant changes of temperature occur during device operation
- Impedance changes about 1.5 times at 10°C change
- To predict remaining runtime, knowledge of the resistance/temperature dependence is not enough
- Future temperature profile has to be known or calculated

How to Predict Remaining Runtime?

◆ Load and environment information

- Average power usage
- Recent power usage
- Future temperature profile (thermal modeling needed)

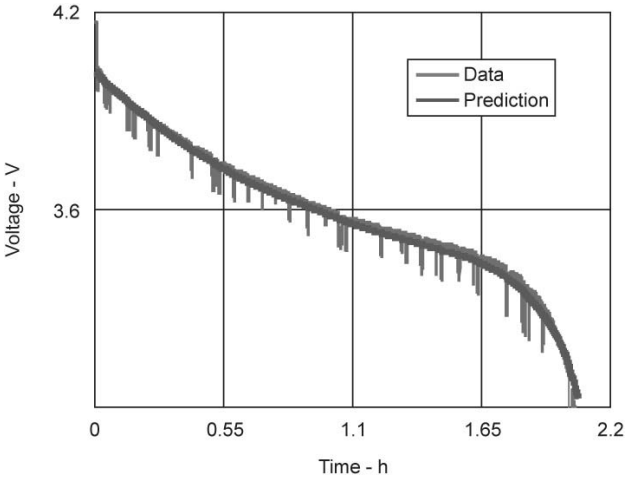
◆ Battery related information

- OCV (DOD,T)
- Full charge capacity, most recently updated
- R (DOD,T) most recently updated
- Starting DOD, from last wake-up OCV

◆ Calculations

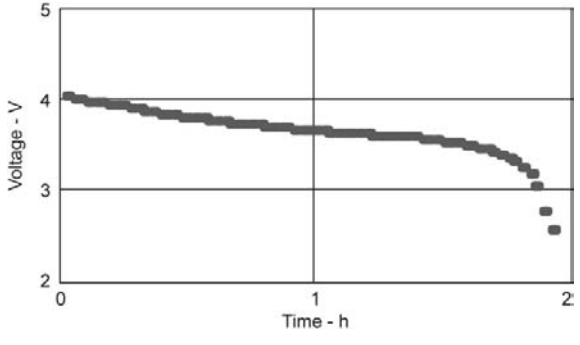
- Simplified DC-model in case of constant current
- Step-wise calculation in case of constant power
- Termination time is found when predicted voltage equals minimal voltage

Run-time Estimation for Constant Current



- In order to estimate the runtime until termination, we need to predict voltage profile during discharge
- Sufficiently accurate calculation of voltage profile can be made using simple DC-model using OCV and impedance information
- Starting depth of discharge is obtained from last relaxed period OCV
- Impedance profile and total capacity needed for calculation are updated during each discharge period regardless of its duration
- OCV profile is used as-is from generic database, valid for all batteries with same chemistry
- Remaining capacity and other parameters of interest are found from runtime using simple relations

Run-time Calculation for Constant Power



- Voltage change with time at constant power operation can not be given as an equation
- Stepwise calculation is possible by assuming constant current at small intervals (dt)
  1. Current is calculated using known starting voltage and impedance
  2. DOD is calculated by adding step DOD to previous
  3. Total voltage is found using estimated current and impedance for given DOD and compared with V_{LIM}
  4. If exceeded, find exact termination time from last step
- Once termination time is found, remaining energy is simply $t_{TERM} \bullet W$
- Termination DOD and remaining capacity, found using simple relations

Summary

- **Problems solved**
  - Need for full-discharge removed for capacity correction
  - Difficulty with low-current coulomb counting removed
  - Cumulative uncertainty associated with self-discharge correction removed
  - Correction for change in cell impedance eliminates large errors in run-time estimation in aged cells
- **Implementation improvements**
  - Easy implementation on user side: removed the need for user-database collection for most cases
  - Additional flexibility: Automated database collection for new chemistries supported on chip
- **New services provided**
  - Report of remaining runtime based on measured power usage and temperature
  - Report of battery aging in terms of run-time degradation
  - Report of remaining energy at given load along with remaining capacity
  - Report of average power usage
  - New level of precision due to continuously updated total capacity and resistance

Battery Circuit Architecture

Bill Jackson

Block Diagram of Circuitry in a Typical Lithium-Ion Battery Pack

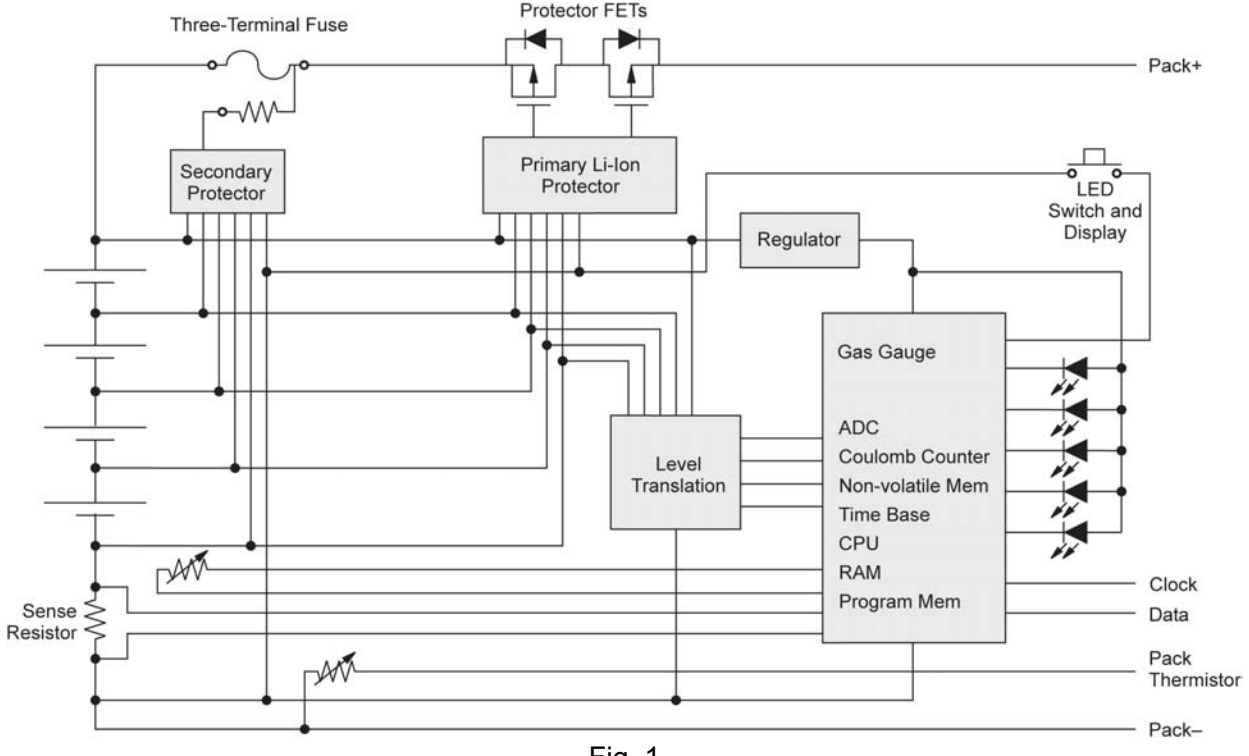
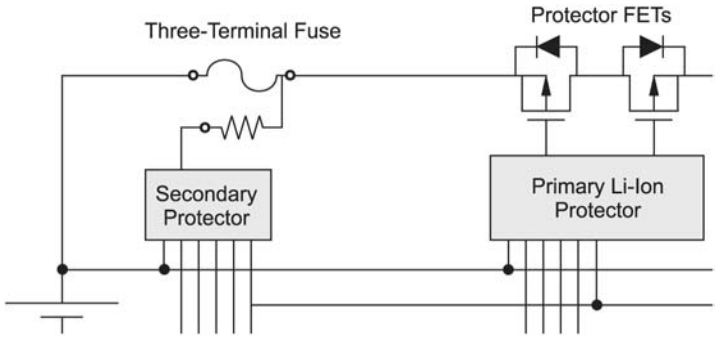


Fig. 1

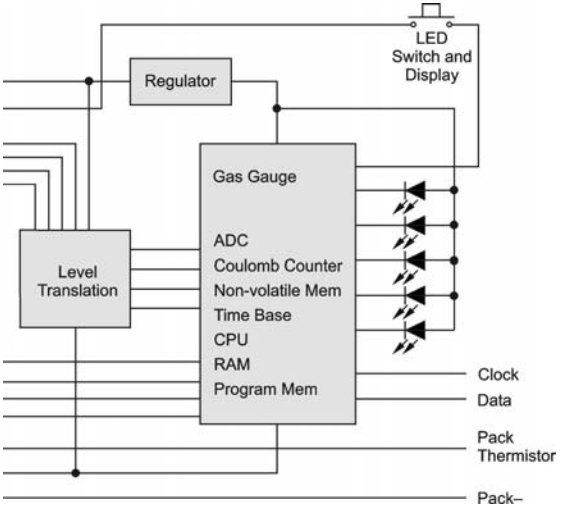
Typical Circuitry for Lithium-Ion Battery Pack



- Lithium-ion safety protection (Fig.1)
  - Overvoltage protection
    - Most critical safety issue
      - Often redundant protection for overvoltage
      - Cell venting and fire may result at extreme overvoltage
  - Short-circuit
  - Overtemperature
  - Undervoltage
    - Overdischarge will shorten battery life

Typical Circuitry for Lithium-Ion Battery Pack (cont)

- Gas Gauge (Fig. 1)
  - Sense resistor for current/charge measurement
  - Low-offset current/charge measurement device
  - Voltage measurement
  - Temperature measurement
  - Processor with RAM and program memory
    - Gas gauging algorithm firmware
      - Remaining capacity, state-of-charge, etc.
    - Time-to-empty and other computations
  - Communication to user/host
    - LEDs and display switch for visual capacity display
    - Serial communication
  - Possible secondary control of protector FETs



Optimizing the Design for Measurement Accuracy

- Component selection must support desired measurement accuracy
  - Use low temperature coefficient current-sense resistors (<10 ppm/°C)
  - Use high-accuracy current-sense resistors (1% or better)
  - Determine adequate performance level required of measurement sensors/circuits
    - Versus temperature
    - Versus battery voltage

Optimizing the Design for Measurement Accuracy (cont)

- PCB layout issues
  - Cell voltage measurements
    - PCB trace voltage drops
    - External battery wiring drops
    - Ground reference for single-ended measurements
  - Charge or discharge current measurements
    - Kelvin connections to sense resistor
    - High temperature coefficient of any included copper trace resistance (0.39%/°C)
  - Separate measurement-system ground from high-current ground path
    - Improves accuracy of low signal level measurement
    - Reduces ESD susceptibility

Transient Protection

- Place thermal sensor to measure temperature of cells, not PCB
  - Avoid heat from sense resistor
  - Avoid heat from protector FETs
  - Avoid heat from high-current traces
- Separate measurement system from heat sources
  - Improved measurement accuracy
    - Reduced component and reference drift due to temperature

Thermal Issues

- Need transient protection because of distributed inductance in the battery pack
  - Unplugging battery while under load
  - Protector opening to break overload or short circuit load fault condition
  - Inrush surge to charge backplane capacitance when battery pack is plugged in
- Provide transient suppressors or sufficient capacitance to absorb the inductive energy due to potential load or load fault transients

Low-Side Protector Issues

- Low-side protector FETs are used on virtually all 1-cell and most 2-cell designs
  - Low-threshold NFETs are cheaper and better than low-threshold PFETs
- Choice of host- or cell-side of protector for grounding battery pack circuitry
  - Open protector may disrupt host communication with battery pack circuitry with cell-side grounding
  - Open protector may remove power from battery pack circuitry with host-side grounding

Low-Side Protector Issues (cont)

- Host charger failure with high-voltage output will cause protector to open, but when host pulls interface line low, there is a sneak charge-current path that can allow continued charging
  - Substrate diode from V_{SS} to communication/interface line may allow unintentional battery charging when protector FETs are open (Fig. 2)

Sneak Charge-Current Path From a High-Voltage Charger Failure

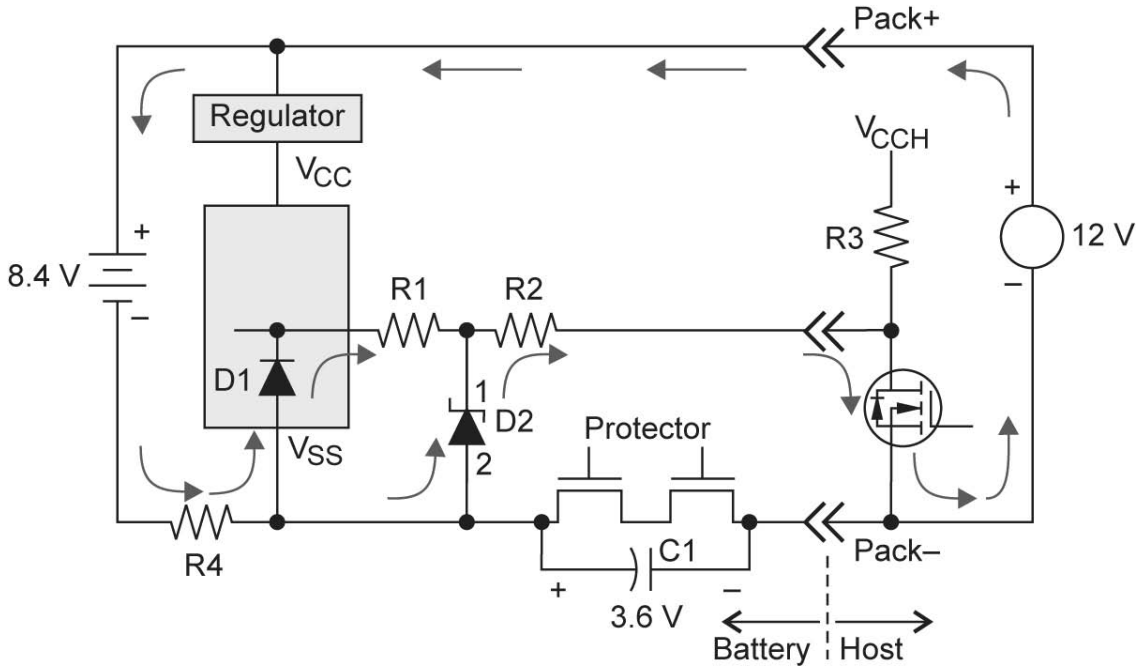


Fig. 2

Low-Side Protector Issues (cont)

- Need positive mechanism to prevent sneak-path charging of battery (Fig. 3)
  - Add diode in communication/interface line (usual solution)
    - Add parallel capacitor to pass AC, improving communication integrity and for ESD protection of diode
    - Shunt resistance to allow logic low condition when the diode is back-biased

Preventing the Sneak Charge-Current Path From a High-Voltage Charger Failure

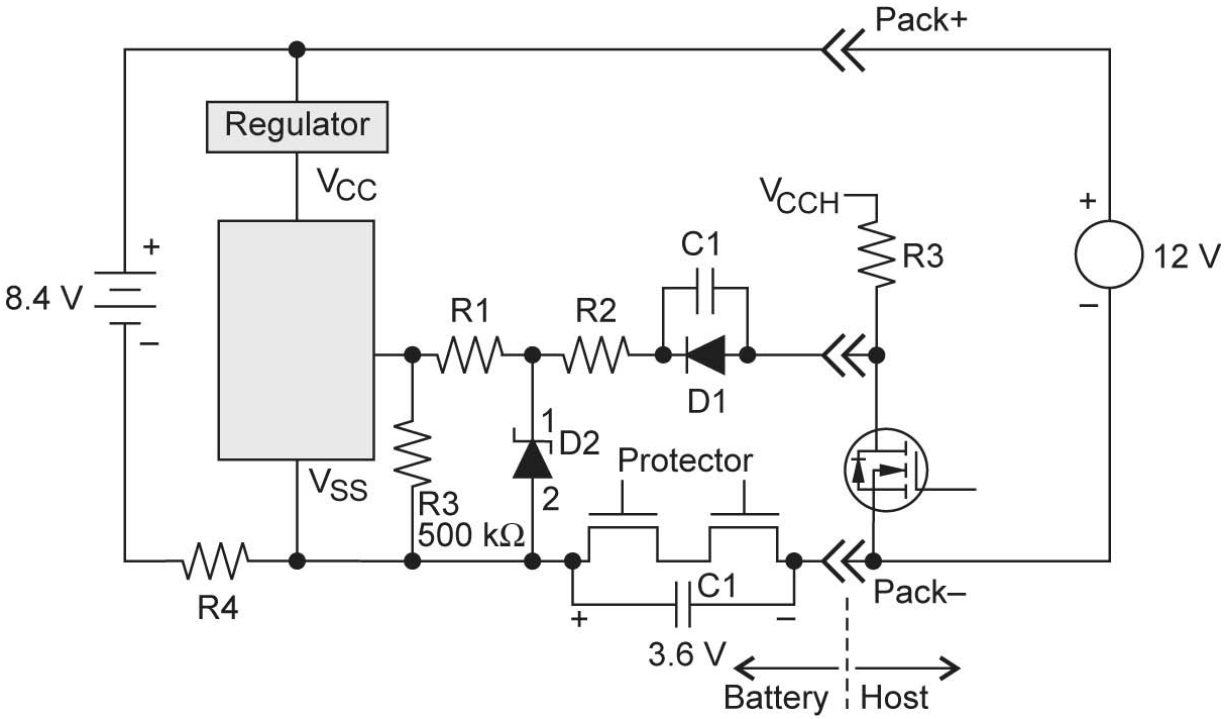


Fig. 3

ESD Considerations

- ESD requirements may be greater than damage threshold of integrated circuits
  - Most applications must withstand ±15 kV
    - Need to add external protection components
    - 15 kV may arc across body of small components
- ESD current will usually flow to the battery cells and then to earth ground
  - Current will flow in path with highest capacitance (lowest AC impedance) to earth ground
  - 1-ns rise-time voltage (>3 kV) and current (>30 A) transients can occur in affected traces
    - Large voltage drops along inductance of traces
    - Capacitive and magnetic coupling to adjacent components and traces

ESD Considerations (cont)

- Most battery-pack requirements include surviving multiple ESD hits from both direct connection and air-gap spark discharges
  - Discharges typically a human-body model of 150 pF with 1-kΩ series resistance, charged to 15 kV
  - Multiple positive and negative voltage discharges applied to all connector pins
  - Air-gap spark discharges to battery case

ESD Design Hardening

- Add spark gap structure at PCB connector pads (Fig. 4)
  - Reduces peak voltage seen by internal circuitry
  - Must be on PCB external layer
  - Must be free of solder mask or other non-conductive coating
  - A 10-mil (0.25-mm) spark gap will arc at about 1500 V at sea level

Typical ESD Spark-Gap Structure at Pack Connector

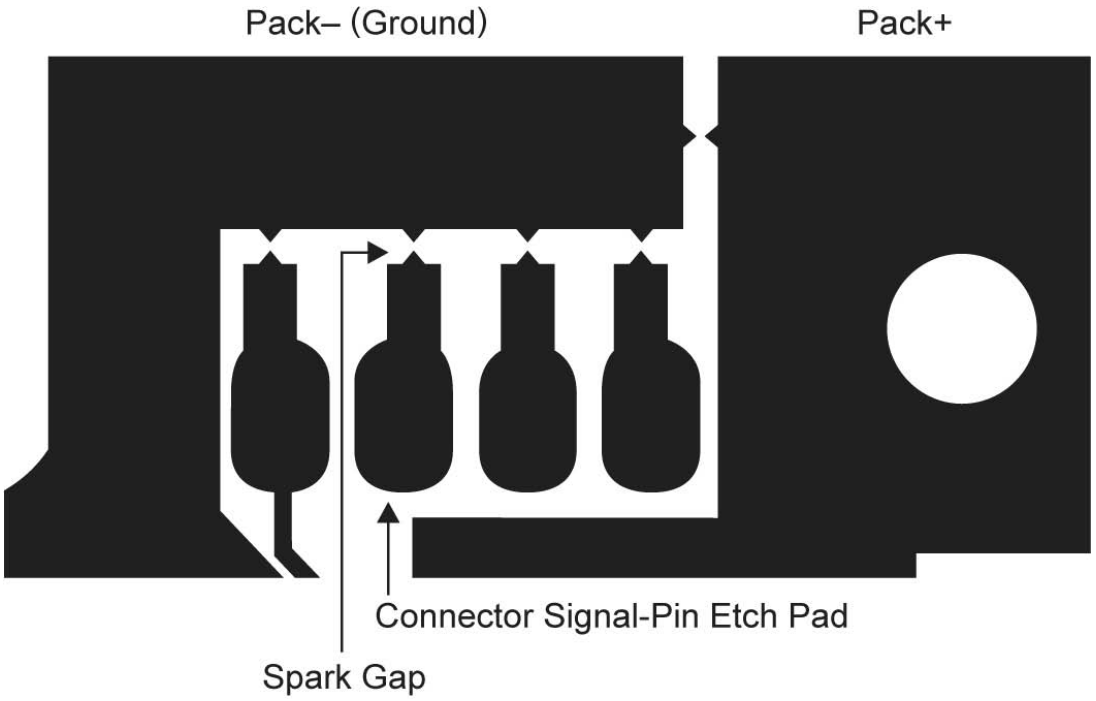


Fig. 4

ESD Design Hardening (cont)

- Component placement and routing to achieve good ESD performance (Fig. 5)
  - Keep high-current traces away from low-level circuitry
  - Separate measurement-system ground from high-current ground (tie together only at one point)
  - Capacitor from Pack+ to Pack– at connector
  - Capacitors across protector FETs
  - Keep bypass cap leads short
  - Add small value parallel bypass caps (lower ESR)

Component Placement and Routing to Achieve Good ESD Performance

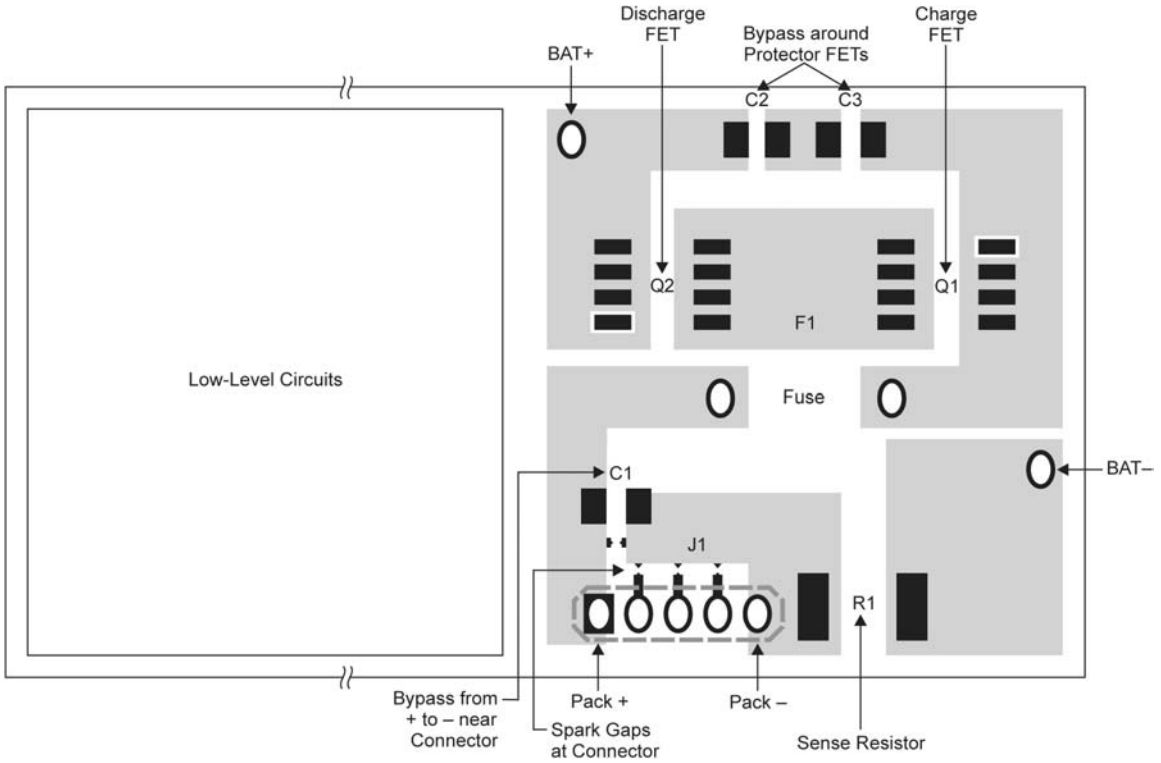


Fig. 5

I/O Interface Issues

- Substrate diode from I/O line to V_{CC} is potential problem
  - V_{CC} to IC in battery pack can be pulled up if host V_{CC} is higher
    - Unintentional charging of battery can also result
  - Depleted battery can pull I/O line low
  - Pack insertion issue if ground connection makes last (Fig. 6)
    - Potential for transient increase in V_{CC} to IC in battery pack, causing improper operation
    - Issue can be controlled by zeners that clamp the I/O lines to less than the maximum allowable V_{CC}

Pack Insertion Issue When Ground Pin Makes Last Connection

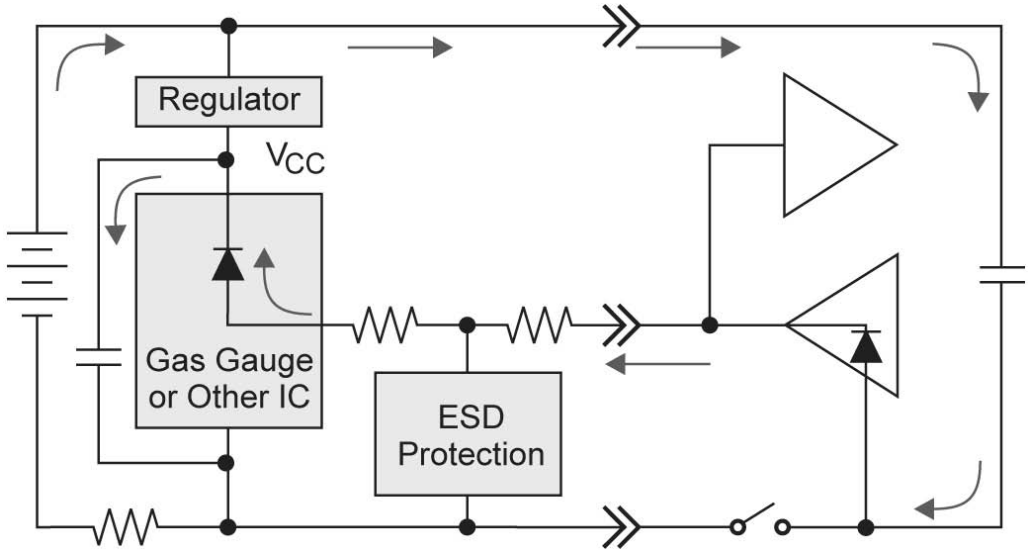


Fig. 6

Conclusions

- Recognize potential issues prior to starting the design
  - Thermal
  - Voltage drops along high-current traces
  - ESD and load transients
  - Potential fault conditions
  - Hot-plug issues
- Close control of PCB layout by designer

Design Considerations and Advances in Portable Power Battery Chargers

Charles Mauney

Battery Charger Design Topics

- Linear or switcher charger
- Design for transient conditions
- Powering a system load from the battery charger output
- Alternative solutions – powering a system from the input

Linear Charger

- Design considerations
  - Less complex – fewer components
  - Low cost for low-power designs
  - Low noise design
  - Typical poor efficiency for multiple cells
  - Thermal issues with high voltage, multiple cell designs

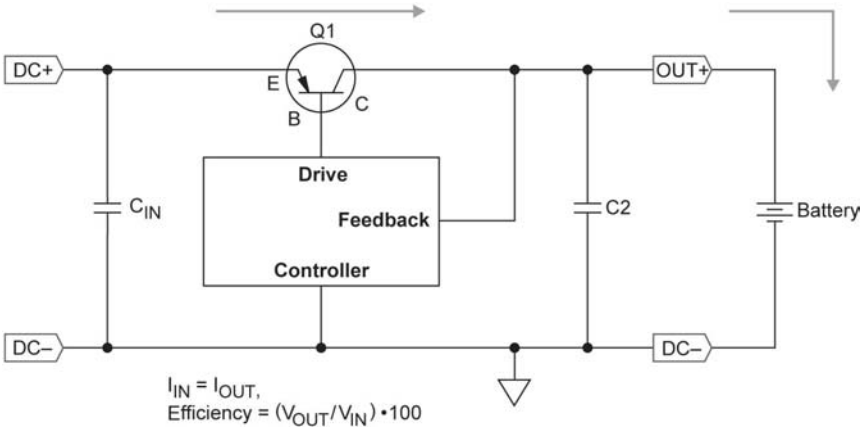


Fig. 1a. Linear regulator

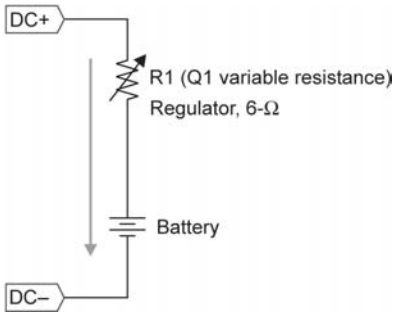


Fig. 1b. Equivalent DC circuit

Switching Charger

- Design considerations
  - More complex than linear
    - Additional components: L, D4 and C_{OUT}
  - Cost is attractive at higher power levels
  - Efficient at higher power levels – less heat

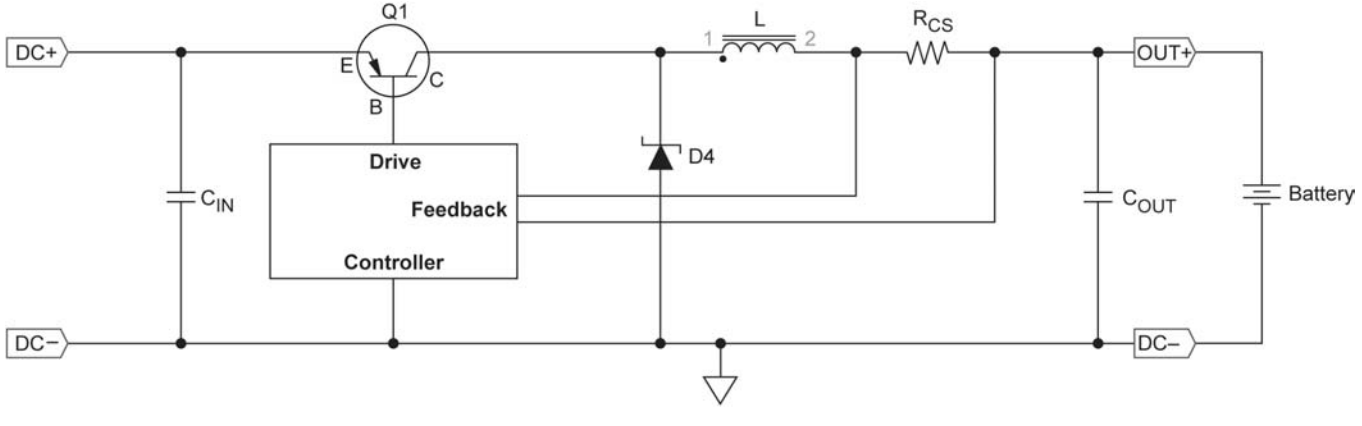


Fig. 2a. Buck power stage

Power Stage Modes

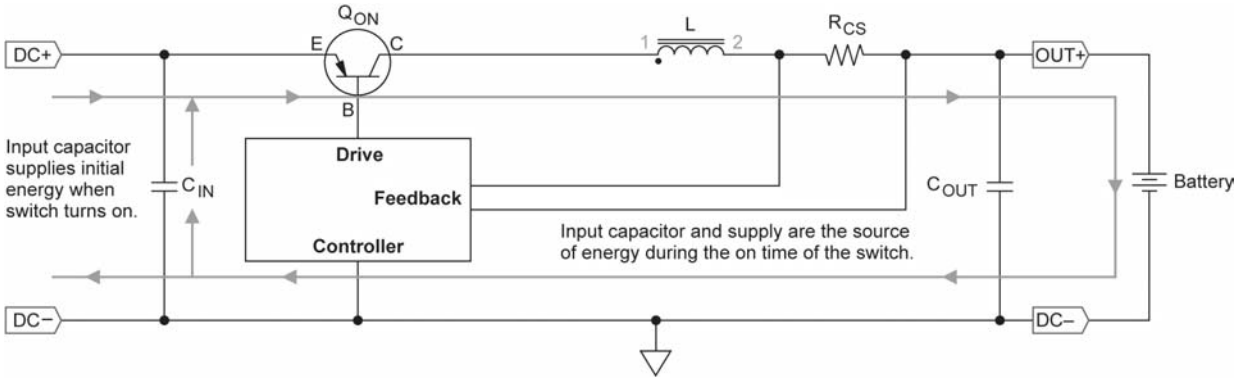


Fig. 2b. Current flow when switch is on

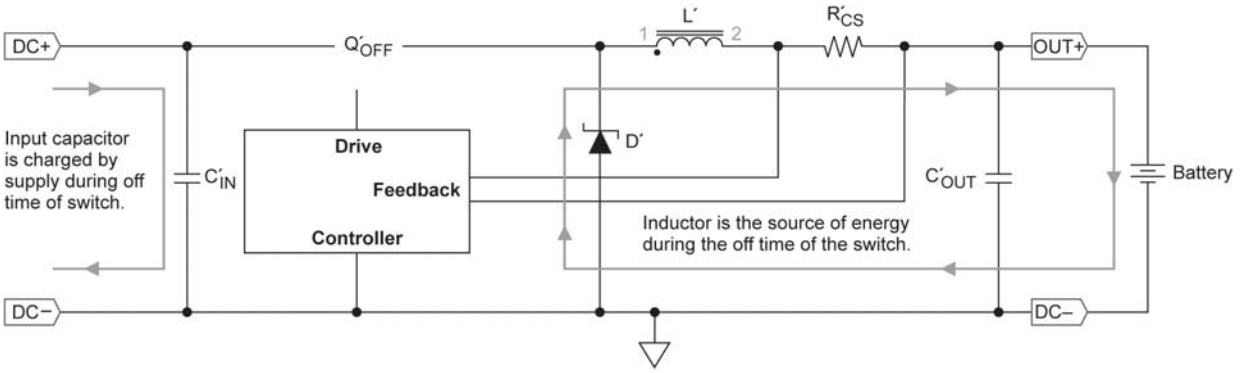


Fig. 2c. Current flow when switch is off

Switcher Design Considerations

- Input capacitor
  - Low ESR – example: Panasonic, FK series
    - Use enough capacitors in parallel to handle input RMS current
  - Verify capacitor listed impedance is less than $0.5 \cdot V_{INMIN}/I_{MAX-CHG}$, to prevent input from ringing
  - Ringing may cause false charge termination

- Power switch
  - FET: Low V_{GS} threshold, low gate capacitance to minimize switching losses
  - Bipolar: Large h_{fe} to minimize drive circuit requirement
  - Note: If drive is not sufficient, the transistor will stay in its linear range and dissipate more power which may affect performance and reliability

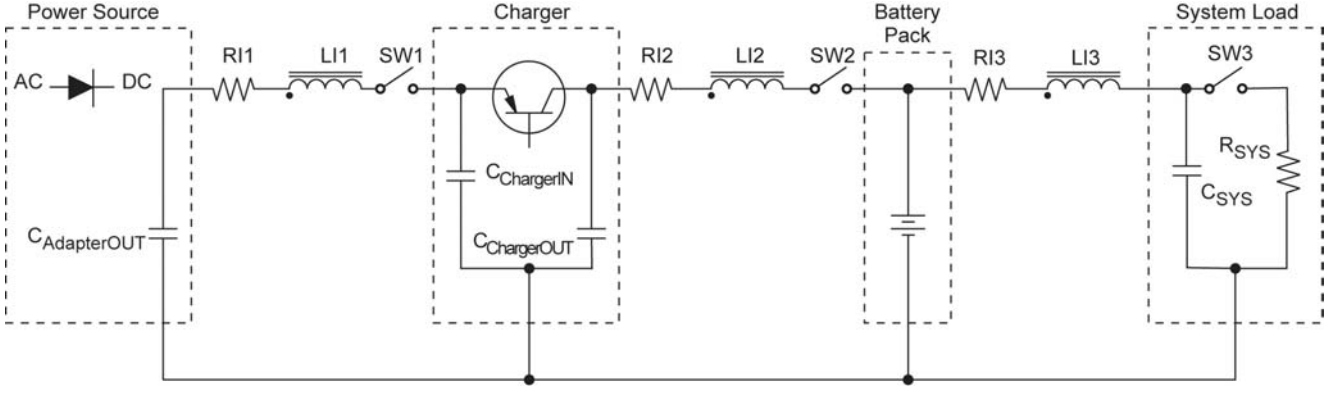
- Output inductor
  - Inductance must be rated for maximum peak current
  - Limit current ripple to 30% typical (60% maximum) of I_{MAX}, $I_{MAX} = (V_{OUT}+V_D) \cdot (1-V_{OUT}/V_{IN})/L$
    - Higher RMS current leads to more power dissipation

Switcher Design Considerations (cont)

- Charger output capacitor
  - Lowers impedance at output of charger – cancels effect of inductive battery leads and helps stability
  - The charger output capacitor helps stabilize charger operation when the battery is removed
- PWM
  - Constant switching frequency
  - Switching noise at narrow frequencies – easy to filter
- Hysteretic switcher
  - Operates between two thresholds – fixed ripple
  - Variable switching frequency produces noise in a wide spectrum – harder to filter
  - Place output capacitor across battery, when using low-side current-sense resistor

Designing for Transient Conditions

- Voltage transients will be generated when connecting/disconnecting power adapter, battery and system load
- These transients happen mainly because of parasitic inductance
- The transients must be considered during the design phase



Typical Charging System

Powered AC Adapter Plugged Into Charger

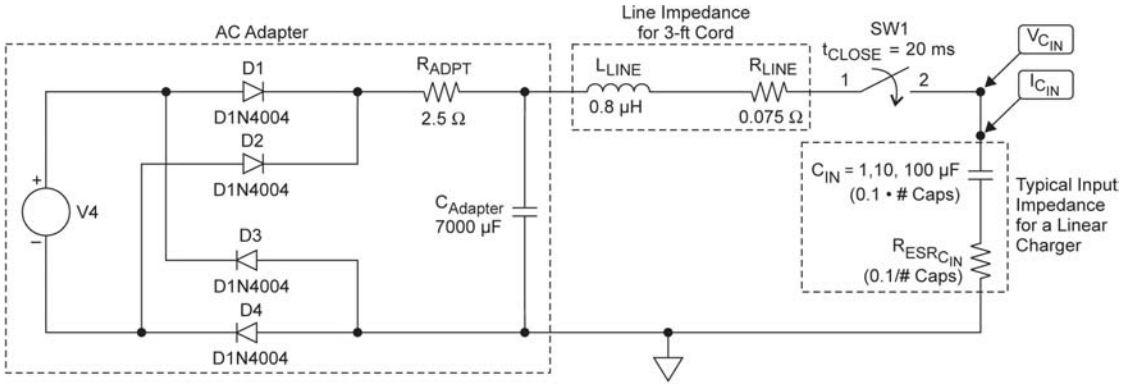


Fig. 6a. Hot plugging an adapter into a charger circuit as a function of charger capacitance

- A transient simulation was done on the above circuit for three values of C_{IN}, 1 µF, 10 µF, 100 µF
- SW1 is closed after the adapter has charged to its peak value ~5 V • $\sqrt{2}$ = 7 V. The voltage and current waveforms, at $V_{C_{IN}}$, are plotted

Powered AC Adapter Plugged Into Charger (cont)

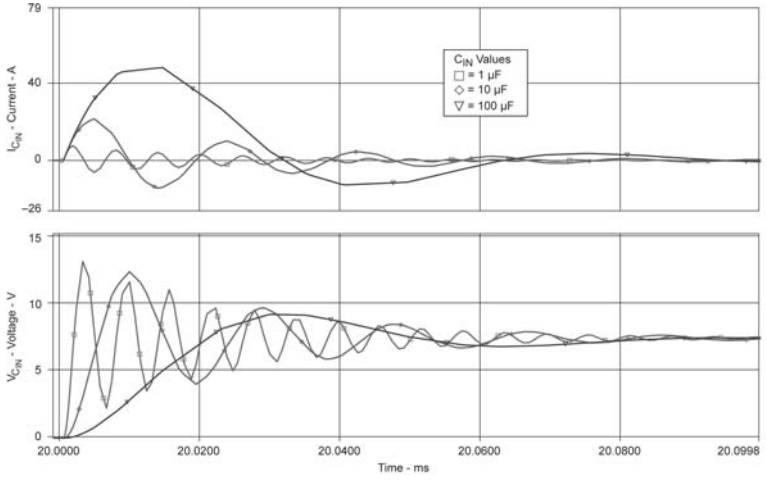


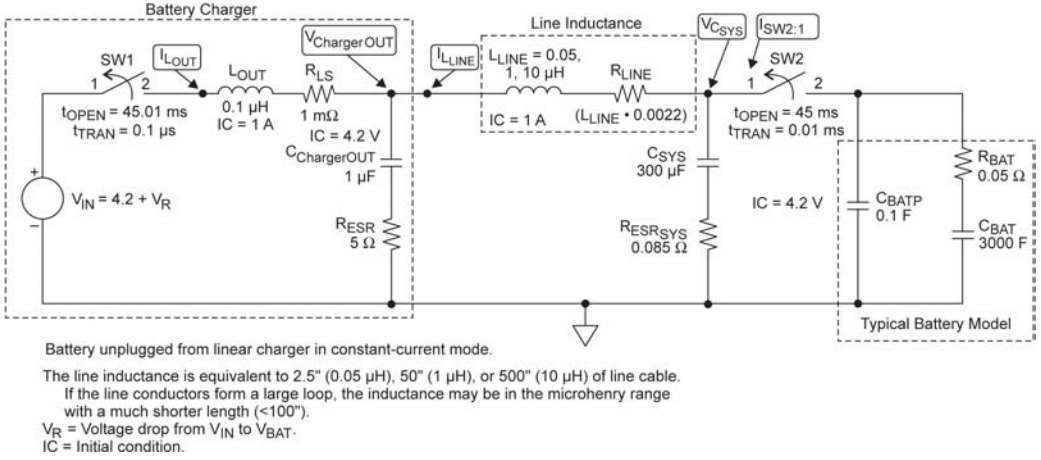
Fig. 6b. Plot of current and voltage waveforms

- Transient results, at $V_{C_{IN}}$, from plugging AC power into the charger input
  - Increasing input capacitance reduces the ringing frequency and voltage amplitude (1 µF, 10 µF, 100 µF)
  - As the input capacitance is increased, the impedance of the circuit is lowered. The line resistance is now closer to the characteristic impedance which is where critical damping occurs, $Z = \sqrt{L/C}$
  - At 100 µF input capacitance, the voltage peaks at 8 V and the current reaches ~40 amps

Powered AC Adapter Plugged Into Charger (cont)

- How do we reduce the input transients?
  - Adding capacitance – lowers voltage transient at the expense of higher inrush currents
  - Adding an input resistor in series with the line cord works well but continually dissipates power in steady-state operation
  - Placing a zener at the input of the charger works well since this is a single transient event

Disconnecting the Battery From a Linear Charger During Charge



Battery unplugged from linear charger in constant-current mode.

The line inductance is equivalent to 2.5" (0.05 µH), 50" (1 µH), or 500" (10 µH) of line cable. If the line conductors form a large loop, the inductance may be in the microhenry range with a much shorter length (<100").

V_R = Voltage drop from V_{IN} to V_{BAT}.

IC = Initial condition.

Fig. 10a. Battery unplugged from linear charger in constant-current mode

- Three transient simulations were run on the above circuit for three values of L_{LINE} and R_{LINE} (0.05 µH, 1 µH, 10 µH and 0.1 mΩ, 2.2 mΩ, 22mΩ)
- SW2 opening action simulates battery removal
- L_{OUT} and L_{LINE} in steady-state condition have the same charger output current
- The voltage at C_{SYS} will not change much due to its large capacitance
- $C_{ChargerOUT}$ is a 1-µF capacitor and will be charged by L_{OUT} and discharged by L_{LINE} during the transient

Disconnecting the Battery From a Linear Charger During Charge (cont)

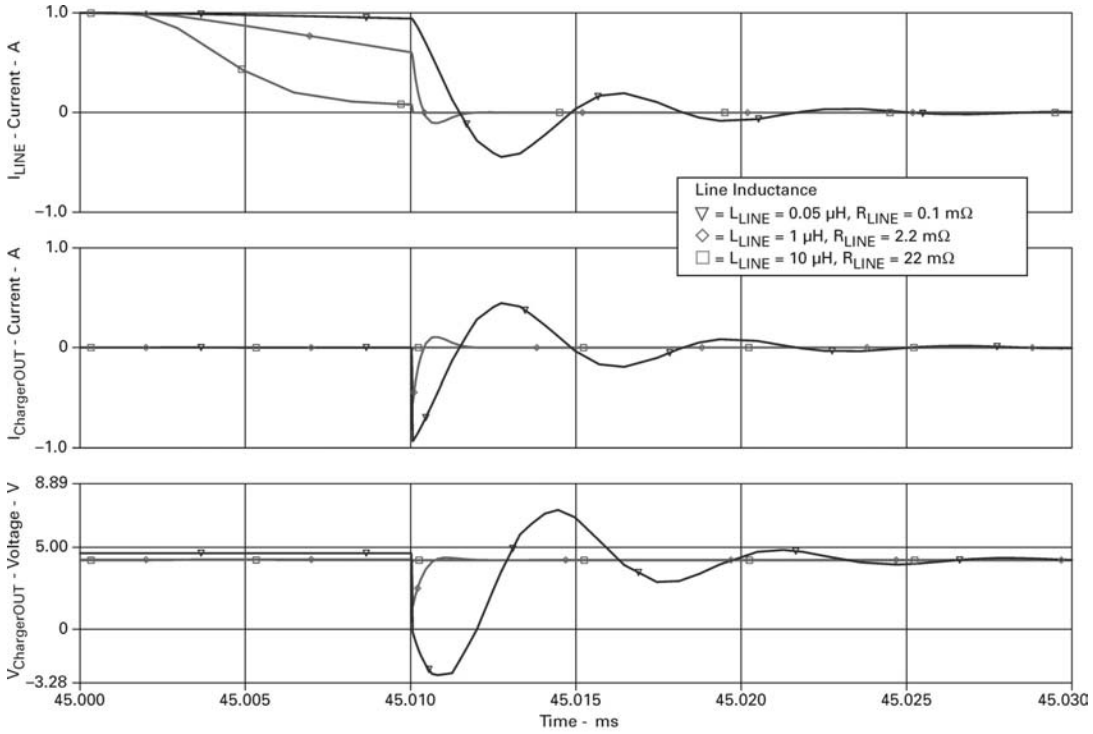


Fig. 10b. Plots of current and voltage

Disconnecting the Battery From a Linear Charger During Charge (cont)

- Results of disconnecting the battery from the charger
  - If L_{LINE} is less than L_{OUT}, then $C_{ChargerOUT}$ is charged
  - If L_{LINE} is greater than L_{OUT}, then $C_{ChargerOUT}$ is discharged

- How do we reduce charger output transients?
  - Minimize cable inductance to reduce transient amplitude
  - Increase charger output capacitance to minimize transient
  - Clamp from going negative with a Schottky diode

Battery Charging w/Parallel Load

- Typical Li-ion battery modes
  - Precharge
    - V_{BAT} < 3 V/cell
    - $I_{PRE-CHG} = I_{MAX-CHG}/10$
    - Charger output power, $P_{OUT} = I_{MAX}/10 \cdot V_{BAT}$
  - Constant-current fast charge
    - 3 V/cell < V_{BAT} < 4.2 V/cell
    - $I_{CHG} = I_{MAX} = I_{PGM}$
    - Charger output power, $P_{OUT} = I_{MAX} \cdot V_{BAT}$
  - Voltage-regulation fast charge
    - V_{BAT} = 4.2 V/cell
    - I_{CHG} tapers toward the termination current threshold
    - Charger output current, $P_{MAX} = I_{MAX} \cdot$ 4.2 V/cell

Battery Charging w/Parallel Load (cont)

- Battery charging issues
  - The system current decreases the charge current
    - Precharge mode: System will not operate or precharge fault timer will expire
      - In precharge keep system off or in low-power mode
    - Constant-current mode: System operational but fast charge safety timer expires
      - Increase safety timer value
      - Increase charge current
    - Voltage-regulation mode: Safety timer expires due to not detecting full battery and properly terminating charge cycle
      - Taper current threshold not reached due to system DC load
        - See supplemental charge circuit
      - Taper current threshold is reached but dynamic load resets it
        - Average load below taper threshold – put capacitor on sense pin to filter spikes
        - Average load above taper threshold – see termination circuit
- Charge complete issues
  - Done state – if battery is removed, charger output may discharge to a critically low voltage prior to refresh of charger
- Notes
  - Stand-alone charger assumes all the charger current is going to battery
  - Safety timers and termination thresholds are based on current leaving the charger
  - System loads pull more current as their input voltage drops to maintain constant power
  - If the system current exceeds charge output current then battery will discharge

Termination Solutions for Pulsed Loads and DC Loads > C/10

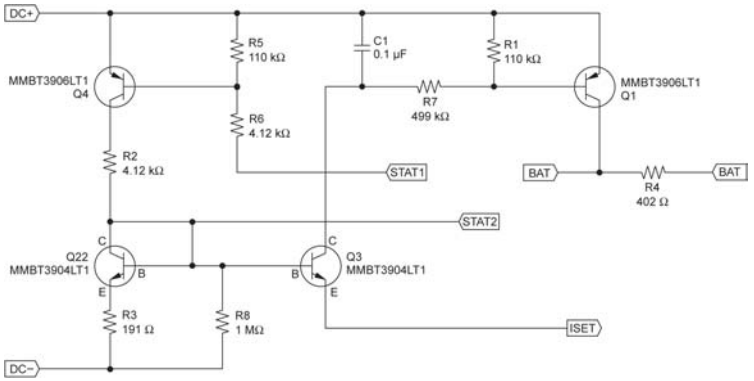


Fig. 11. Termination circuit triggered by minimum sense current

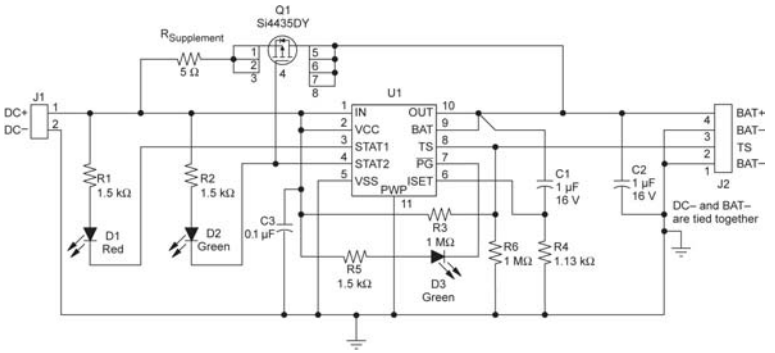


Fig. 12. Supplemental charging current to offset system minimum load

Switching From Adapter to Battery Power

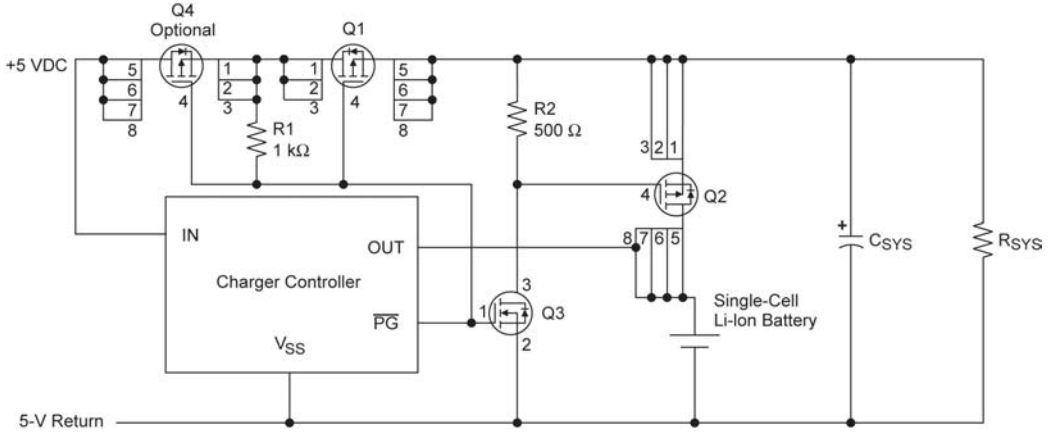


Fig. 13. Stand-alone battery charger controls power to system and battery

- Circuit operation
  - 5-V input source powers the charger directly and the system via transistors Q4 and Q1
  - Q3 and Q2 are off as long as the charger output is supplying current
  - If input power is lost, Q1 and Q4 turn off and Q3 and Q2 turn on, which are controlled by the PG (power good) pin. This action ties the battery to the system
  - Shoot-through current is minimized since both switches are passing through their linear state during the transition

Switching From Adapter to Battery Power (cont)

- Advantages
  - Charger circuit is able to manage battery charge current and charge battery properly
  - System receives 100% of power from the input, improving power conversion efficiency

- New challenges
  - Switching from adapter to battery power
    - Connecting battery to system prior to disconnecting input
      - A minimum system capacitance is needed
      - Shoot-through current occurs if adapter voltage is different than battery voltage
    - Connecting battery to system after input connection to battery is broken
      - Needs a large capacitor for system holdup
      - Avoids shoot-through currents between power sources

Conclusions

- Linear vs. switcher charger
  - A linear design is preferred for
    - Single Li-ion cell charging
    - Low-overhead-voltage designs, $V_{IN} – V_{OUT}$
    - Low-noise designs with few components
  - A switcher design is preferred for
    - Multiple-cell, higher-power designs
    - Large-overhead designs, $V_{IN} – V_{OUT}$ is > 2 V
- Hot plugging
  - Minimize the inductance of any current (power line) carrying conductor
  - Identify the main current carrying conductors that can be abruptly disconnected and verify that there is sufficient filtering or clamping to avoid excessive voltage spikes
  - Breaking the connection of an inductive loop will result in larger voltage spikes across high-impedance components
- Charging with a system load
  - There are many issues with connecting the system load across the battery
    - Charger delivers less power the lower the battery voltage
    - Charger cannot make the proper taper and termination decisions
    - Transients could cause the battery to terminate early
  - Connecting the system load to the input eliminates most issues. The main decision is whether to implement make-before-break or break-before-make switching

Design Trade-offs for Switch-Mode Battery Chargers

Jose Formenti
Robert Martinez

Design Trade-offs for Switch-Mode Battery Chargers

Why do we need specialized DC/DC converters to charge a battery?

- The charger must be designed to work with a battery as a load. A battery is a dynamic load with sink/source capability, its characteristics are dependent on the charge state

- Possible problems when using a standard converter
  - Stability issues on distinct charge regions
  - Battery discharge happens instead of battery charge
  - Charge never starts, system lockout
  - Charger parasitic leakage paths cause system failure/damage

To implement a reliable battery charging system the converter must have additional functions to support battery charging!

Design Trade-offs for Switch-Mode Battery Chargers (cont)

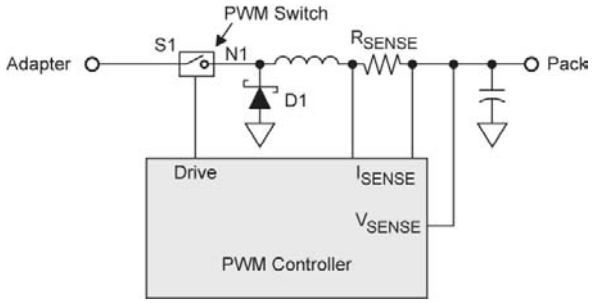
- Topics to be discussed
  - Selecting a DC/DC converter topology
    - High-side FET selection: PMOS vs. NMOS
    - Synchronous vs. nonsynchronous rectification
  - Power dissipation vs. switching frequency trade-offs
  - Unique converter design requirements for DC/DC battery chargers
    - Preventing battery discharge
    - Battery behavior as a load
    - PWM control schemes
  - Unique system design requirements for DC/DC battery chargers
    - Preventing AC adapter failure modes
    - Optimizing AC adapter power usage
    - Charger startup issues
    - Preventing battery charger failures

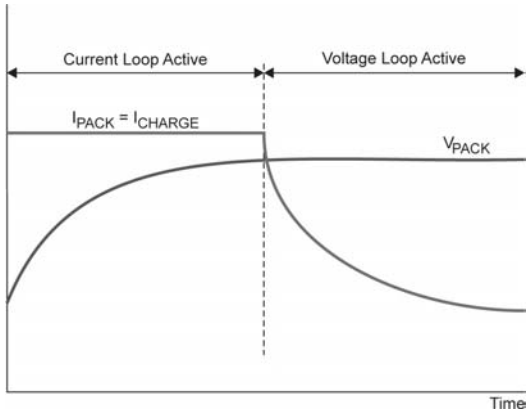
Selecting a DC/DC Converter Topology and Function Set

- System level design inputs to be considered when selecting a topology
  1) Charge current level
  2) Operating ambient temperature and maximum power dissipation for controller and external switches
  3) AC adapter input range
  4) Output voltage range
  5) Target PCB area
  6) Resources available on the system to implement power management functions

- Items 1) through 5) define converter power-stage topology
- Item 6) defines level of controller complexity required

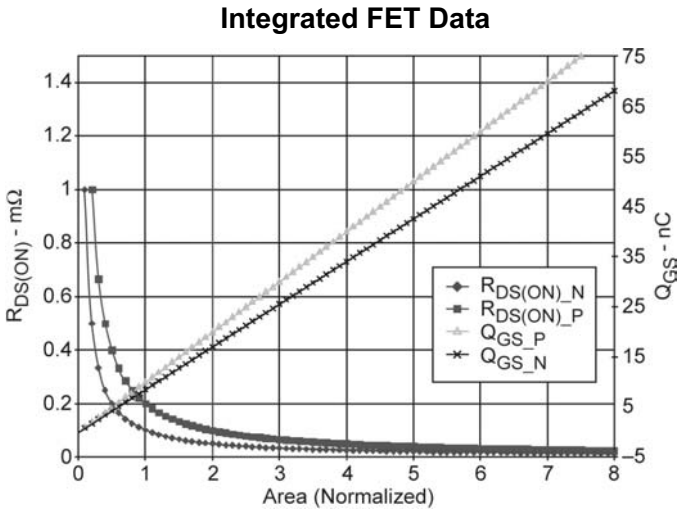
Design Options for a Switching Converter





- Minimum requirements
  - Voltage loop to regulate charge voltage
  - Current loop to regulate charge current
  - Input voltage range compatible with AC adapter used in application
- What we need to define
  - High-side switch type – NMOS or PMOS?
  - Converter topology – Synchronous or nonsynchronous?
    (Applications where $V_{IN} > V_{BAT(max)}$)

Selecting a High-Side Switch



Usually NMOS devices are selected for higher current designs to minimize overall power dissipation and use smaller, high current inductors commercially available!

Comparing PMOS and NMOS devices with same $R_{DS(ON)}$

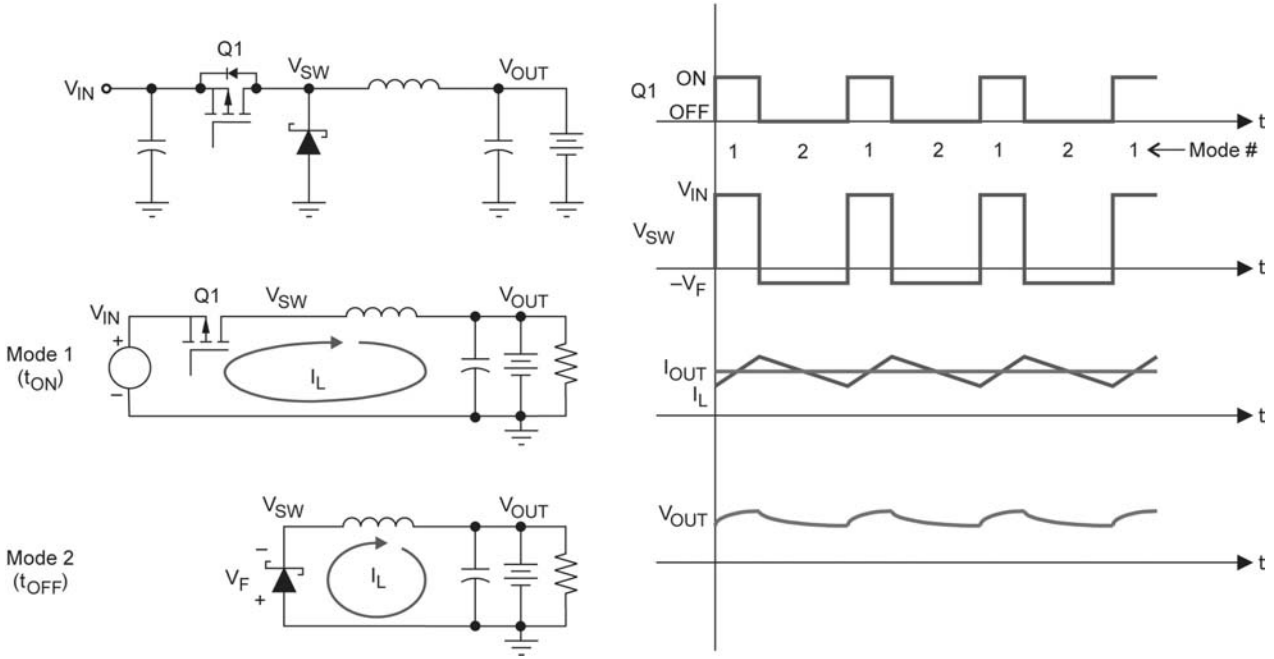
- PMOS devices
  - Simple controller driver requires fewer external components
  - 100% max duty cycle
  - Operates at lower switching frequencies, inductor and capacitor have larger size
  - Higher cost
- NMOS devices
  - Lower cost
  - Operates at higher switching frequencies, reducing inductor and capacitor size
  - Controller driver is more complex and requires additional external components
  - < 100% max duty cycle

Nonsynchronous Topology, PMOS High-Side Switch

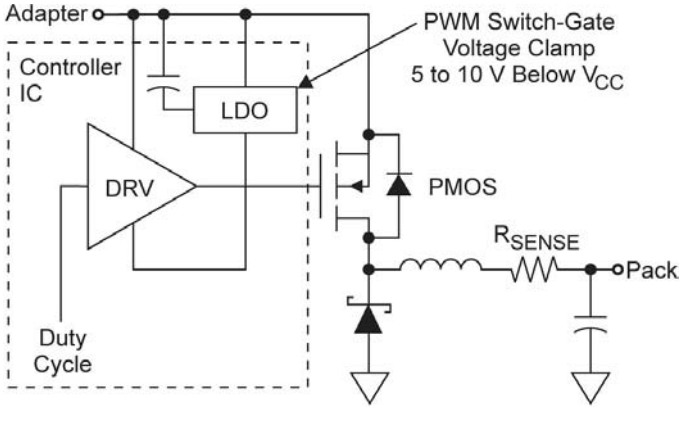
Nonsynchronous operation modes and waveforms

Mode 1: Charge inductor

Mode 2: Discharge inductor, freewheels through low-side diode



Nonsynchronous Topology, PMOS High-Side Switch (cont)



Nonsynchronous topologies are a good low-cost choice for low-current designs (3 to 4 A) where the end equipment can tolerate the power dissipation requirements!

◆ Advantages

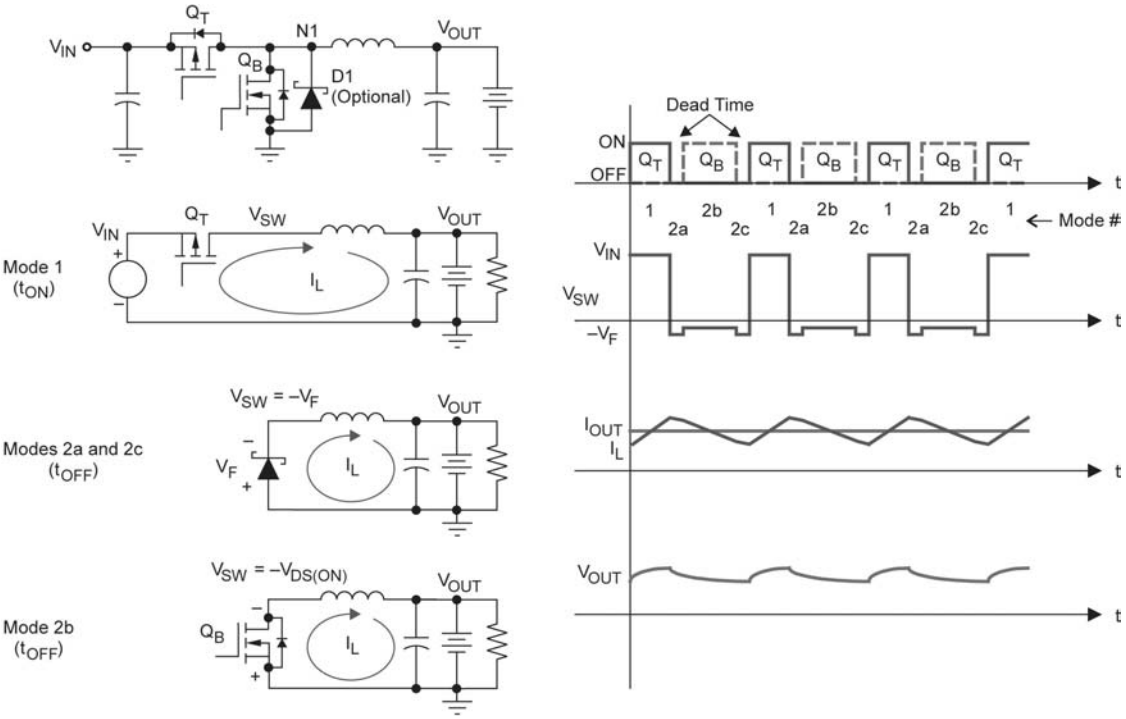
- 100% duty cycle
- Uses 20-V PMOS FETs (gate clamp)
- No shoot-through currents when switching high-side PMOS
- No parasitic paths from battery to ground

◆ Disadvantages

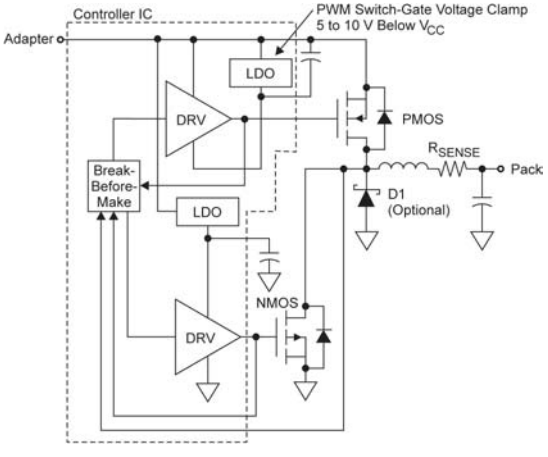
- Power dissipation in freewheeling diode
- Power dissipation in controller
- Low switching frequencies
- High inductor/capacitor values

Synchronous Topology, PMOS High-Side Switch

Synchronous operation modes and waveforms: Dead-time required to avoid cross-conduction



Synchronous Topology, PMOS High-Side Switch (cont)



Better power dissipation than non-synchronous; can operate at higher currents

Main limitation for high current designs: Controller power dissipation when using large PMOS FETs, large inductor availability

PMOS makes sense for lower currents & lower voltages with integrated solution

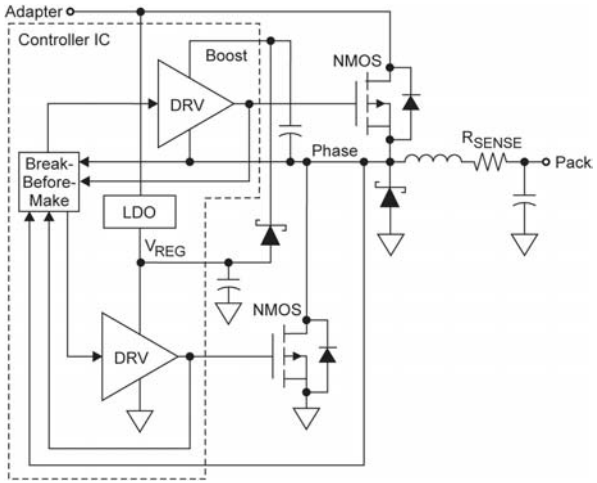
◆Advantages

- 100% duty cycle
- Uses 20-V PMOS FETs (gate clamp); bootstrap diode is not an issue
- Reduces power dissipation when compared to nonsynchronous topology

◆Disadvantages

- Power dissipation in controller
- Low switching frequencies
- High inductor/capacitor values
- Requires break-before-make on high/low-side drivers to avoid shoot-through currents
- Controller must turn off low side during start-up and taper to prevent battery discharge

Synchronous Topology, NMOS High-Side Switch



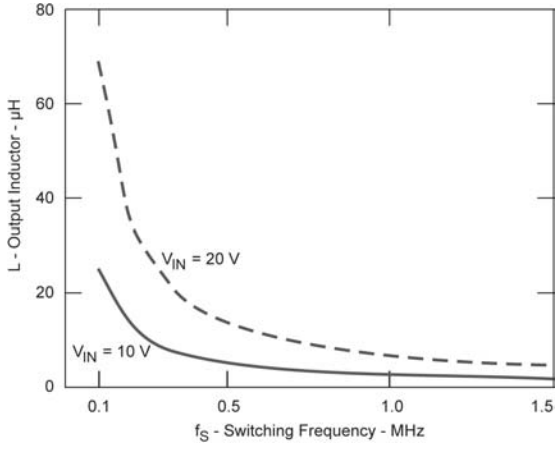
Best solution for high-current and/or low-power-dissipation designs!

The increase in complexity does not affect the user if DC/DC converters specifically designed for battery charge applications are used!

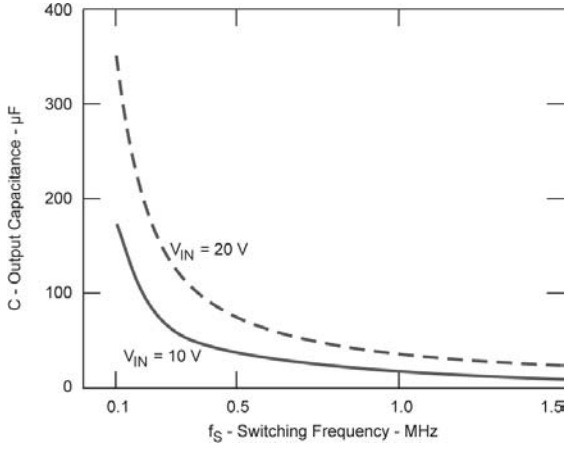
- Advantages
  - Low-cost NMOS used for high- and low-side FETs
  - Higher operating frequency decreases inductor/capacitor size
- Disadvantages
  - Maximum duty cycle below 100%
  - Requires additional circuitry in controller and application circuit to drive high-side NMOS
  - Requires break-before-make on high/low-side drivers to avoid shoot-through currents
  - Controller must turn off low side during start-up and taper to prevent battery discharge lockup

Switching Frequency x Power Dissipation Trade-offs

$$L = \frac{V_L \cdot \Delta t_{ON}}{\Delta I_L} = \frac{\left(V_{IN} - V_{OUT}\right) \cdot \left(\frac{V_{OUT}}{V_{IN} \cdot f_S}\right)}{\Delta I_L}$$

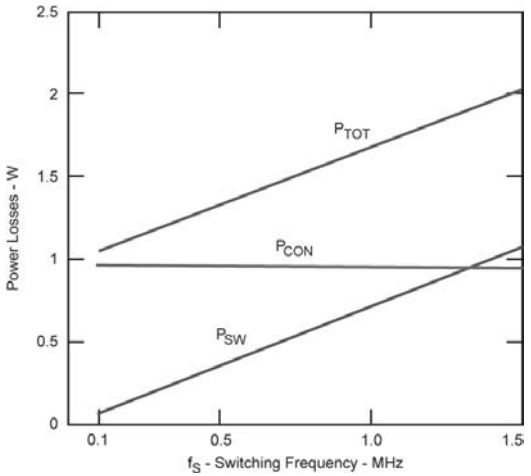


$$C = \frac{\Delta I_L \cdot \left(\frac{V_{OUT}}{V_{IN} \cdot f_S}\right)}{\Delta V_C}$$



- Advantage
  - Higher switching frequency reduces output filter inductor and capacitor values

Switching Frequency x Power Dissipation Trade-offs (cont)



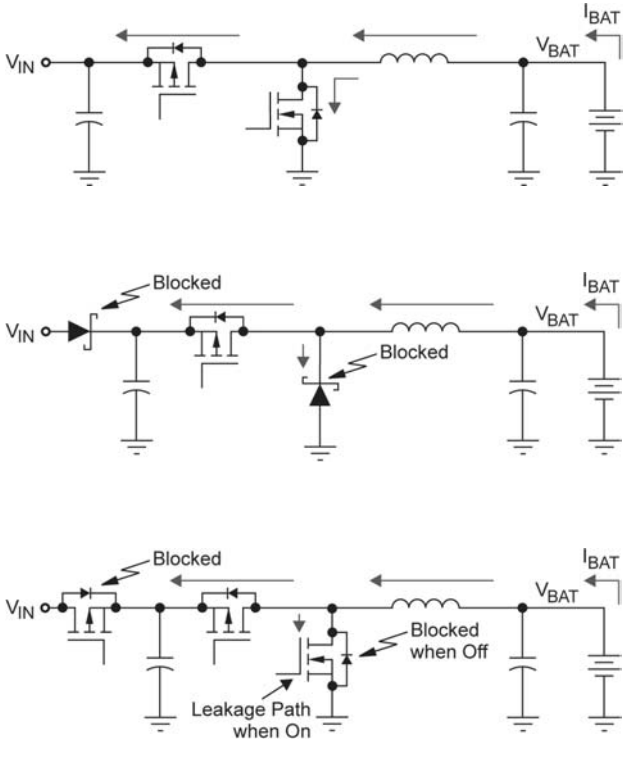
$$P_{TOT} = P_{CON} + P_{SW}$$

$$P_{CON} = P_{ON\_T} + P_{ON\_B} + P_{R_{SENSE}} + P_L + P_C$$

$$P_{SW} = P_{SW\_T} + P_{SW\_B} + P_{SCH} + P_{GD}$$

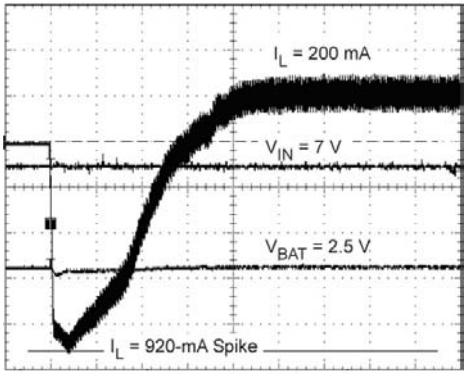
- Disadvantages
  - Power dissipation increases as switching frequency increases due to higher switching losses
    - High-side FET is dominant switching loss
    - Low-side FET has negligible switching losses, except for Q_{RR} and C_{OSS}
    - Gate drive losses for both high side and low side are dissipated within the IC driver and regulator
  - Conduction losses affected little by the switching frequency
    - Low-side power FET losses are primarily conduction
    - For large duty cycles, the high-side FET will dominate conduction losses

Avoiding Undesired Battery Discharge

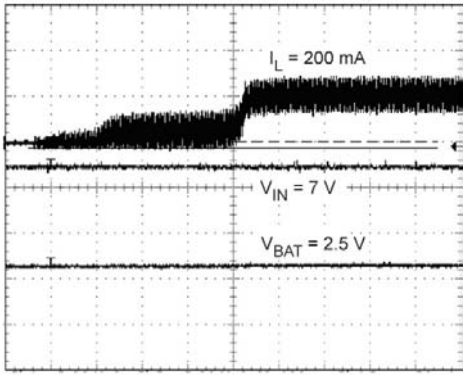


- DC/DC discharge paths
  - From battery to input – through inductor and high-side FET
  - From battery to power ground – through inductor and low-side FET
- Protection required
  - From battery to input
    - Put Schottky diode – but conduction losses increase
    - Put PMOS FET – reduces conduction losses, but must synchronize switching
  - From battery to power ground
    - Put Schottky diode – but conduction losses increase
    - Put NMOS FET – reduces conduction losses, but must synchronize switching

Avoiding Undesired Battery Discharge (cont)



Time - 50 µs/Div

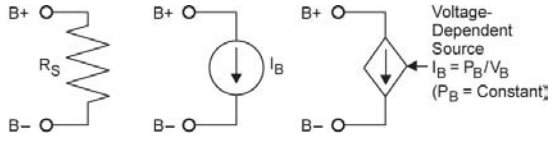


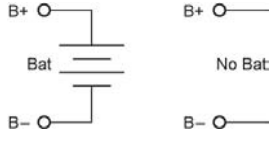
Time - 100 µs/Div

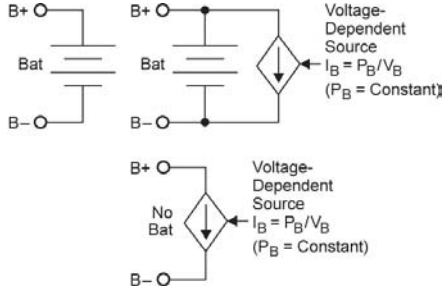
- Allowing low-side NMOS FET to leak reverse current causes large negative current discharge spikes when powering up. Continuous inductor current always switching

- Turning-off low-side NMOS FET before the current is allowed to reverse prevents the large negative current discharge spikes when powering up. High current operation is continuous. Low current operation is discontinuous

The Battery as a Unique Load



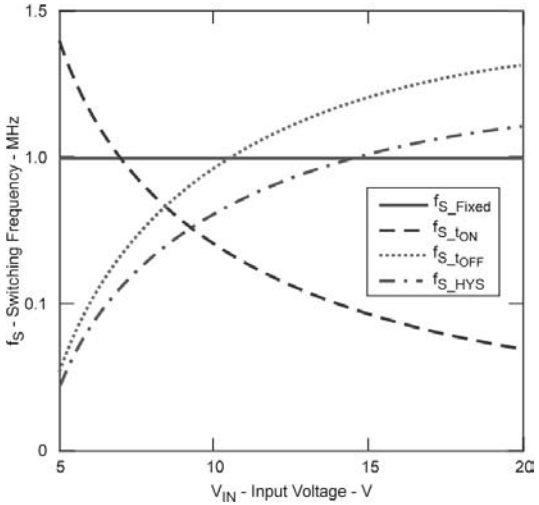




Battery looks like an inductor in series with a resistor in small signal analysis

- Typical DC/DC load
  - Resistor
  - Constant current
  - Constant power
- Typical cradle charger load
  - Battery
  - No battery
- Typical embedded charger load
  - Battery
  - Battery and constant power
  - Constant power and no battery

Trade-offs in PWM Control Scheme

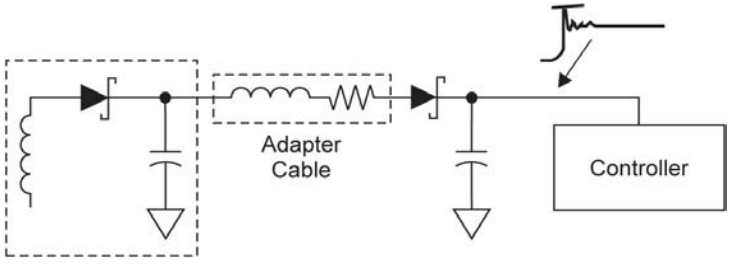


$$f_{S\_t_{ON}} = \frac{D}{t_{ON}} \qquad f_{S\_t_{OFF}} = \frac{1-D}{t_{OFF}}$$

$$f_{S\_HYS} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{L \bullet \Delta I_C \bullet \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{OUT}} \right)}$$

- Constant frequency – switching frequency is always fixed, irrespective of operating conditions
- Constant on-time – switching frequency decreases as input voltage increases
- Constant off-time – switching frequency increases as input voltage increases
- Hysteretic – both on-time and off-time varies. Switching frequency increases as input voltage increases

Preventing AC Adapter Related Failure Modes

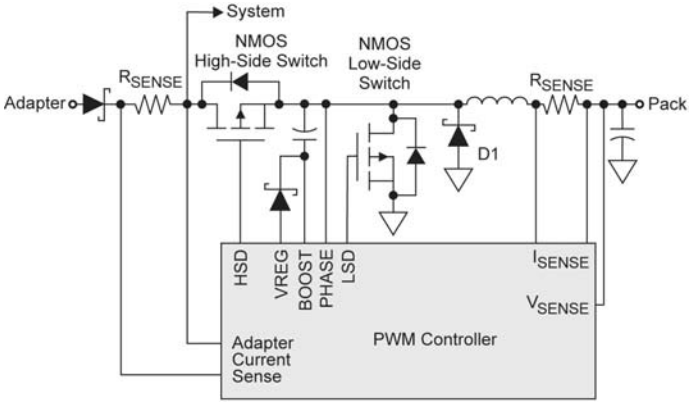


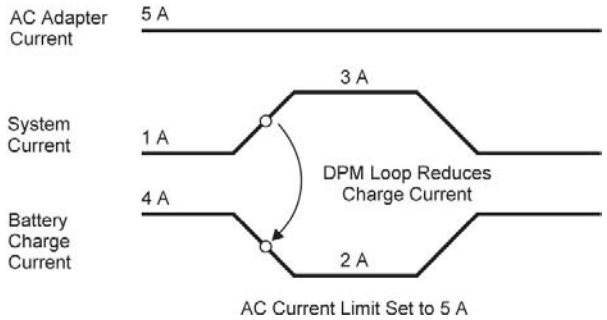
To prevent those failure modes

1) *Characterize the voltage overshoot at controller positive supply line when hot plugging a real adapter (with real cable) into the system and make sure it is below the maximum voltage ratings for controller and power stage switches*
2) *Design the system so a blocking diode or FET is always present, as shown above, when adapter is not powering the system*

- Problem description
  - PWM controller is damaged after adapter insertion or removal
  - PWM high-side switch is damaged
- Possible root causes for failures
  - Positive supply voltage overshoots when adapter is hot-plugged into system, causing controller or switch to operate outside their SOA
  - System design allows for a parasitic discharge path from system to ground, through the PWM high-side switch, when adapter is removed

Optimizing AC Adapter Power Usage

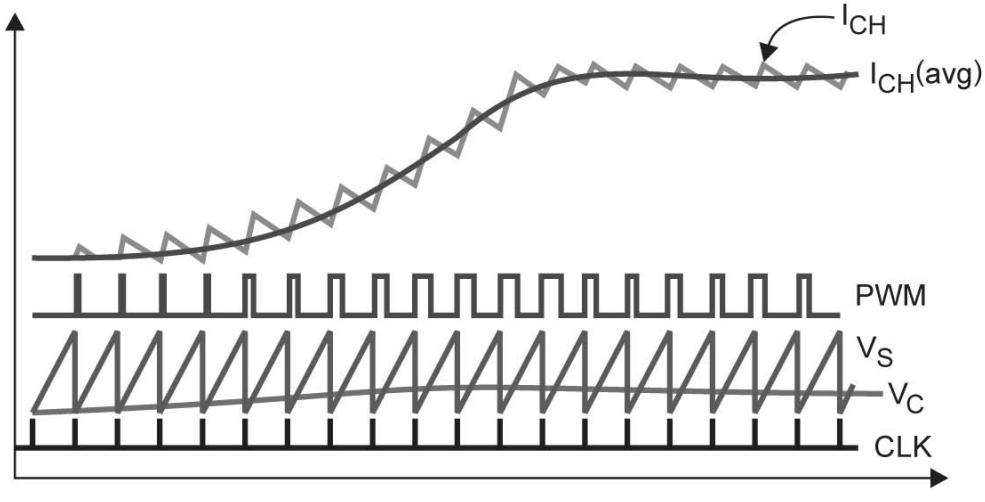




AC Current Limit Set to 5 A

- Adapter cost increases when the adapter must supply system current and charge current when pack is being charged and system is running
- To optimize adapter power usage
  - Monitor the current being supplied by the adapter to the system
  - When the adapter current reaches the maximum allowable limit reduce the charge current
  - This method is called DPM (dynamic power management)

Charger Start-up



- Any battery charger must have a controlled start-up mode (soft start) to avoid undesired current transients into the battery
- Requirements
  - Ramp up the charge current slowly
  - The soft start should ALWAYS be enabled when a new charge cycle starts or when charge resumes (if suspended)

Battery Chargers 2nd Level Failure Protection Functions

Event	Detection/Action
Charge time exceeds normal charging time	Monitor converter on time; End charge
Battery pack temperature is out of range	Monitor pack thermistor; End charge
Converter IC temperature exceeds safe operating region	Monitor converter-IC junction temperature (thermal shutdown); End charge
Charge current exceeds target value while pack is connected	Monitor charge current; End charge
Voltage overshoot at pack removal when charger is on (due to loop delay)	Detect pack removal; End charge
Pack cell or pack terminal short circuited; or pack opens, resulting in low pack visible voltage	None; Design PWM loop with ground-compatible common-mode range
High-side switch is damaged due to thermal overload and shorts adapter to pac	Monitor charge current; Add additional on/off switch in series with high-side device to isolate pack from adapter
Overvoltage condition occurs	Detect output voltage above target voltage; End charge

MUST HAVE **OPTIONAL**

Optimizing Low-Power DC/DC Designs – External versus Internal Compensation

Michael Day

Product Development

- Traditionally, each engineer had a specific area of expertise
  - Processor
  - Interface
  - Programmer
  - Power supply
- Today, one engineer may have to do it all

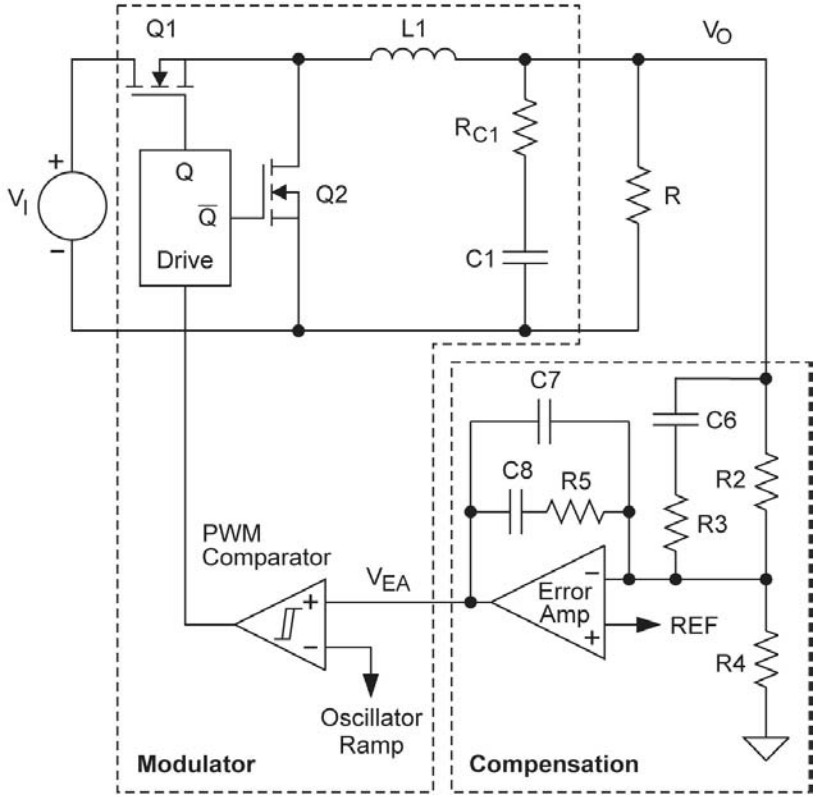
Traditional Power Supply Design

- Power supply given only to the “experts”
- Considered “black magic”
  - Discrete components selection
  - FET capacitances
  - Switching waveforms
  - Critical layout issues
  - Magnetic design
  - Loop compensation
  - Fairly long, complicated design process

Modern Power Supply Design

- Integrated ICs eliminate the need for
  - FET selection
  - Compensation
  - Magnetic design
- Simplify and shorten the design process
- You still need to understand
  - How the supply operates
  - The effect of modifying the external components

Basic Buck Converter



Voltage-mode control implementation for synchronous buck converter with external pole-zero compensation

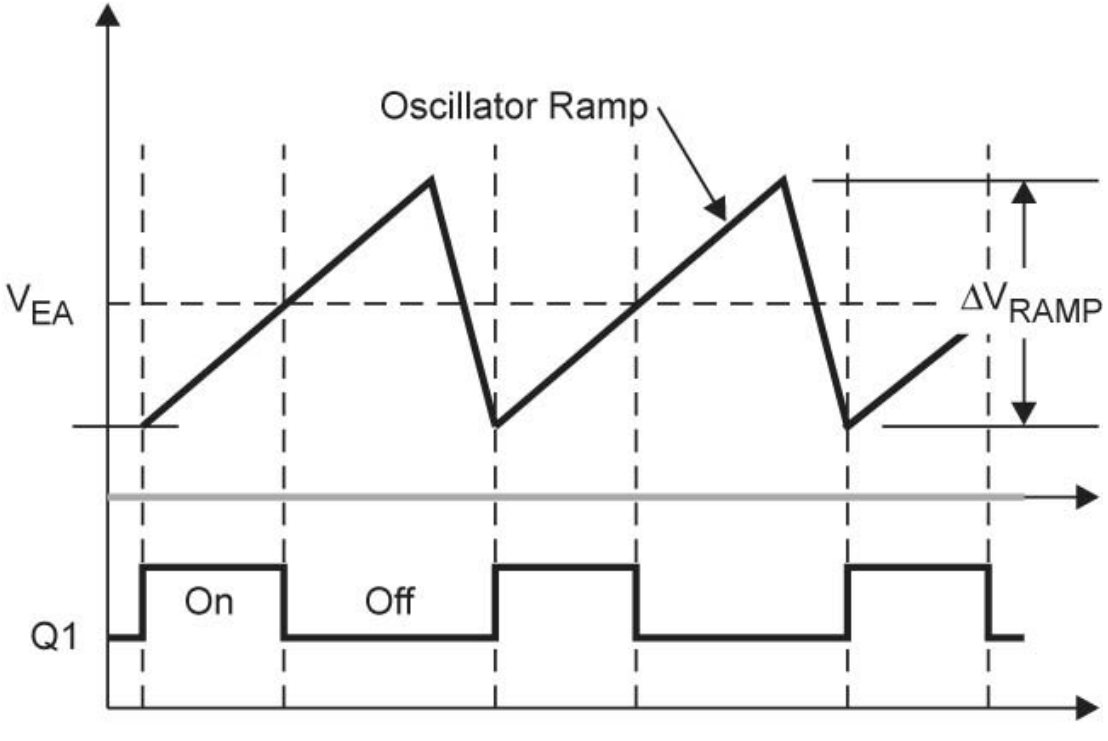
Compensation

- Power supply is a closed loop system
- The feedback loop ensures that the output voltage is constant and independent of variations in
  - Input voltage
  - Load current
- The feedback loop “compensates” for changes in the input voltage or load current

Compensation (cont)

- DC modulator gain
- $$G_{MOD\_DC} = \frac{V_{IN}}{\Delta V_{RAMP}}$$
- Voltage feedforward
  - Eliminates gain with changes in input voltage
  - Simplifies compensation
  - Improves transient response

Compensation (cont)



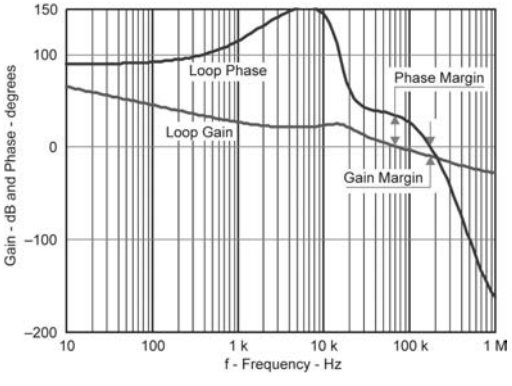
Modulator operation waveforms

Compensation (cont)

- AC modulator gain
  - Function of the external L and C values
  - $$G_{MOD\_AC} = \frac{1 + j \cdot \omega \cdot C1 \cdot R_{C1}}{1 + j \cdot \omega \cdot C1 \cdot R_{C1} + (j \cdot \omega)^2 \cdot L1 \cdot C1}$$
- Total modulator gain is the product of G_{MOD_AC} and G_{MOD_DC}

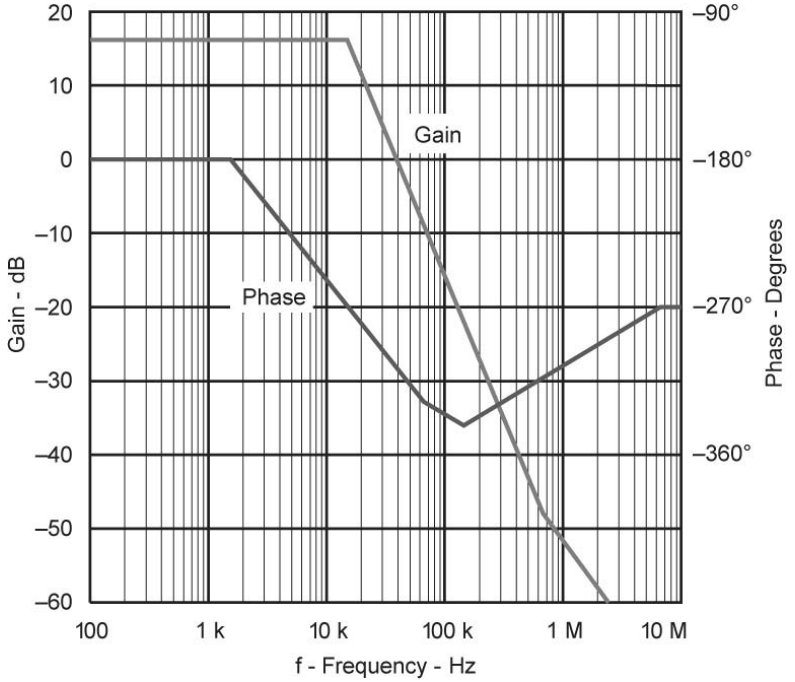
Stability

- **Gain margin:** The difference between unity gain and the actual power supply gain at the frequency where the phase reaches 180º
- **Phase margin:** The difference between 180º and the actual power supply phase when the gain reaches 0 dB



- **Stability criteria:** A minimum value for both the gain and phase margin of a power supply. In power supply design, a power supply is typically defined to be stable if the gain margin is greater than 6 dB and the phase margin is greater than 45º. The requirement for stability is typically met if the overall gain crosses 0 dB with a slope of –20 dB/decade

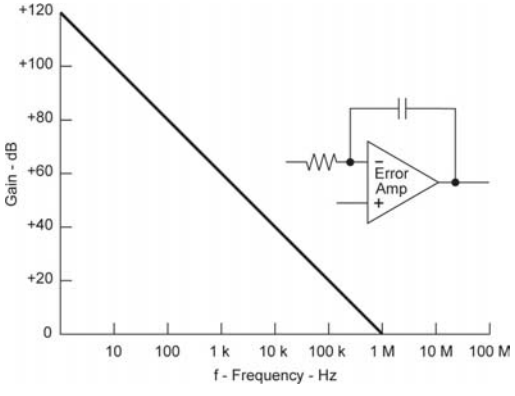
Example Modulator Response



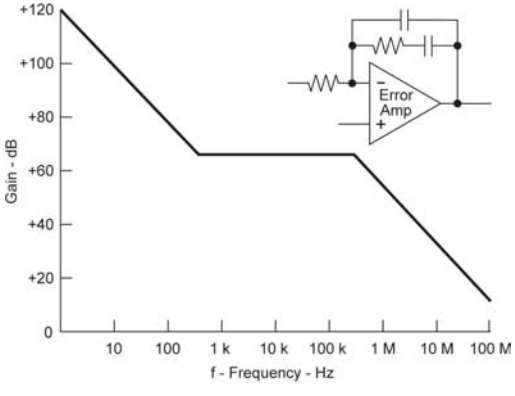
Bode plot of G_{MOD} showing the gain and phase

- V_{IN} = 6 V
- V_{RAMP} = 1 V
- L_{OUT} = 10 µH
- C_{OUT} = 10 µH
- R_{ESR} = 25 mΩ

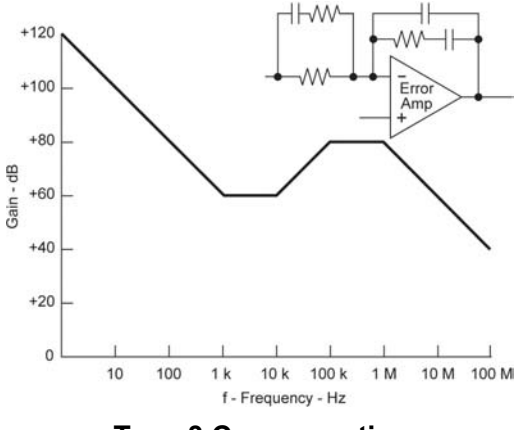
Types of Compensation



Type 1 Compensation



Type 2 Compensation



Type 3 Compensation

Power Supply Design Example

- Requirements
  - V_{IN} = 3 V to 8 V ⇨ Li-Ion (3.0 to 4.2 V) or AC wall adapter (5 to 8 V)
  - V_{OUT} = 1.8 V ⇨ Processor core voltage
  - I_{OUT} = 600 mA
  - V_{Ripple} = 25 mV

Power Supply Controller Design Steps

- Choose an IC
- Choose a switching frequency (500 kHz is a good start)
  - Higher frequency
    - Smaller layout
    - Lower efficiency
  - Lower frequency
    - Larger layout
    - Higher efficiency
- Choose inductor value
  - Sets ripple current
  - Ultimately determines required capacitance and ESR

Power Supply Controller Design Steps (cont)

- Select inductor part number
  - Tolerance
  - Resistance
  - Saturation current
- Calculate max ESR and min capacitance
- Select capacitor
- Examine overall power stage solution
  - Size
  - Ripple
  - Cost
  - Efficiency

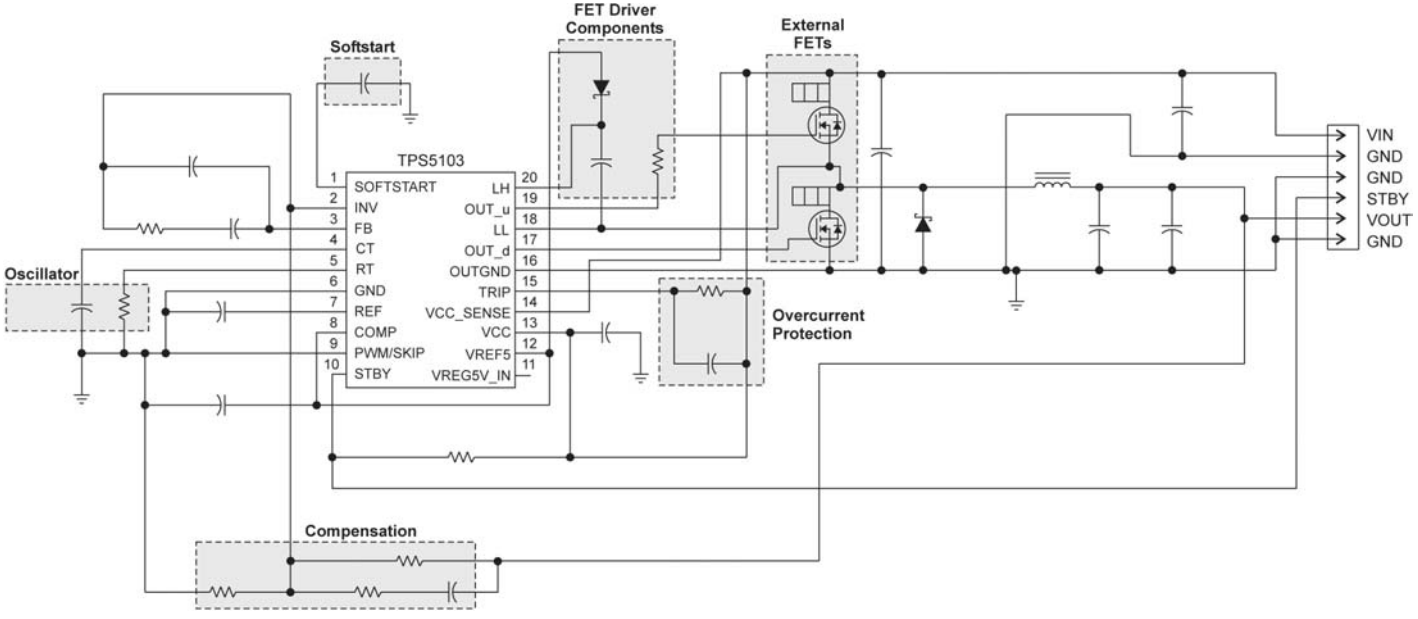
Power Supply Controller Design Steps (cont)

- Repeat previous steps
  - Optimization may require several iterations
- Calculate modulator gain
- Choose overall supply response
- Calculate the required error-amplifier gain

Power Supply Controller Design Steps (cont)

- After choosing the poles and zeroes for the compensation network, you must still
  - Ensure that variations in input voltage do not cause instability
  - Ensure that the crossover frequency is less than 1/10 of the switching frequency
  - Allow for variations in the peak-to-peak oscillator voltage
  - Ensure that the error amp has sufficient attenuation at the switching frequency so it does not amplify the output voltage ripple and cause subharmonic oscillations
  - Ensure that the midfrequency gain is greater than zero to prevent a large overshoot at turn-on and during transient conditions
  - Ensure that the error amp has the drive capability to properly drive the feedback network

Power Supply Controller Solution

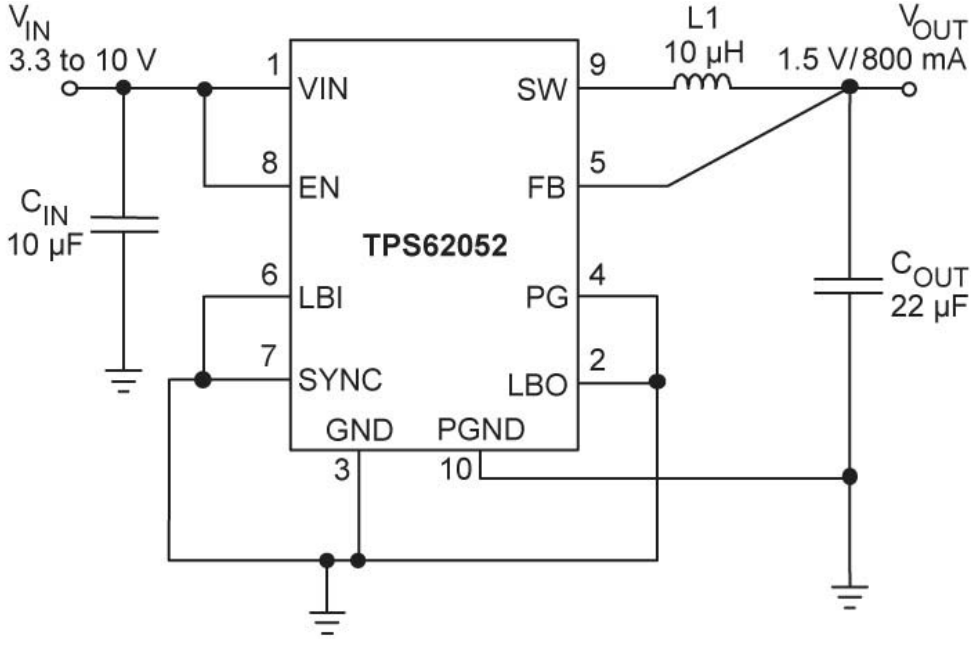


Schematic of TPS5103 solution

Power Supply Converter Design Steps

- Choose an IC that meets the V_{IN}, V_{OUT}, and I_{OUT} requirements
- Choose an external inductor and capacitor from the list of recommended components in the datasheet
- Verify that the design meets the ripple requirements

Power Supply Converter Solution



Integrated TPS62050 solution

Difference Between Two Designs

◆ Controller

- Designer has control over all aspects of the design
  - Switching frequency
  - Component selection
  - Loop response
- Fairly complex design process
- Long design time

◆ Converter

- Little control over any aspect of the design
  - Fixed frequency
  - Fixed component selection
  - Internal compensation
- Simple design process
- Short design time

Integrated Power Supply ICs

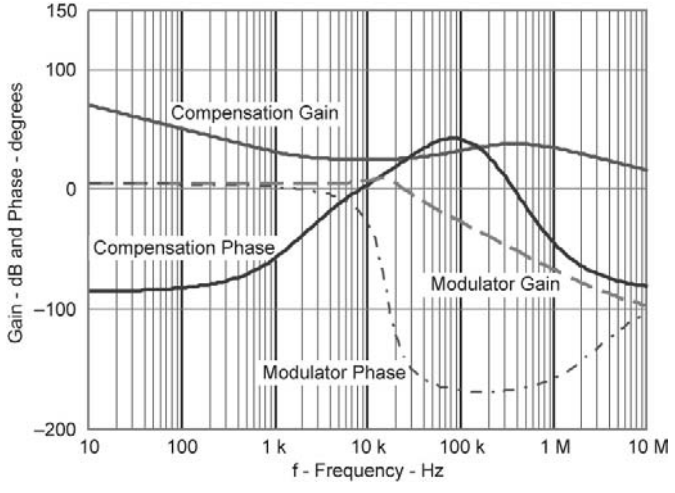
- If everything is fixed, what control does the designer have over the design?
- Stability?
- Transient Response?
- Size?
- Efficiency?

Stability

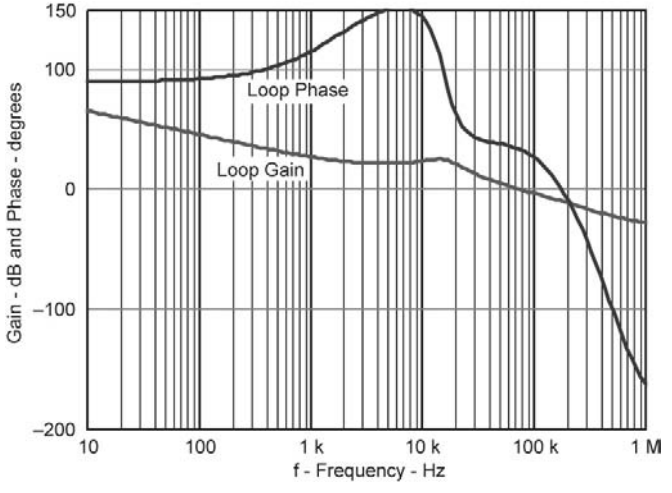
- Proper external filter component selection is required for stability
- Datasheet provides recommended values
- You can change external filter values
  - Optimize efficiency
  - Optimize size
  - Transient response

Stability (cont)

- Careful examination reveals that the LC filter pole must be less than 24 kHz



Compensation and filter response of an internally compensated power-supply IC



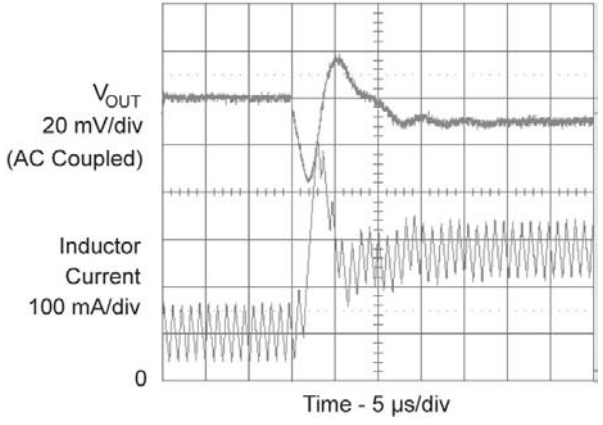
Overall power-supply response with the recommended 10-µH and 10-µF output filter

Stability (cont)

L (μH)	C (μF)	Pole (kHz)	Pole with 20% Tolerance (kHz)	Result
10	4.7	23.2	29.0	Unstable
15	4.7	19.0	23.7	Marginally Stable
22	4.7	15.7	19.6	Stable
10	10	15.9	19.9	Stable
6.8	10	19.3	24.1	Marginally Stable
4.7	10	23.2	29.0	Unstable
2.2	22	22.9	28.6	Unstable
4.7	22	15.7	19.6	Stable
6.8	22	13.0	16.3	Stable

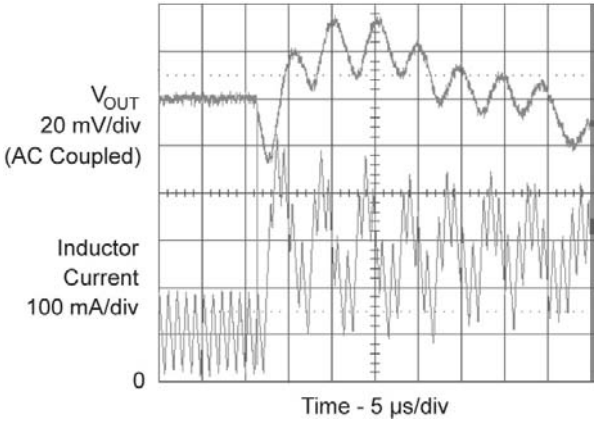
Stability (cont)

- 15.9 kHz to 19.9 kHz is stable



Transient response of stable, internally compensated power supply with 10-µH and 10-µF output filter

- 23.2 kHz to 29.0 kHz is marginally stable



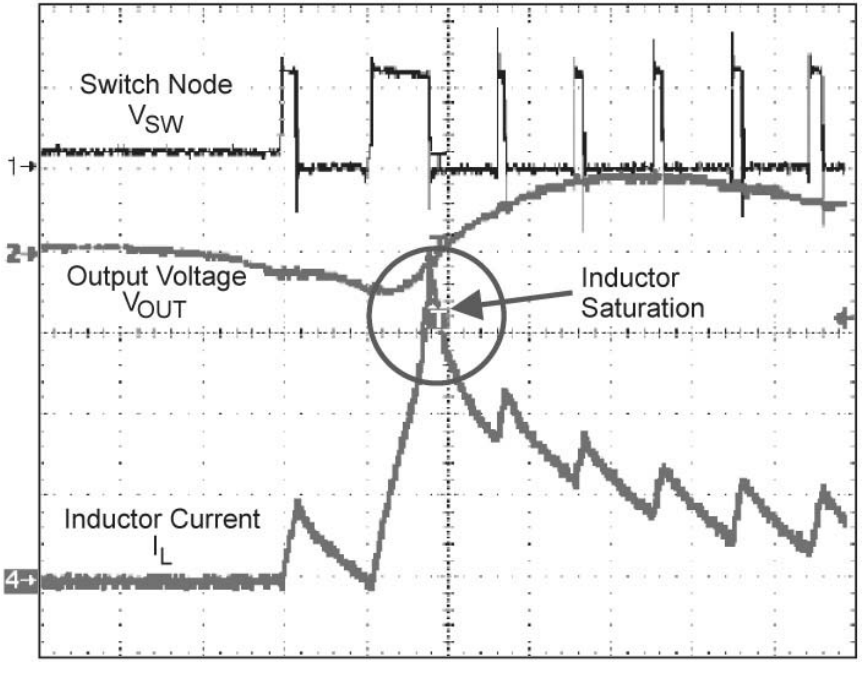
Transient response of unstable, internally compensated power supply with 4.7-µH and 10-µF output filter

Optimizing Inductor

- Reducing Size
  - Larger series resistance
  - Possible saturation issues
- Increasing Efficiency
  - Physically larger size
  - Smaller series resistance

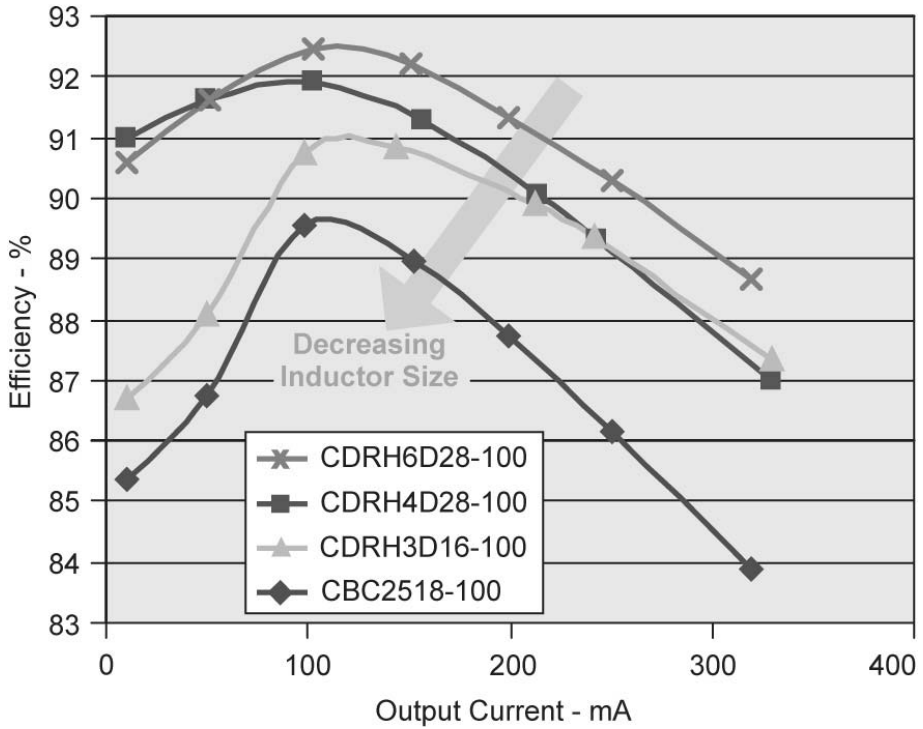
Saturated Inductor

- Physically smaller inductor with lower saturation current



Transient response with inductor current entering saturation

Optimized for Efficiency



Reduction in efficiency versus decreased inductor size

Peak Current

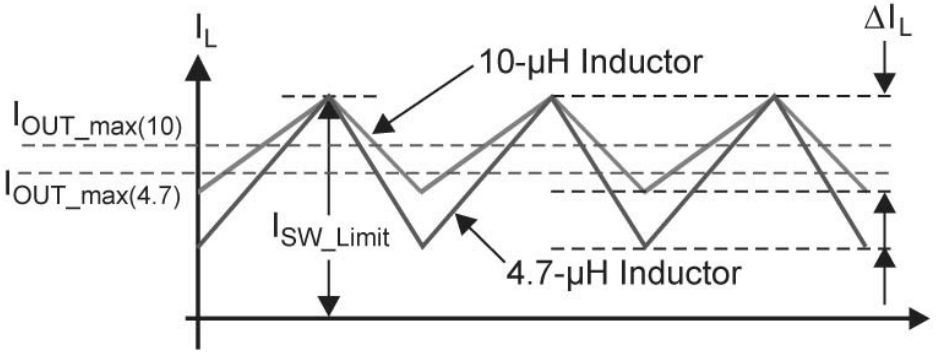
- Lower inductance = higher ripple current
- Higher inductance = lower ripple current

$$\Delta I_{Inductor} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L_{OUT} \cdot f_{Oscillator}}$$

- Maximum output current set by
  - Fixed peak FET current
  - Inductor ripple current

Peak Current (cont)

$$I_{OUT\_max} = I_{SW\_Limit} - \frac{\Delta I}{2}$$



Effects of inductor on output current

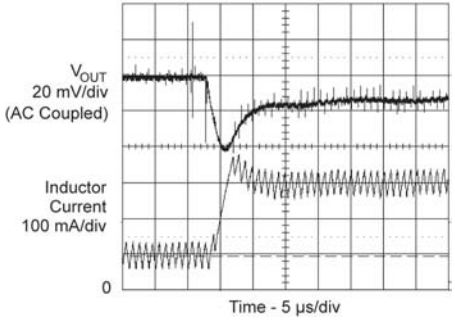
- Assume V_{IN} = 5 V, V_{OUT} = 1.5 V, I_{SW_PK} = 380 mA

L ➔ 10 µH	L ➔ 4.7 µH
ΔI = 105 mA	ΔI = 224 mA
I_{OUT_max} = 328 mA	I_{OUT_max} = 268 mA

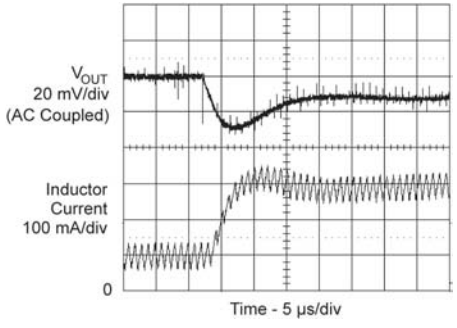
Transient Response

- Lower filter output impedance = better transient response

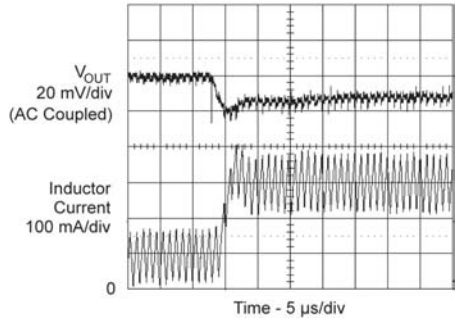
$$Z_{Filter} = \sqrt{\frac{L}{C}}$$



Transient response with a 10-µH and 10-µF filter



Transient response with a 10-µH and 22-µF filter



Transient response with a 4.7-µH and 22-µF filter

Total Solution Size

- Low-power supplies
  - Integrated solutions typically provide smaller solutions
  - External FETs and compensation components are a large percentage of total supply area
- High-power supplies
  - Discrete solutions typically provide smaller solutions
  - External compensation allows optimization of power stage
  - External compensation is a small percentage of overall solution size

Total Solution Size (cont)

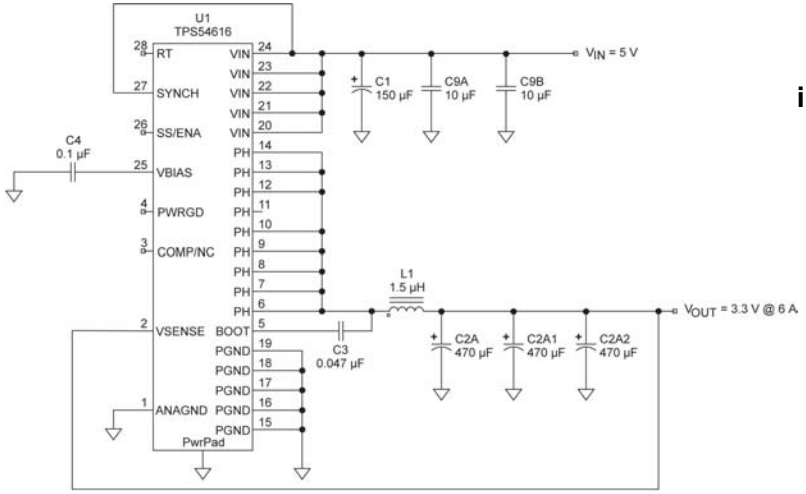
Externally compensated TPS54610

versus

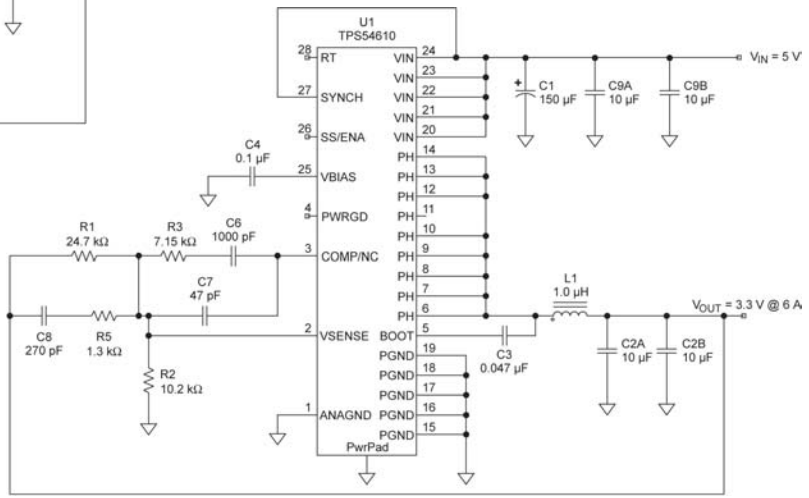
Internally compensated TPS54616

V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 5 A

Total Solution Size (cont)

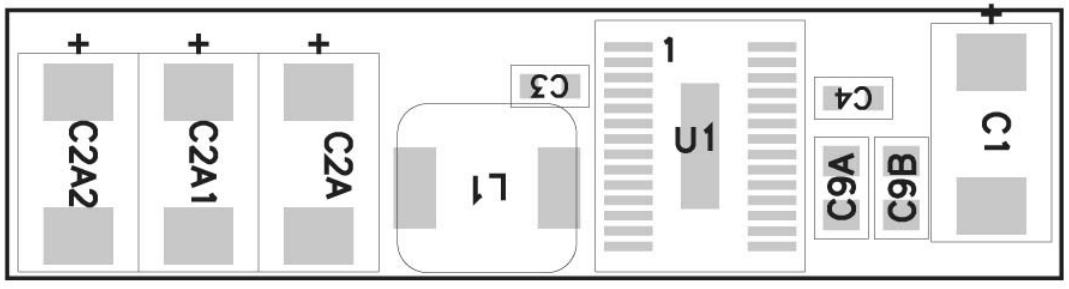


Typical supply with internal compensation

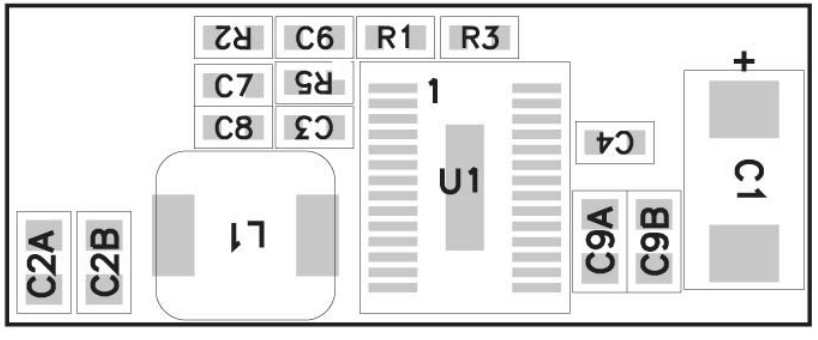


Typical supply with external compensation

Total Solution Size (cont)



Internal compensation (1.750 × 0.45 in)



External compensation (1.200 × 0.525 in)

Conclusion

- Stability is important
- Power-supply design is easier today
- Space, time and effort are reduced at the expense of flexibility
- Optimization is still possible for integrated supplies if you understand the trade-offs

Noise Management in Portable RF Systems

Ray Crampton
Dennis Hudgins
Dave Heisley

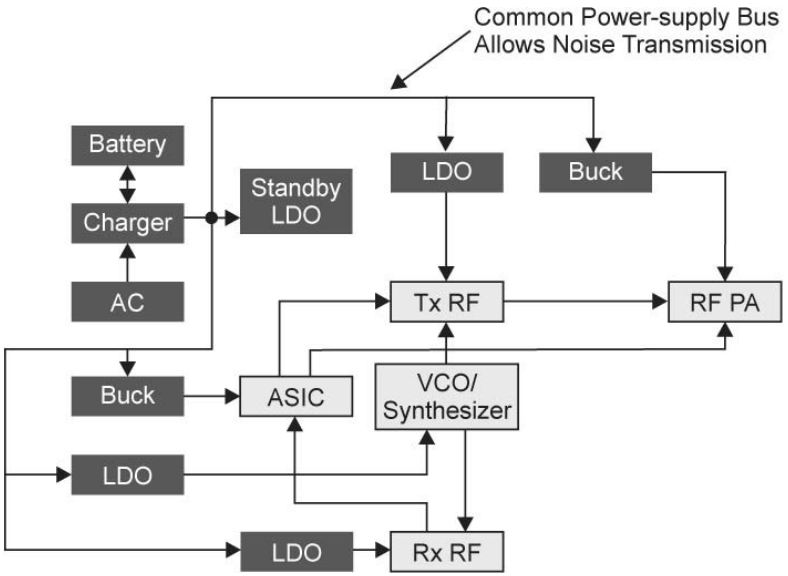
Introduction

Many portable RF applications have special noise requirements. The design of the power supply is an integral part of the overall management of these issues.

This paper will discuss technical challenges in typical portable RF applications and will offer suggestions for overcoming them.

- Cell phones
- WLAN 802.11 cards
- Bluetooth headsets
- Wireless barcode readers
- Wireless infrastructure

Typical Portable Wireless Block Diagram

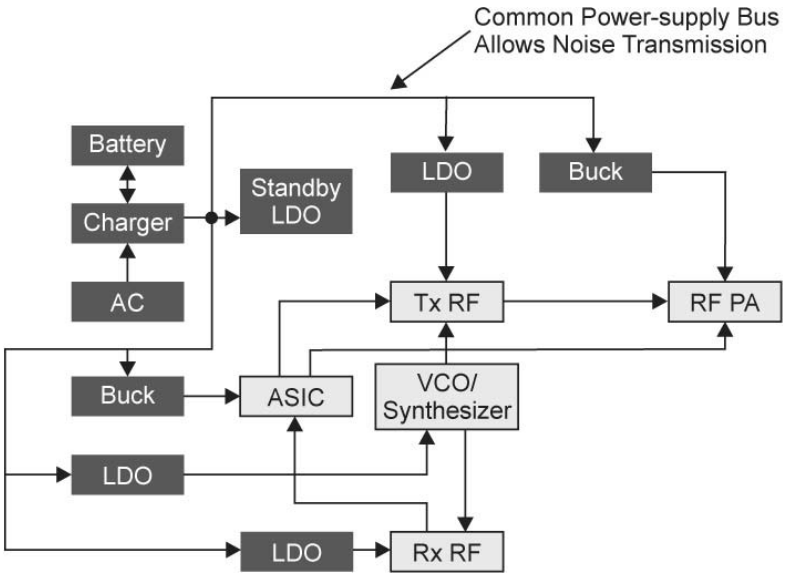


- Noise sources
  - AC power
  - RF oscillators
  - Regulators
  - External sources
- 3 ways noise couples
  - Electromagnetic coupling
  - Conduction through PCB traces
  - Conduction through ground plane

Troubleshooting Noise Problems

- Determine the noise source
  - Switching frequencies
  - RF oscillator frequencies
  - Unrelated external frequencies
- Determine coupling mechanism
  - Electromagnetic coupling
  - Conduction through PCB traces
  - Conduction through ground plane
- Fix the problem
  - Electromagnetic: Improve layout, add shielding
  - Conduction: Add noise filtering (capacitors, LDOs, ferrite beads)
  - Ground plane: Improve layout

Source Impedance Can Be a Noise Source

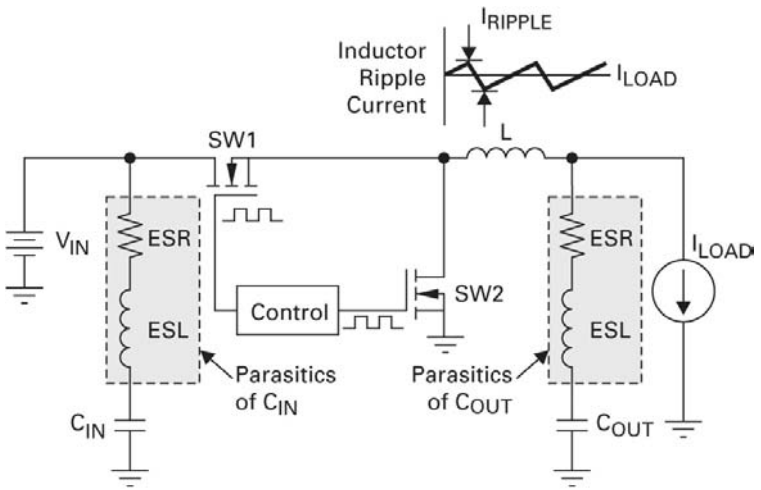


- Inductive part of source impedance causes voltage spikes on power supply line during load transients. This creates noise spikes and could even damage ICs
- Inductance sources
  - Battery is low-impedance with full charge but higher-impedance as it discharges
  - PCB traces, vias and interconnect wires add to battery or AC source impedance

Switched Mode Power Supplies

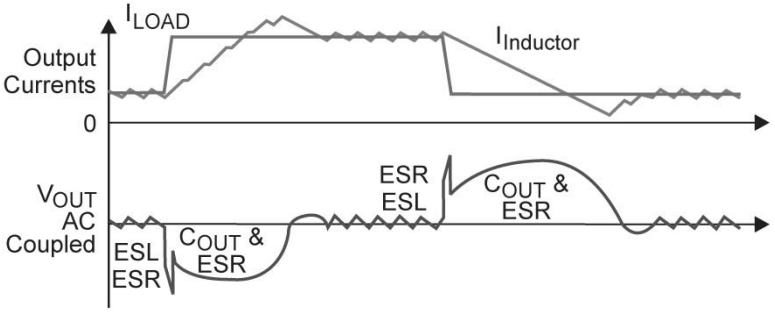
- Switched power supplies are becoming more widely used due to efficiency demands and improved power supply IC products
- These supplies may generate unwanted noise
- Noise may be present across a wide frequency range
- PCB layout, control loop characteristics, circuit topology, and bypassing largely determine how much noise is generated

Buck Regulator Topology Review



- Input is switched on and off at an appropriate duty cycle, then is filtered by an L-C to create a stable DC output
- Many noise sources are present in the circuit
  - Inductor current waveform
  - Switch gate waveform
  - ESR, ESL of input/output capacitors

Output Capacitor Selection and Load Transients



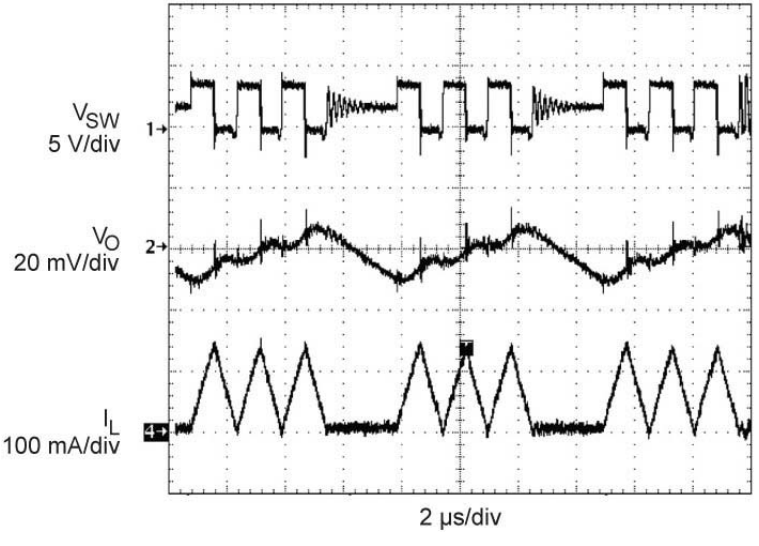
- ESL and ESR of output capacitor significantly affect noise spikes during load transients
- Smaller value inductors improve load transient response because inductor current can increase/decrease more quickly. Smaller inductors also have larger ripple current, possibly increasing radiated noise

Frequency Synchronized and Phase Offset Supplies

- Multiple switching supplies can be synchronized and phase-offset to minimize the peak to average load on their input bus. This reduces maximum current ratings of the input supply and reduces noise voltage magnitude on the common bus

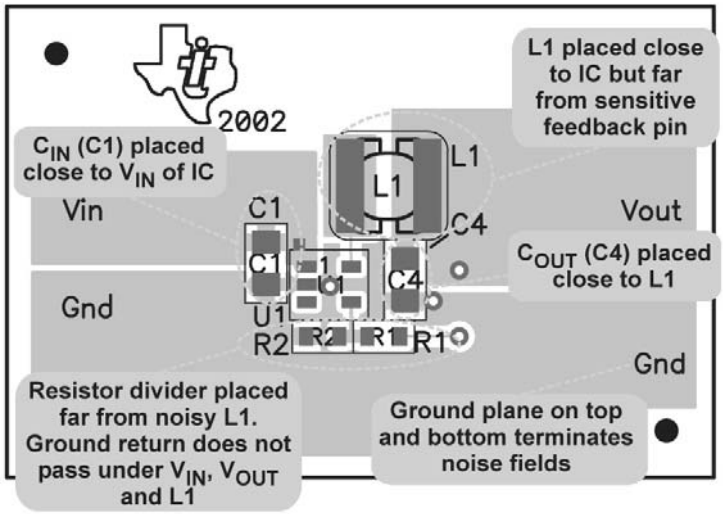
- Switching supplies can be synchronized to a common frequency to ease filtering of switching noise

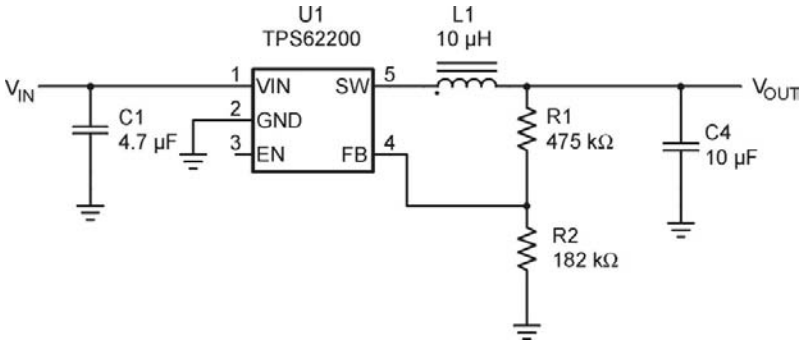
Power Savings Modes



- Many switched supplies utilize power savings modes to reduce supply current during low-load states
- Pulse-skipping is shown here. This reduces the number of times switch gates are charged/discharged which reduces supply current
- Pulse skipping does not change the switching frequency but it adds an additional, smaller magnitude spurious at a lower frequency

SMPS Layout Considerations

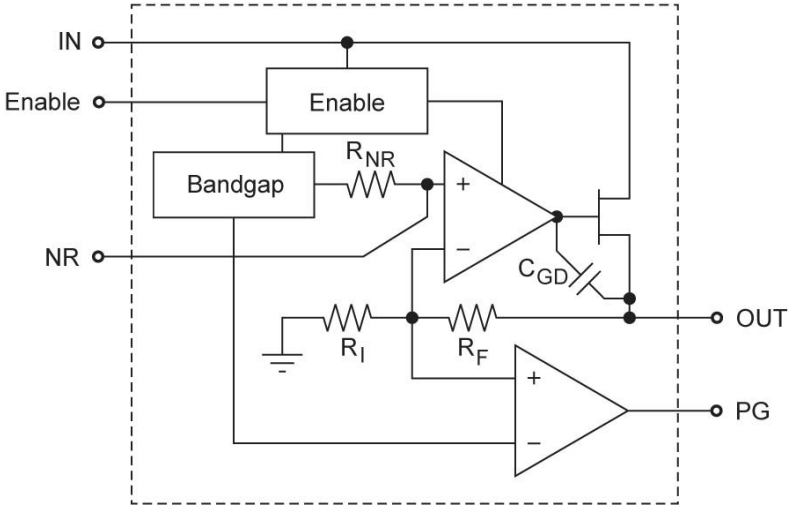




Linear Regulators

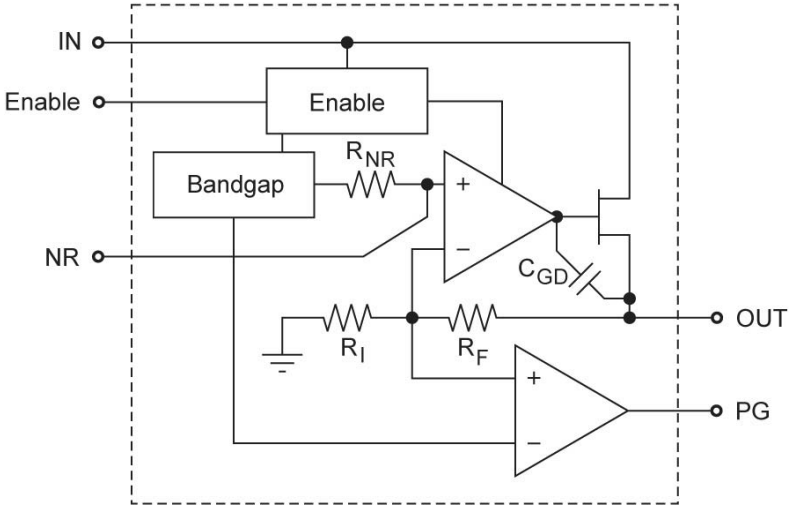
- Linear and low dropout (LDO) regulators generate far less noise than switched supplies, normally at the expense of efficiency
- Offer very high-power supply rejection, reducing the effects of noise at the input to the IC
- Transient performance is normally very good, resulting in more stable voltage rails during load changes
- Linear regulators are generally very easy to use and offer a very low solution price

Linear Regulators (cont)



- Close-loop feedback system that drives a pass transistor such that a scaled output voltage is equal to an internal reference voltage

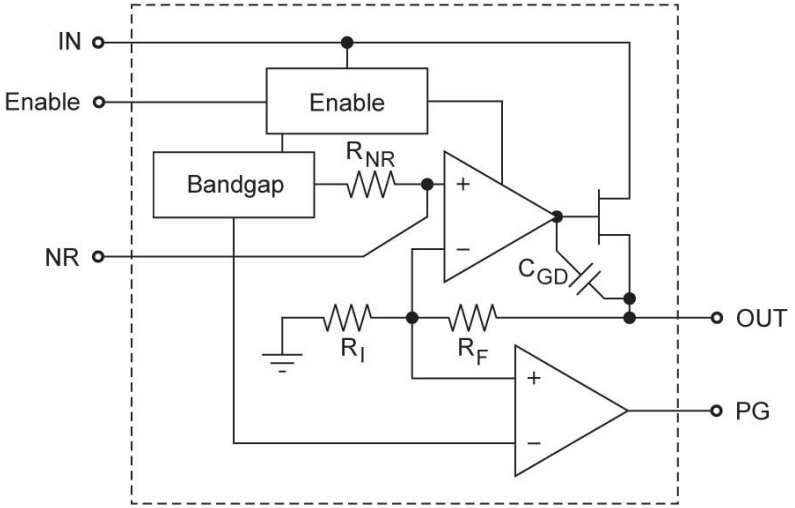
LDO Broadband Noise



- Output cap selection (large ceramic)
- External bandgap bypass cap value/location/type – start-up time/noise trade-off
- Input cap may reduce input noise

- The bandgap (BG) is typically the dominant noise source in an LDO
- BG noise is gained up by V_{OUT}/V_{BG}
- Some LDOs have low bandgap noise (usually with higher I_{GND} or external cap)
- Watch how noise is specified in the data sheet (V_{OUT}, frequency range, I_{OUT})

LDO Power Supply Rejection/ Input Transient Response

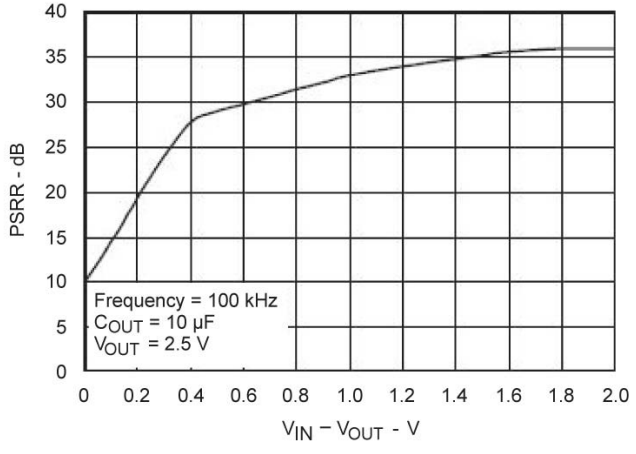


- Feedback loop bandwidth limits high frequency rejection
- C_{GD} reduces high frequency rejection
- Error amp output stage drive capability limits how fast pass-element gate can be charged/ discharged. Related strongly to I_{GND} in error amp output stage
- Degrades in dropout

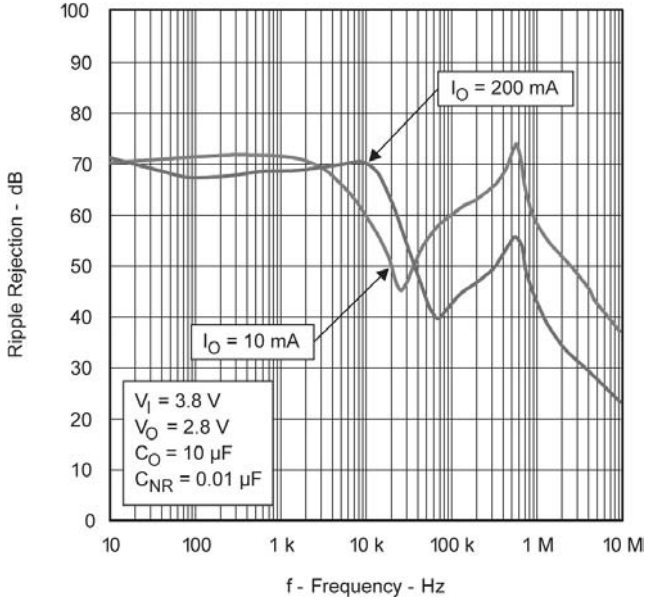
- Choose proper input/output bypass capacitor to filter input and output noise
- Be aware of behavior near and into dropout, taking into account size of signals on the power supply line
- Watch how PSRR is specified (C_{OUT}, frequency, C_{NR})

Typical LDO Power Supply Rejection Performance

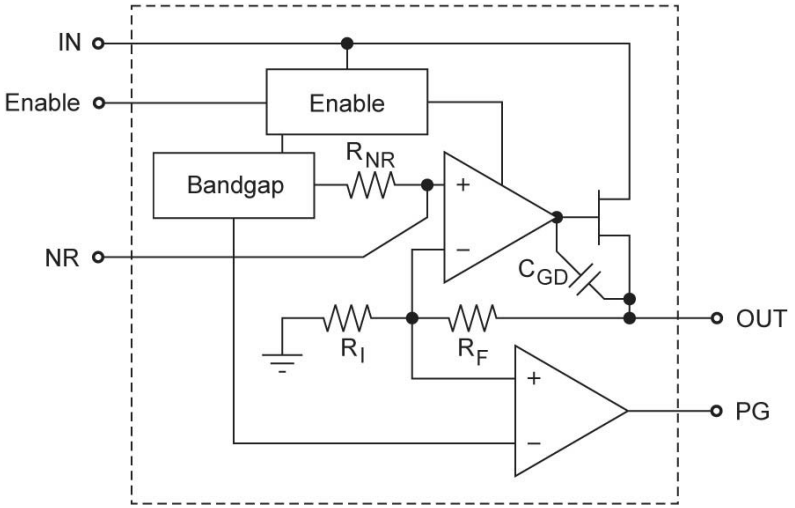
Part A



Part B



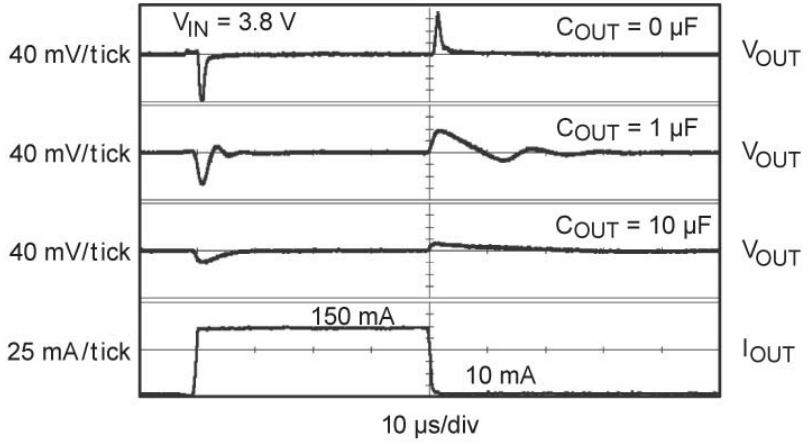
LDO Transient Behavior



- Choose proper input/output bypass capacitors to filter input and output transients
- Be aware of behavior near and into dropout and small vs. zero load
- This is generally poorly characterized in data sheets

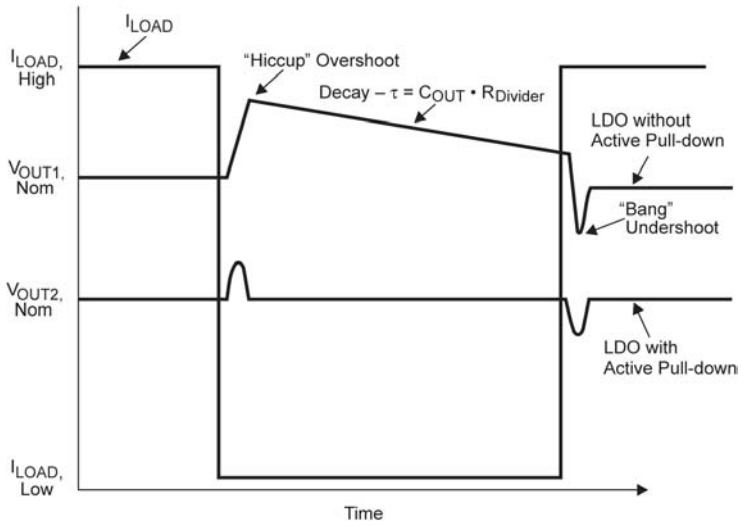
- Bandwidth of feedback loop determines how fast LDO can react to changes
- Error amp output stage drive capability limits how fast pass element gate can be charged/discharged
- Degrades in dropout since pass transistor gm falls
- May be much different for transients to/from no current vs. small current
- Active output pull-down may be present
- Related to I_{GND}

LDO Transient Behavior (cont)



- N-type LDO can be designed for transient response that is relatively insensitive to output capacitance

Transient Effects of Active Pull-down



- LDOs exhibit overshoot when the load is quickly removed due to the time it takes to turn off the pass device
- Active pull-down on the output minimizes the duration of overshoot. It can cause problems if a secondary supply with a higher voltage than the LDO is connected to the output
- Repetitive load transients could cause large noise magnitude under these conditions

Summary

- Power supply design is an integral part of managing noise in portable RF applications
- Careful attention to layout can eliminate troubleshooting time and extra components (normally capacitors) used to fix noise problems
- Carefully read product data sheets to get an accurate comparison between products
- Use field applications engineers to help select the best device, give layout guidance, and make sure your design is a success

APPLICATION REPORTS

power.ti.com

Advanced Gas Gauge Host Firmware Flow Chart for the TI Battery Monitor ICs

Doug Williams *Power Management Products*

ABSTRACT

TI advanced battery-monitoring ICs, such as the bq2018, bq2019, and bq2023, are designed to accurately measure the charge and discharge currents in rechargeable battery packs. Intended for pack integration, these devices contain all the necessary functions to form the basis of a comprehensive battery capacity management system in applications such as cellular phones, PDAs, Internet appliances, or other portable products. TI battery monitors work with the host controller in the portable system to implement the battery gas gauging and management system. The host controller is responsible for interpreting the battery monitor data and communicating meaningful battery data to the end-user or power management system.

This document, written around the bq2019, is designed to assist the firmware engineer engaged in development of advanced gas gauging routines in the host controller. A flow chart is presented for implementing the gas gauging function in the host firmware. Suggested constant and variable values are outlined and described.

This document is designed to be used in conjunction with the related application note *Advanced Gas Gauge Host Firmware Guide for the TI Battery Monitor ICs (SLVA100)*

Gas Gauging Functions

Apart from the required general read and write functions, gas gauge firmware may be broken down into six tasks as in table 1. The flowchart is organized according to these functions.

Table 1. Gas Gauge Firmware Tasks

Name	Recommended Interval	Description
GGInitialize( )	On power up	Qualify the battery and communication. Read and convert constants and scratch pad variables from bq2019 into the host.
GGUpdate( )	Once per minute (typical)	Calculate capacity, average current, run time and charge time. Manage full, empty and learning. Update display.
GGRegisterMaint( )	Hourly	Do register maintenance. Store remaining capacity in the bq2019. Clear registers.
GGSelfDischarge( )	Several times per day	Make corrections to remaining capacity for self-discharge.
GGMeasBattVltg( )	Every 20 seconds	Measure the battery voltage. Call GGUpdate( ) if battery crosses the empty voltage threshold.
GGPwrDwnSave( )	On power down	Provide an orderly shutdown. Update bq2019 registers.

Gas Gauging Constants

Table 2 below outlines a set of suggested constants for gas gauge implementation. Notice that the last three are only used as a mechanism to simplify calculations in the firmware. The flowchart refers specifically to many of these constants.

Table 2. Typical Gas Gauge Constants

Class	Name	Suggested bq2019 Address [1]	Used In	Type/Units	Description/Comment
Mfg Data	ID_ROM	78~7F	GGInitialize( )	8 bytes	Factory programmed ROM
	sMFG_DATA	20~25	GGInitialize( )	(str) ASCII	Manufacturers data
	sMODEL	26~2B	GGInitialize( )	(str) ASCII	Battery model
	sMFG_NAME	2C~35	GGInitialize( )	(str) ASCII	Manufacturer name
	iSERIAL_NO	36/37	GGInitialize( )	(uint)	Serial number
	iMFG_DATE	38/39	GGInitialize( )	(uint) Date	Manufactured date
Design Data	iDES_CAP	3A/3B	GGInitialize( ) GGUpdate( )	(uint) Milliampere Hours	Pack design capacity
	iSNS_RES	3C/3D	GGInitialize( )	(uint) mΩ * 327.68	Sense resistor mΩ x 2^{15} / 100
	iSLF_DSG_RATE	3E/3F	GGInitialize( ) GGSelfDischarge	(uint) %/Day * 105.8	Self discharge rate
	iEND_DSG_VLTG	40/41	GGInitialize( ) GGUpdate( ) GGMeasBattVltg( )	(uint) Millivolts	End of discharge voltage
	iTERM_CURR	42/43	GGInitialize( ) GGUpdate( )	(uint) Milliamperes	Charge taper termination current
	iCAP_COMP_TE	44	GGInitialize( ) GGUpdate( )	(byte) % of full capacity	Capacity compensation for temperature
	iCAP_COMP_LD	45	GGInitialize( ) GGUpdate( )	(byte) % of full capacity	Capacity compensation for load current
	iTALK_LD	n/a	GGInitialize( )	(uint) mA	Estimated talk load
	iSTBY_LD	n/a	GGInitialize( )	(uint) mA	Estimated standby load
	iTALK_LD_CNTS	n/a	GGInitialize( ) GGUpdate( )	Counts @ 3.05 µVh	= iSNS_RES * iTALK_LD / 1000
	iSTBY_LD_CNTS	n/a	GGInitialize( ) GGUpdate( )	Counts @ 3.05 µVh	= iSNS_RES * iSTBY_LD / 1000
	iCYCL_CAP	n/a	GGInitialize( ) GGUpdate( )	(uint) = iDES_CAP * iSNS_RES* 0.8/1000	May be used to simplify math in GGUpdate( )

[1] Addresses are in hex. n/a indicates that the values are maintained by the host since they are not a function of the battery. ID_ROM is a fixed address in the bq2019.

Gas Gauging Variables

Table 3, below outlines suggested variables and memory addresses for gas gauge implementation. The flowchart refers specifically to most of these values.

Table 3. Typical Gas Gauge Variables

Class	Name	Suggested bq2019 Address [2][3]	Used In	Type/Units	Description/Comment
Computed Values	iLastMeasDsg	00/01	GGInitialize( ) GGUpdate( ) GGSelfDischarge( )	(uint) Counts @ 3.05 µVh	Last measured discharge. (Initial value set during mfg.)
	iRemCap	02/03	GGInitialize( ) GGUpdate( )	(uint) Counts @ 3.05 µVh	Remaining capacity (Initial value set during mfg.)
	iCycleCnt	04/05	GGUpdate( )	(uint) Units	Cycle count (Typically increased if iDsgCntrCuml has reached 80% of design capacity)
	iMaxTemp	06	GGInitialize( ) GGUpdate( ) GGPwrDwnSave( )	(byte) °K	Max temp seen by this bq2019. Update it in the host during GG_Update.
	iValidDsg	07	GGInitialize( ) GGPwrDwnSave( )	(uint) Flag	Valid discharge flag. This is a flag, but 0x55 is used to indicate true to avoid possible corruption on power down/up cycles.
	iDsgCntr	08/09	GGInitialize( ) GGUpdate( ) GGSelfDischarge( ) GGPwrDwnSave( )	(uint) Counts @ 3.05 µVh	Discharge counter for learning a new iLastMeasDsg
	iDsgCntrCuml	0A/0B	GGInitialize( ) GGUpdate( ) GGSelfDischarge( ) GGPwrDwnSave( )	(uint) Counts @ 3.05 µVh	Cumulative discharge counter tracks partial discharges for iCycleCnt update.
	iLastRemCap	0C/0D	GGInitialize( ) GGPwrDwnSave( )	(uint) Counts @ 3.05 µVh	Last computed remaining capacity value
	iCumlCorrectn	0E/0F	GGInitialize( ) GGUpdate( ) GGSelfDischarge( ) GGPwrDwnSave( )	(uint) Counts @ 3.05 µVh	Tracks cumulative self-discharge corrections. Disqualifies learning cycle if it exceeds 10% of iDES_CAP.
	iTimeSinceMaint	n/a	GGInitialize( ) GGUpdate( ) GGRegisterMaint( )	(uint) Minutes	Minutes elapsed since last register maintenance.
	iRunTime	n/a	GGUpdate( )	(uint) Minutes	Estimated remaining run time at present current.

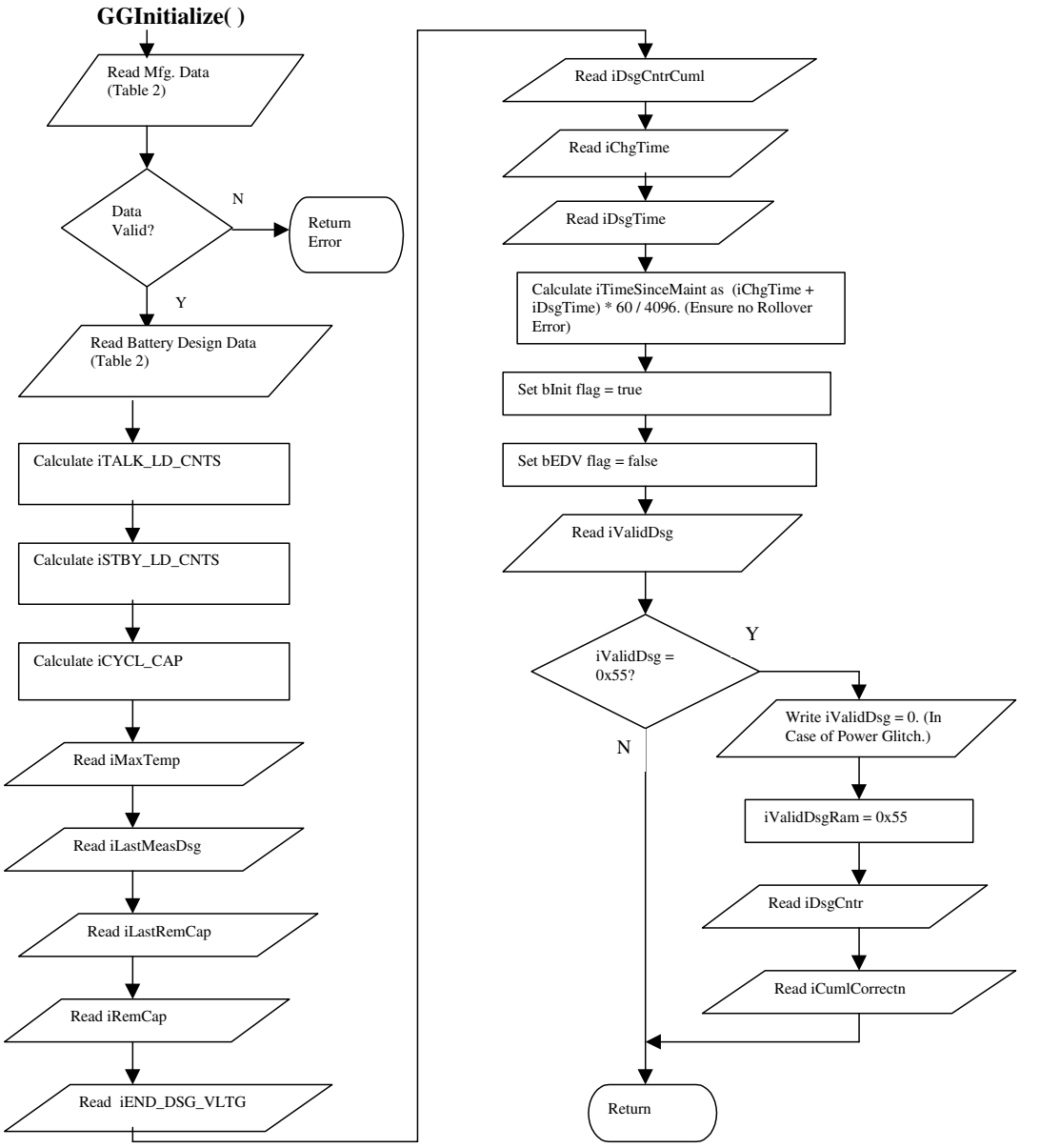
Table 3. Typical Gas Gauge Variables (Continued)

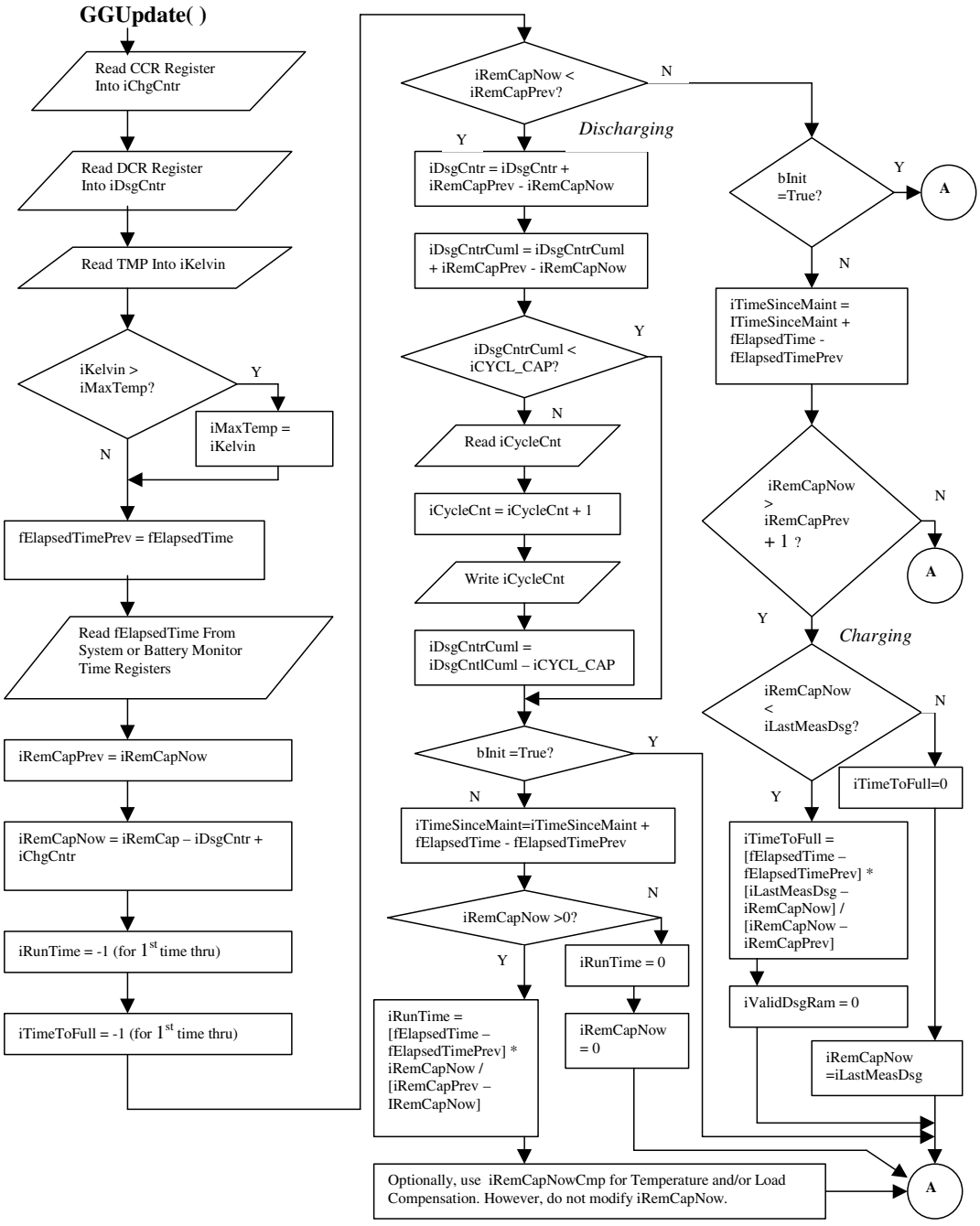
Class	Name	Suggested bq2019 Address [2][3]	Used In	Type/Units	Description/Comment
Computed Values	iTimeToFull	n/a	GGUpdate( )	(uint) Minutes	Estimated remaining time to charge to full.
	iTalkTime	n/a	GGUpdate( )	(uint) Minutes	Estimated remaining run time at iTALK_LD
	iStbyTime	n/a	GGUpdate( )	(uint) Minutes	Estimated remaining run time at iSTBY_LD
	iRelChgPercent	n/a	GGUpdate( )	(uint) %	Relative charge in percent of full charge. aka 'RSOC'
	bInit	n/a	GGInitialize( ) GGUpdate( )	(bool) Flag	Initial pass flag. Inhibits iRunTime and iTimeToFull calculations the first time through GGUpdate( )
	bEDV	n/a	GGInitialize( ) GGUpdate( )	(bool) Flag	Flag to notify other host process that battery is at end of discharge voltage.
	bChgFull	n/a	GGUpdate( )	(bool) Flag	Flag used by the charger or other host process to indicate that the battery is fully charged.
	iValidDsgRam	n/a	GGInitialize( ) GGUpdate( ) GGPwrDwnSave( )	(uint) Flag	Host version of iValidDsg. This is a flag, but 0x55 is used to indicate true to avoid possible corruption on power down/up cycles.
	iRemCapNow	n/a	GGInitialize( ) GGUpdate( ) GGRegisterMaint( ) GGSelfDischarge( ) GGPwrDwnSave( )	(int) Counts @ 3.05 µVh	Most recent calculation of remaining capacity.
	iRemCapNowCmp	n/a	GGUpdate( )	(int) Counts @ 3.05 µVh	If load and/or temperature compensation are used for remaining capacity, this separate variable is required for the most recent calculation of compensated remaining capacity.
	iRemCapPrev	n/a	GGUpdate( )	(int) Counts @ 3.05 µVh	Calculation of remaining capacity from the previous update.
	iRemCapTemp	n/a	GGSelfDischarge( )	(uint) Counts @ 3.05 µVh	Temp variable for iterative self-discharge estimate.
	iSlfDsgEst	n/a	GGSelfDischarge( )	(uint)	Temp self-discharge variable.
	iTempCorrection	n/a	GGSelfDischarge( )	(uint)	Temp self-discharge variable.
	fElapsedTime	n/a	GGUpdate( )	(float) Minutes	Value in minutes, with resolution to seconds since power on reset detected.

Table 3. Typical Gas Gauge Variables (Continued)

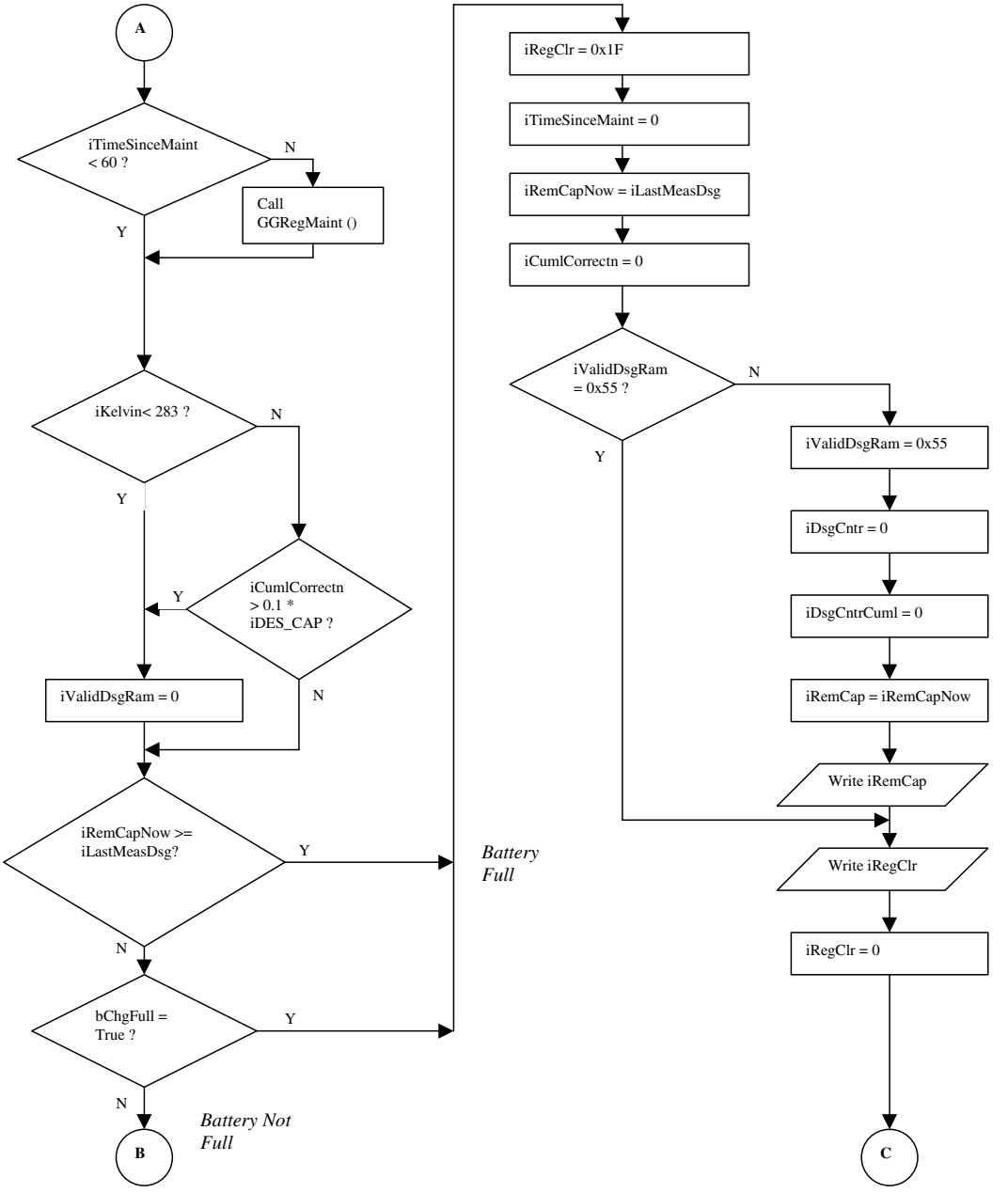
Class	Name	Suggested bq2019 Address [2][3]	Used In	Type/Units	Description/Comment
Computed Values	fElapsedTimePrev	n/a	GGUpdate( )	(float) Minutes	Value in minutes, with resolution to seconds since the power on reset detected previous to fElapsedTime.
bq2019 Gas Gauge Registers and corre-sponding host vars.	iKelvin (Host) TMPL (bq2019) TMPH (bq2019)	 60 61	GGInitialize( ) GGUpdate	(uint) °K	TMPH, TMPL in the bq2019 contain die temperature in °K.
	iRegClr (Host) CLR (bq2019)	 63	GGUpdate( ) GGRegisterMaint( ) GGSelfDischarge( )	(uint) Bits	CLR is used to quickly clear DCR, CCR, SCR, DTC, CTC in any combination. iRegClr is used by the host to set up the next desired clearing pattern.
	iChgTime (Host) CTCL (bq2019) CTCH (bq2019)	 65 66	GGInitialize( ) GGUpdate( ) ??	(uint) 4096 counts per hour	Charge Time Counter. May be used in GGUpdate( ) if no timer or time function is available in the host.
	iDsgTime (Host) DTCL (bq2019) DTCH (bq2019)	 67 68	GGInitialize( ) GGUpdate( ) ??	(uint) 4096 counts per hour	Discharge Time Counter. May be used in GGUpdate( ) if no timer or time function is available in the host
	iSlfDsgCntr (Host) SCRL (bq2019) SCRH (bq2019)	 69 6A	GGInitialize( ) GGSelfDischarge( )	(uint) 1 count per hour (20 – 30°C)	Self Discharge Counter. Rate varies automatically with temperature.
	iChgCntr (Host) CCRL (bq2019) CCRH (bq2019)	 6B 6C	GGUpdate( )	(uint) Counts @ 3.05 µVh	Charge count register in bq2019 increments when voltage at the SR pin is positive.
	iDsgCntr (Host) DCRL (bq2019) DCRH (bq2019)	 6D 6E	GGUpdate( )	(uint) Counts @ 3.05 µVh	Discharge count register in bq2019 increments when voltage at the SR pin is negative.

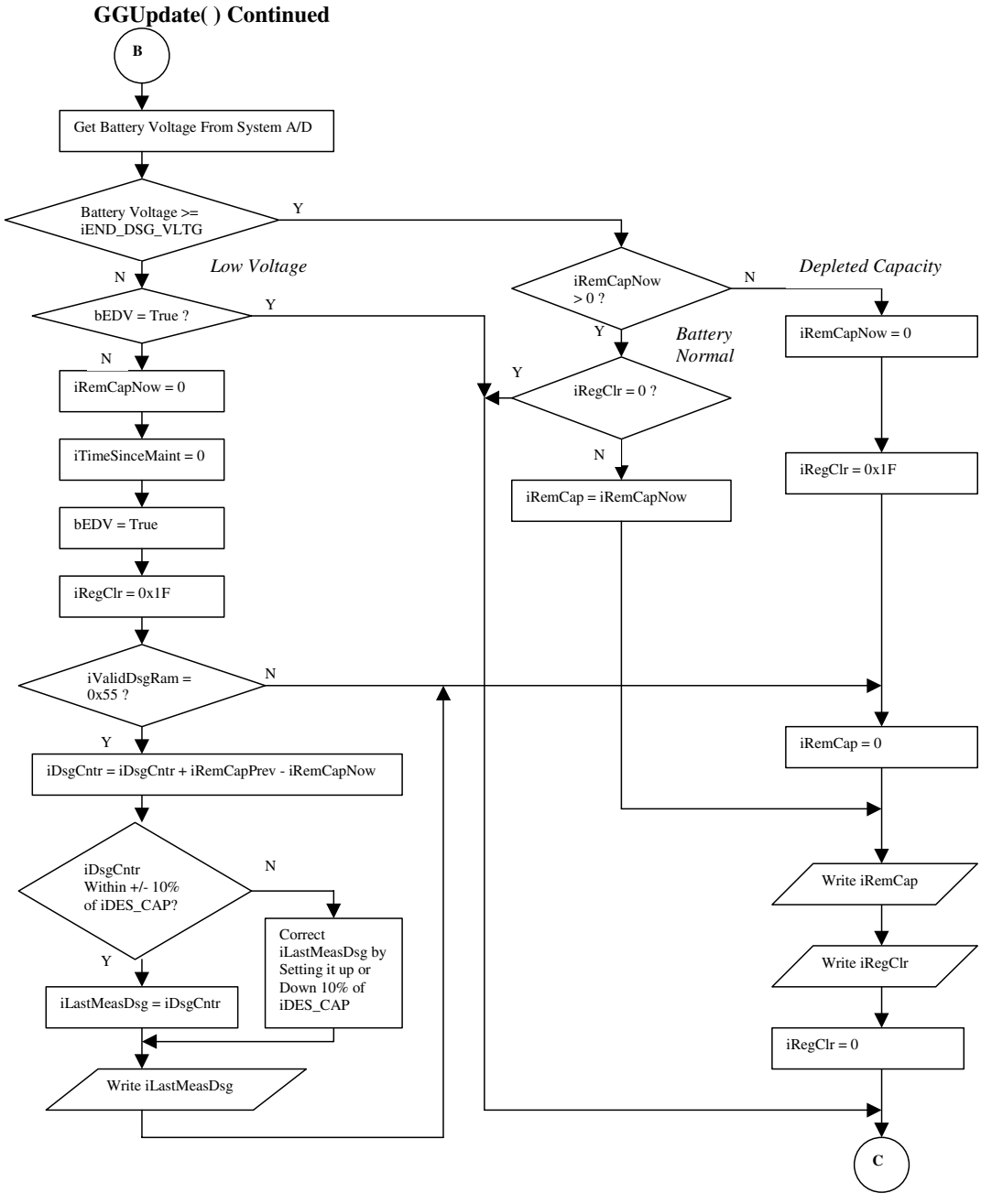
[2] Addresses are in hex. [3]Gas gauge registers are at fixed locations.


GGInitialize( )
Read Mfg. Data (Table 2)
Data Valid?
N
Return Error
Y
Read Battery Design Data (Table 2)
Calculate iTALK_LD_CNTS
Calculate iSTBY_LD_CNTS
Calculate iCYCL_CAP
Read iMaxTemp
Read iLastMeasDsg
Read iLastRemCap
Read iRemCap
Read iEND_DSG_VLTG
Read iDsgCntrCuml
Read iChgTime
Read iDsgTime
Calculate iTimeSinceMaint as (iChgTime + iDsgTime) * 60 / 4096. (Ensure no Rollover Error)
Set bInit flag = true
Set bEDV flag = false
Read iValidDsg
iValidDsg = 0x55?
Y
N
Write iValidDsg = 0. (In Case of Power Glitch.)
iValidDsgRam = 0x55
Read iDsgCntr
Read iCumlCorrectn
Return

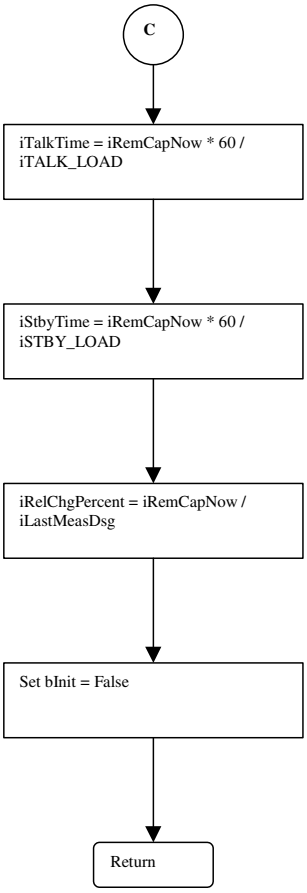

GGUpdate( )
Read CCR Register Into iChgCntr
Read DCR Register Into iDsgCntr
Read TMP Into iKelvin
iKelvin > iMaxTemp?
Y
N
iMaxTemp = iKelvin
fElapsedTimePrev = fElapsedTime
Read fElapsedTime From System or Battery Monitor Time Registers
iRemCapPrev = iRemCapNow
iRemCapNow = iRemCap – iDsgCntr + iChgCntr
iRunTime = -1 (for 1st time thru)
iTimeToFull = -1 (for 1st time thru)
iRemCapNow < iRemCapPrev?
N
Y
Discharging
iDsgCntr = iDsgCntr + iRemCapPrev - iRemCapNow
iDsgCntrCuml = iDsgCntrCuml + iRemCapPrev - iRemCapNow
iDsgCntrCuml < iCYCL_CAP?
Y
N
Read iCycleCnt
iCycleCnt = iCycleCnt + 1
Write iCycleCnt
iDsgCntrCuml = iDsgCntlCuml – iCYCL_CAP
bInit =True?
Y
N
iTimeSinceMaint=iTimeSinceMaint + fElapsedTime - fElapsedTimePrev
iRemCapNow >0?
N
Y
iRunTime = 0
iRemCapNow = 0
iRunTime = [fElapsedTime – fElapsedTimePrev] * iRemCapNow / [iRemCapPrev – IRemCapNow]
bInit =True?
Y
N
A
iTimeSinceMaint = ITimeSinceMaint + fElapsedTime - fElapsedTimePrev
iRemCapNow > iRemCapPrev + 1 ?
N
A
Y
Charging
iRemCapNow < iLastMeasDsg?
N
Y
iTimeToFull=0
iTimeToFull = [fElapsedTime – fElapsedTimePrev] * [iLastMeasDsg – iRemCapNow] / [iRemCapNow – iRemCapPrev]
iValidDsgRam = 0
iRemCapNow =iLastMeasDsg
Optionally, use iRemCapNowCmp for Temperature and/or Load Compensation. However, do not modify iRemCapNow.
A

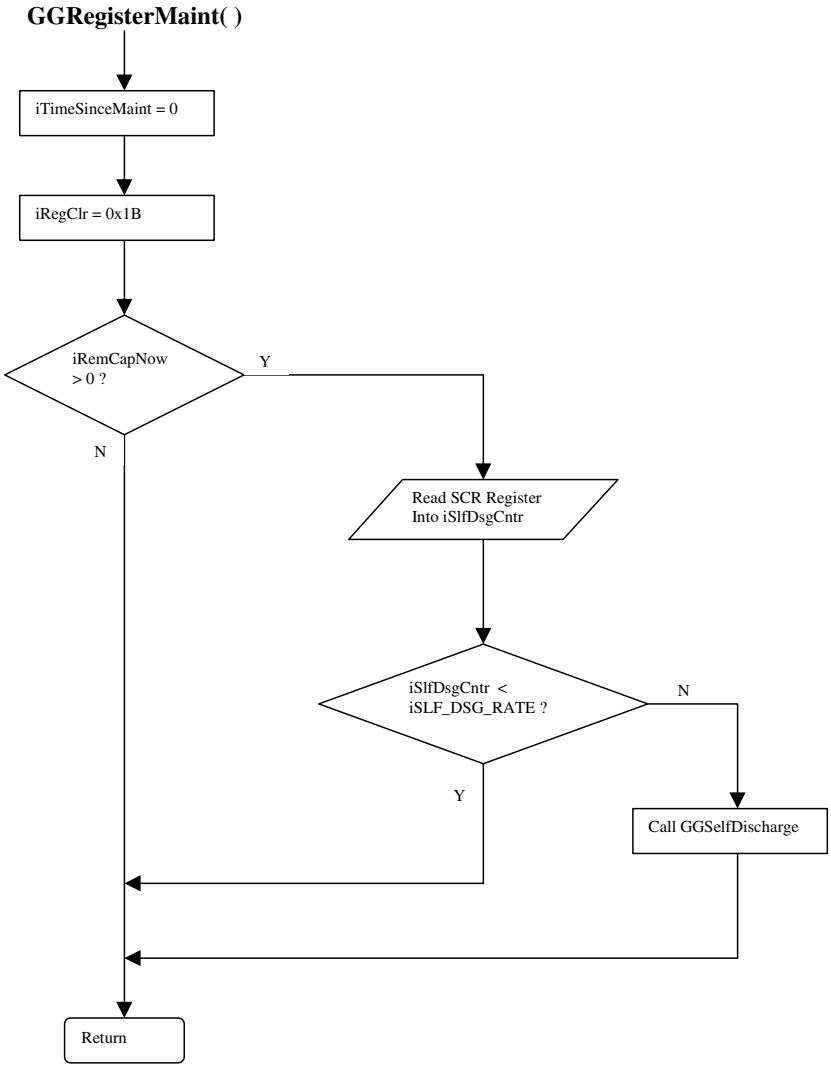
GGUpdate( ) Continued

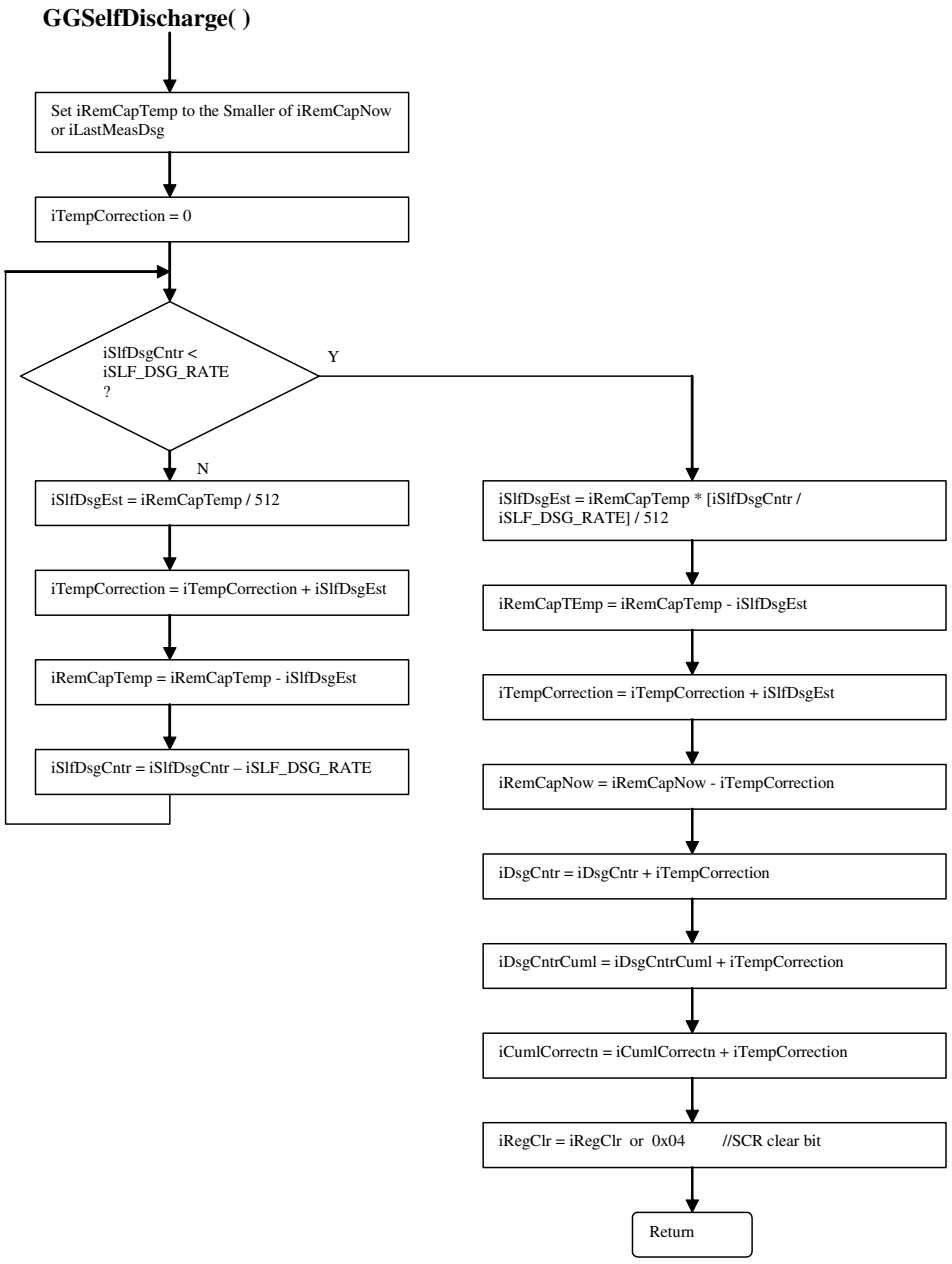


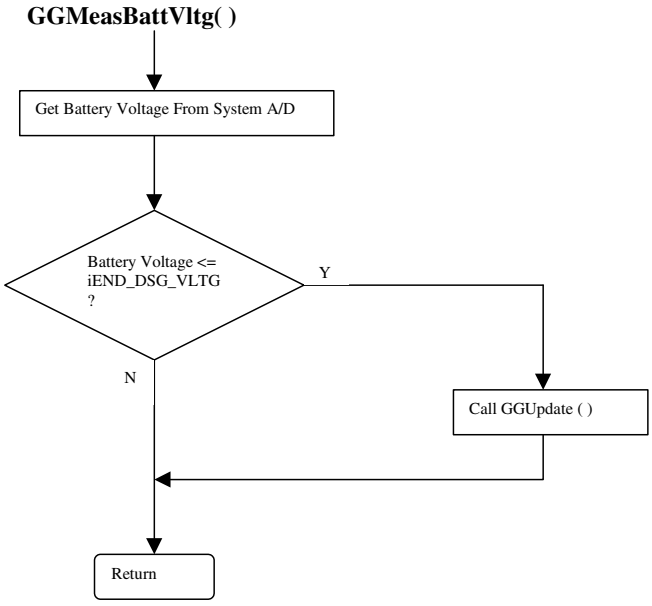

GGUpdate( ) Continued
B
Get Battery Voltage From System A/D
Battery Voltage >= iEND_DSG_VLTG
Y
N
Low Voltage
bEDV = True ?
Y
N
iRemCapNow = 0
iTimeSinceMaint = 0
bEDV = True
iRegClr = 0x1F
iValidDsgRam = 0x55 ?
N
Y
iDsgCntr = iDsgCntr + iRemCapPrev - iRemCapNow
iDsgCntr Within +/- 10% of iDES_CAP?
N
Correct iLastMeasDsg by Setting it up or Down 10% of iDES_CAP
Y
iLastMeasDsg = iDsgCntr
Write iLastMeasDsg
iRemCapNow > 0 ?
N
Depleted Capacity
Y
Battery Normal
iRegClr = 0 ?
Y
N
iRemCap = iRemCapNow
iRemCapNow = 0
iRegClr = 0x1F
iRemCap = 0
Write iRemCap
Write iRegClr
iRegClr = 0
C

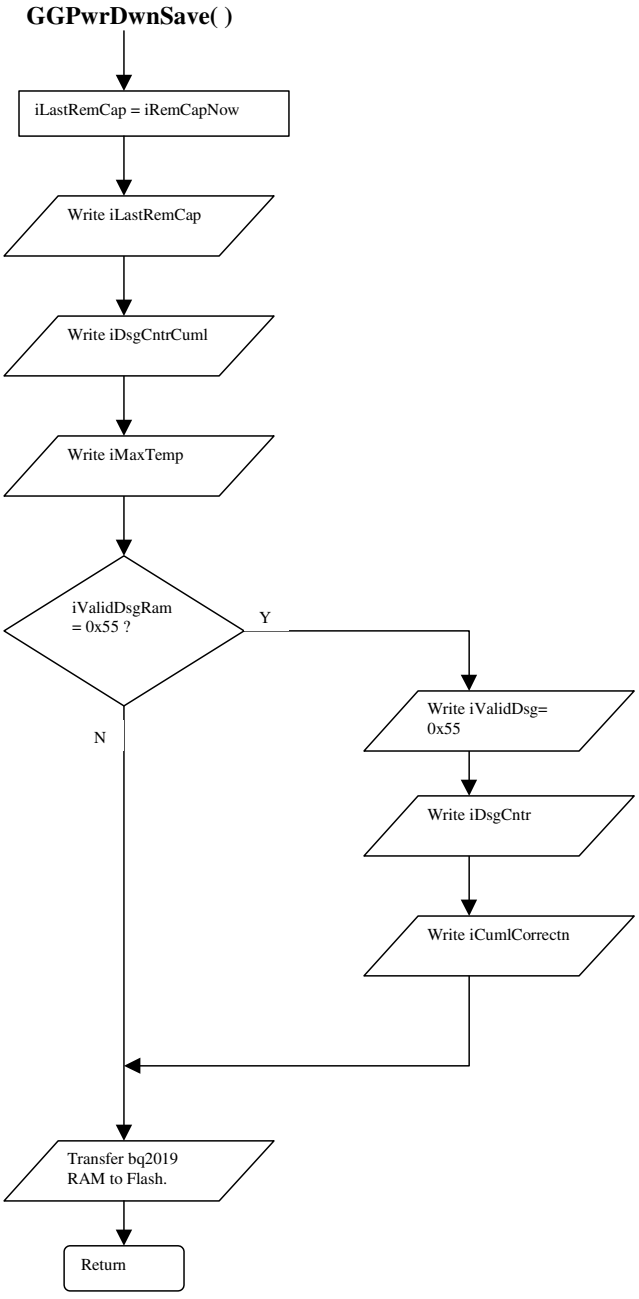
GGUpdate( ) Continued




GGRegisterMaint( )
iTimeSinceMaint = 0
iRegClr = 0x1B
iRemCapNow
> 0 ?
Y
N
Read SCR Register
Into iSlfDsgCntr
iSlfDsgCntr <
iSLF_DSG_RATE ?
N
Y
Call GGSelfDischarge
Return


GGSelfDischarge( )
Set iRemCapTemp to the Smaller of iRemCapNow or iLastMeasDsg
iTempCorrection = 0
iSlfDsgCntr < iSLF_DSG_RATE ?
Y
N
iSlfDsgEst = iRemCapTemp / 512
iTempCorrection = iTempCorrection + iSlfDsgEst
iRemCapTemp = iRemCapTemp - iSlfDsgEst
iSlfDsgCntr = iSlfDsgCntr – iSLF_DSG_RATE
iSlfDsgEst = iRemCapTemp * [iSlfDsgCntr / iSLF_DSG_RATE] / 512
iRemCapTEmp = iRemCapTemp - iSlfDsgEst
iTempCorrection = iTempCorrection + iSlfDsgEst
iRemCapNow = iRemCapNow - iTempCorrection
iDsgCntr = iDsgCntr + iTempCorrection
iDsgCntrCuml = iDsgCntrCuml + iTempCorrection
iCumlCorrectn = iCumlCorrectn + iTempCorrection
iRegClr = iRegClr or 0x04 //SCR clear bit
Return


GGMeasBattVltg( )
Get Battery Voltage From System A/D
Battery Voltage <= iEND_DSG_VLTG ?
Y
N
Call GGUpdate ( )
Return


GGPwrDwnSave( )
iLastRemCap = iRemCapNow
Write iLastRemCap
Write iDsgCntrCuml
Write iMaxTemp
iValidDsgRam = 0x55 ?
Y
N
Write iValidDsg= 0x55
Write iDsgCntr
Write iCumlCorrectn
Transfer bq2019 RAM to Flash.
Return

References

1. *Texas Instruments. data sheet for bq2019 Advanced Battery Monitor IC (SLUS456)*
2. *Texas Instruments. Advanced Gas Gauge Host Firmware Guide for the TI Battery Monitor ICs (SLVA100)*

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Best Practices for Designing Battery Packs for Portable Devices

by Katherine Mack, Micro Power Electronics

Fueled by businesses and consumers alike, demand for portable products is increasing.

To address this rising demand, electronics manufacturers are leveraging faster processors, enhanced color displays and backlighting, wireless networking, voice and multimedia capabilities for next-generation portable devices. But the transition to highly sophisticated, power-hungry portable electronic systems in smaller, lighter and more ergonomic packages is creating new challenges for battery system designers.

Higher pulse currents and extreme operating environments have put a strain on the battery's performance capabilities. In addition, the pressure continues for smaller form factors. To maximize worker efficiency, the battery's design requirements include being able to last a full workday, shift or session.

Planning for the battery system early in the design process for portable devices overcomes many of these challenges, maximizing performance, durability, reliability and safety.

Battery pack design has become a real challenge

Design engineers know that designing a battery to its fullest potential is more challenging than ever. They are inundated with information from various cell vendors on the Internet stating they have the highest capacity or longest service life.

It has become crucial that battery system engineers effectively design power systems for their portable devices. Currently, average battery life is on the order of 3 to 4 hours, much too short for all-day usage in a corporate environment.

By effectively planning, developing and implementing smart-battery system solutions into their portable applications, designers can extend battery life. Designing a power-management system for mobile PC and other high-power electronics applications can be a difficult process, however, even for the most experienced design engineer. Underestimating the complexity of the battery system and the interrelationship between the battery circuitry and the device circuitry can lead to setbacks during product development, or worse, the potential failure of the entire system in the field. Battery subsystems are often not designed holistically, and therefore available power is left "on the table" unused.

These problems indicate that many original equipment manufacturers (OEMs) are facing design issues that they may not have the tools or internal expertise to solve when it comes to developing high-performance battery systems. Fortunately, planning for the battery system early enough in the design process, along with proper implementation, can maximize battery run time.

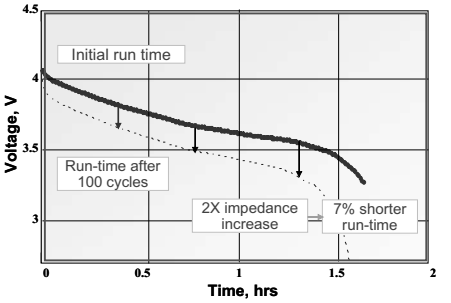
This whitepaper will direct battery system designers to best practices for designing battery subsystems for portable devices. It will help designers not only to maximize available power but also to help avoid problems that could deplete run-time.

Recognizing Critical Performance Factors

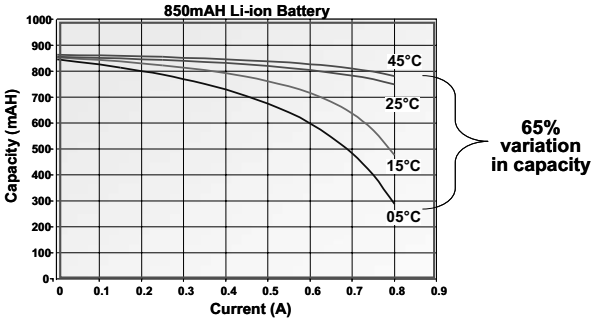
Batteries for portable devices are used in many ways, and their performance often hinges on operating conditions. For these reasons, it is important to first understand the factors that affect battery performance before establishing best-practice guidelines.

When designing a smart-battery system that can offer optimal performance characteristics in the target application, engineers must approach the problem holistically. This holistic approach calls for a complete front-to-back development process, one that emphasizes early design characterization, optimization and validation. This tactic will create a higher likelihood that the battery solution will provide the maximum power, reliability and safety for field-service applications.

The first critical performance factor to consider is battery aging. The fresher and more fully charged the battery cell, the lower its impedance. Manufacturers rate their cells at their optimum freshness, of course, but this rarely reflects real-world usage profiles. After 100 cycles, for example, impedance can double, a problem that will bring down the entire voltage curve of the pack. The result is that, in some cases, run time will drop by up to 7 percent.

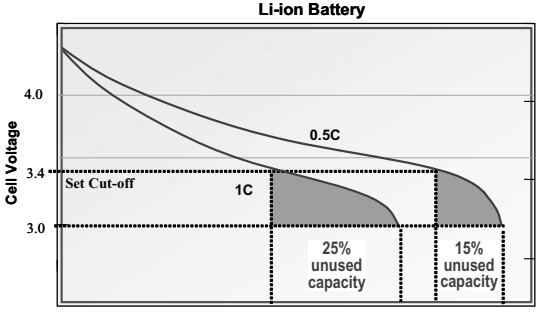


The second critical performance factor is battery temperature. Most cells are rated at 20 degrees C, or room temperature. Any deviation from this ambient will impair battery performance, either in run time per cycle or in cycle life. In the case of Lithium-ion (Li-ion) chemistry, a higher ambient temperature, such as 45°C, will actually improve per-cycle run time due to lower impedance; however, cycle life will suffer. Conversely, lower temperatures will shorten run time per cycle. An operating temperature variation of 40°C, from 0°C to +45°C, will result in a 65 percent capacity variation.



A third critical performance factor is discharge current. Nickel-based chemistries such as nickel cadmium (Ni-Cd) and nickel metal hydride (Ni-MH), and rechargeable lithium chemistries such as Li-Ion and lithium polymer (Li-polymer) are all rated at C/5, which is the cell manufacturer's rated capacity divided by five hours, or at a five-hour discharge rate. This gives a baseline of comparison. However, no mobile PC application is ever used at a constant C/5 discharge rate at 20°C. Users may go from controlled office environments into the summer heat or winter cold and then back again. They may send e-mails that cause high pulse currents. Their laptop may be in sleep mode. Whether or not a pulse current or constant discharge current is in use will determine the internal heating of the pack and will cause differences in long-term cycle-life performance.

A fourth critical performance factor is cutoff voltage in the operating system. Cell manufacturers rate their cells based on specific cutoff voltages. If the cutoff voltage is higher than specified, per-cycle run time will be shorter, and depending on the discharge current, the user may lose up to 25 percent of available capacity. Conversely, if the cutoff voltage is too low, this will shorten cycle life.



Best Practices: Create a real-world operating profile

The first step in maximizing battery performance is to create a real-world operating profile for the user equipment. Defining how the battery is going to be used, in what circumstances, and in what temperatures, are keys to designing a performance-maximized battery system. By answering questions about minimum operating time needed, various current loads, different voltage levels, interior operating temperatures, and battery-pack location in the unit, you can narrow the best solution for the end-product.

Understanding the usage profile is critical in determining what cell to use. The usage profile will indicate the optimum quantity and type of cells. Because battery cells have different impedance levels, current demands may exclude some types of cells from consideration. The designer can then further narrow the cell options, based on size and weight constraints.

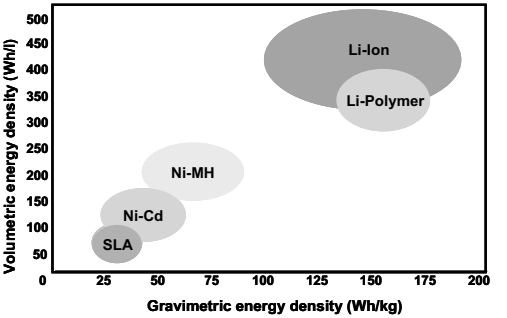
The frequency and method of pack charging can greatly influence the available capacity and cycle life of the pack. Many cell manufacturers place more restrictions on the charging of their cells than on the discharging of them.

Once the operating parameters have been defined, weak options can be eliminated. At this point, the designer can nominate the best battery system at a theoretical level, establishing an operating window. Then, the theory can be tested and validated to ensure that the selection was correct.

Best Practices: Cell Selection

The biggest payoff in battery design is matching the right cell, the right chemistry, and the right manufacturer with the operating profile of the cell. In mobile PC applications, with voltages generally required above 3-V operating, and with critical portability and weight thresholds, designers typically prefer rechargeable Li-ion chemistries. Li-ion offers operating voltages generally from 3 V to 4.2 V per cell, cell capacities from 130 mAh to 5.6 Ah (at C/5), and cycle life in the 500 range (down to 80 percent of rated capacity).

With nominal operating voltages ranging from 3.6 V to 3.8 V, only one rechargeable lithium chemistry cell is required for a 3-V operating system. In contrast, yesterday's nickel-based technologies, which operate at 1.2 V, required three cells for a 3-V operating system. Today, some rechargeable lithium technologies offer improved energy densities of greater than 500 Wh/l, and can handle 1C (1 times the rated capacity) continuous discharge rates.



All that dense power can be an unstable mix. Li-ion can be very volatile on overcharge, and because of its volatility, a safety circuit must be added to prevent the battery from exceeding 4.25 V per cell. This differs from Ni-MH batteries, which are exothermic in nature and where heating is the danger. Ni-MH packs must include devices that prevent over-heating, and/or devices that prevent over-currents that can cause over-heating.

Cell matching must be considered in creating a battery pack, as the closer the cells are matched, the better the pack will perform. Batteries operate on a weakest-link model: The weakest cell will drag down an entire pack's performance. For this reason, nickel-based technologies should not exceed 10 cells in series, and rechargeable lithium should not exceed four cells in series.

Advancements in Li-ion have overtaken Li-polymer in energy density, not only volumetrically (in Watt hours per liter) but gravimetrically (Watt hours per kilogram). Unless the mobile PC application absolutely calls for 3.5-mm thinness or less, Li-ion should be strongly considered.

Cells come in two form factors: cylindrical and prismatic. The most popular cell size, where most cell manufacturers have concentrated their development efforts, is in the 18650 sizes of cylindrical cells. These cells are 18-mm diameter by 65-mm long. This cell size not only offers the highest gravimetric and volumetric energy density, but also provides the most cost-effective solution. However, if the mobile PC being designed cannot tolerate an 18mm cell due to thickness, prismatic cells offer several options. Advancements have increased volumetric efficiency in these cells, and their intrinsically thin profile makes them attractive for ergonomic applications.

In addition to examining different cell chemistries, each chemistry also offers a variety of sub-types or "recipes," each of which provides varied performance characteristics. In Li-ion, for example, there are three main chemistry sub-types: LiCo02/Graphite (Cobalt/Graphite), Li-Mn204/Graphite (Manganese/Graphite), and LiCo02/Coke (Hard Carbon).

Cobalt/Graphite has a flat discharge curve and has enjoyed the most attention by cell manufacturers with regard to increasing cell capacity. Manganese/Graphite is intrinsically the safest chemistry. In one-cell applications, no safety circuit is needed; only a one-shot thermal fuse and current interrupt device is necessary. Manganese/Graphite also offers a higher operating voltage than the other two types, which yields better performance for high-power applications, and can take a 2C discharge. Hard Carbon has a sloping discharge curve, which has the advantage of being able to accurately gauge fuel supply using an inexpensive voltage-based system; however, because of its sloping curve, performance during the discharge cycle will be uneven.

Best Practices: Cell Manufacturer

Available battery capacity depends on operating temperature and discharge current. Keep in mind that battery manufacturers rate their cells at an "ideal" performance level of standard C/5 constant current at 20 degrees C. It is also important to note that some manufacturers rate their

cells on typical performance, while some rate their cells based on nominal or minimum performance. The designer should always use nominal or minimum performance, never typical, when selecting cells, as this level is where cell manufacturers can guarantee performance. The exposure of the battery system to high temperatures or high discharge rates will impair its capacity and service life.

The number of cell manufacturers available on the market today presents a broad yet confusing number of choices. Look for product consistency and quality to ensure dependable battery-pack performance. Test to validate cell manufacturers' performance claims. In addition, compare packaging dimensions (tolerance specifications), since manufacturers' claims may differ from actual specifications.

Process consistency, or a cell manufacturer's ability to repeatedly make the same high-quality cells, is extremely important for multi-cell battery packs. Quality cell manufacturers will use automated processes, with clean production areas, resulting in good lot-to-lot cell matching. As a rule, the more human touch-points batteries are exposed to during manufacturing, the greater the possibility for lot-to-lot variances. In turn, poorly matched cells can lead to batteries with lower overall run times.

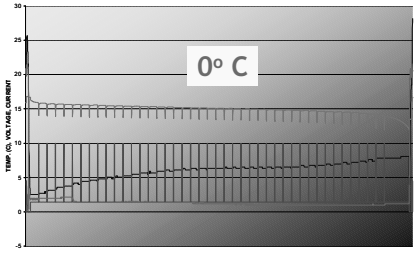
Best Practices: Cell and Pack Verification

Once the cell manufacturer's specification has been validated, the next step is to test various cell manufacturers against one another. You should test using the portable product's usage profile, first at the cell level and then at the pack level.

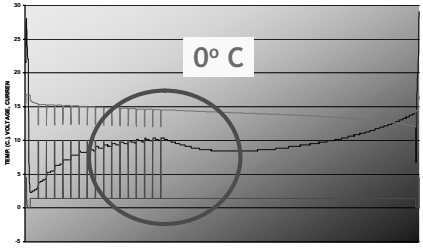
Although the baseline at C/5 performance at 20°C has now been validated, testing is not complete. Because the recipes and processes used by each cell manufacturer are unique, each cell will perform differently at various temperatures and discharge loads. In addition, single cells will perform better than they will in pack form. Testing different manufacturers' cells in the specified configuration is essential for predicting user outcomes.

The graphs below show an actual comparison between two similarly rated packs for a defibrillator application at 0°C. It should be noted that both Battery A and Battery B performed equally well at 40°C and at 20°C.

Battery A @ 0° C



Battery B @ 0° C



Pack B failed after 16 defibrillations because of the voltage depression that happened during use due to the cold.

Obviously, then, the designer should test the cells and battery pack both at room temperature and at anticipated operating temperatures, as well as at expected loads. By validating the battery system against the specifications set by the application at each stage of the design process, the designer will be able to ensure that the battery system will perform as expected. This early involvement helps to certify that the battery system has been optimized to deliver the maximum runtime, reliability and manufacturability.

Best Practices: Pack Manufacturing for Safety and Durability

In today's competitive marketplace, however, it is no longer enough to have the most exceptional design created from advanced characterization and validation procedures. Modern smart battery systems must also be cost-effective and easy to build. Designers should adhere to design-for-manufacturability principles. Work closely with the manufacturing staff beginning early in the development process to ensure that the battery systems will be easy and cost-effective to manufacture and test.

The need for smaller battery systems is making design for manufacturability increasingly important. As form factors shrink, design and manufacturing challenges grow. Due to diminishing real estate in portable applications, it has become even more difficult to fit the required components into the available space. As component congestion increases, so too does the risk for accidentally pinching or shorting wires and contacts.

The physical layout of the components also becomes important in battery systems. A poor layout can complicate the assembly process or create hot spots inside the pack. Although venting is less crucial with Li-ion than with Ni-MH, ensuring that heating is even throughout the pack enables safety devices to trip when appropriate.

Furthermore, the designer must work carefully to ensure that vital contacts are not placed too closely together. Inappropriately close contacts can short if the battery system is dropped or subjected to vibration. The designer also must ensure that contacts are recessed, to prevent external short circuits.

Another design challenge associated with smaller battery systems is the mechanical fit. With smaller tolerances, the contact points, energy director (for ultrasonic welding) and locking mechanism must be designed and manufactured with greater precision and care. Smaller packs usually use thin-walled plastic (.060" thick) that can be difficult to ultrasonically weld without cracking and must be tested to ensure adherence to drop-test requirements.

Soldering, resistance welding and ultrasonic welding also can be challenging processes. It takes many years of experience to be able to create high-quality joints consistently. Poor solder and weld joints are the greatest source of industry defects. Without effective training, controlled processes, high-quality equipment and rigorous inspection procedures, it is possible to create weak weld and solder joints that may not be discovered until the portable unit is in the field and something goes wrong.

Major causes of battery-pack field defects are cold, fractured or missing solder joints, which can create an electrical connection that manages to pass a functional test, but breaks in the field due to vibration or heat. Occasionally, failures are intermittent, making the problem more difficult to diagnose.

Solder balls, which are tiny drops of solder that remain in the battery system after production due to careless soldering procedures, are also a source of defects. When vibration or thermal stress causes these conductive balls to break free inside the battery system, they can short and damage the battery system.

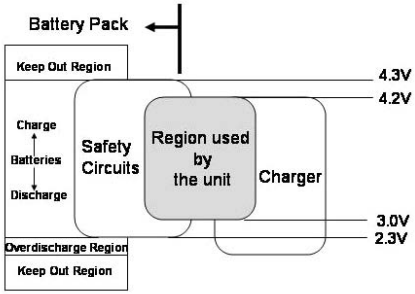
Resistance welding is particularly difficult to master with Li-ion chemistries. Because they have thinner outer walls, Li-ion cells are more delicate than Ni-MH and Ni-Cd cells, and the welding process must be commensurately more precise and consistent. If excessive energy is applied during the welding process, the heat burns a hole in the cell wall, thus destroying it. If there is too little energy, a weak joint is created. Resistance welding must be done in a unique window of pull strength, and the industry standard is 2 kilograms (Kg) (1 weld hit) to 3-Kg (2 weld hit) minimum. Additionally, Li-ion can be less forgiving than other cell chemistries. For example, Ni-based cells, with their thicker cans, can usually sustain multiple welding attempts, while Li-ion will not.

Soldering and welding not only are core processes, but they also are critical success factors in the development of a reliable battery system. To ensure consistent, high-quality welds, it is

important to use only state-of-the-art, computer-controlled welding equipment; perform window studies on every cell; use statistical process-control methods; and perform rigorous pull tests to ensure the highest levels of reliability.

Another design method to achieve higher system reliability and greater manufacturing efficiency is to minimize the number of components used in the battery system by leveraging common components whenever possible. It is important that designers look for opportunities to leverage existing modules, or building blocks, to reduce development time and cut costs.

The development of leading-edge battery technologies does present several design challenges. Because Li-ion and Li-polymer technologies can be hazardous when over-stressed, extra caution must be taken during the design process to ensure that the cells are being utilized in a manner appropriate to their technology. Voltages must be kept between strict operating ranges. Additionally, the use of a safety circuit, separate in function and purpose from any fuel-gauging capability within the battery pack, should be utilized to protect the pack from external stressors, such as overcharging, over-discharging, short-circuiting and excessively high or low operating temperatures. The illustration below is a typical example of recommended operating voltage range for proper lithium ion and lithium polymer safety circuit:



The introduction of complex printed circuit assemblies (PCAs) within a battery pack introduces a number of considerations to be addressed during the design and assembly of a smart battery system. Because most battery packs are encased in plastic that requires ultra-sonic welding (USW), the PCA may be damaged during the assembly process. The importance of proper PCA location and securing within the battery system cannot be overstated.

The PCA's physical configuration and method of connectivity to the rest of the battery system directly influences the reliability, quality and cost-effectiveness of the battery system. Mistakes made by the less-experienced design engineer in this area are among the most common and expensive in the development of battery systems. For example, high current and temperature extremes can cause internal heating within the pack and the pack's electronics. Even though cells may be specified at 1C discharge currents, large packs—for example, three or more cells in parallel—constantly drained at this level may experience internal heating of 15°C to 20°C above ambient. This can harm the battery system's electronics, damaging key components, destroying traces on the circuit board, melting the wires, or degrading the performance of the safety circuitry, battery management electronics and system communications.

Best Practices: Smart Battery System Components

Smart battery systems, or battery systems that can communicate back to the host, are the preferred choice in mission-critical applications such as portable devices. A smart battery pack has the ability to monitor its status, accurately predict its remaining run time, and communicate its operational status to the host device. These features allow the end-user to intelligently manage a device's use and avoid unexpected failures or shutdowns.

A smart battery pack, when programmed to the end-user's unique discharge profile or characteristics, will be better able to deliver a much higher percentage of available power over the operational lifetime of the battery pack. A smart battery pack also can give some feedback on its usage history, which is convenient for traceability and warranty issues.

Only a smart battery system can meet all the requirements of today's portable electronic devices by providing a solution that promises high-performance, maximum durability, long-term reliability and safety.

Smart batteries generally contain a communication device which might count the number of charge and discharge cycles for warranty purposes fuel gauge remaining run time per cycle and battery state of health.

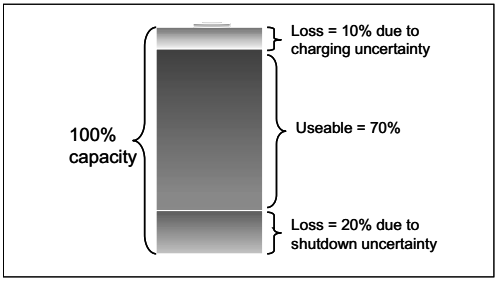
Fuel gauging can be done in several ways. The two most common methods are voltage-based via one-wire protocol and coulomb counting via two-wire protocol.

Voltage-based fuel gauging is the simplest and least expensive to perform. It relies on the periodic voltage measurements of the battery pack, and works best on a cell technology with a sloping discharge curve. This method has its limitations, however, since it only estimates relative capacity and only gives capacity information outside of product use.

The one-wire method (also known as DQ or HDQ) can determine battery capacity by monitoring the amount of current input to, or removed from, a rechargeable battery. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground in order to determine the charge and discharge activity of the battery.

Two-wire, or coulomb counting, is the most accurate method, and allows absolute capacity estimation while giving capacity information during use. The most common protocols for the two-wire method are I^2C and SMBus.

While fuel gauging can make the end-user's life easier, poor fuel-gauge accuracy can limit the performance of the battery system. If temperature, discharge rate and age of the battery are not compensated for, an inaccurate fuel gauge can leave up to 30 percent of available battery capacity unused. Poor accuracy of the fuel gauge may also cause inefficient charging. If the battery is left undercharged or if it overcharges, run time or service life can be shortened.



The ICs must also be calibrated to ensure that they are functioning and communicating properly with the battery pack. Finally, once the battery pack is assembled, a "learn cycle" must be completed so that the battery will remember where "empty" and "full" are, so that the fuel gauge will be set correctly.

Conclusion

Today's sophisticated portable electronic systems have created new challenges for battery system designers. A good design will take into consideration numerous best practices, particularly those related to power needs, safety and accuracy.

The choice of battery chemistry is critical for performance, reliability and cost issues. For these reasons, more designers are turning to advanced formulations, such as Li-ion and Li-polymer. These chemistries deliver high energy densities and competitive cost-per-output for their weight. Chemistry choice and circuitry are defined further by characterizing and validating cells to fit their usage profile.

Advanced battery chemistries demand extra attention for safety considerations. Voltages must be kept within strict operating limits. Safety circuits are mandatory to protect against hazards caused by external stresses. Placement of PCAs is more critical safety issue in smart battery systems as well.

Additionally, smart battery systems require extra attention to highly accurate fuel gauging. Inaccurate fuel gauges may fail to optimize all of a cell's available power, as well as cause inefficient charging.

By recognizing and considering these design challenges, battery system designers can avoid or minimize problems early on, and they can maximize performance, durability, reliability and safety.

Further information about battery chemistries, components and smart battery manufacturing techniques is available at the Micro Power web site, www.micro-power.com, or by contacting Micro Power directly at experts@micro-power.com or 1-800-576-6177.

Digital Designer's Guide to Linear Voltage Regulators and Thermal Management

Bruce Hunter and Patrick Rowland *PMP Portable Power*

ABSTRACT

This application report evaluates the thermal considerations for linear regulator design. The thermal equations governing a linear regulator and the evaluation and selection of a linear regulator for a particular design are presented.

Contents

List of Figures

1 Purpose

The purpose of this application report is to explore the thermal considerations in using linear regulators. When finished, the reader will understand the following:

- Why thermal considerations are important for every linear regulator design
- The thermal equations governing a linear regulator
- How to evaluate/choose linear regulators for a design

In addition, this document provides a *summary of approach and equations* in Chapter 6. This chapter is designed as a one page reference for the reader.

2 The Basics

The first considerations for choosing a linear regulator are input voltage (V_I), output voltage (V_O), and output current (I_O). These are necessary for selecting the appropriate linear regulator for an application. Other very necessary, although often over looked, considerations in linear regulator selection are the application specific thermal considerations. These thermal considerations are the topic of this application report.

For a short review on the theory of operation, a linear regulator has a pass element that is managed by the controller portion of the IC. The controller monitors the feedback and either opens or restricts the pass element to maintain a constant output voltage over variation in the input voltage and the output current required by the load. A helpful analogy is to think of the control portion of the regulator as a lamp dimmer switch or potentiometer.

Where altering a dimmer switch varies the amount of light, a linear regulator alters the pass element to maintain a constant output voltage. We know that Ohm's law states $V = I \times R$. If a linear regulator maintains a constant output voltage (V) over varying input voltage and output current into the load, it follows that R is what is being controlled by the regulator. So that is how we maintain the output voltage, but where does the heat come from?

The difference between the input voltage and output voltage with a fixed load current is energy that is dissipated by the linear regulator. Nearly all of this energy is converted to heat. How to calculate and manage this heat is the topic of this application report.

3 Power Dissipation in the Linear Regulator

To help us understand the power dissipation requirements at a high level, we use the potentiometer model shown in Figure 1.

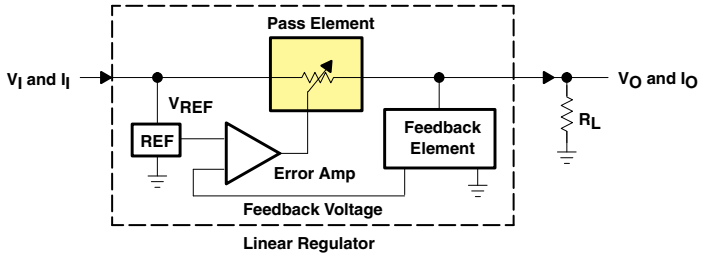


Figure 1. Potentiometer Model of a Linear Regulator

While regulating, the pass element is always on in a linear regulator. Using the potentiometer model as a guide and remembering Kirchoff's current law, we can see how the input current must be equal to the output current. Armed with that knowledge, we can look at power and power dissipation in our system.

Since our system must observe physics and the conservation of energy, we can use our knowledge of V_I, V_O, and current to identify how power is distributed in our model. We start with the power placed into our system:

$$P_I = I_I \times V_I \quad (1)$$

Following the same thought process, the power delivered to the load is:

$$P_O = I_O \times V_O \quad (2)$$

Now, looking back at Figure 1 we remember that I_I roughly equals I_O. The difference between P_I and P_O is the power that is burned or dissipated by the regulator. The quantity of dissipated power (P_D) can be extracted by the following equation:

$$P_D = P_I - P_O \quad (3)$$

P_D is almost entirely heat dissipated by the linear regulator thus P_D is precisely what we are concerned with thermally when selecting a package. If we use equation 3 to arrive at a maximum P_D for an application, we refer to that variable as $P_{D(max)}$. Making this distinction becomes useful in later equations.

Before moving on, we should take a moment to look at equation 3 in slightly more detail. Equation 3 can be rewritten from before as:

$$P_I = P_O + P_D \quad (4)$$

In most applications, the approximation of assuming $I_I = I_O$ is sufficient for thermal calculations. The model we have used up to now has ignored the quiescent current of the linear regulator. If we add the quiescent power (P_Q) required by the linear regulator, equation 4 changes to:

$$P_I = P_O + P_D + P_Q \quad (5)$$

P_Q is derived by multiplying the input voltage by the quiescent current of the regulator. Thermally, P_Q is usually insignificant, as it is orders of magnitude smaller than the output current. For example, the TPS789xx series of 100 mA (or 0.1 A) low dropout regulators (LDO) has a typical I_Q of 17 μA (or 0.000017 A). In an example where the TPS78925 is used with V_I = 3.3 V, V_O = 2.5 V, and I_O = 100 mA we can see how P_Q (56 μW) is substantially smaller than P_D (80 mW). Thus, out of practicality and for simplicity we examine the thermal considerations for linear regulators based on equation 4 ignoring quiescent current.

Quiescent current can have a significant impact on efficiency in power sensitive applications. This is covered briefly in *Other Useful Items* (Chapter 8) and in more detail in the *Efficiency* portion of TI application reports SLVA079 – *Understanding the Terms and Definitions of Low-Dropout Voltage Regulators* and SLVA072 – *Technical Review of Low Dropout Voltage Regulator Operation and Performance,* as listed in Appendix B.

Another topic that warrants a brief commentary is steady state verses transient or pulsed current demand of a load from its power supply. In many applications, an LDO supplies both steady-state and pulsed load current. A given design may have low duty cycle load transient currents in addition to the steady-state load. The current transients can approach the internal fixed current limit of the LDO, which is normally between 2 and 4 times the continuous current rating of the device. However, if we have an excessive junction temperature rise, thermal shutdown is activated. The thermal shutdown junction temperature typically occurs at 150°C. Whether the thermal design is based upon the average load current or designed to handle the maximum peak current depends upon the duration and frequency of occurrence of the load transient. In either case we are safe if we do not exceed the absolute maximum junction temperature rating of the device.

Returning to P_D, the power ratings of LDOs are normally based upon steady state operating conditions. Steady-state conditions between junction and case are typically achieved in less than 10 seconds where several minutes may be required to achieve steady-state junction to ambient. Transient thermal impedance illustrates the thermal response to a step change in power. This information is provided for discrete power devices and normally not for integrated circuits. The transient thermal response is a function of die size, die attach, and package. We limit the scope of our discussion to steady-state thermal resistance.

By utilizing the thermal equations that follow in Chapter 4, we ensure that the junction temperature of our linear regulator remains within acceptable limits. A semiconductor's long term reliability is affected by its operating junction temperature; therefore, it is important to maintain a junction temperature that falls below the manufacturers absolute maximum operating junction temperature. This restriction limits the device's power dissipation capability. To do this, we need to calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$. How to make these calculations is what we explore next.

Factors which influence thermal performance include PCB design, component placement, interaction with other components on the board, airflow, and altitude. There is no substitute for a system level thermal analysis to ensure a successful design.

4 Thermal Equations—Will My Part Work?

With an understanding of P_D, now we can examine the thermal considerations P_D generates. The following equation links P_D to the thermal specifications for a linear regulator:

$$P_D = (T_J - T_A)/\theta_{JA} \quad (6)$$

Where

θ_{JA} = theta ja (junction to ambient) – °C/W

T_J = junction temperature rating – °C

T_A = ambient temperature – °C

P_D = power dissipated in watts – W

Equation 6 enables us to relate power dissipation with the thermal characteristics of the die/package combination and ambient temperature. It is useful to manipulate equation 6 to:

$$\theta_{JA} = (T_J - T_A)/P_D \quad (7)$$

Equation 7 is useful as T_J, T_A, and $P_{D(max)}$ (see equation 3) are often known quantities in an application. By using these three known values, equation 7 will tell us what value of θ_{JA} is necessary in order to have enough thermal conductance or thermal dissipation capability for our linear regulator in a particular application. Having the appropriate thermal conductance ensures that the $P_{D(max)}$ does not exceed the P_D that the linear regulator is capable of supporting. Exceeding the P_D that the regulator can support creates extreme junction temperatures which in turn impact the reliability of the design. For the remainder of this application note, if we use $P_{D(max)}$ in equation 7 to determine a maximum θ_{JA} for an application, we are referring to it as $\theta_{JA(max)}$.

In looking at equation 7, θ_{JA} decreases with an increase in T_A or P_D. It follows that the lower θ_{JA} is from equation 7, the more challenging the thermal requirements. Additionally, the lower a θ_{JA} is specified in a data sheet, the better thermal conductance a device exhibits.

Most vendors specify θ_{JA} in a linear regulator data sheet as the thermal specification. At TI, this was the case until recently and is still the case for higher power, higher output current linear regulators. To make regulator selection easier, TI has moved to a different way of representing the same information. As an example, data sheet examples have been provided below. (NOTE: xx is the voltage option. For example: TPS77618 is the 1.8 V option in the family). Figure 2 and Figure 3 show power dissipation ratings based on package, airflow, ambient temperature, and in the case of the PowerPAD™ package, copper area underneath the device. In this case, instead of looking for a θ_{JA}, we can simply compare $P_{D(max)}$ from equation 3 to these tables so long as we cross-reference the appropriate package, ambient temperature, copper area, and airflow. Figure 4 is from page 13, of the REG103 data sheet. It demonstrates how drastically factors such as airflow or copper area, as in this case, can alter the thermal properties of a linear regulator.

PowerPAD is a trademark of Texas Instruments.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range **(see Note 1)**	–0.3 V to 10 V
Voltage range at EN	–0.3 V to V_I + 0.3 V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See Dissipation Rating Tables
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

Pdmax table

DISSIPATION RATING TABLE

	PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I†	2.7		10	V
Continuous output current, I_O	0		150	mA
Operating junction temperature, T_J	–40		125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation:

$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$

Tj specification

Figure 2. Power Dissipation Table From the TPS763xx Data Sheet (April 00)

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568.18 mW	5.6818 mW/°C	312.5 mW	227.27 mW
	250	904.15 mW	9.0415 mW/°C	497.28 mW	361.66 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP‖	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).
‖ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

Note: different Pdmax with different copper & airflow!

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I★	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	1.0	A
Operating virtual junction temperature, T_J (Note 1)	−40	125	°C

★ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

Figure 3. Power Dissipation Table From the TPS768xx Data Sheet (July 99)

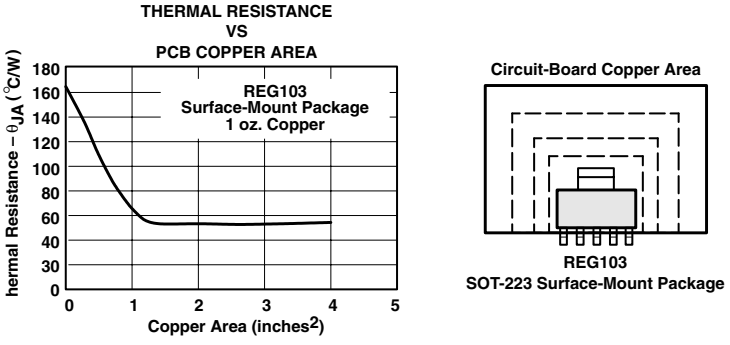


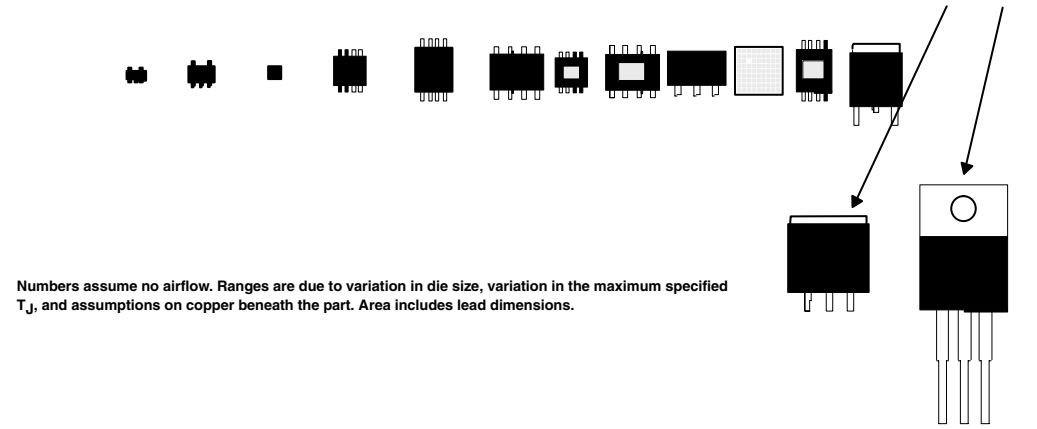
Figure 4. Thermal Resistance vs PCB Area for 5 Leaded SOT223

Depending on the data sheet, either $\theta_{JA(max)}$ or $P_{D(max)}$ can be used as a reference to determine which package meets the thermal requirements in an application. If the θ_{JA} on the data sheet is lower than the calculated $\theta_{JA(max)}$ from equation 7 or $P_{D(max)}$ from equation 3 is lower than the power dissipation tables provided, then our linear regulator is appropriate for the thermal requirements of an application. If we do not meet these criterions we must take additional steps to accommodate the thermal dissipation required by the application. Failure to do so potentially impacts the reliability of the design.

5 Thermal Equations—What to Do if My Part Does not Work?

In situations where a device or package is thermally insufficient, the first step is to look at other package options. This is one significant reason why vendors often offer linear regulators in multiple package options and why the smallest package is not always the appropriate choice. It is also possible that, if the original device does not have an appropriate package option, an engineer needs to look at a linear regulator with higher output current than is required by the application to obtain the necessary θ_{JA} to ensure reliable operation. Linear regulators with higher output current generally have a larger die and come in larger, more thermally efficient, packages. Both of these items lead to better, lower θ_{JA} or higher $P_{D(max)}$, ratings. The following figure shows a list of packages relative to thermal efficiency.

Package - # Pins	SC70 (SOT323)	SOT23-5	Chipscale 4-1 bump	MSOP-8	TSSOP 14-20	SOIC-8	PowerPad MSOP-8	PowerPad SOIC-8	SOT223	uBGA-24	PowerPad TSSOP-24	DDPAK	TO263	TO220
Suffix	DCK	DBV	YEA/YZA	DGK	PW	D	DGK	D	DCQ	GQE	PW	KTP	KTE/KTG	KC
θ_{JA} (°C/W)	314-478	9.00	154-330	160-235	148-172	97-178	58-83	55	53-175	48	42-48	28-65	23-38	22-58
Area (mmsq)	4.94	9.00	0.81-3.20	15.18	33.96-43.95	31.00	15.18	31.00	47.55	10.24	52.14	59.72	101.58	196.54



Numbers assume no airflow. Ranges are due to variation in die size, variation in the maximum specified T_J, and assumptions on copper beneath the part. Area includes lead dimensions.

Figure 5. Thermal and Area Comparison of Packages

θ_{JA} for a package varies between different parts and different vendors. Variables that affect θ_{JA} include the copper properties of a board, the number of layers of a board, the airflow over a board, and whether a high K or low K model was used (see TI application note SCAA022A – *K–Factor Test Board Design Impact on Thermal Impedance Measurements*), etc. Figure 5 is an estimate for comparison purposes only. Always consult the data sheet to obtain θ_{JA} or $P_{D(max)}$ for a given device and package option.

There is some overlap and minor variation in packages depending on pin count and die size, but Figure 5 is a starting point for comparison of common packages. Also included in the list is TI's patented PowerPAD™ packaging technology. PowerPAD footprints and dimensions remain standard while the exposed thermal pad greatly enhances the thermal capabilities of the PowerPAD MSOP, TSSOP, and SOIC packages. For more information about PowerPAD, see TI application brief SLMA004, *PowerPAD Made Easy*, and/or application note SLMA002, *PowerPAD Thermally Enhanced Package*. Both of these documents are listed in Appendix B.

Where thermal considerations are challenging, another approach is to look at a switching regulator. Often, the additional efficiency that can be possible with a switching design can alleviate thermal issues faced when using a linear regulator approach. There are many considerations in migrating from a linear to a switching design that are beyond the scope of this application report.

Continuing with linear regulators, if by using equation 7 we arrive at a θ_{JA} that indicates that we have no package options to meet the thermal dissipation, the addition of a heatsink is an alternative. While often a last resort, a heatsink adds thermal mass that improves the thermal conductivity of a regulator. This effectively lowers θ_{JA} of the system and enables the linear regulator to dissipate a higher $P_{D(max)}$. A helpful analogy is to think of our thermal system in terms of resistance as shown in Figure 6.

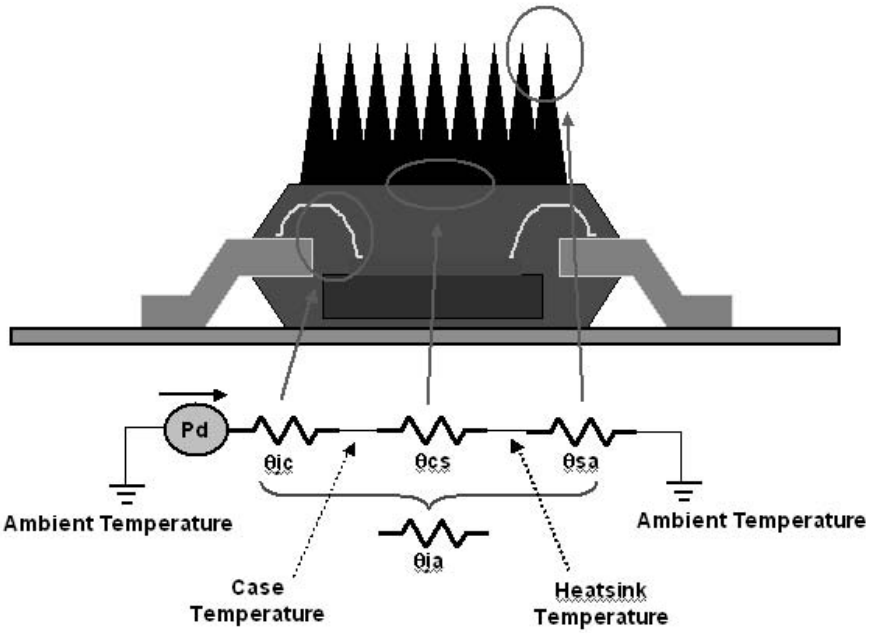


Figure 6. Steady State Thermal Equivalent Model

In this example, we are referring to:

θ_{JA} = theta JA (junction to ambient) – °C/W
θ_{JC} = theta JC (junction to case) – °C/W
θ_{CS} = theta CS (case to heatsink) – °C/W
θ_{SA} = theta SA (heatsink to ambient) – °C/W

NOTE: θ_{CS} is the thermal interface between the device case and the sink whether it is air, PCB/solder, or any other kind of heatsink.

Our simplified steady state heat transfer model is analogous to Ohm's law. Power dissipation is analogous to current, θ is analogous to electrical resistance, and ambient temperature is analogous to ground potential or our reference point. We have used θ_{JA} up to now as we were depending on the package for a complete thermal system from junction to ambient. Since a heatsink has been added, it is necessary to break the system down into more granular components.

Adding a heatsink achieves a system θ junction to ambient low enough to meet the system thermal requirements. A heatsink accomplishes this by offering a better thermal interface to air versus the package alone. Thus, we require the following to be met:

$$\theta_{JA(max)} \geq \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (8)$$

Where $\theta_{JA(max)}$ is the max acceptable thermal rating that meets the system requirements. This equation can be manipulated to:

$$\theta_{SA} \leq \theta_{JA(max)} - \theta_{JC} - \theta_{CS} \quad (9)$$

If we refer back to equation 7, we can substitute $(T_J - T_A)/P_D$ for θ_{JA} to obtain a $\theta_{JA(max)}$ and arrive at:

$$\theta_{SA} \leq [(T_J - T_A)/P_{D(max)}] - \theta_{JC} - \theta_{CS} \quad (10)$$

Equation 10 gives the designer one equation of what are normally known variables and yields the maximum allowable value for a heatsink in an application.

The value of θ_{CS} depends upon the interface material and device mounting. In the case of a PowerPAD or a TO-263 package where the exposed pad is soldered directly to the bare printed-circuit board copper, θ_{CS} is essentially 0°C/W. For a TO-220 package, which is mounted to a heatsink with a bolt or clip, a thermal interface material is used to fill voids between the tab and heat sink. The interface thermal resistance depends upon the material used and is effected by the mounting pressure, material thickness, and flatness of each surface. Typical values of common interface material range between 0.1°C/W and 1°C/W and if no interface material is used could be as high as 5°C/W.

The user should consult the interface or heat sink vender to determine a suitable material to meet the desired design goals.

By solving equation 10, we arrive at the required thermal impedance of the heatsink. Some packages, such as the TO-220, TO-263, or DDPAK better lend themselves to using heatsinks. Packages such as the SC70 and SOT23 due to their physical size, are not generally considered for use with heatsinks. Appendix A has a short list of some thermal management vendors. The vendors listed do offer various solutions for different package types. TI does not endorse one vendor over another and there are many other thermal management vendors not listed.

Having read this far, the reader should have a basic understanding of the following:

- Why thermal considerations are important in linear regulator design
- Thermal equations for a linear regulator
- How to thermally evaluate different regulators for a design

The subsequent chapters of this applications report include a summary, real world examples, items to look out for, and appendixes including reference material, and additional useful information on linear regulators and TI PowerPAD packaging technology.

6 Summary of Approach and Equations

This chapter is a one page summary engineers can use to quickly evaluate a linear regulator.

With V_I, V_O, and $I_{O\ (max)}$ in hand, calculate $P_{D(max)}$ with:

$$P_{D(max)} = P_I - P_O \quad (3)$$
$$= (V_I - V_O) \times I_O \quad (11)$$

NOTE: The I_Q of the linear regulator is ignored due to its relative small size to I_O. Thus, we assume $I_I = I_O$.

Then, take $P_{D(max)}$ and consult the data sheets of all perspective linear regulators. If the data sheet has power dissipation tables in watts, use $P_{D(max)}$ and compare the package with the rating associated with the appropriate ambient temperature, copper area, and airflow. If the data sheet only offers a θ_{JA} for the package, calculate $\theta_{JA(max)}$ using:

$$\theta_{JA(max)} = (T_J - T_A)/P_{D(max)} \quad (7)$$

If $P_{D(max)}$ is less than the power noted in the power dissipation table or θ_{JA} in the data sheet is less than the $\theta_{JA(max)}$ calculated in equation 7, the package is thermally acceptable. Otherwise, the package is not acceptable and an alternative should be found. Also, always be sure to reference θ_{JA} or $P_{D(max)}$ with the appropriate copper area and airflow for the application when reading a data sheet.

In the case where the initial linear regulator is thermally insufficient, the easiest alternative is to look for a different package. Figure 5 is a reasonable reference to help start such a search. It is possible a linear regulator with more output current capability than required by the application may be necessary to obtain the appropriate thermal properties.

If no package can be found to meet the thermal needs for the application, the next step is to consider the addition of a heatsink or move to a switching power solution. When looking for a heatsink, use θ_{JA} calculated in equation 7 and substitute it into equation 9:

$$\theta_{SA} \leq \theta_{JA(max)} - \theta_{JC} - \theta_{CS} \quad (9)$$

This yields the θ_{SA} required for the heatsink. The other major considerations in choosing a heatsink are form factor and mounting options for the linear regulator package.

7 Things Often Overlooked

Included in this chapter are answers to common questions and items that are often overlooked.

7.1 Differences Between Vendors

In making a thermal comparison between linear regulator vendors, always check the data sheet. Different manufacturers are more or less aggressive in specifying θ_{JA} and the maximum recommended junction temperature for a given package type. In addition, different vendors make different assumptions on things such as airflow or copper area under a device. Lead frame options such as TI's PowerPAD can also drastically alter the thermal capabilities of a package.

Never assume similar parts have similar thermal capabilities, particularly when they come from different vendors, and always be aware of what assumptions or conditions the specifications assume.

7.2 The Math Does Not Work... But the Part Does

It is not uncommon to find situations where the thermal equations indicate a potential problem but a part seems to work. Recall equation 7:

$$\theta_{JA} = (T_J - T_A)/P_D \quad (7)$$

does not take into account airflow or the potential benefits of heatsinking into the PCB copper. In addition, manufacturers build headroom into their specifications. The cumulative headroom this provides could allow a part to work outside what is covered in the data sheet and this document.

If additional factors such as heatsinking into the PCB copper cannot account for why a part works, it is not advised to continue to use it in a design. Violating the thermal ratings on a device can reduce the long-term reliability of the design.

The flip side to this is the situation where the original circuit was over-engineered for prototyping and exceeds what current the application requires. While the temptation is to leave the circuit as is, technically and financially it is often worth re-examining an over-engineered LDO. It can be possible to obtain advantages in both cost and space with a minimal amount of work to populate the function with a properly sized LDO.

7.3 Derating

Often, in demanding applications, companies have a policy of derating the integrated circuits they use. Depending on the project or end equipment this can be done in a variety of ways. From a thermal perspective, one often derates the absolute maximum junction temperature (T_J) for specific system reliability considerations when derating is necessary. This, in turn, decreases $\theta_{JA(max)}$ in equation 6, which causes the application's thermal design to be more demanding and operation more robust.

It is up to the user to determine device suitability for a given application. It is important that the device operate within the manufacturers operating conditions stated in the data sheet. Device operation at or above the absolute maximum ratings, which includes temperature, voltage, and current causes premature device failure.

Several reliability prediction standards are used to assess product life such as MIL-HDBK-217F and Bellcore TR-NWT-000332. Mil-HDBK-217F defines two prediction methods; a part stress analysis and parts count reliability prediction.

Common stresses that are known to accelerate device failure mechanisms include temperature, voltage, current, humidity, and temperature cycling. Temperature accelerates many chemical or physical processes that may shorten the usable life of a semiconductor device.

The Arrhenius model is commonly used for semiconductor reliability prediction. The model assumes that device failure rate is linear with time and that the acceleration factor is a function of device junction temperature. The mean time between failure (MTBF) is defined as the inverse of the acceleration factor (f). Equation 12 shows the acceleration factor expressed as the ratio of a time to fail at one temperature to a time to fail at a different temperature.

$$\text{Acceleration factor } f = \frac{t1}{t2} = \exp\left[\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right] \quad (12)$$

Where:

Ea = Activation energy (ev)
K = Boltzmans constant 8.6 x 10E–5 ev/°K
t1 = Time between failure at temperature T1
t2 = Time between failure at temperature T2
T1 = Junction temperature (°K) at time t1
T2 = Junction temperature (°K) at time t2 where T2 >T1

We can use this equation to illustrate the effect on the MTBF by derating the maximum allowable junction temperature of the device. For this exercise we assume an activation energy of 0.9 ev. The manufacturers maximum operating junction temperature is found in the absolute maximum ratings table in the data sheet. Many low dropout regulators are specified with an absolute maximum rating of 125°C. If we reduce the maximum allowable junction temperature by 10°C for a given design we see that the MTBF approximately doubles.

In many applications it is unnecessary to derate components. This discussion was provided as an example of one common way to derate components when necessary.

8 Other Useful Items

Included in this chapter are quick references to a few useful items regarding linear regulators.

8.1 Linear Regulator Efficiency

Efficiency of any power regulator is:

$$\text{Eff} = P_O/P_I \times 100\% = (V_O \times I_O)/(V_I \times I_I) \times 100\% \quad (13)$$

If we make the assumption as we did before that $I_I = I_O$ for a linear regulator discounting I_Q due to its relative size compared with I_O, this can be simplified to:

$$\text{Eff} = V_O/V_I \times 100\% \quad (14)$$

This is a good rule of thumb, but remember, this only holds for a linear regulator design. Switching power supplies cannot be analyzed in this way.

There are applications that need to take into account the I_Q of the linear regulator. To consider I_Q, I_O no longer equals I_I and thus equation 14 is invalid. To consider I_Q, we examine equation 5:

$$P_I = P_O + P_D + P_Q \quad (5)$$

Since quiescent power dissipation, P_Q, is also derived from the input voltage, equation 13 can be manipulated to:

$$\text{Eff} = (V_O \times I_O)/[(V_I \times I_I) + (V_I \times I_Q)] \times 100\% \quad (15)$$

Assuming I_Q comes from the same source, V_I, as does I_I. An example where this is not the case is the UC382 as it has a bias supply input, V_B, which draws I_Q. The UC382 aside and assuming both I_I and I_Q come from the same source, we return to our potentiometer module from Chapter 3, and we conclude that:

$$\text{Eff} = (V_O \times I_O)/[V_I \times (I_O + I_Q)] \times 100\% \quad (16)$$

Again, remember these equations only apply to a linear regulator design. One example of an application where this granularity could be important is in portable end equipments where the load is *asleep* for the majority of the time. With a very small load current for a significant amount of time, I_Q can become a significant factor in efficiency and product run time. This is why companies such as TI have low I_Q families of linear regulators. For comparison, the TPS761xx family of LDO's has a typical quiescent current of 2.6 mA where the TPS769xx family has a typical quiescent current of 0.017 mA. Both are 100-mA LDOs, but the TPS769xx was designed for power sensitive applications as are other TI LDOs which offer even lower I_Q than the TPS769xx.

With regard to I_Q, we must also keep in mind what the relationship is between I_Q and output current. PMOS linear regulators are generally load independent.

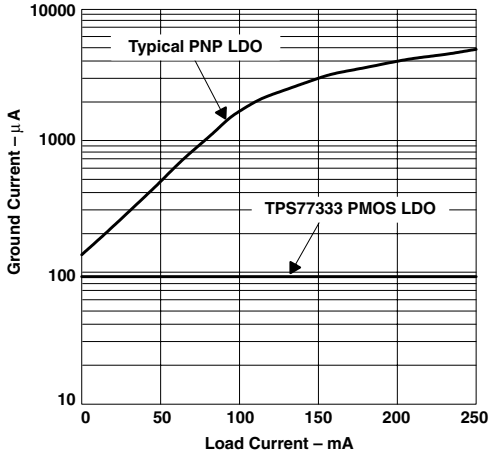


Figure 7. Comparison of 100- A I_Q PMOS and PNP LDOs

As illustrated in Figure 7, the PMOS linear regulators I_Q is essentially constant as a function of load current. In contrast, bipolar linear regulators have I_Q characteristics that are load dependent. This can be important to take into account before deciding that I_Q is negligible. Particularly for bipolar linear regulators, it is good practice to consult the graphs in the data sheet if they are provided.

8.2 Input Voltage, Dropout Voltage (V_{DO}), and Low Dropout Regulators (LDO's)

Dropout voltage for linear regulators is often misunderstood. As discussed previously, the difference between V_I and V_O is the voltage drop across the linear regulator. The lower the difference between the input and output voltage, the lower the power dissipation for a given load current. The dropout voltage is defined as the minimum difference required between V_I and V_O for the regulator to operate within specification. A subset of linear regulators called *low dropout regulators* (or *LDO*) exhibits small dropout specifications. This can be an advantage when:

- V_I and V_O are close in value
- V_I can be manipulated to be close to V_O thus reducing P_D and increasing efficiency
- A battery is the V_I source, thus allowing the regulator to draw voltage from the battery and regulate over a wider range

Figure 8 demonstrates what a dropout voltage specification means visually.

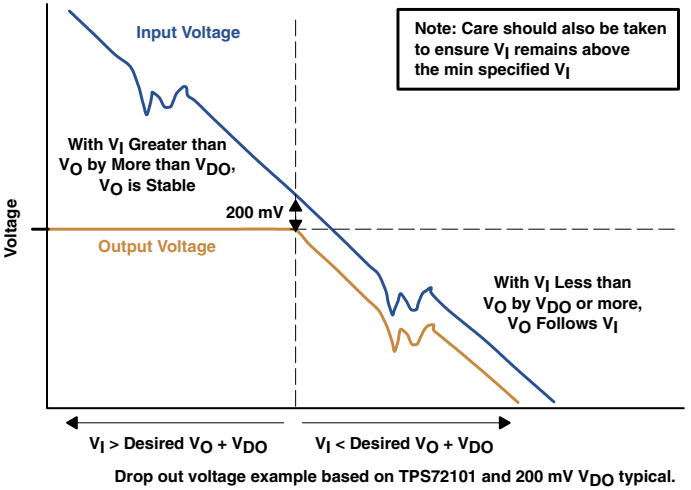


Figure 8. Dropout Voltage Example

To highlight the difference between a standard linear regulator and what is considered an LDO, look at the V_{DO} specification on both the TPS77601 and the LM317M. TI considers anything with a V_{DO} < 1 V to be an LDO and anything with V_{DO} > 1 V to be a *standard* linear regulator. In summary, the minimum input voltage as shown in Figure 8 is the greater value of either V_O + V_{DO} or the minimum specified input voltage.

The ultimate combination is an LDO that has both a low dropout and an input voltage range that extends to relatively low voltages. An example of this is the TPS721xx (150 mA), TPS722xx (50 mA), and TPS725xx (1 A) series. This series is the first LDO in the industry to allow V_I down to 1.8 V and a very small V_{DO} which allows these parts to run directly off batteries in portable applications or off other core voltages for point-of-use needs. As a side note, this family of LDOs also features stability with any output capacitor providing even more flexibility in designs.

9 Real World Examples

Included in this chapter are four real world examples to further illustrate the thermal concepts presented in this application report.

Example 1:

We need to power a C5409 DSP core with a small amount of additional logic at 1.8 V. The application calls for a 100 mA solution at 1.8 V and this rail needs to be created from 5 V. The maximum ambient temperature is 70°C, and we assume zero airflow. The TPS76318 and REG101-A linear regulators are under consideration. Which device(s) and package options are acceptable?

Answer:

As a side note, if we take a quick look at efficiency with equation 14:

$$\text{Eff} = V_O/V_I \times 100\%$$
$$\text{Eff} = 1.8\ V/5\ V \times 100\% = \sim 36\%$$

Obviously, a linear regulator is not the optimal solution for efficiency in this case but we assume efficiency is not a primary design goal in this application.

Both the TPS76318 and REG101-A have an acceptable input voltage range, output voltage range, and output current capability. The potential pitfall in this application are the thermal considerations.

Ignoring the I_Q of the linear regulator, at 100 mA output current we calculate the input and output power:

$$\text{Output Power: } P = I \times V = 100\ mA \times 1.8\ V = 180\ mW$$
$$\text{Input Power: } P = I \times V = 100\ mA \times 5\ V = 500\ mW$$

$$P_D = P_I - P_O$$
$$P_{D(max)} = 500\ mW - 180\ mW = 320\ mW$$

With the TPS76318 data sheet, we cross reference $P_{D(max)}$ with our ambient temperature in the thermal tables.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K‡	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K§	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

‡ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
§ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I¶	2.7		10	V
Continuous output current, I_O	0		150	mA
Operating junction temperature, T_J	−40		125	°C

Figure 9. Power Dissipation Table From the TPS76318 Data Sheet (May 01)

We see that 320 mW at 70°C is a problem and that the SOT23 package is not suitable for this application. The REG101-A data sheet addresses thermal considerations in terms of θ_{JA}. Using equation 7, T_A, and $P_{D(max)}$ we can evaluate the REG101-A:

$\theta_{JA} = (T_J - T_A)/P_D$
$\theta_{JA} = (125°C - 70°C)/0.320\ W = \sim 171°C/W$

In looking at the θ_{JA} ratings shown in Figure 10 for the REG101–A we see that the SOT23 package option is still unacceptable. However the SO-8 package option is suitable having a θ_{JA} less than 171°C/W.

TEMPERATURE RANGE						
Specified Range	T_J		–40		+85	°C
Operating Range	T_J		–55		+125	°C
Storage Range	T_A		–65		+150	°C
Thermal Resistance						
SOT23-5 Surface Mount	θ_{JA}	Junction-to-Ambient		200		°C/W
SO-8 Surface Mount	θ_{JA}	Junction-to-Ambient		150		°C/W

Figure 10. From the REG101 Data Sheet (July 01)

In this example, we see quickly how thermal considerations can impact component selection with linear regulators.

To take this example a step further:

- *What would happen if the output current increased to 150 mA?*
  - $P_{D(max)}$ increases to 580 mW, θ_{JA} decreases to 95°C/W, and Eff is the same. Neither part is an option as neither has an acceptable package. 150 mA is beyond the REG101-A specification for output current also. A more appropriate part may be the 250 mA REG102-A in a SOT223 package with a θ_{JA} close to 60°C/W among other choices from TI.
- *What would happen if V_I were lowered to 3.3 V with 100-mA output current?*
  - $P_{D(max)}$ becomes 190 mW, θ_{JA} becomes to 289°C/W, and Eff is ~54%. Now, both of our original parts would work in the smaller SOT23 package option.

These basic changes produce drastic differences to our thermal considerations.

Example 2:

The TPS76833 linear regulator is available in an 8-pin SO and a 20-pin TSSOP package. Determine which package option will meet the following criteria:

$V_I = 5.0\ V + 5\%$
$V_O = 3.3\ V \pm 2\%$
I_O: 0.95 A
$T_A = 50°C$, natural convection air flow

Answer:

First, determine the required worst case power dissipation.

$P_{D(max)} = (V_I - V_O) \times I_O$
$= [(V_I \times 1.05) - (V_O \times 0.98)] \times I_O$
$= (5.25 - 3.234) \times 0.95$
$= 1.915\ W$

Now determine the maximum package thermal impedance requirement given the above criteria.

$P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$ Rearranging and solving for θ_{JA}

$\theta_{JA} \leq (T_{J(max)} - T_A)/P_{D(max)}$

From the TPS76815 data sheet we see that the absolute maximum junction temperature is 125°C. In this application, your company mandates that all components have derated $T_{J(max)}$. For this example we derate by 10°C.

Let $T_{J(max)} = 115°C$

Therefore the required $\theta_{JA} \leq (115 - 50)°C/1.915\ W = 33.9°C/W$

From the data sheet we see that the 8-pin SOIC package (D) does not meet the requirement since it has a θ_{JA} of 172°C/W. The 20-pin TSSOP PowerPAD package (PWP) meets the requirement having a θ_{JA} of 32.6°C/W if it is mounted on a board having a copper heat sink area of at least four square inches (1 oz. copper).

Example 3:

The REG104 linear regulator is available in a SOT223 and TO-263 surface mount packaging. Determine which package option meets the following criteria:

$V_I = 5.0\ V + 5\%$

$V_O = 2.5\ V \pm 2\%$

I_O: 1.0 A

$T_A = 50°C$, natural convection air flow

Answer:

First, determine the required worst case power dissipation:

$P_{D(max)} = (V_I - V_O) \times I_O$

$= [(V_I \times 1.05) - (V_O \times 0.98)] \times I_O$

$= (5.25 - 2.45) \times 1 = 2.8\ W$

Now determine the maximum package thermal impedance requirement given the above criteria.

$P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$ Rearrange and solving for θ_{JA}

$\theta_{JA} \leq (T_{J(max)} - T_A)/P_{D(max)}$

From the REG104 data sheet we see that the absolute maximum junction temperature is 150°C. Thus,

Let $T_{J(max)} = 150°C$

Therefore the required $\theta_{JA} \leq (150 - 50)°C/2.8\ W = 35.7°C/W$

From Figure 10 of the REG104 data sheet we see that a TO-263 mounted on 1.5 square inches of 1 oz. copper has a θ_{JA} of 32°C/W. Since the mounting tab is at ground potential, the entire ground plane can be used to further reduce the thermal impedance.

Example 4:

Given that a TMS320C6201 DSP has the following system requirements:

Core: 1.8 V ±3% at 1.0 W
I/O: 3.3 V ±5% at 0.2 W
V_I = 5.0 V ±5%
T_A = 50°C

Find a suitable power solution using a dual LDO regulator to power the DSP system.

We must first determine the total power dissipation required for the dual regulator.

$P_{D(core)} = (V_I - V_{core})) \times I_{(core)}$
$= (V_I(1.05) - V_{core}(0.97)) P_{core}/V_{core}(0.97)$
$= (5.25 - 1.75)\ (1.0)/1.75 = 2.0$ W

$P_{D(I/O)} = (V_I - V_{O(I/O)}) \times I_{(I/O)}$
$= (V_I(1.05) - V_{I/O}(0.95)) P_{I/O}/V_{I/O}(0.95)$
$= (5.25 - 3.14)\ (0.2)/3.14 = 0.134$ W

Total regulator dissipation = $P_{D(core)} + P_{D(I/O)}$ = 2.0 W + 0.124 W = 2.124 W

Next, determine the required maximum package thermal impedance.

Maximum allowable dissipation:

$P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$
$\theta_{JA} \leq (T_{J(max)} - T_A)/P_{D(max)}$

Most of the TI LDO data sheets list an absolute maximum junction temperature rating of 125°C. Thus,

Let $T_{J(max)}$ = 125°C
Therefore $\theta_{JA} \leq (125 - 50)/2.124 = 35.3$°C

The DSP power selection matrix table (page 35) of the *Power Management Selection Guide*, literature number SLVT145 recommends the TPS767D318 as a possible product to meet the system requirements. From the TPS767D318 data sheet we find that it meets the voltage and tolerance requirements as well as thermal. It features a θ_{JA} of 32.6°C/W if at least four square inches of 1 oz. copper heat sink area is used. Since the thermal pad is at ground potential, the entire ground plane could be used to further reduce the thermal impedance.

Appendix A Thermal Managment Vendors

- Aavid Thermal Technologies http://www.aavidthermalloy.com/
- Bergquest Company http://www.bergquistcompany.com/
- IERC http://www.ctscorp.com/ierc/
- Wakefield Engineering http://www.wakefield.com/

Appendix B Additional TI Documentation on Thermal Topics, Packaging, and Linerar Regulators

1. Fundamental Theory of PMOS Low-Dropout Voltage Regulators
   http://www–s.ti.com/sc/psheets/slva068/slva068.pdf
   Covers the basics of how a linear regulator, specifically a PMOS Low-Dropout regulator, functions.
2. Understanding the Terms and Definitions of Low-Dropout Voltage Regulators
   http://www–s.ti.com/sc/psheets/slva079/slva079.pdf
   Briefly defines common terms associated with Low-Dropout regulators including Quiescent Current, Efficiency, Dropout Voltage, Line and Load Regulation, and more.
3. Technical Review of Low Dropout Voltage Regulator Operation and Performance
   http://www–s.ti.com/sc/psheets/slva072/slva072.pdf
   A more in depth discussion of common Low-Dropout regulator specifications including Quiescent Current, Efficiency, Dropout Voltage, Line and Load Regulation, Stability, and more.
4. PowerFLEX™ Surface Mount Power Packaging
   http://www–s.ti.com/sc/psheets/slit115a/slit115a.pdf
   This document could be particularly helpful with TI's surface mount alternatives to TO-220 packages.
5. Thermal Characteristics of SLL (Standard Linear Logic) Package and Devices
   http://www–s.ti.com/sc/psheets/scza005b/scza005b.pdf
   This document has an exhaustive list of packages covered and runs though some of the same calculations covered in this paper.
6. K-Factor Test-Board Design Impact on Thermal Impedance Measurements
   http://www–s.ti.com/sc/psheets/scaa022a/scaa022a.pdf
7. PowerPAD Made Easy
   http://www–s.ti.com/sc/psheets/slma004/slma004.pdf
   This application note is a quick reference explaining what is TI's PowerPAD thermal enhancement and how does one use a part in this package.
8. PowerPAD Thermally Enhanced Package
   http://www–s.ti.com/sc/psheets/slma002/slma002.pdf
   This application note is a more extensive review of the PowerPAD technology and equations behind and implementation of products using this package.
9. MicroStar BGA Packaging Reference Guide
   http://www–s.ti.com/sc/psheets/ssyz015b/ssyz015b.pdf
   This contains 6x6 – 16x16 BGA thermal information.
10. Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs
    http://www–s.ti.com/sc/psheets/szza017a/szza017a.pdf

11. Thermal Derating Curves for Logic-Products Packages
http://www–s.ti.com/sc/psheets/szza013a/szza013a.pdf

12. PT3100/4100 Series Application note revised 5/15/98.

13. TI external website for packaging information
http://www.ti.com/sc/docs/package/pkg_thermal_db.htm
As an example, if looking for TSSOP information: *Enter packaging group = all, package type TSSOP, JEDEC design guidelines = all, Then SEARCH.*

NOTE: *urls are provided for quick reference, but as the web is always changing please be aware that these links may change as well! If you have trouble finding one of these documents, please contact your local TI representative or your regional TI Product Information Center.*

Appendix C Other References

1. S. M. Sze, VLSI Technology, McGraw-Hill, New York, 1988.
2. AN1029 Fairchild, April, 1996
   Maximum Power Enhancement Techniques for SO-8 Power MOSFETs
   Alan Li, Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong
   Note: Related documents include AN1028, AN1025, AN1026 for other packages.
3. AN–569, Motorola, 1973
   Transient Thermal Resistance—General Data and Its Use
   Bill Roehr and Bryce Shiner

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Gas Gauging Basics Using TI's Battery Monitor ICs

Battery Management

Introduction

The new generation of wireless devices, PDAs, internet audio players and other appliances demand accurate battery capacity monitoring. The improvement in feature content and complexity of these portable devices has had a dramatic impact on the battery and battery management. The simple and inaccurate voltage-based capacity-monitoring schemes of the past are no longer acceptable. The users demand to know the *real* available capacity. They need to know how many more audio files can be downloaded, how many more stock trades can be placed, and how many more calls can be made before the battery finally runs out. An inaccurate capacity gauge is both annoying and frustrating to the end-user.

A voltage-based capacity-monitoring scheme lacks the required accuracy for today's wireless applications. Lithium-Ion and Lithium-Polymer batteries, for instance, have a relatively flat voltage profile in both charge and discharge directions. In fact, during a typical charge cycle, more than 70% of the charge time is spent in a *constant voltage* mode. This mode is responsible for replenishing more than 40% of the charge capacity. Similarly, on a discharge cycle, most of the capacity is available in a relatively narrow voltage range, from 3.7 down to 3 V.

To make matters worse, the available capacity also changes as a function of self-discharge, cell aging, temperature, and discharge rate or profile. The latter is particularly important in wireless applications. For instance, the discharge profile of a GSM handset is a pulse of over 1 A in amplitude at approximately a 10% duty cycle. During standby mode the current is reduced to less than 10 mA.

To solve the challenges of precise capacity tracking and monitoring, Texas Instruments has developed a family of accurate battery monitor devices. These devices use the coulomb counting method in order to provide the user with accurate and reliable information about the battery's state of charge. The purpose of this report is to provide the basics of building an accurate gas-gauging feature using these devices.

Product Comparison

The following table provides a comparison between the available battery monitor ICs.

TABLE 1: FEATURE COMPARISON FOR THE BATTERY MONITORS

Feature	bq2018	bq2019	bq2023	bq26200	bq26220
Memory	115 bytes RAM	32 bytes RAM			
		96 bytes FLASH	224 bytes FLASH	96 bytes FLASH	224 bytes FLASH
		8 bytes ID ROM			
	13 hardware registers	19 hardware registers	15 hardware reg.	17 hardware reg.	19 hardware reg.
Memory backup (RBI)	Yes	No	Yes	No	Yes
Current Sense	Differential	Single-ended	Differential		
Chg/Dsg Count Rate	12.5µVH	3.05µVH			
Offset Calibration	Initiated by the host and takes one hour (1)	Initiated by host and takes up to 42.6 min. (1)	Continuous auto-calibration and compensation		
Offset Compensation	Offset results are stored in internal register, host makes compensation	**Option 1:** Host makes compensation **Option 2:** Automatic compensation	Continuous auto-calibration and compensation		
Temp. Resolution	10°C	1°C	0.25°C	1°C	1°C
Voltage Meas.	No				Yes
GPIO Pin	None	Open-drain status output			Input or open-drain output
Current Drain	60 µA	80 µA	32 µA	78 µA	30 µA
Package	8-lead SOIC or TSSOP	8-lead TSSOP			

(1) Can be initiated as the last step in final test and while pack is in transit

System Components

Measuring battery charge and discharge current and reporting state of charge to an end user requires several components (see Figure 1). These include:

- A battery monitor such as the bq2018, bq2019, or bq2023. Battery monitor ICs contain highly-accurate coulomb counters, temperature monitors, communication interfaces, and other functions.
- A current sense resistor: The low-value (typically between 10 to 20 mΩ) sense resistor provides a means for the battery monitor to measure the current flowing into or out of the battery. The battery monitor senses the voltage across this resistor.
- A host controller with one free general-purpose I/O for communication: The host controller is required to provide intelligence to the battery monitoring setup. The host controller handles all communication with the battery monitor IC. Since the HDQ and SDQ communication protocols are asynchronous one-wire based, a general-purpose I/O is dedicated to handle the communication flow. The host also performs calculations with data read from the battery monitor to determine the battery's state of charge.

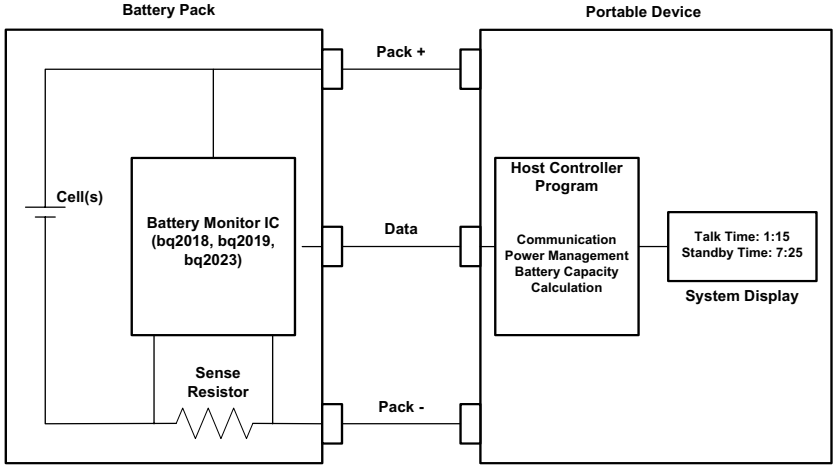

FIGURE 1: System Components

What Is Coulomb Counting?

Coulomb counting simply means measuring the charge input to and subsequently removed from the battery. In order to accomplish this, first the charge and discharge current is measured across a low-value series sense resistor between the negative terminal of the battery and the battery pack ground contact. The voltage drop across the sense resistor is then integrated over time to provide an accurate representation of the state of the charge of the battery.

Battery monitor devices from Texas Instruments use a highly accurate and low-offset voltage to frequency converter (VFC) to measure the voltage drop across the sense resistor. The output of the VFC is then converted to an accumulated count in either the charge or the discharge register to represent the charge flow into and out of the battery. See Figure 2.

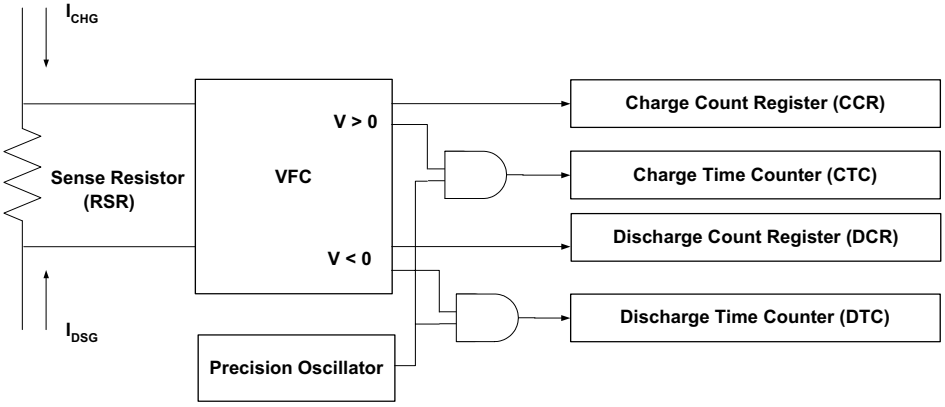

FIGURE 2: Simplified Block Diagram of the Coulomb Counter

The VFC is connected such that a positive voltage is developed across the sense resistor when current is flowing into the battery (i.e. charge). Conversely, a negative voltage is developed across the sense resistor, and thus the VFC inputs, when current is flowing out of the battery (i.e. discharging). Charge and discharge activities are accumulated in 2 independent registers: Charge Count Register (CCR) and the Discharge Count Register (DCR).

The VFC is designed to count at a fundamental rate. This rate, also known as the VFC gain (or simply G_{VFC} throughout this app note), provides a conversion factor from the output of the VFC to the input voltage. The data sheets for the battery monitors report the VFC gain as a Hz/V value. This simply means that a given input voltage produces a certain number of

counts in some period of time. For instance, the bq2018 has a typical VFC gain of 22.2 Hz/V while the bq2019 has a typical gain of 90.51 Hz/V. This means that if the bq2018 CCR incremented one count every second, the input voltage would be 45 mV (1 sec ÷ 22.2 Hz/V). An increase of CCR every second in the bq2019 would mean an input voltage of 11.05 mV (1 sec ÷ 91.1 Hz/V).

In addition to the charge/discharge count register, the battery monitors have two time registers, charge time counter (CTC) and discharge time counter (DTC). The CTC runs while the battery charges, and DTC runs while the battery discharges. Only one timer will always be running at a rate of 4096 counts per hour, provided the registers have not experienced a rollover.

Sense Resistor Selection

The sense resistor must be sized properly to measure the entire range of charge and discharge currents in the application within the limits of the battery monitor. The items to consider include:

1. The maximum potential of the SR input as specified in the IC's data sheet. This limit for the bq2019, for instance, is –100 mV to +100 mV. Therefore charge/discharge currents through the sense resistor must not produce a voltage greater than ±100 mV.

2. The VFC gain as specified in the IC's data sheet. The bq2018, for instance, counts charge and discharge at a rate of 12.5 μV per hour. Signals less than 12.5 μV require greater than one hour to resolve. The designer should consider the resolution vs. time when selecting a sense resistor.

3. The sense resistor must also handle the power dissipation of all charge and discharge activity.

Calculating Charge and Discharge Time

The host system can calculate the change in time by reading CTC/DTC at time zero, designated as CTC0/DTC0, and then reading them again some time later, designated as CTC1/DTC1. The change in time, in seconds:

$$\Delta t\ (s) = [(CTC1 - CTC0) + (DTC1 - DTC0)] * 3600/4096 \quad (1)$$

After Δt is calculated, the host system should store CTC1/DTC1 as CTC0/DTC0 for the next time period calculation.

The preceding discussion is meant to serve as a basis for the calculations to determine remaining capacity. The charge/discharge count registers, VFC gain, and the change in time

are three of the fundamental values necessary to calculate remaining capacity and time to empty.

Calculating Average Current

The host system does not communicate with the battery monitor on a continuous basis. The microcontroller spends most of its time controlling other system components. But when the battery monitor is accessed, one of the values the host microcontroller may calculate is average current during the last time period. This discussion assumes that the host has communicated with the battery monitor and either stored initial values or performed maintenance to clear the CCR/DCR and CTC/DTC registers. Either way, designate the initial readings as CCR0/DCR0 and CTC0/DTC0. The host should read the CCR/DCR and CTC/DTC registers, referenced in the equation below as CCR1/DCR1 and CTC1/DTC1. The average current during the last time period:

$$IAVG\ (A) = [(CCR1-CCR0) – (DCR1-DCR0)] / (\Delta t * G_{VFC} * RSR) \quad (2)$$

Δt (s) is calculated from equation (1) or calculated from the host controller's internal timer, G_{VFC} is the VFC gain (Hz/V), and RSR (Ω) is the sense resistor. A negative IAVG indicates discharge and a positive IAVG indicates charge.

This value can be used to calculate the time to empty at the discharge rate calculated.

Calculating Accumulated Current

Accumulated current is used to calculate the absolute remaining capacity of the battery. It requires knowledge of the capacity at some time. The battery design capacity is typically used when the battery goes through its first discharge from full. After that, a simple algorithm can be generated to learn the true battery capacity. The accumulated current during the last time period:

$$IACC\ (As) = IAVG * \Delta t$$
$$= [(CCR1-CCR0) – (DCR1-DCR0)] / (G_{VFC} * RSR) \quad (3)$$

After the calculation for IAVG or IACC is complete, the host system should store CCR1/DCR1 to CCR0/DCR0 for the next time period.

Calculating the Remaining Capacity

Remaining capacity is the entire goal of gas gauging. This value can be manipulated in a number of ways to display for the end user. It can be presented as a percentage of total capacity, which is either the design value, or the learned value, or used to calculate time to empty, which is detailed below. The remaining capacity calculation:

RM1 (As) = RM0 + IACC (4)

IACC (As) is calculated from equation (3), RM0 (As) is the last calculated remaining capacity.

After the calculation for remaining capacity, the host system should store RM1 to RM0 for the next time period.

Calculating the Time to Empty @ Rate

The basic assumption behind this calculation is that the user is interested in the time to empty at the average current consumption during some time period. This might require that IAVG, calculated in equation (2), be calculated at a longer time period than IACC. More accurate average current results in a more accurate time-to-empty calculation. The time-to-empty at IAVG rate calculation:

TTE@RATE (s) = RM1 / IAVG (5)

IAVG (A) is calculated from equation (2), RM1 (As) is the remaining capacity calculated in equation (4).

Other Battery Parameters

Other battery parameters include temperature and voltage. All TI battery monitors measure and report the die temperature to the host controller. Refer to Table 1 for a feature comparison.

Most host controllers monitor the battery voltage through an ADC channel. By measuring the battery voltage, the host controller can signal the end user when the battery has reached its end of discharge voltage. This voltage, which varies from design to design and by cell type, is the absolute minimum at which the battery should be operated to maintain cell life.

Summary

This application report provides an overview of the components necessary for gas-gauging a battery with the TI battery monitors. A very simple system and understanding of some basic equations allow a basic gas-gauging application to be built.

This application report does not cover some other steps needed to create a more sophisticated gas-gauging algorithm. These topics include capacity-learn cycles, charge-efficiency correction, self-discharge correction, VFC gain error over temperature and voltage, VFC offset, and device-temperature reporting. Proper handling of these topics results in a remaining capacity calculation that is extremely accurate across a system's temperature and voltage range. These topics are covered in other application reports.

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Reverse Current/Battery Protection Circuits

Jeff Falin *PMP Portable Power*

ABSTRACT

Users of battery powered equipment expect safeguards to prevent damage to the internal electronics in the event of reverse battery installation, accidental short circuiting, or other inappropriate operation. These safeguards can be either mechanical or electronic. An example of a mechanical safeguard is requiring the use of special connectors and instructional pictures and symbols. For example, a 9-V battery has different terminals, and its rechargeable battery packs are physically designed for one direction of insertion. Other battery types, like single-cell alkaline, are not so easily protected by mechanical safeguards. Therefore, battery powered equipment designers and manufacturers must ensure that any reverse current flow and reverse bias voltage is low enough to prevent damage to either the battery itself or the equipment's internal electronics. To provide these electronic safeguards, manufacturers typically chose either a diode or transistor for reverse battery protection.

Using a Diode

The simplest protection against reverse battery protection is a diode in series with the battery, as seen in Figure 1.

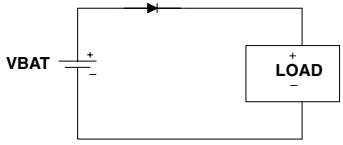

Figure 1. Diode in Series With Battery

In Figure 1, the diode becomes forward biased and the load's normal operating current flows through the diode. When the battery is installed backwards, the diode reverse–biases and no current flows. This approach is used for any battery type, from single-cell alkaline to multiple Li-Ion, but it has two major disadvantages. The forward voltage drop across the diode shortens the usable battery life, i.e., a dual alkaline battery pack capable of providing 1.8 V, is limited to 1.8 V – 0.6 V = 1.2 V. In addition, the efficiency of the power circuitry (e.g., a boost converter) following the battery suffers due to this drop. To minimize these disadvantages, many designers use a Schottky diode, since its forward drop is lower than that of a regular diode. However, the disadvantage of using a Schottky diode is that it is more expensive than a standard diode.

Using a FET

The most recent MOSFETs are very low on resistances, and therefore, are ideal for providing reverse current protection with minimal loss. Figure 2 shows a low-side NMOS FET in the ground return path and Figure 3 shows a high-side PMOS FET in the power path.

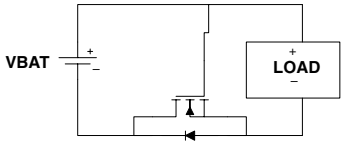

Figure 2. NMOS FET in the Ground Return Path

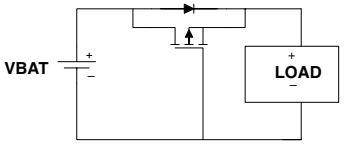

Figure 3. PMOS FET in the Power Path

In each circuit, the FET's body diode is oriented in the direction of normal current flow. When the battery is installed incorrectly, the NMOS (PMOS) FET's gate voltage is low (high), preventing it from turning on.

When the battery is installed properly and the portable equipment is powered, the NMOS (PMOS) FET's gate voltage is taken high (low) and its channel shorts out the diode

A voltage drop of $r_{DS(on)} \times I_{LOAD}$ is seen in the ground return path when using the NMOS FET and in the power path when using the PMOS FET. In the past, the primary disadvantage of these circuits has been the high cost of low $r_{DS(on)}$, low-threshold voltage FETs. However, advances in semiconductor processing have resulted in FETs that provide minimal drops in small packages. Some of the latest FET's threshold voltages and $r_{DS(on)}$'s are shown in Table 1.

Table 1. Small Packaged FETs With Low $r_{ds(on)}$

MANUFACTURER	PART NO	PACKAGE	$r_{DS(on)}$
NMOS			
IRF	ILRML2502	SOT–23	80 mΩ at 2.7 V
Vishay	Si2312	SOT–23	51 mΩ at 1.8 V
PMOS			
IRF	ILRML6401	SOT–23	85 mΩ at 2.7 V
Vishay	Si2323	SOT–23	68 mΩ at 1.8 V

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SOLDER PAD RECOMMENDATIONS FOR SURFACE-MOUNT DEVICES

By Wm. P. Klein, P.E.

Cost and performance requirements continue to push the packaging of electronic systems into smaller and smaller spaces. At one time, the standard center-to-center pin spacing was 100 mils (0.1") on through-hole parts (DIPs). The advent of surface-mount devices (SMD) has brought pin spacings that differ from one package series to the next. The solder joint of pin-foot to printed circuit board (PCB) must provide the strength to hold the device in place. The close lead spacings make lead-to-lead solder bridges more prevalent. These factors increase the importance of an optimized PCB design.

The criteria for a well-designed solder joint is based on both empirical data and reliability testing. Solder-joint strength is directly related to the total solder volume. An observable solder fillet is evidence of proper wetting. Therefore, a positive solder fillet is usually specified. A joint can be described by the solder fillets formed between the device pins and the PCB pads. Figure 1 shows the three fillets: toe, heel, and side.

A properly designed solder pad minimizes solder bridging while affording a strong and easily inspected joint. These goals have conflicting dimensional requirements.

Factors to consider when determining the dimensions of the solder pads include part dimension tolerances, PCB production tolerances, and accuracy-of-placement tolerances. Figure 2 shows how placement accuracy can affect solder bridge formation. The designer should also consider the limitations of the soldering process. Boards designed for wave soldering usually have slightly wider pads than those designed for reflow techniques.

Two trade organizations provide industry standards. The Electronic Industries Association (EIA)[1] represents manufacturers in all areas of the electronics industry. The EIA's Joint Electron Device Engineering Council (JEDEC)[2] establishes standard package dimensions. The Institute for Interconnecting and Packaging Electronic Circuits (IPC)[3] has established standards for PCB design. The Surface Mount Land Pattern Subcommittee of the Printed Board Design Committee of IPC has developed standard pad dimensions for the packages defined by the JEDEC committee. The IPC document Surface-Mount Design and Land Pattern Standard is designated IPC-SM-782.

To further assist the designer, the mathematical relationships in the standard have been programmed in a spreadsheet calculator. Access to this program is available at the IPC

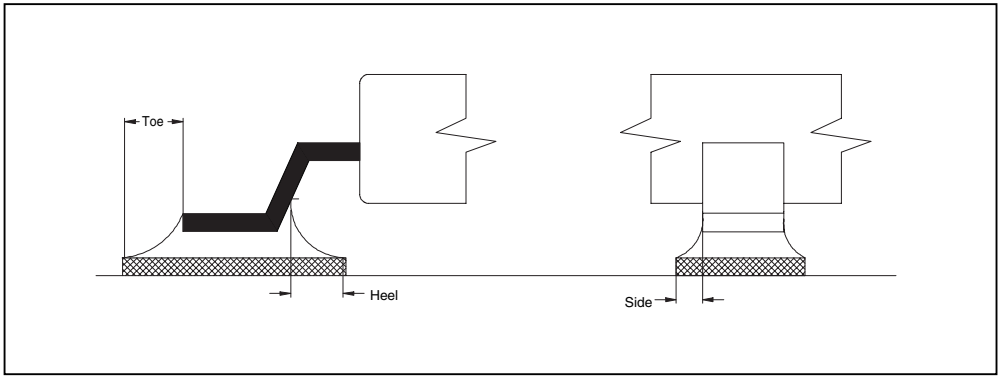

FIGURE 1. Solder Joint Fillets.

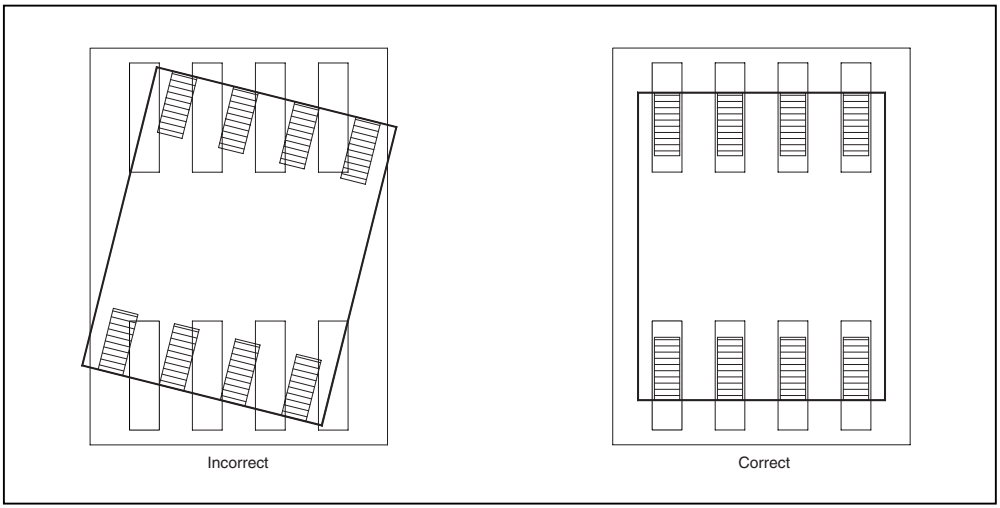

FIGURE 2. Device Placements.

internet web site[3]. Surface-mount land patterns are given for many JEDEC standard packages. Capability to customize the patterns for special designs is also provided. The results of this program are tabulated in the appendices of this paper for some of the more popular packages currently supplied by Texas Instruments.

The values listed in the following tables are based on the assumptions shown in Table I. Performance will also depend on process variables. While an effort has been made to select nominal values for these variables, the design engineer should determine the optimum value through experimentation.

Fabrication Tolerance	0.1mm
Placement Tolerance	0.1mm
Toe Joint Minimum	0.4mm
Heel Joint Minimum	0.5mm
Side Joint Minimum	0.0mm

TABLE I. Assumed Basic Dimensions.

NOTES: (1) Electronic Industries Association (EIA)
2500 Wilson Boulevard
Arlington, VA 22201
http://www.eia.org/

(2) Joint Electron Device Engineering Council (JEDEC)
http://www.jedec.org

(3) The Institute for Interconnecting and Packaging Electronic Circuits (IPC)
2215 Sanders Road
Northbrook, IL 60062-6135
Phone: 847-509-9700 Fax: 847-509-9798
http://www.ipc.org/index.html

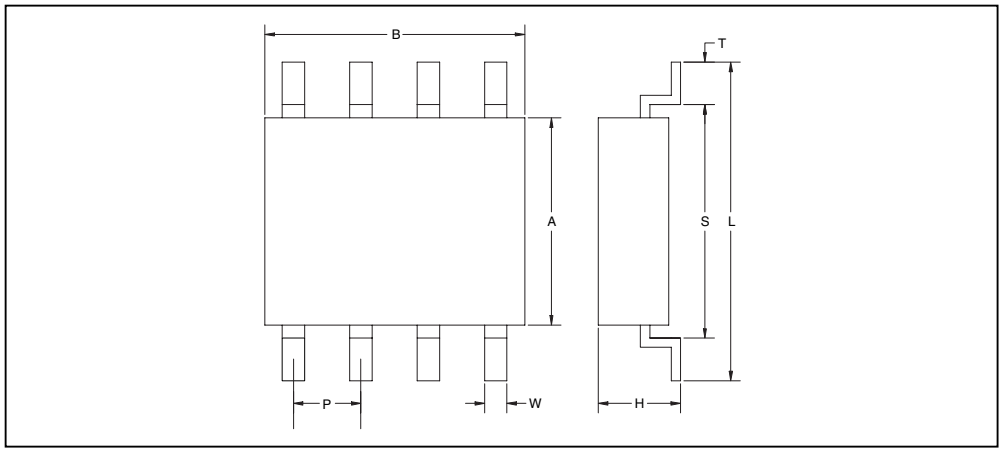

FIGURE 3. Package Dimensions.

PACKAGE	PKG #	L MIN	L MAX	W MIN	W MAX	T MIN	T MAX	A MIN	A MAX	B MIN	B MAX	H MIN	H MAX	P NOM	LEAD COUNT
SO-8	182	0.228	0.244	0.013	0.020	0.016	0.050	0.150	0.157	0.189	0.196	0.053	0.069	0.0500	8
SO-14	235	0.228	0.244	0.013	0.020	0.016	0.050	0.150	0.157	0.337	0.344	0.053	0.069	0.0500	14
SO-16	265	0.228	0.244	0.013	0.020	0.016	0.050	0.150	0.157	0.386	0.394	0.053	0.069	0.0500	16
SO-16W	211	0.394	0.419	0.013	0.020	0.016	0.050	0.291	0.299	0.398	0.413	0.093	0.104	0.0500	16
SO-18	219	0.394	0.419	0.013	0.020	0.016	0.050	0.291	0.299	0.447	0.463	0.093	0.104	0.0500	18
SO-20	221	0.394	0.419	0.013	0.020	0.016	0.050	0.291	0.299	0.496	0.512	0.093	0.104	0.0500	20
SO-24	239	0.394	0.419	0.013	0.020	0.016	0.050	0.291	0.299	0.598	0.614	0.093	0.104	0.0500	24
SO-28	217	0.398	0.419	0.013	0.020	0.020	0.040	0.291	0.299	0.697	0.713	0.093	0.104	0.0500	28
SOT-23-5	331	0.102	0.118	0.010	0.020	0.014	0.022	0.059	0.069	0.110	0.118	0.035	0.057	0.0374	5
SOT-23-6	332	0.102	0.118	0.010	0.020	0.014	0.022	0.059	0.069	0.110	0.118	0.035	0.057	0.0374	6
SOT-23-8	348	0.102	0.118	0.011	0.018	0.004	0.024	0.059	0.069	0.110	0.118	0.035	0.057	0.0256	8
MSOP-8	337	0.189	0.197	0.011	0.015	0.018	0.026	0.114	0.122	0.114	0.122	0.032	0.048	0.0256	8
SSOP-20	334	0.291	0.323	0.009	0.015	0.022	0.037	0.197	0.220	0.272	0.295	0.077	0.079	0.0256	20
SSOP-24	338	0.291	0.323	0.009	0.015	0.022	0.037	0.197	0.220	0.311	0.335	0.077	0.079	0.0256	24
SSOP-28	324	0.291	0.323	0.009	0.015	0.022	0.037	0.197	0.220	0.390	0.413	0.077	0.079	0.0256	28
SSOP-16	322	0.228	0.244	0.008	0.012	0.016	0.050	0.149	0.157	0.188	0.197	0.053	0.069	0.0250	16
SSOP-48	333	0.395	0.420	0.008	0.013	0.020	0.040	0.291	0.299	0.613	0.630	0.053	0.069	0.0250	48
SSOP-56	346	0.395	0.420	0.008	0.013	0.020	0.040	0.291	0.299	0.720	0.730	0.095	0.110	0.0250	56

TABLE II . Package Dimensions—Inches.

PACKAGE	PKG #	L MIN	L MAX	W MIN	W MAX	T MIN	T MAX	A MIN	A MAX	B MIN	B MAX	H MIN	H MAX	P NOM	LEAD COUNT
SO-8	182	5.79	6.20	0.33	0.51	0.41	1.27	3.81	3.99	4.80	4.98	1.35	1.75	1.270	8
SO-14	235	5.79	6.20	0.33	0.51	0.41	1.27	3.81	3.99	8.56	8.74	1.35	1.75	1.270	14
SO-16	265	5.79	6.20	0.33	0.51	0.41	1.27	3.81	3.99	9.80	10.01	1.35	1.75	1.270	16
SO-16W	211	10.01	10.64	0.33	0.51	0.41	1.27	7.39	7.59	10.11	10.49	2.36	2.64	1.270	16
SO-18	219	10.01	10.64	0.33	0.51	0.41	1.27	7.39	7.59	11.35	11.76	2.36	2.64	1.270	18
SO-20	221	10.01	10.64	0.33	0.51	0.41	1.27	7.39	7.59	12.60	13.00	2.36	2.64	1.270	20
SO-24	239	10.01	10.64	0.33	0.51	0.41	1.27	7.39	7.59	15.19	15.60	2.36	2.64	1.270	24
SO-28	217	10.11	10.64	0.33	0.51	0.51	1.02	7.39	7.59	17.70	18.11	2.36	2.64	1.270	28
SOT-23-5	331	2.59	3.00	0.25	0.51	0.36	0.56	1.50	1.75	2.79	3.00	0.89	1.45	0.950	5
SOT-23-6	332	2.59	3.00	0.25	0.51	0.36	0.56	1.50	1.75	2.79	3.00	0.89	1.45	0.950	6
SOT-23-8	348	2.60	3.00	0.28	0.46	0.10	0.61	1.50	1.75	2.80	3.00	0.90	1.45	0.650	8
MSOP-8	337	4.80	5.00	0.28	0.38	0.46	0.66	2.90	3.10	2.90	3.10	0.81	1.22	0.650	8
SSOP-20	334	7.39	8.20	0.23	0.38	0.56	0.94	5.00	5.59	6.91	7.49	1.96	2.01	0.650	20
SSOP-24	338	7.39	8.20	0.23	0.38	0.56	0.94	5.00	5.59	7.90	8.51	1.96	2.01	0.650	24
SSOP-28	324	7.39	8.20	0.23	0.38	0.56	0.94	5.00	5.59	9.91	10.49	1.96	2.01	0.650	28
SSOP-16	322	5.79	6.20	0.20	0.30	0.41	1.27	3.78	3.99	4.78	5.00	1.35	1.75	0.635	16
SSOP-48	333	10.03	10.67	0.20	0.33	0.51	1.02	7.39	7.59	15.57	16.00	1.35	1.75	0.635	48
SSOP-56	346	10.03	10.67	0.20	0.33	0.51	1.02	7.39	7.59	18.29	18.54	2.41	2.79	0.635	56

TABLE III. Package Dimensions—Millimeters.

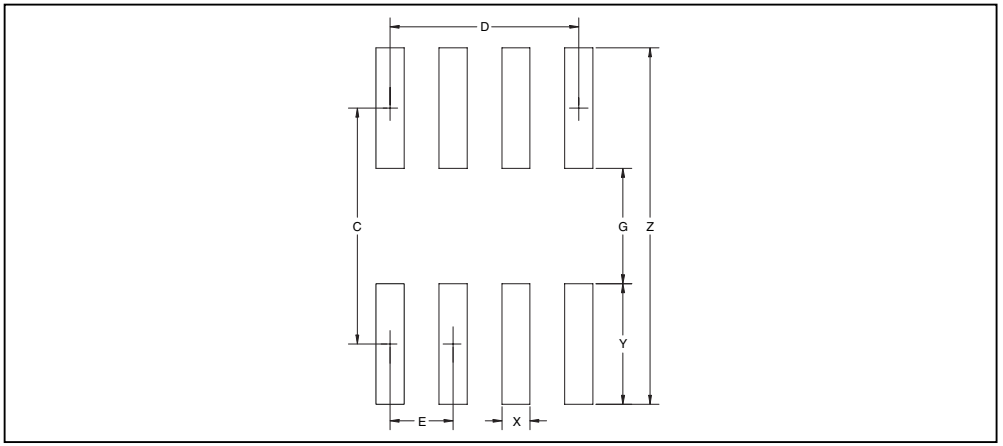

FIGURE 4. Pad Dimensions.

PACKAGE	PKG #	Z MIN	Z MAX	G MIN	G MAX	X MIN	X MAX	Y REF	C/C REF	D REF	E NOM
SO-8	182	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.150	0.0500
SO-14	235	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.300	0.0500
SO-16	265	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.350	0.0500
SO-16W	211	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.350	0.0500
SO-18W	219	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.400	0.0500
SO-20W	221	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.450	0.0500
SO-24W	239	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.550	0.0500
SO-28W	217	0.448	0.451	0.278	0.282	0.018	0.022	0.099	0.365	0.650	0.0500
SOT-23-5	331	0.147	0.151	0.034	0.038	0.017	0.021	0.058	0.093	0.075	0.0374
SOT-23-6	332	0.147	0.151	0.034	0.038	0.017	0.021	0.058	0.093	0.075	0.0374
SOT-23-8	348	0.147	0.151	0.015	0.019	0.016	0.020	0.068	0.083	0.077	0.0256
MSOP-8	337	0.226	0.230	0.097	0.101	0.014	0.018	0.066	0.164	0.077	0.0256
SSOP-20	334	0.351	0.355	0.177	0.181	0.013	0.017	0.089	0.266	0.230	0.0256
SSOP-24	338	0.351	0.355	0.177	0.181	0.013	0.017	0.089	0.266	0.281	0.0256
SSOP-28	324	0.351	0.355	0.177	0.181	0.013	0.017	0.089	0.266	0.333	0.0256
SSOP-16	322	0.273	0.277	0.089	0.093	0.011	0.015	0.094	0.183	0.175	0.0250
SSOP-48	333	0.448	0.452	0.275	0.279	0.012	0.016	0.089	0.364	0.575	0.0250
SSOP-56	346	0.448	0.452	0.275	0.279	0.012	0.016	0.089	0.364	0.675	0.0250

TABLE IV. Pad Dimensions—Inches.

PACKAGE	PKG #	Z MIN	Z MAX	G MIN	G MAX	X MIN	X MAX	Y REF	C/C REF	D REF	E NOM
SO-8	182	6.934	7.036	2.261	2.362	0.457	0.559	2.388	4.648	3.810	1.270
SO-14	235	6.934	7.036	2.261	2.362	0.457	0.559	2.388	4.648	7.620	1.270
SO-16	265	6.934	7.036	2.261	2.362	0.457	0.559	2.388	4.648	8.890	1.270
SO-16W	211	11.354	11.455	6.452	6.553	0.457	0.559	2.515	8.966	8.890	1.270
SO-18W	219	11.354	11.455	6.452	6.553	0.457	0.559	2.515	8.966	10.160	1.270
SO-20W	221	11.354	11.455	6.452	6.553	0.457	0.559	2.515	8.966	11.430	1.270
SO-24W	239	11.354	11.455	6.452	6.553	0.457	0.559	2.515	8.966	13.970	1.270
SO-28W	217	11.379	11.468	7.061	7.163	0.457	0.559	2.515	9.271	16.510	1.270
SOT-23-5	331	3.734	3.835	0.864	0.965	0.432	0.533	1.473	2.362	1.905	0.950
SOT-23-6	332	3.734	3.835	0.864	0.965	0.432	0.533	1.473	2.362	1.905	0.950
SOT-23-8	348	3.734	3.835	0.381	0.483	0.406	0.508	1.727	2.108	1.950	0.650
MSOP-8	337	5.740	5.842	2.464	2.565	0.356	0.457	1.676	4.166	1.950	0.650
SSOP-20	334	8.915	9.017	4.496	4.597	0.330	0.432	2.261	6.756	5.842	0.650
SSOP-24	338	8.915	9.017	4.496	4.597	0.330	0.432	2.261	6.756	7.137	0.650
SSOP-28	324	8.915	9.017	4.496	4.597	0.330	0.432	2.261	6.756	8.458	0.650
SSOP-16	322	6.934	7.036	2.261	2.362	0.279	0.373	2.388	4.648	4.445	0.635
SSOP-48	333	11.379	11.481	6.985	7.087	0.305	0.406	2.261	9.246	14.605	0.635
SSOP-56	346	11.379	11.481	6.985	7.087	0.305	0.406	2.261	9.246	17.145	0.635

TABLE V . Pad Dimensions—Millimeters.

SOT223

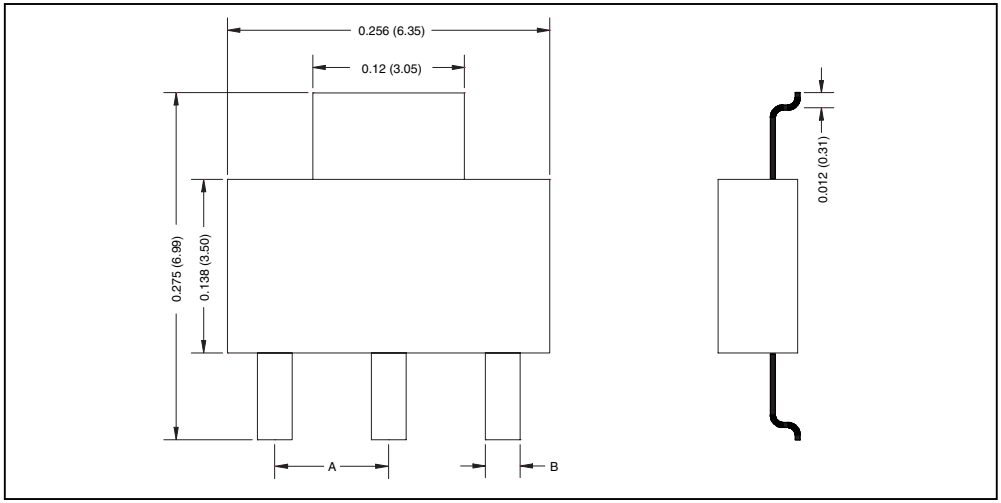

FIGURE 5. SOT223 Package Dimensions—Inches (mm).

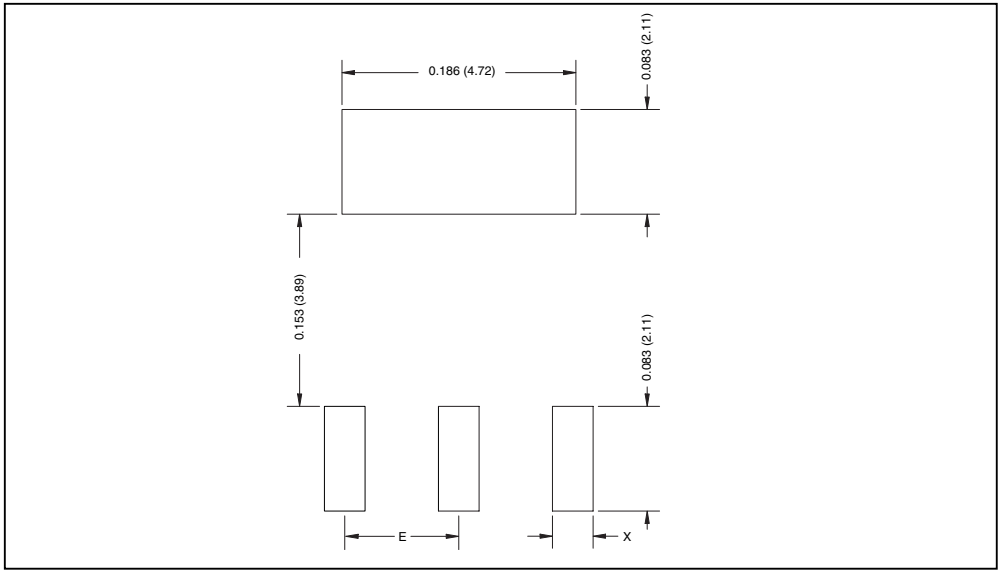

FIGURE 6. PCB Pad Dimensions for SOT223—Inches (mm).

# OF LEADS	PKG DESIGNATOR	A AND E FIGURES 5 AND 6	B FIGURE 5	X FIGURE 6
3	DCY	0.0905 (2.30)	0.03 (0.76)	0.032 (0.81)
5	DCQ	0.05 (1.27)	0.017 (0.43)	0.020 (0.51)

TABLE VI. Dimensions for SOT-223—Inches (mm).

NOTE: Pad sizes are the minimum recommended and may be increased for improved heat dissipation.

DDPAK DEVICES

The three DDPAK surface-mount power package types all have the same body dimensions. They differ only in the number of leads and their associated lead dimensions. These values are given in Table VIII.

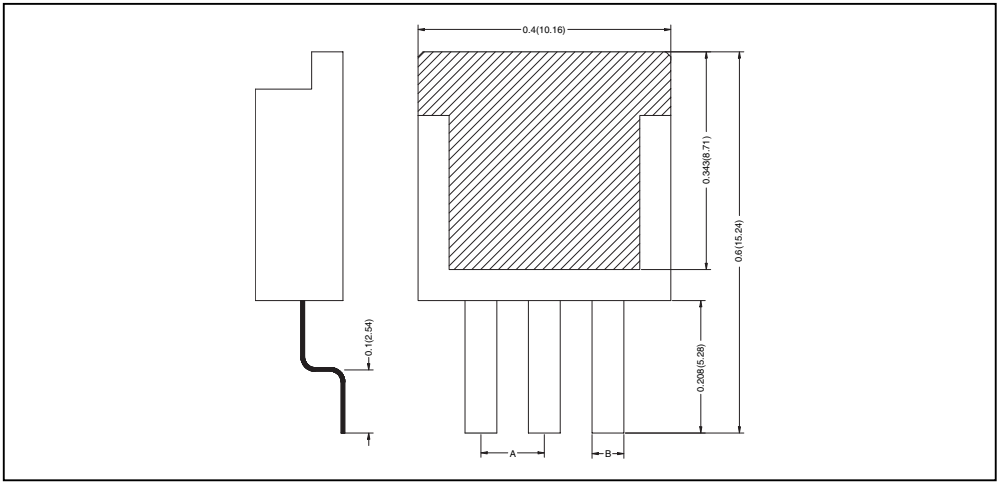

FIGURE 7. DDPAK Package Dimensions—Inches (mm).

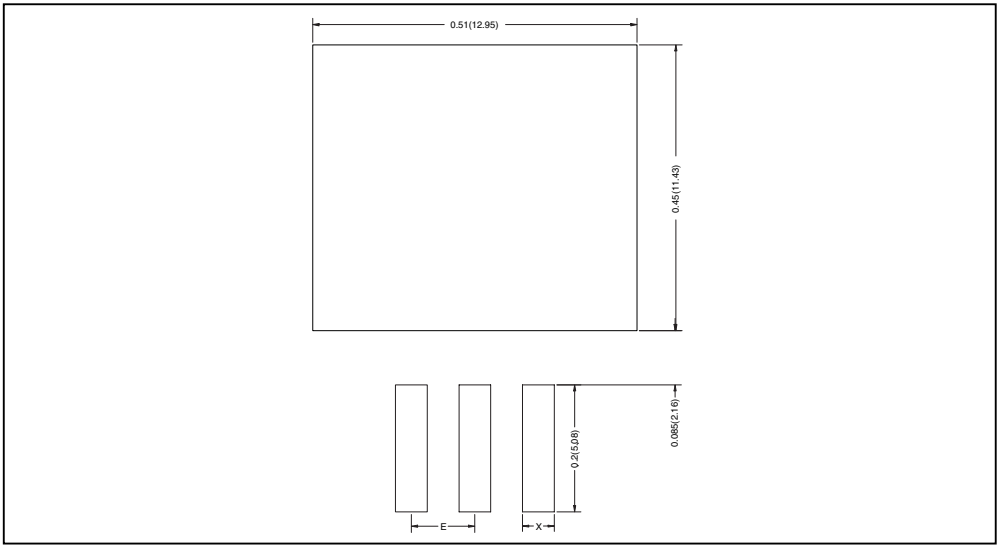

FIGURE 8. PCB Pad Dimensions for DDPAK—inches (mm).

# OF LEADS	PKG DESIGNATOR	A AND E FIGURES 5 AND 6	B FIGURE 5	X FIGURE 6
3	KTT	0.10 (2.54)	0.05 (1.27)	0.055 (1.35)
5	KTT	0.067 (1.70)	0.032 (0.81)	0.038 (0.97)
7	KTT	0.05 (1.27)	0.028 (0.71)	0.035 (0.89)

TABLE VII. Dimensions for DDPAK—Inches (mm).

NOTE: Pad sizes are the minimum recommended and may be increased for improved heat dissipation.

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Thermal Design of a Notebook Li-Ion Battery

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Abstract:

Demand for high power and small size portable electronic products is growing daily. In particular, notebook computer applications have become more popular than anyone could have imagined a decade ago. Today, notebook computers comprise about 54 percent of retail computer sales because they can offer 1.2-2.0 GHz CPU's, CD/DVD players, high resolution LCDs, hundreds of megabits of memory, and remote information sensing. However, the compilation of so much functionality and the associated electronics and electrical energy requirements has created new challenges in managing potential thermal issues in this product. One fundamental issue is that circuit components are less than 100 percent efficient, and therefore considerable heat is generated while a notebook computer operates under power hungry applications such as playing movies or simulating electrical/thermal design of products. Another drawback is that rechargeable batteries used for powering notebooks self-heat while charging/discharging because of their inherent electrical, thermodynamic and electrochemical impedances.

This article covers basics of predicting thermal performance of a notebook battery during operation at 42°C ambient using a combination of thermal analysis and modeling.

Introduction

Battery-Pack: Rechargeable Li-ion cells have become the power source of choice for most portable electronic products because of their high energy densities, long cycle-lives, and practical range of operating voltages (2.8-4.2 V). Today's cylindrical 18650 Li-ion cells provide more than 500 Wh/L of energy. However, a limitation of Li-ion cells arises from their self-heating under moderate/high levels of discharging current (>C-rate), or exposure to elevated temperatures. Temperatures above 60°C degrade cycling performance of Li-ion batteries by permanently reducing their cells capacities. However, existing notebook computers may require at least one hour of 50 to 70-W discharge power at temperatures above 50°C. In the case of most Li-ion notebook batteries, combinations of such power/temperature cause the Li-ion cell temperatures to rise above 60°C. This issue becomes even more critical when using faster processors, such as a Pentium-IV™, which dissipates twice the power (27-31.0 W) of the Pentium-III™ (15-16 W). Therefore, the main challenges in thermal management of Li-ion batteries are the incorporation of electrical/thermal control parameters that allow maximum power delivery with controlled levels of heat generation and dissipation. These may include:

1. Selection of Li-ion cells of low operating impedance. Cell impedance plays a critical role in increasing the temperature of a Li-ion battery, especially during discharge. A typical 2.2-Ah 18650 Li-ion cell generates five to six times more heat during discharge than charge, under application of 2.2-A current. Figure 1A and 1B show heat generation profiles of Li-ion cells from 4 different manufactures. Note that the heat generation among these cells is different, especially at high discharge power (10 W). Another important design issue is that the temperature rise and capacity of Li-ion cells depends on the types and manufacturer, the discharge rate, and the ambient temperature (see Figures 2 and 4 for details).
2. Selection of charge/discharge control electronics with thermal breakdown limits 20-30°C higher than their maximum operating temperature.
3. Printed circuit board (PCB) capable of removing sufficient amount of heat from thermally sensitive and hot electronics such as charge/discharge control FETs and sense resistors.

4. Charge/discharge currents appropriate to the thermal stability limits of both Li-ion cells and electronics, as well as the heat dissipation capability of the battery housing and covers.
5. Utilization of low cost battery housing materials that meet design's thermal/mechanical property requirements (thermal conduction, softening/melting point and impact resistance). Thermal conductivity of most plastics (e.g. cycoloy and Laxen) used for battery housings range between 0.3 to 0.40 W/m.K. These conductivity values are less than optimum for keeping battery internal temperature to a minimum. However, plastic-housing materials of higher thermal conductivity than 0.4 W/m.K are costly and also typically does not offer sufficient mechanical strength.
6. Safety protection against abnormal operating conditions such as over/under charge voltages, high charge/discharge currents and temperatures, and components' failure mechanisms such as the ability to open an over-voltage fuse in the event of loss of battery charge control.

Li-Ion Cells: Manufacturing Li-ion cells with optimized cooling capability is more challenging than battery packs because of the opposing nature of increasing cell energy density versus design parameters needed to improve cooling. A Li-ion cell consists of a carbon-based material coated on copper foil (anode); a porous polymer membrane (separator); and lithium metal oxide ($LiMO_2$, M=Co, Ni, or Mn) based material coated on aluminum foil (cathode). A mixture of lithium salt and inorganic solvents provides a medium for lithium ions to shuttle between cathode and anode. Aluminum and copper foils are the main means of transferring heat from the cell interior to the outside surface of the cell can. Cell's can thickness or thermal mass plays a critical role in balancing the heat generation and dissipation from the cell.

To achieve Li-ion cells' high capacities, some progress has been made in producing active cathode and anode materials of higher energy density. This has been achieved mainly though stabilization, structural, and surface morphology of cathode and anode materials, as well as selection of electrolytes with correct combinations of organic solvents and lithium salts. Today's $LiCoO_2$ cells provide capacity values near their theoretical limit (137 mAh/g); and most carbons have less than 6 percent irreversible capacity loss. This increase in capacity, however, could not match the electronics market demand for high energy density batteries. To meet this market demand, manufacturers are forced to increase the amount of cell active materials at the expense of using thinner current collectors, cell-can and separator; and denser cathode and anode coatings. However, large efforts underway to develop and produce cathodes [mixed oxides: $Li(Ni:Co:Mn)O_2$] with capacity values about one-and-half times that of $LiCoO_2$; and anode (metal alloys, Si:Sn) materials with capacity values two times that of graphite (370 mAh/g).

Battery Pack Thermal Modeling

Modeling has been used to predict the thermal behavior of Li-ion cells over a wide range of operating conditions. However, very little simulation has been done on the thermal management of batteries for portable electronics, especially where strings of Li-ion cells are compiled in plastic enclosures. Design of reliable Li-ion batteries is complex and very much depends on the product application, type of cell, and the electronics used. Generally, multiple levels of controls are used to protect notebook batteries against overcharge, over/under currents, electrical hard/soft short circuits, and abnormal temperature rise. Some batteries utilize architectures where the battery has integrated control ICs capable of leveling cells' voltages during charge and to track temperature rise during discharge.

This article covers the basics of modeling thermal response of the electronics and Li-ion cells used to develop a notebook computer battery. The battery consisted of eight 2.2-Ah 18650 cells, and modeled for operation (charge to 16.8 V at 2.2 A and discharge at 55-W of constant power until pack voltage dropped to 12 V) at 42°C ambient. Experimental data in support of the modeling results are also included.

Li-Ion Cells: During discharge, Li-ion cells convert electrochemical energy to electrical energy, and the reverse takes place during charge. Li-ion cells self heat during operation because

of their associated impedance due to IR-drop, polarization, and thermodynamic effects. Total heat generation of a Li-ion cell can be expressed as:

$$\dot{Q} = I\,(V_{ocv} - V_{op}) - I\left(T\frac{dV}{dT}\right)$$

Here, the I is cell operation current (A); V_{ocv} and V_{op} are open circuit and operation voltages (V); T, is ambient temperature (K); and dV, is cell voltage variation versus cell temperature rise. The term $I\,(V_{ocv} - V_{op})$, is "irreversible" heat; and I (TdV/dT) term is considered as "reversible" heat since it becomes exothermic during discharge and endothermic during charge. The irreversible heat is measured using a current interruption method and the reversible heat using a calorimetric method [1]. Note the modeling approach here is based on measuring real time heat profile of cells, not theoretical calculations. This provides more accurate results on predicting the thermal response of a battery pack for given operating conditions. The heat generation profile of a single Li-ion cell is nearly the same regardless of its assembly configuration [2]. Therefore, the measured heat generation profile from one cell can be assigned to any cell in the battery pack. Such an approach allows building thermal models of battery packs with multiple cells simply by measuring the heat generation profile of a single cell rather than building a battery pack first and then measuring its total heat generation. This reduces thermal modeling and design cycle-time for battery packs, without compromising accuracy.

Electronic Components: Detailed modeling is often necessary for thermal simulation of electronic components such as power ICs. However, it is not practical to model battery products, including all electronic components, to the degree of detail used in single-device simulation. Detailed information on simplification of modeling of electronics components is provided elsewhere [3,4]. Here, the capacitors and inductors were treated as a lumped system. Methods of calculating effective density (ρ), heat capacity *(Cp),* and thermal conductivity *(K)* values for lumped electronic parts are covered elsewhere [2,6]. Critical components (PCB, FETs, diodes and temperature sensors) were modeled in detail. The soldering material (Pb 39.2%; Sn 60.8%) thickness was 60 µm.

Table 1 lists the power dissipation values for the battery pack's components during discharge and charge. The values were calculated based on the currents providing 55 W constant power during discharge, and current needed to charge the battery pack to its full level in ~2 hours. The real-time electronics and Li-ion cells power dissipation were used to simulate the battery pack thermal response including for the condition noted above.

Printed Circuit Board (PCB): PCBs are made of multiple layers of thin copper foils and a dielectric material (FR4) with many thermal and electrical vias. Because of the copper-layers, PCBs have a significantly higher thermal conductivity along the in-plane direction than in the cross-plane. Therefore, an orthotropic thermal conductivity was applied in order to account for the differences in PCBs' characteristics (geometry, thickness, and number as well as percentages of copper layer coverage) for the in-plane versus cross-plane direction.

Results:

Table 1 provides the maximum temperature rise values (measured vs. simulated) for the cells and the critical electronic components in the battery at the end of a discharge and charge step. The overall results show that the battery pack's interior temperature during discharge is dominated by the heat dissipation from the cells; and during charge, by the power dissipation from the control electronics. Other critical issues identified were that the cells temperature increased above 60°C, and the non-uniformity in temperature distribution developed. Localized temperature of the cell closest to electronics reached 70°C. Figure 4 shows thermal profile of the battery at the end of discharge.

Conclusion:

This article demonstrates the effectiveness of thermal modeling and the accuracy of the methodology selected in the thermal management of a notebook computer battery pack. The use of thermal modeling facilitated selection of thermally efficient electronic components and circuit board design for the required charge/discharge power and operating temperature limits. These benefits reduced cycle-time for overall product development and increased the product reliability and quality. In addition, this exercise indicated the presence of a non-uniform temperature distribution inside the battery pack that can lead to variation in the capacity loss of the Li-ion cells and ultimately reduce the battery pack's cycle-life and reliability. Motorola Energy Systems Group is continuing to improve thermal modeling to drive better performing batteries for notebook computes and other applications.

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Table 1. Heat generation and temperature rise of the electronic components and cells in battery-pack during discharge and charge

Electronic Components	Components Heat Generation (W)		Temperature Rise (°C) End of the Discharge (12.0 V)		End of Charge (16.8 V)	
	Discharge	Charge	Expr.	Model	Expr.	Model
Capacitor	0.0	0.0829	66	64-66	65	58-61
Cells	Based on profile	Based on profile	60	62-70	52	45-51
Charge Control IC	0.0042	0.5	66	64-67	71	58-67
Diode-B, D2	off	0.0	65	65-68	67	60-61
Diode-F, D1	0.0	0.0451	65	65-66	66	58-61
Fuel Gauge	0.000825	0.000825	63	64-66	62	59
Charge FET	0.00475	0.4639	65	66-68	72	65-69
Discharge FET	0.1447	0.0501	71	66-67	66	59-62
Bypass Discharge FET	0.1102	0.0	66	66-67	66	60-61
Sense Resistor	0.3216	0.1113	87	76-83	64	58-61
Inductor	0.009	0.4103	66	64-68	68	60-63

Figure-1: Heat generation profiles of 2.2-Ah 18650 Li-ion cells from four different manufacturers discharged at 7.5 W and 40-41ºC ambient. Note variation in heat generation among the cells, especially at higher discharge power.

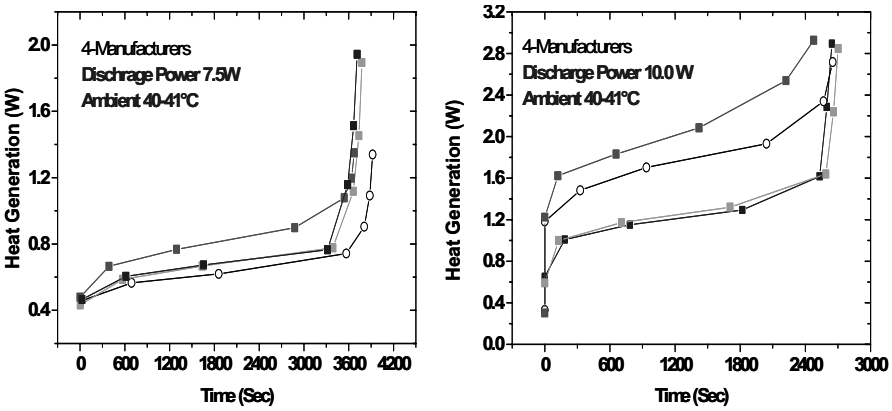


Figure-2: Temperature rise of a 2.2-Ah 18650 Li-ion cell discharged at 6.25-10W and at 27 and 65ºC ambient.

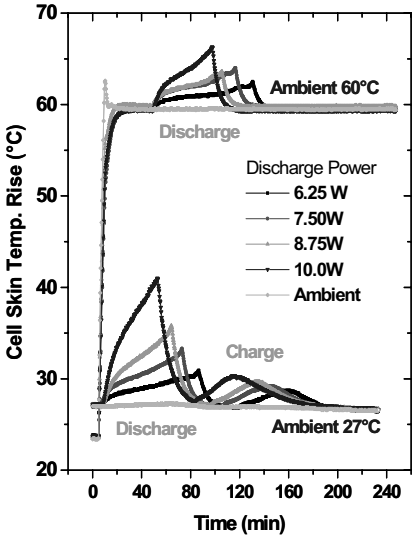


Figure-3: Discharge capacity values of 2.2-Ah 18650 Li-ion cells from three different manufacturers discharged at various power and ambient temperatures.

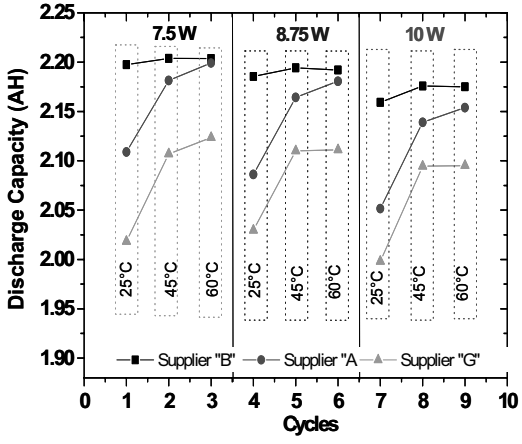
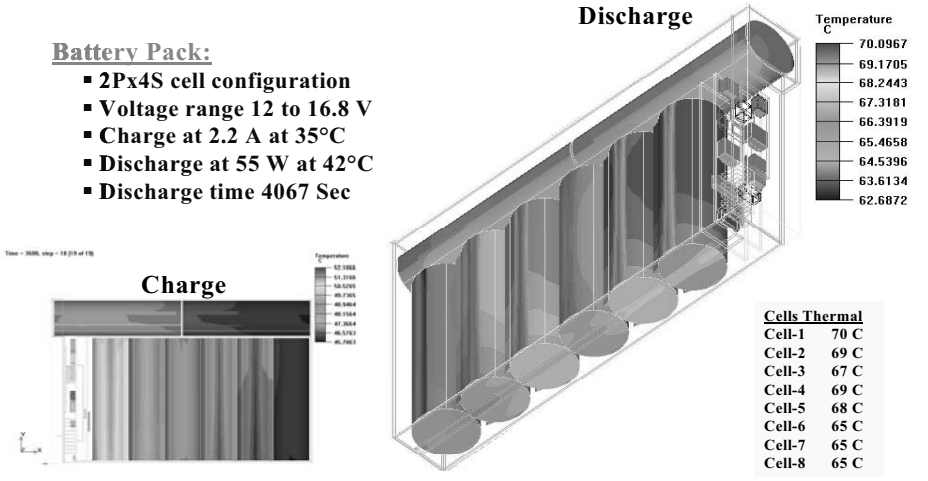


Figure 4: Thermal profiles of a notebook computer at end of charge and discharge.
Note non-uniform temperature distribution among the cells in this battery pack.
The temperature of the cell closest to the electronics reached 70ºC.



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