TI Developer Conference
March 7-9, 2007 • Dallas, TX

Minds in Motion

Real World Analog Solutions for Your Processor Applications

ADC: Delta-Sigma, SAR vs. Pipeline ADCs – When and Where to Use Them

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Senior Applications Engineer, DAP
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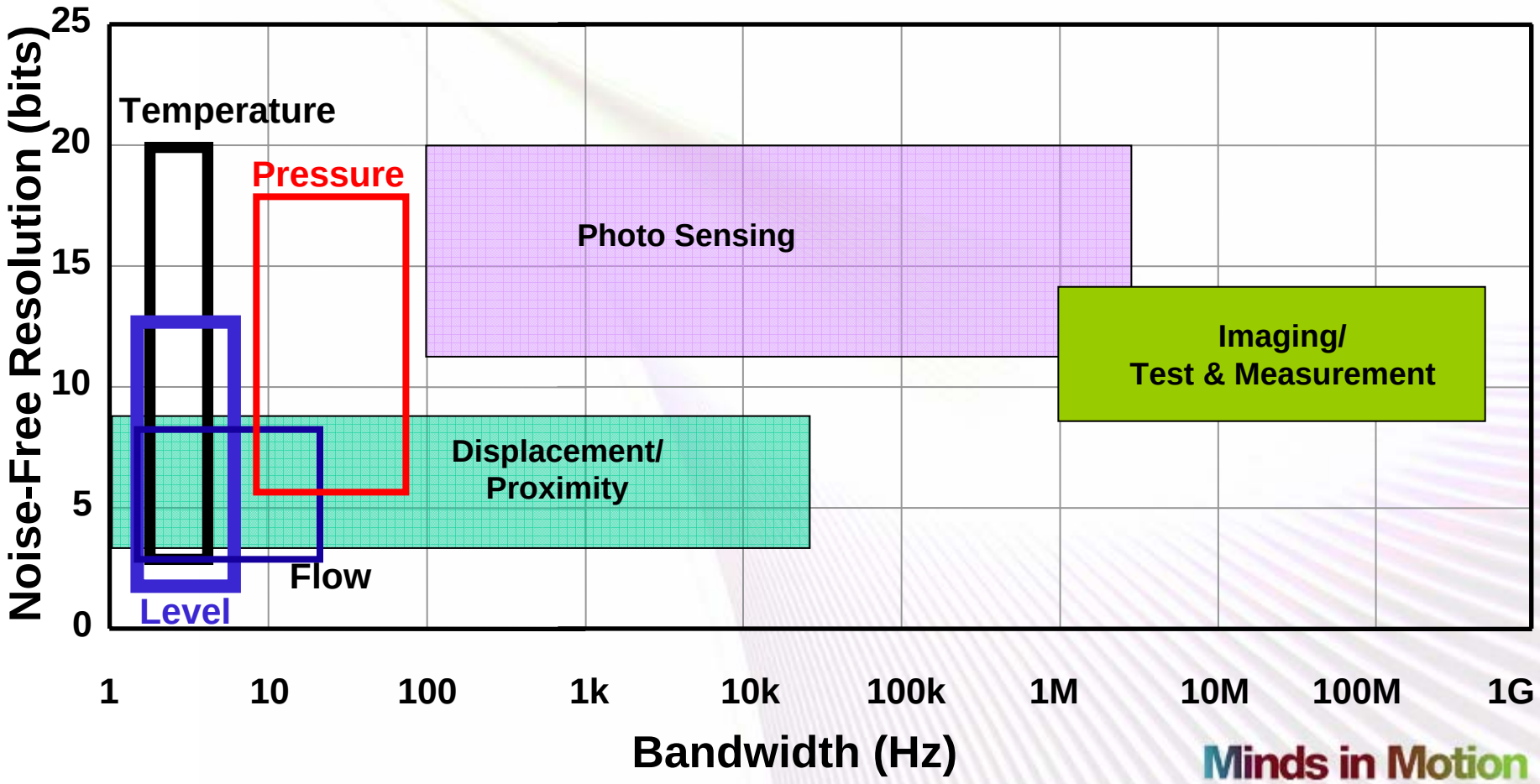
Agenda

- What Are the Signal Frequencies
  - Analog classes of applications
  - Frequency ranges of ADCs
- Nuts and Bolts of Delta-Sigma Converters
  - $\Delta\Sigma$ converter core and auxiliary $\Delta\Sigma$ functions
  - Applications for the $\Delta\Sigma$ converter
- The SAR ADC
  - Input stage dynamics
  - Applications for the SAR converter
- The High-speed Pipeline Topology
  - Driving the capacitive input stage
  - Applications for the pipeline converter
- Conclusion

Real World vs. Bandwidth



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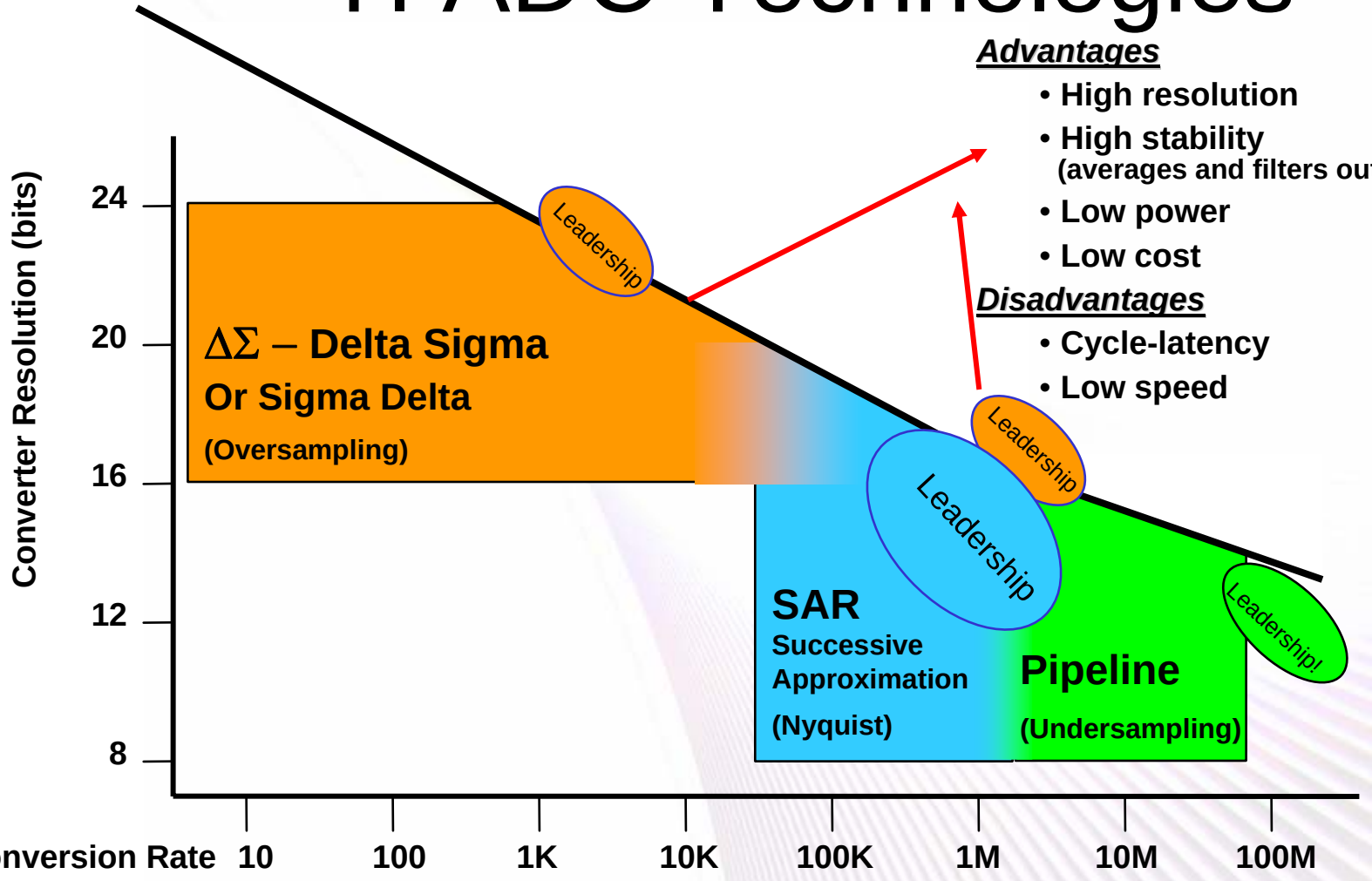
ADC Architectures

- There are many different ADC architectures
  - Successive approximation (SAR)
  - Sigma delta ($\Sigma\Delta$)
  - Slope or dual slope
  - Pipeline
  - Flash ... as in quick, not memory
- Delta-sigma converters determine the digital world by:
  - Oversampling
  - Applying digital filtering
- SARs determine the digital world by:
  - Sampling the input signal
  - Using an iterative process
- Pipeline converters determine the digital world by:
  - Undersampling
  - With sample/gain algorithm topology
  - Multiple stages/larger cycle-latency

TI ADC Technologies



Advantages

- High resolution
- High stability
  (averages and filters out noise)
- Low power
- Low cost

Disadvantages

- Cycle-latency
- Low speed

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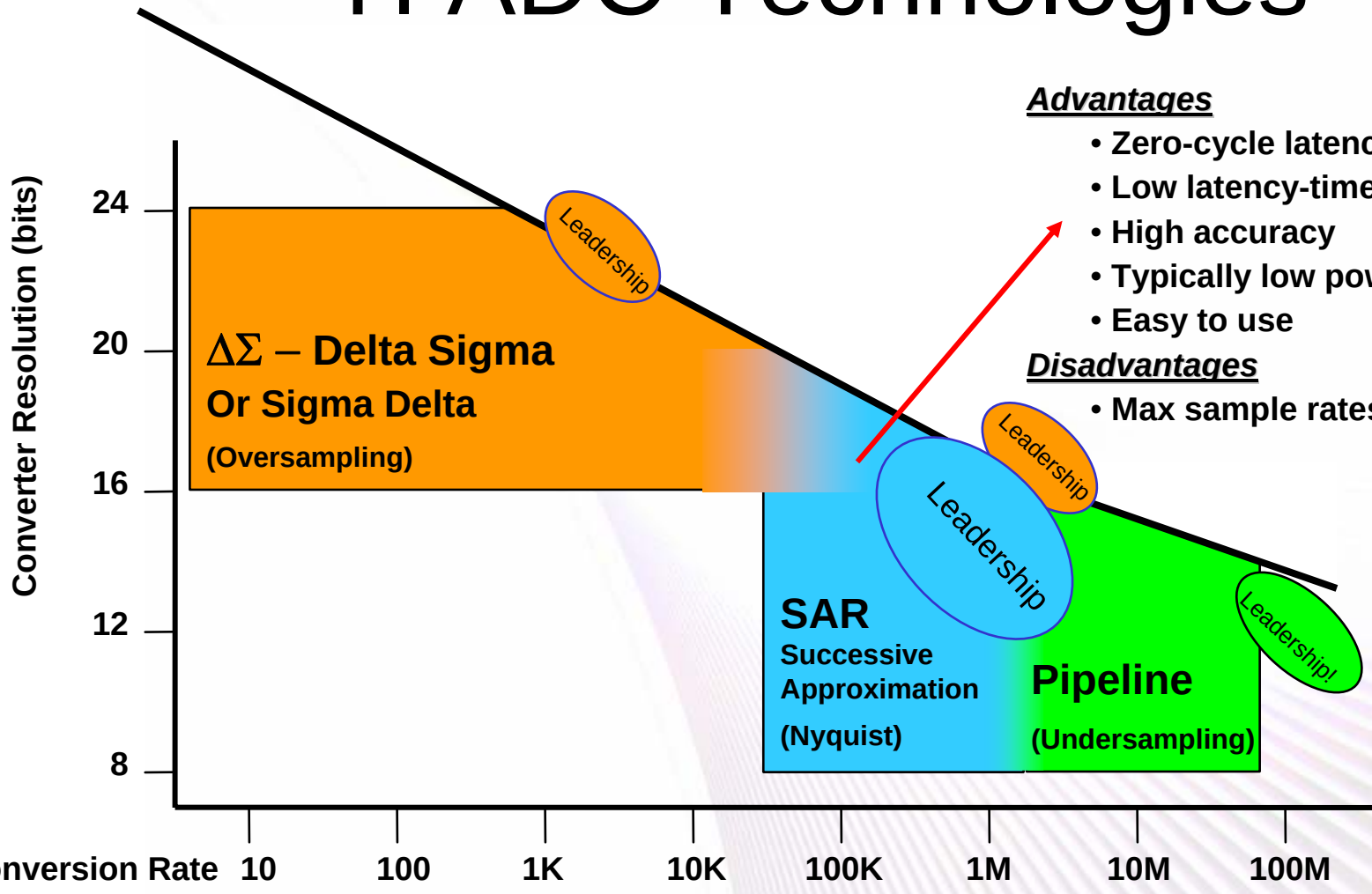
TI ADC Technologies



Advantages

- Zero-cycle latency
- Low latency-time
- High accuracy
- Typically low power
- Easy to use

Disadvantages

- Max sample rates 2-5 MHz

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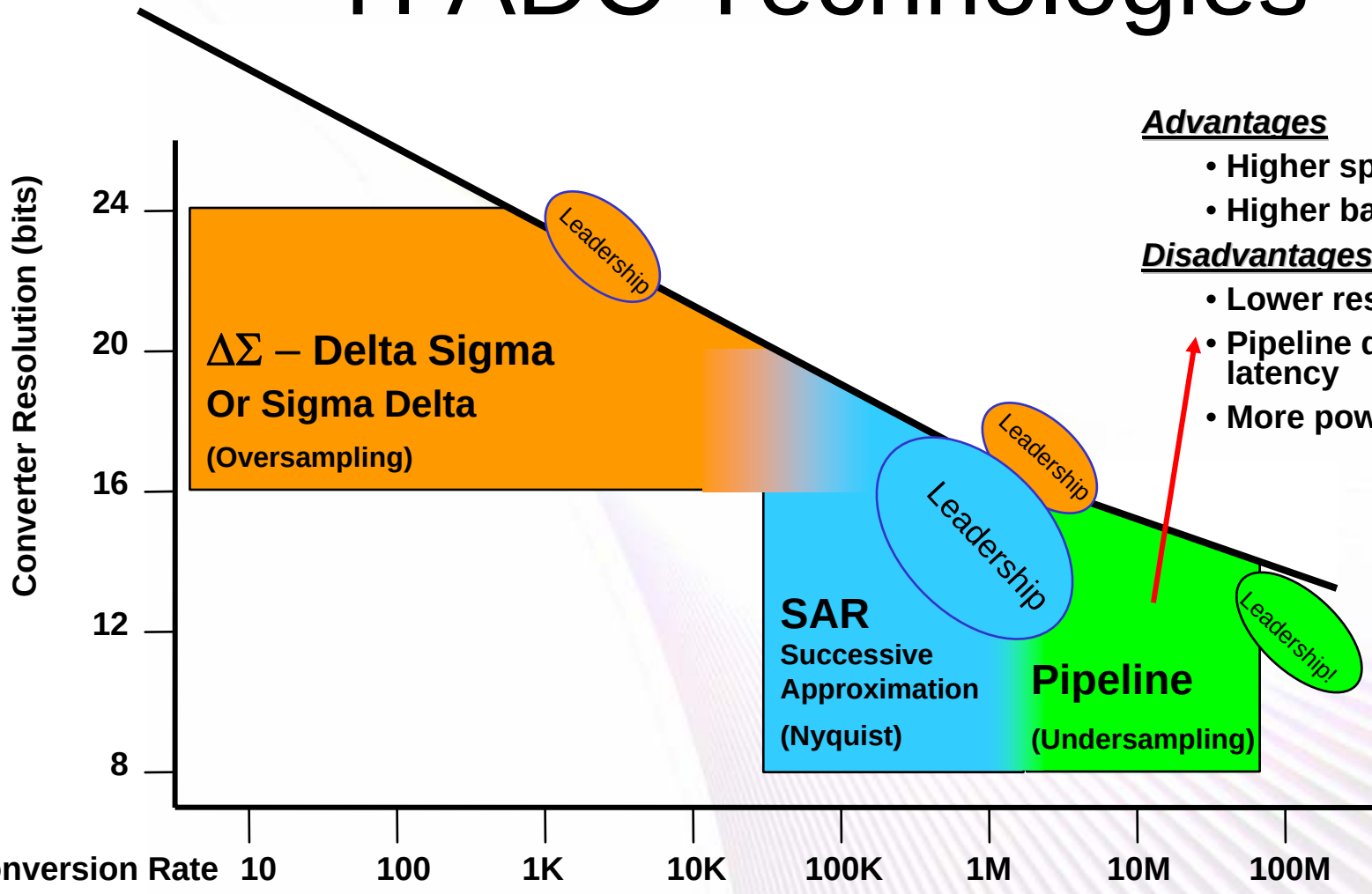
TI ADC Technologies



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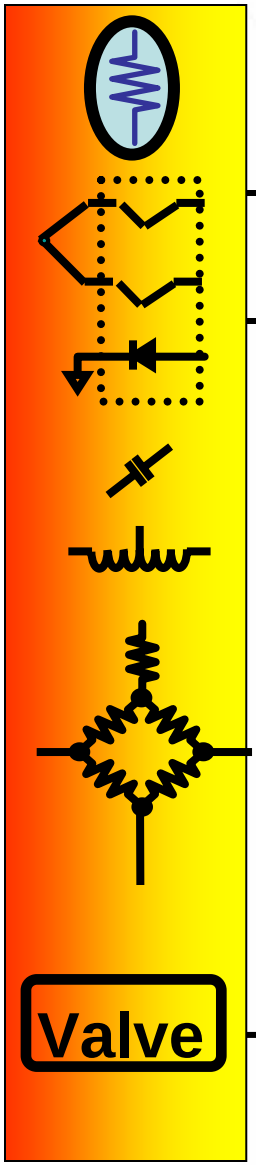
Where to Find Low Freq ADCs



Valve

OP AMP

REF

MUX

Sensor Interface
Voltage Reference Source
Buffer
Gain
Difference Amplifier
Instrumentation Amplifier
Filter
Level Shift

Voltage Reference Source

FILTER

Anti-alias Filter
Band-pass Filter
Programmable Gain Amp
Instrumentation Amp
A/D Converter Driver

A/D

µC or µP

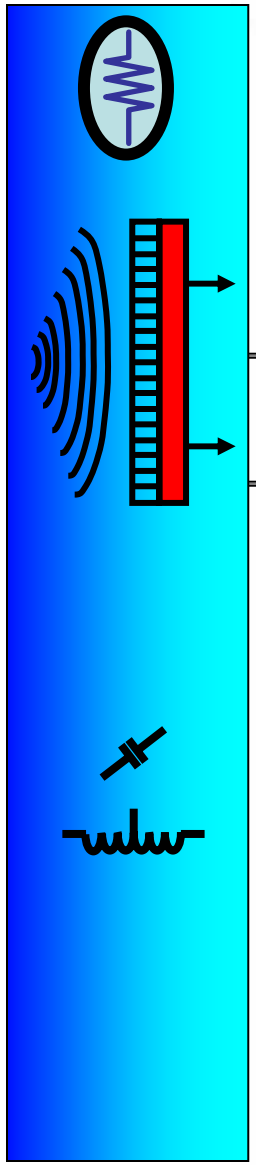
Voltage Reference Source
DDS Synthesis

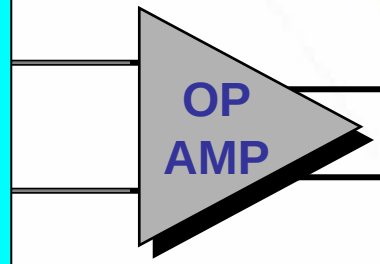
D/A

POWER AMP

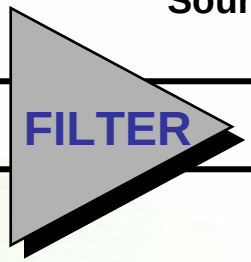
Actuator Driver
Line Driver
4-20mA Driver

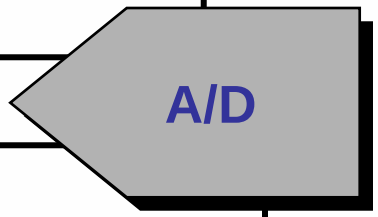
Where to Find High Freq ADCs





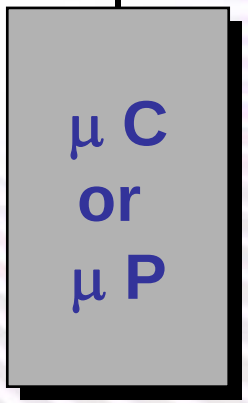
Voltage Reference Source





Buffer
VGA
LNA
Difference Amplifier
Level Shift

Anti-alias Filter
Band-pass Filter
Programmable Gain Amp
A/D Converter Driver



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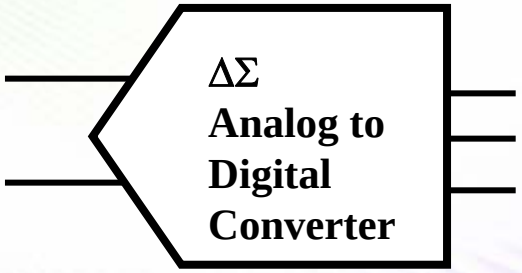
Nuts and Bolts of ΔΣ ADCs

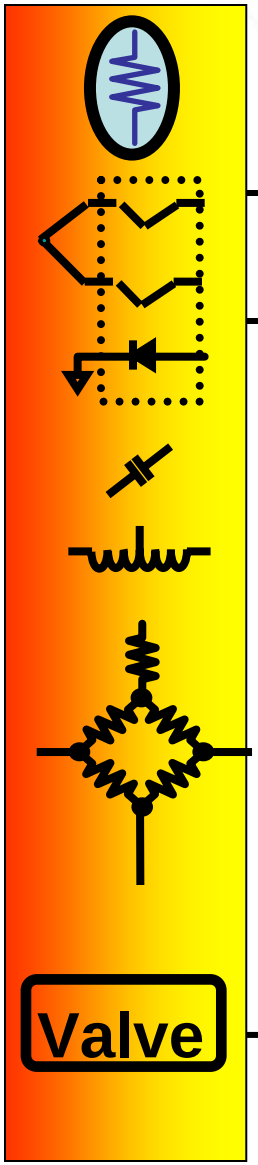
- The system versus ΔΣ (delta-sigma)
- ΔΣ analog-to-digital converter core
  - Programmable gain amplifier (PGA)
  - Analog modulator
  - Digital filter
  - Decimation filter
- Other features and options
- Typical applications



Applications for ΔΣ Converters

- Signal Level: System Clock Range ~ 0.5 to 40 MHz
  - Has an internal digital low-pass filter
    - Uses an integrator
  - Accurate near DC
  - High resolution: Up to 24 bits
- Audio: System Clock Range ~ 20 to 40 MHz
  - Has an internal digital low-pass filter
  - Optimized noise performance
  - Optimized filter in audio frequency for flatness
- High Speed
  - Has an internal digital band-pass filter
    - Uses a band-pass topology instead of integrator

The ΔΣ ADC System



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POWER AMP

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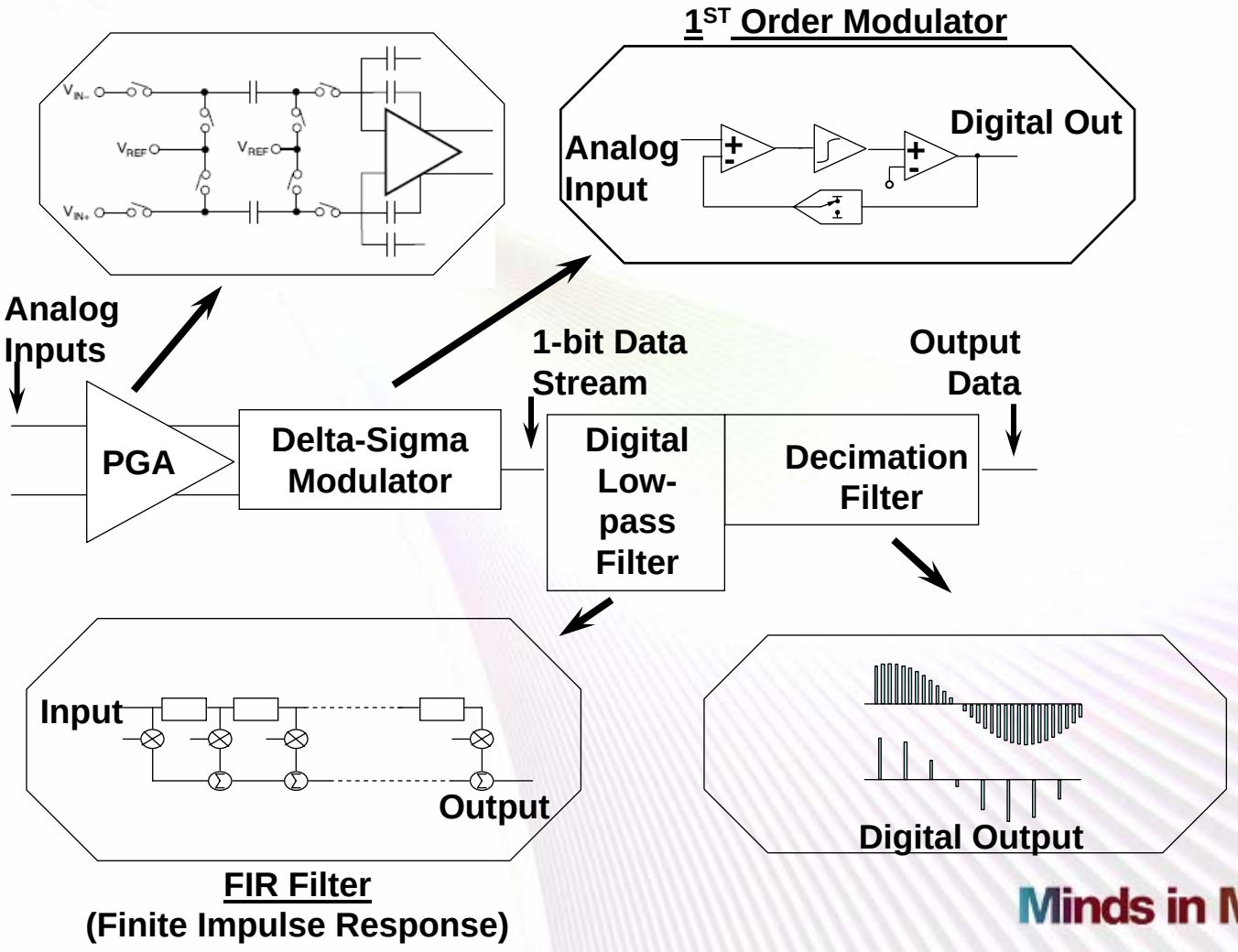
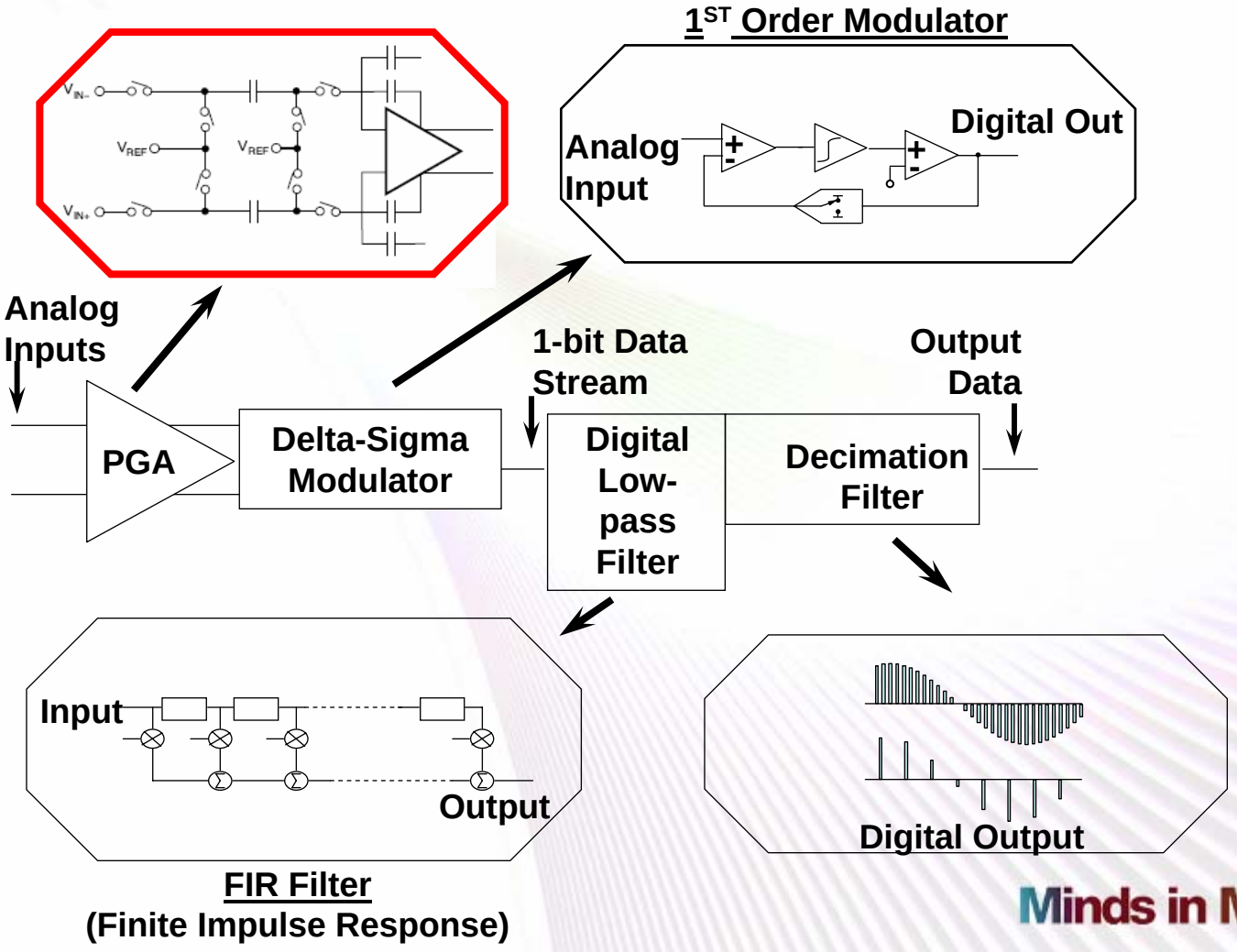
Line Driver
4-20mA Driver

Delta-Sigma ADC Core



Programmable Gain Amp



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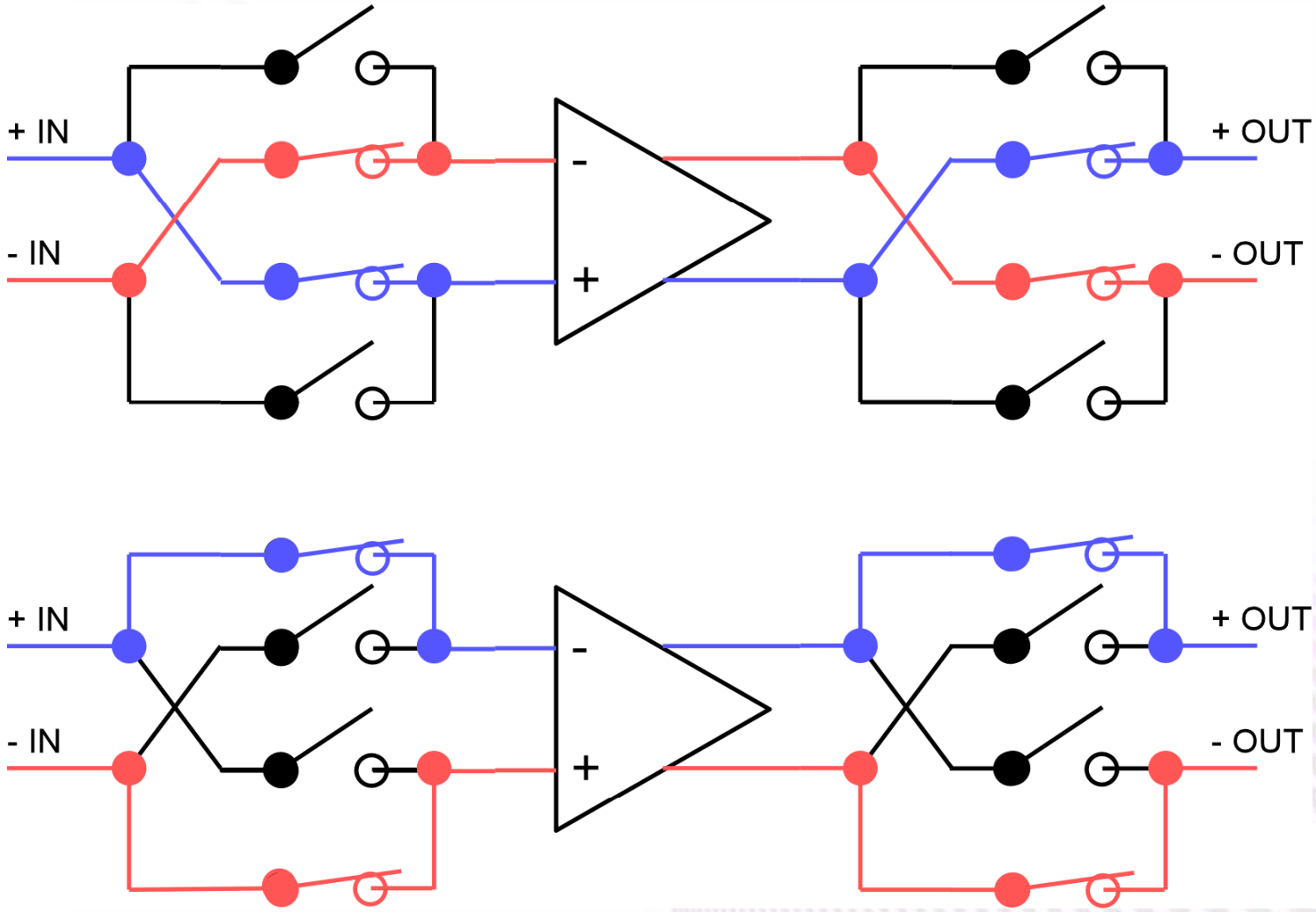
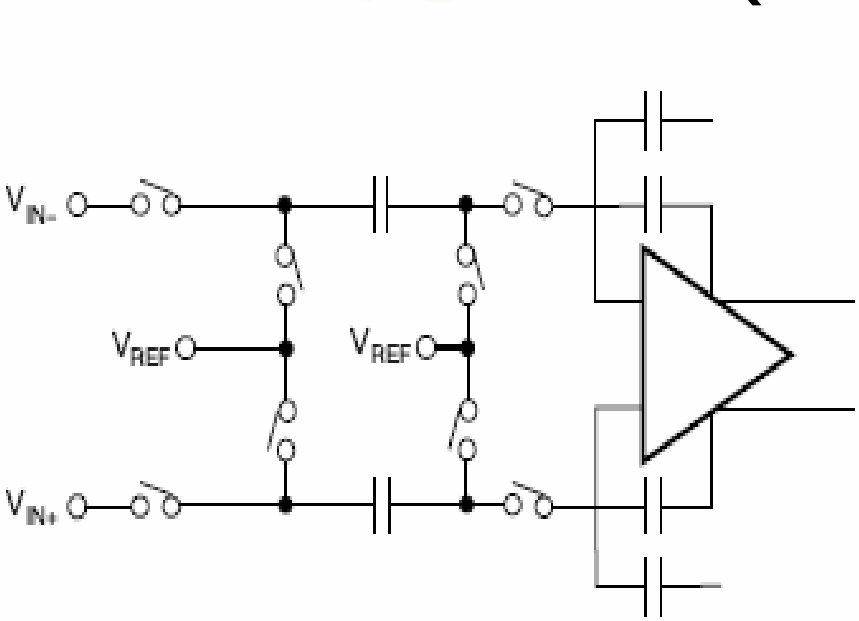
Chopper-Stabilized



Programmable Gain Amplifier (PGA)



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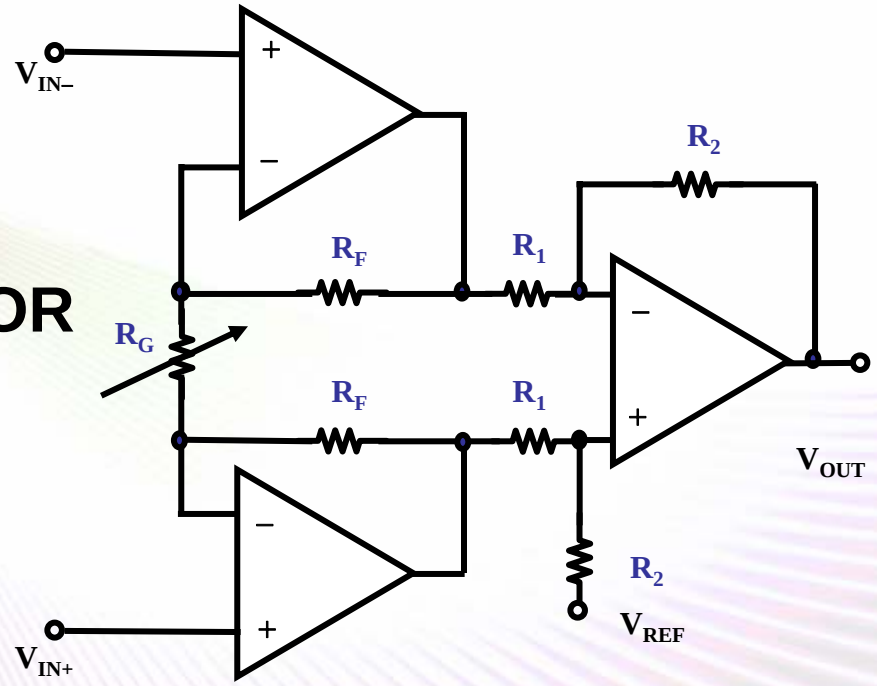

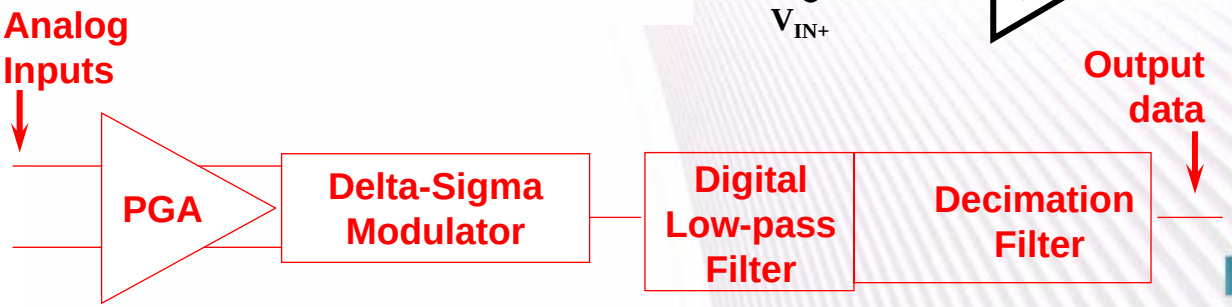

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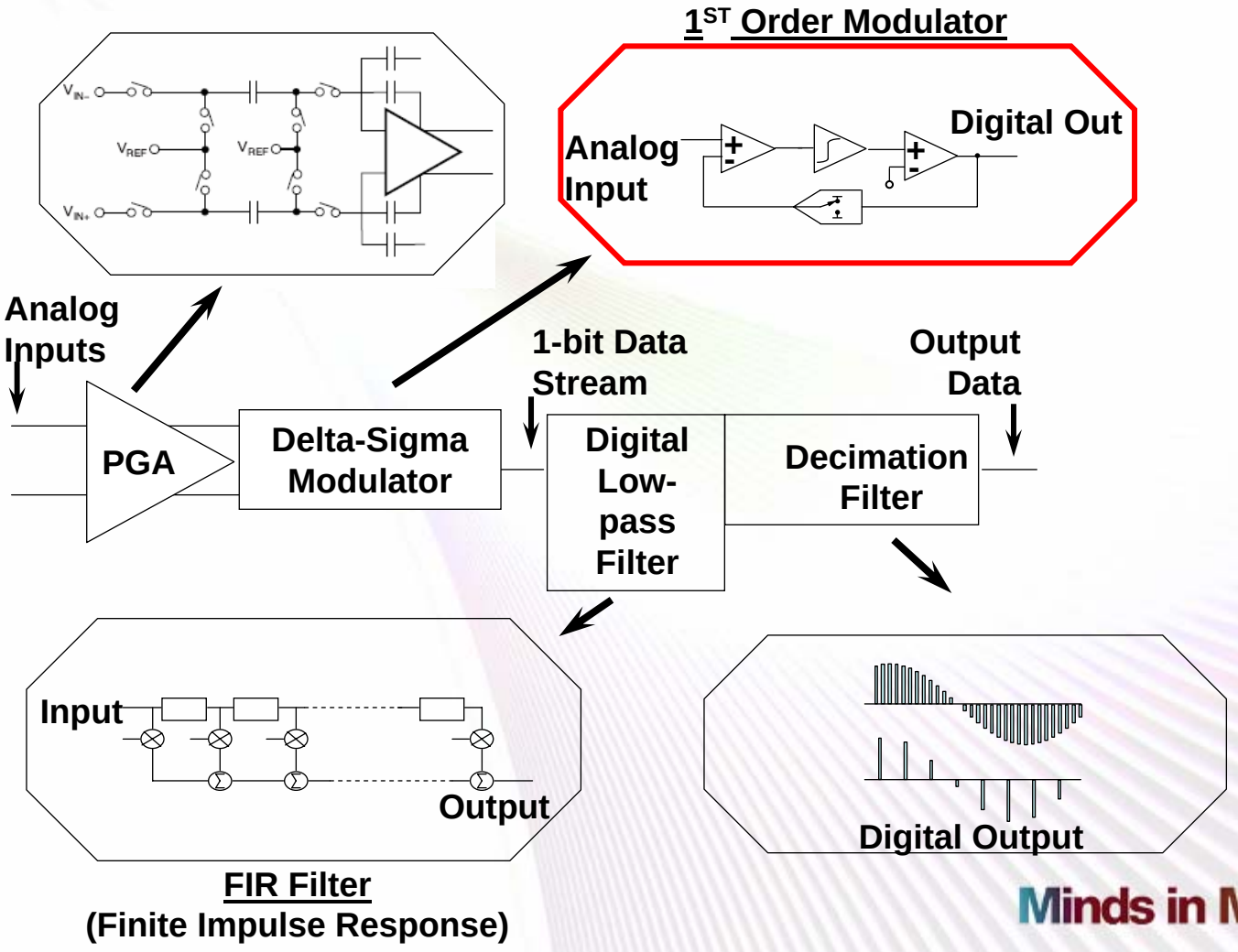
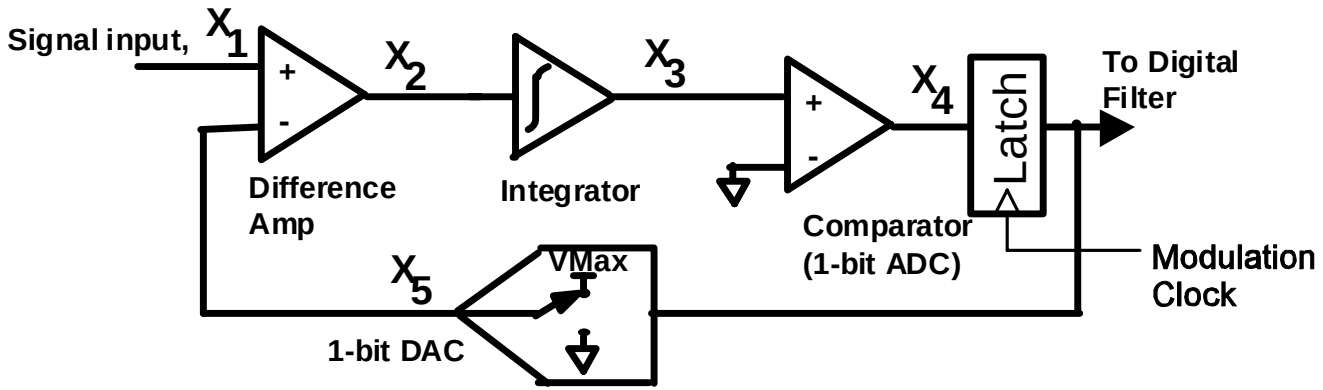
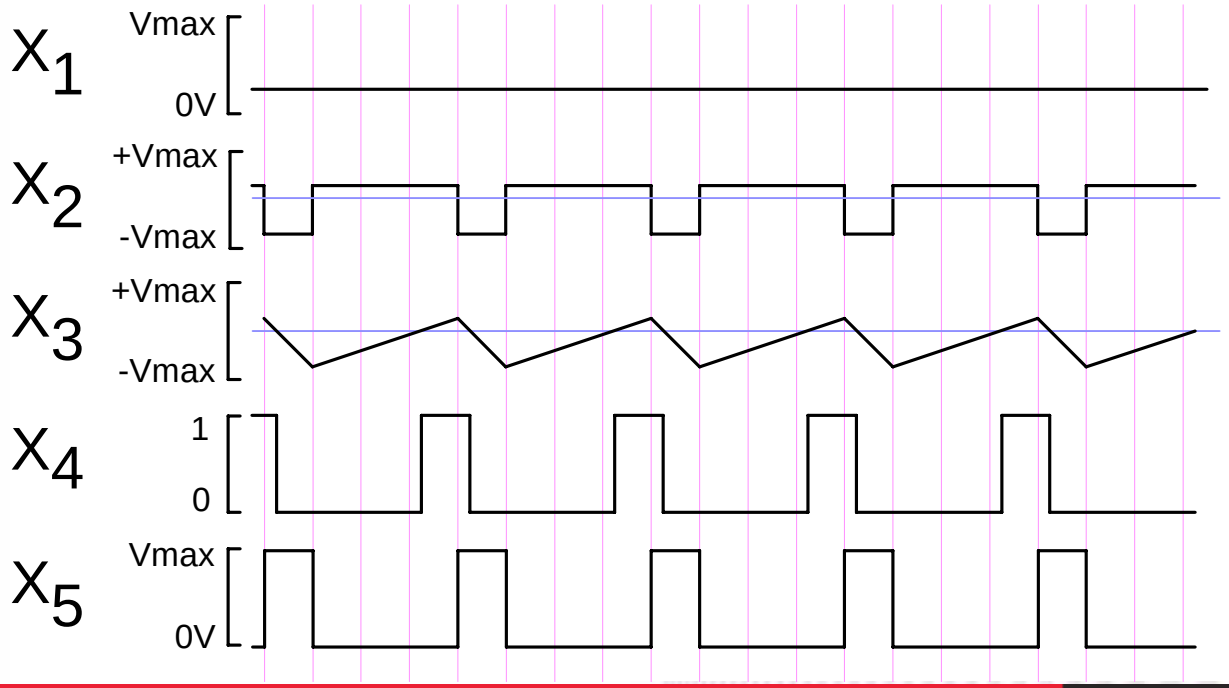
Delta-Sigma ADC Core

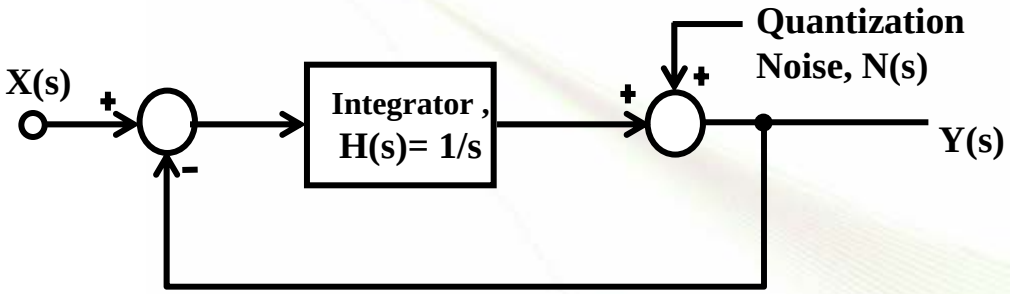


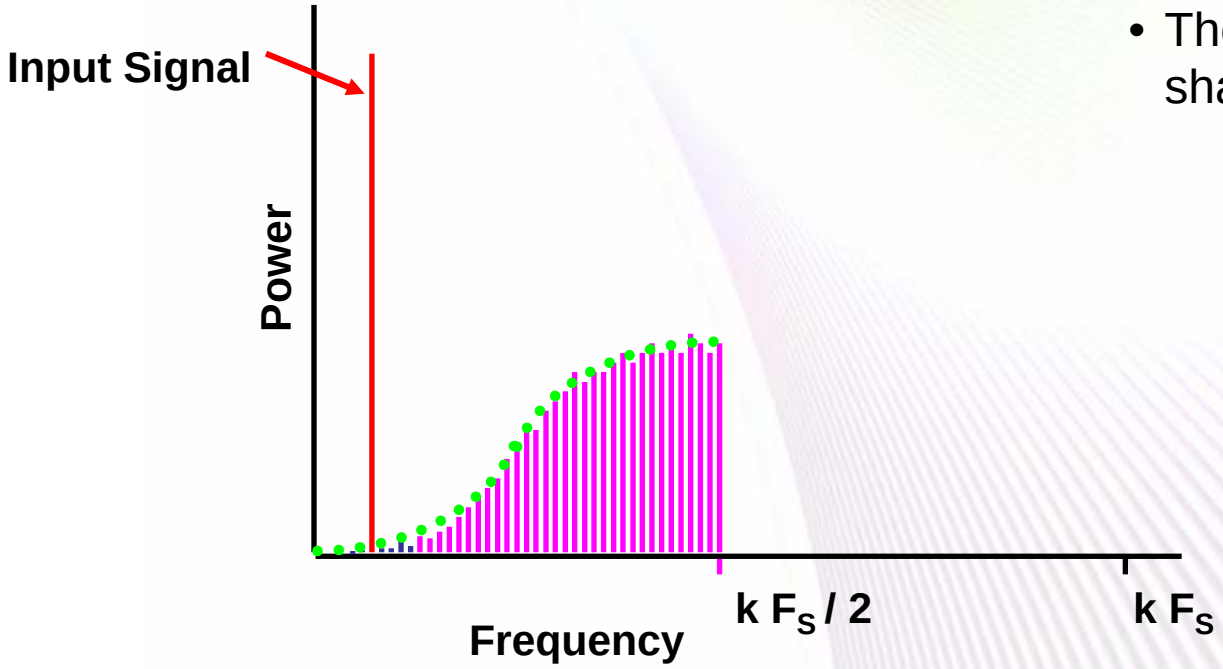
ΔΣ Modulator Time Domain





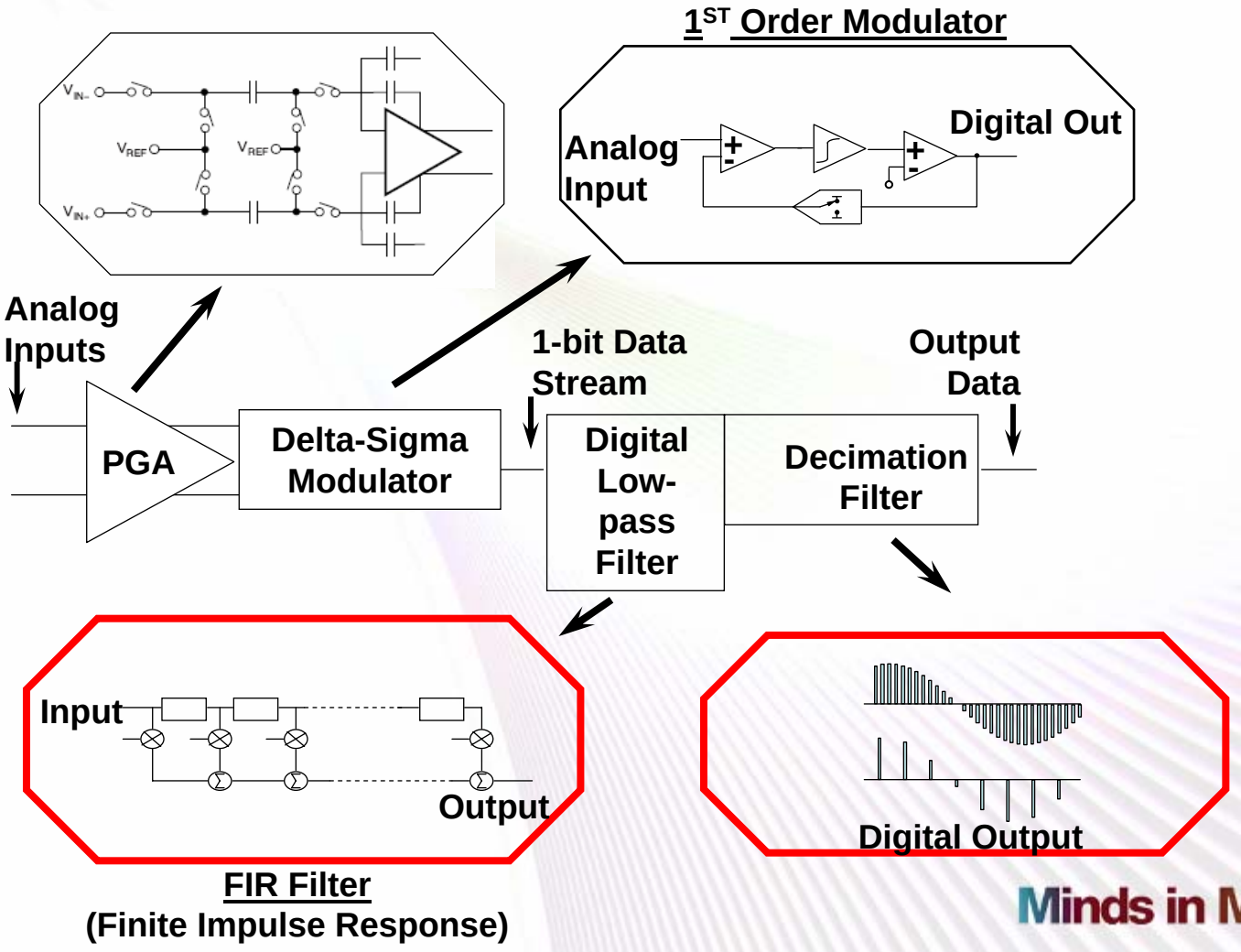
ΔΣ Modulator Frequency Domain





- The integrator serves as a high-pass filter to the noise.
- The result is noise shaping.

Delta-Sigma ADC Core



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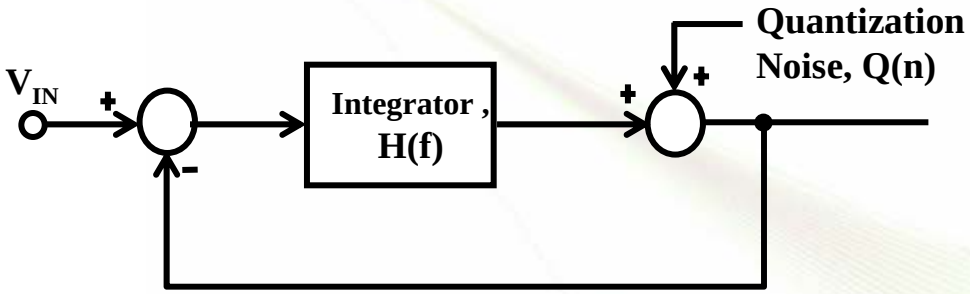

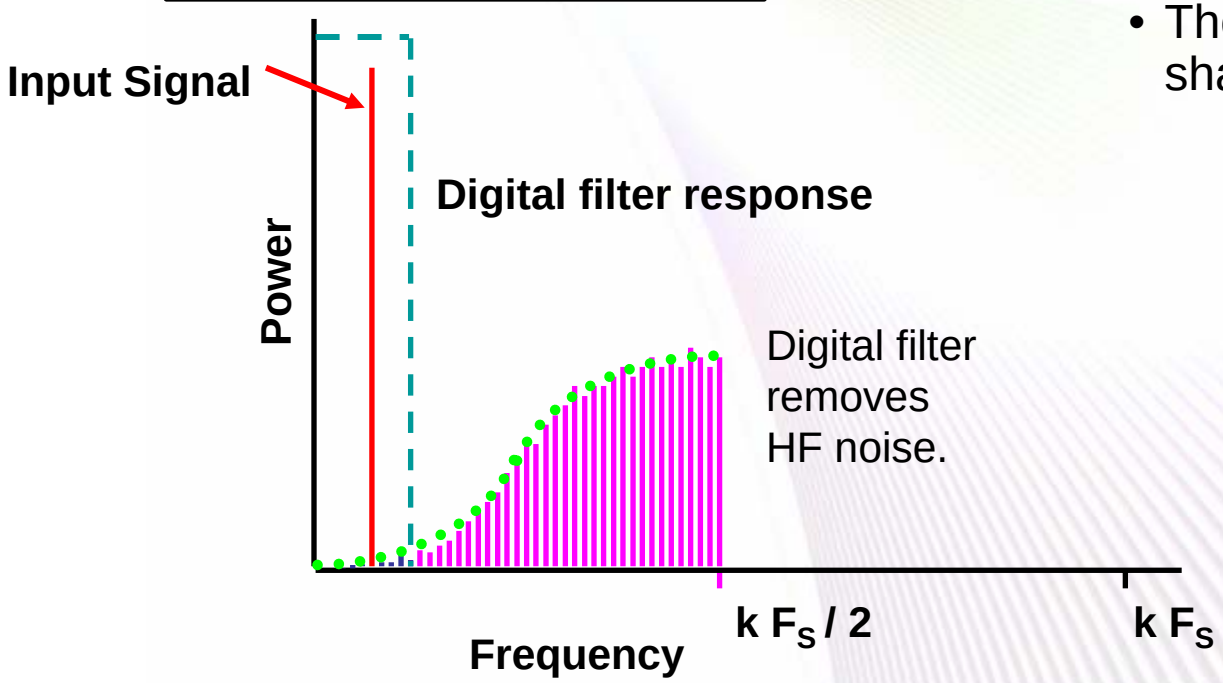

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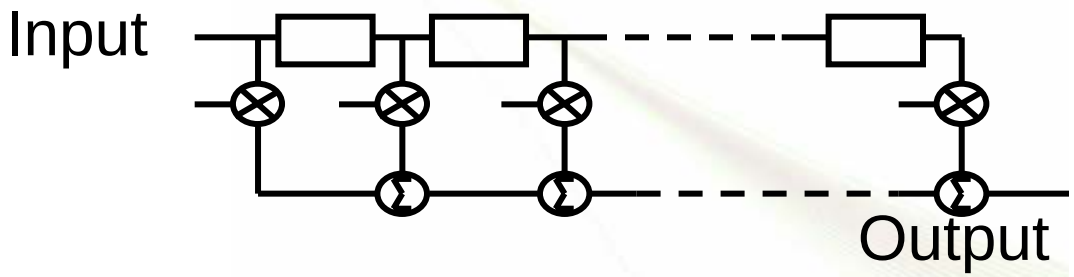
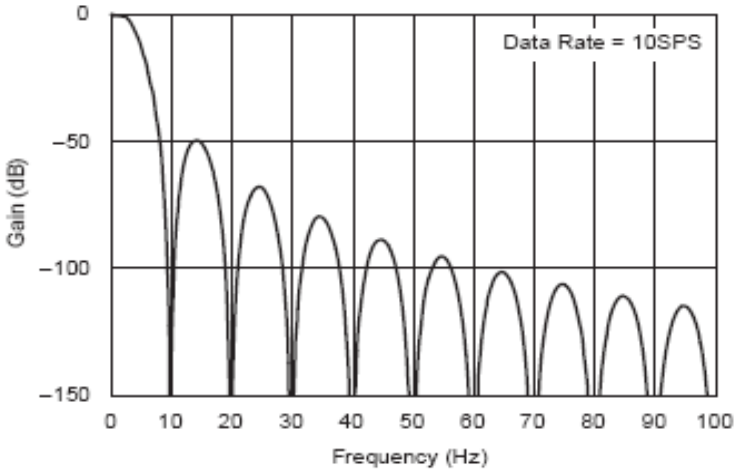
- The result is noise shaping.

Digital Filter

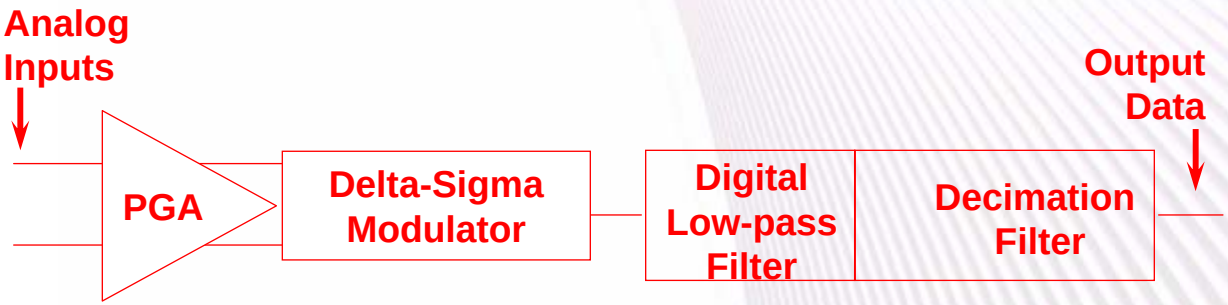


Digital Filter Options

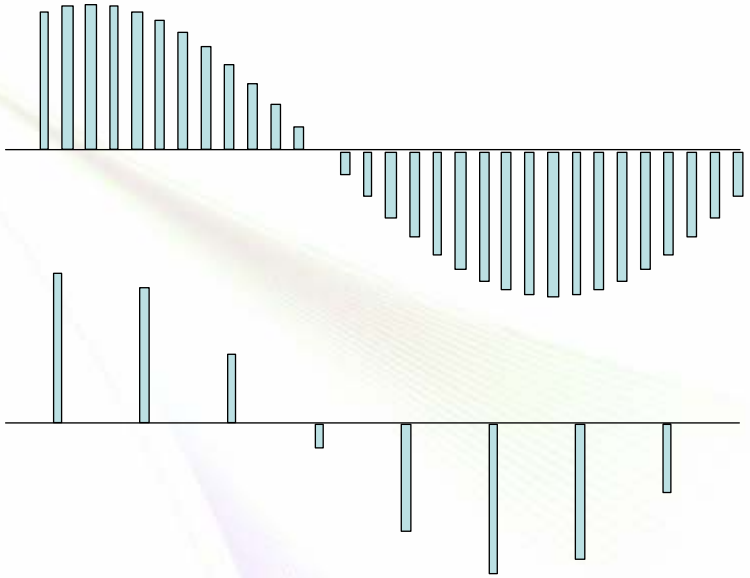
- FIR
- Sinc
- IIR
- Averaging



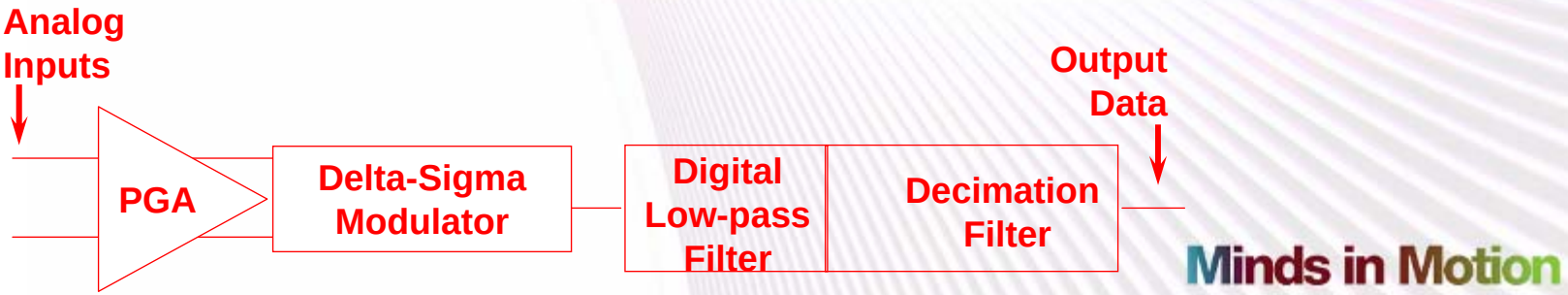
Sinc^4 Digital Filter Response (ADS1232)



Decimation Filter



Digital Output



Other Analog Features and Options

Analog

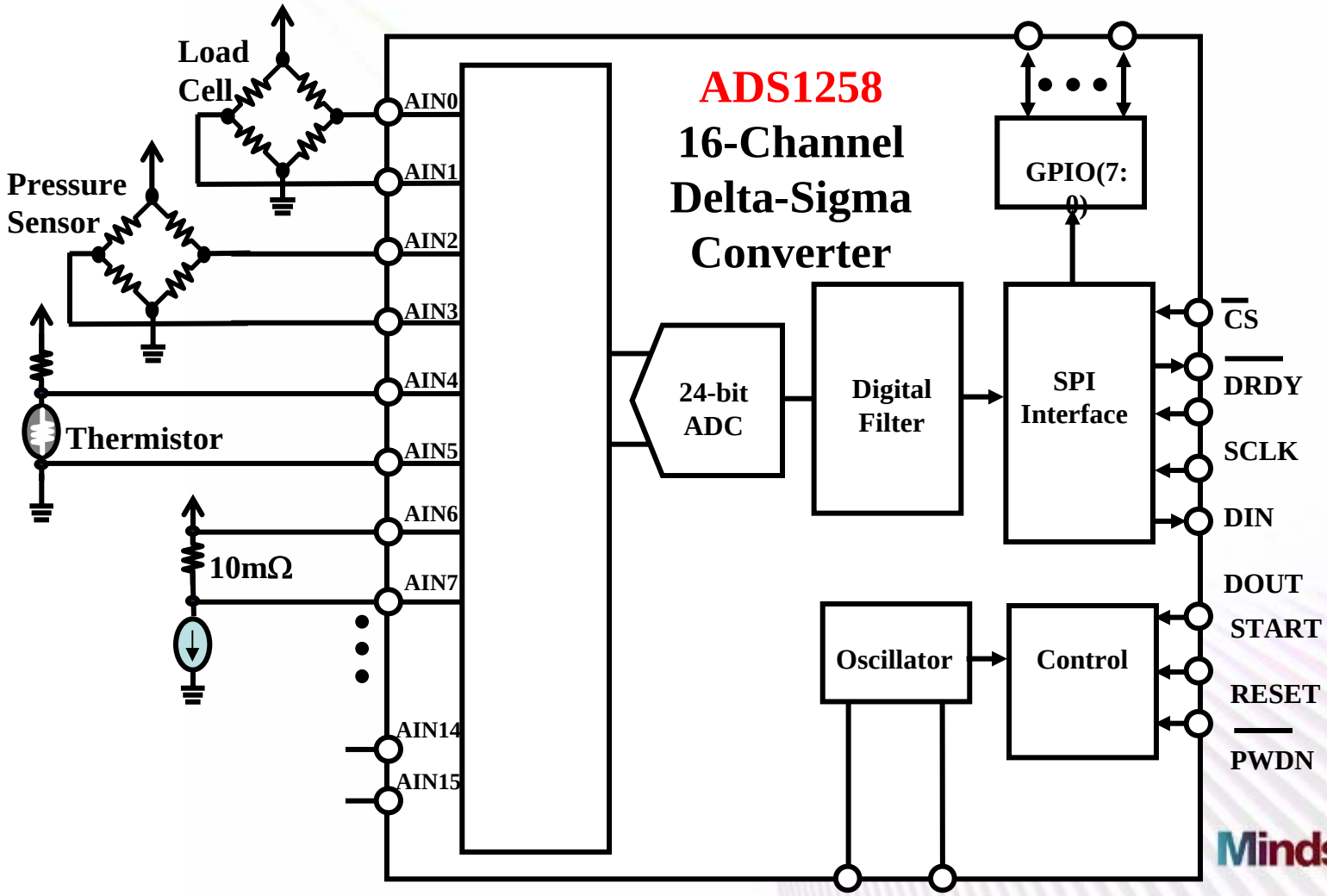
- Features
  - Internal voltage or current reference(s)
  - AC excitation capable
  - DAC for TARE offset adjust
  - Transducer burn-out sensor
- Input Interface
  - Differential and/or multichannel Inputs
  - Buffer input
  - Negative input

Other Digital Features and Options

Digital

- Features
  - Single-cycle conversion (zero-cycle latency)
  - Programmable digital filter
  - Calibration: Offset, gain, self, system
  - Sleep mode, BOR, memory, digital latches
- Interface
  - Slave/master
  - Clock polarity
  - Daisy chain

Zero-Latency in MUX Applications



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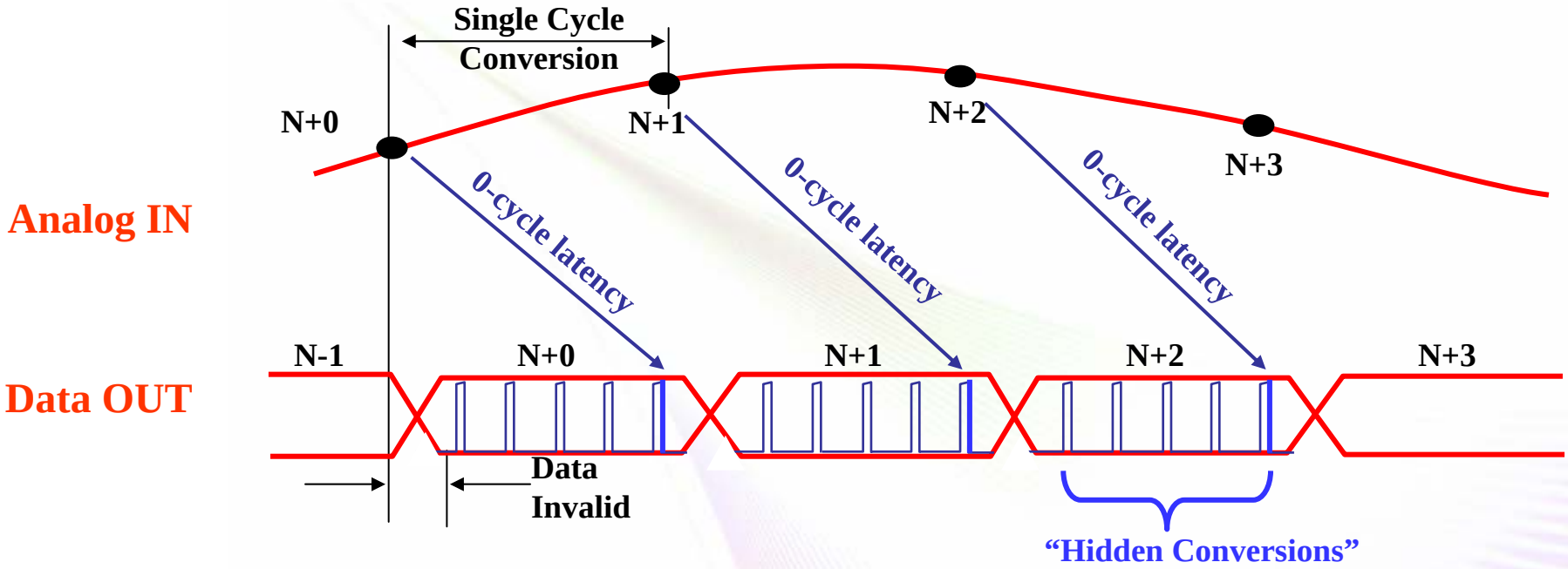
Zero Cycle Latency: ADS1258

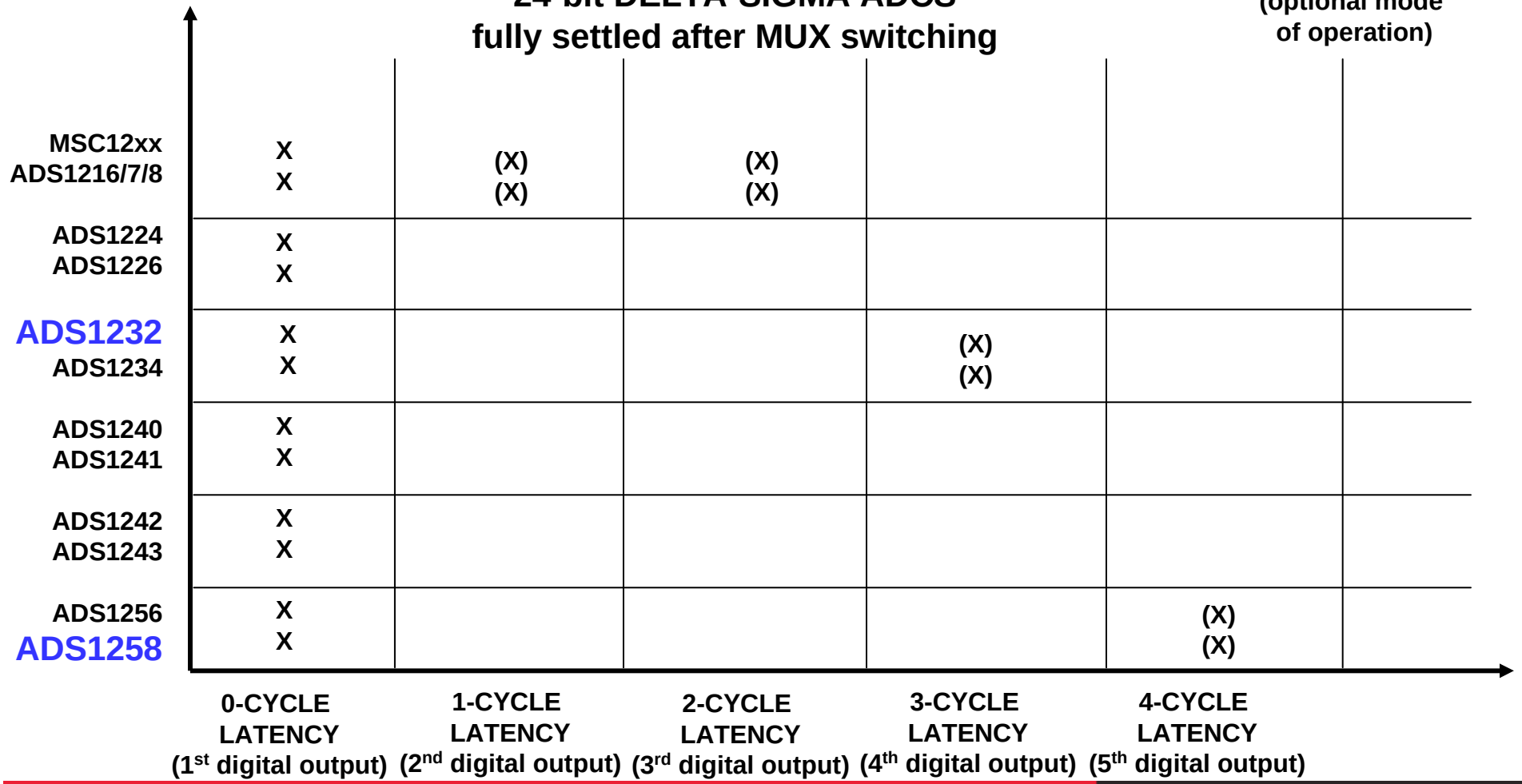


Zero cycle latency =

- Zero latency
- Single cycle conversion
- Single cycle settling
- No latency

TI Del-sig Cycle latency

MULTIPLEXED
24-bit DELTA-SIGMA ADCS
fully settled after MUX switching



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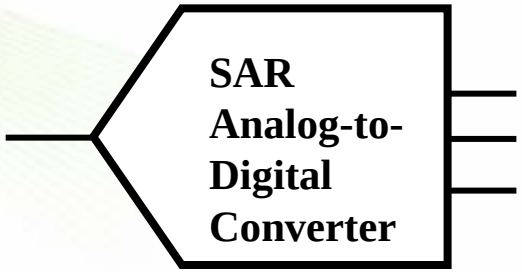
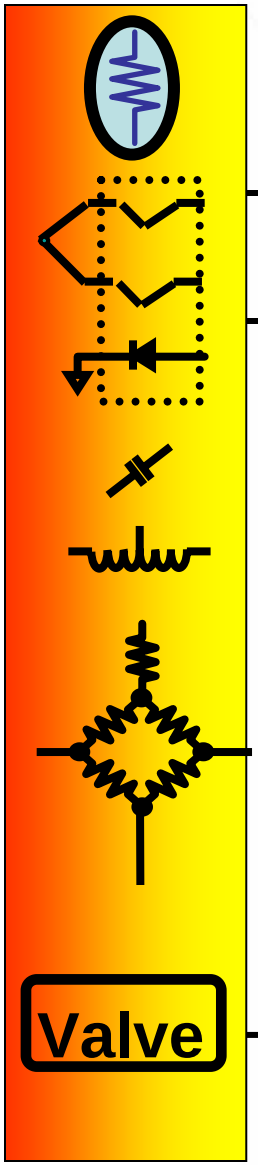
The SAR ADC

- Most serial ADCs are SARs or Del-Sigs.
- SARs are best for general-purpose apps.
  - Data loggers
  - Temp sensors
  - Bridge sensors
  - General purpose
- In the market SARs:
  - Can be 8 to 18 bits of resolution
  - Speed range: >10 ksps to < 5 Msps
- SARs found as
  - Standalone
  - Peripheral in microcontrollers, processors



The SAR ADC System



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A/D Converter Driver

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DDS Synthesis

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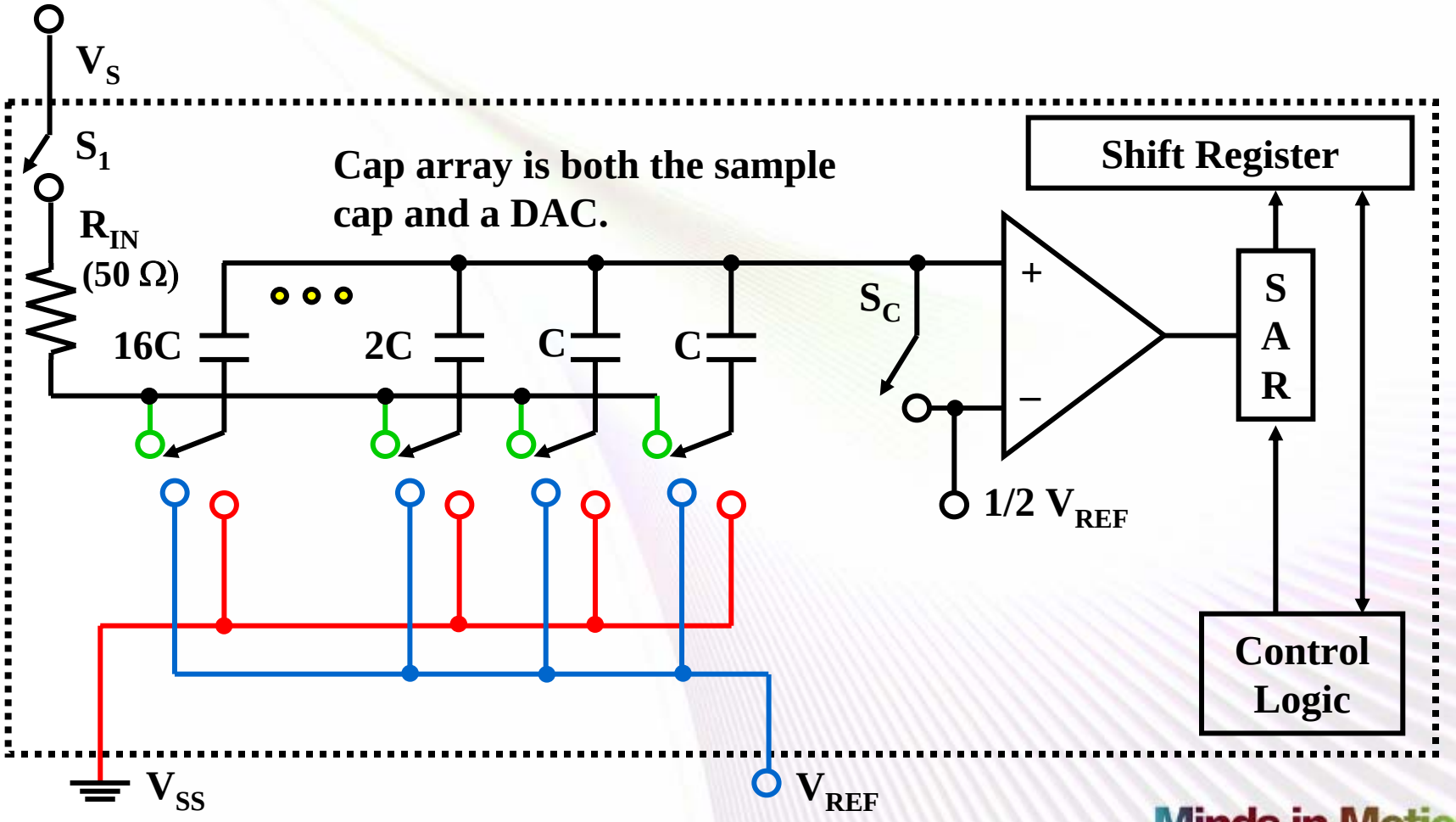
POWER AMP

D/A

Actuator Driver
Line Driver
4-20mA Driver

SAR Converter: Block Diagram



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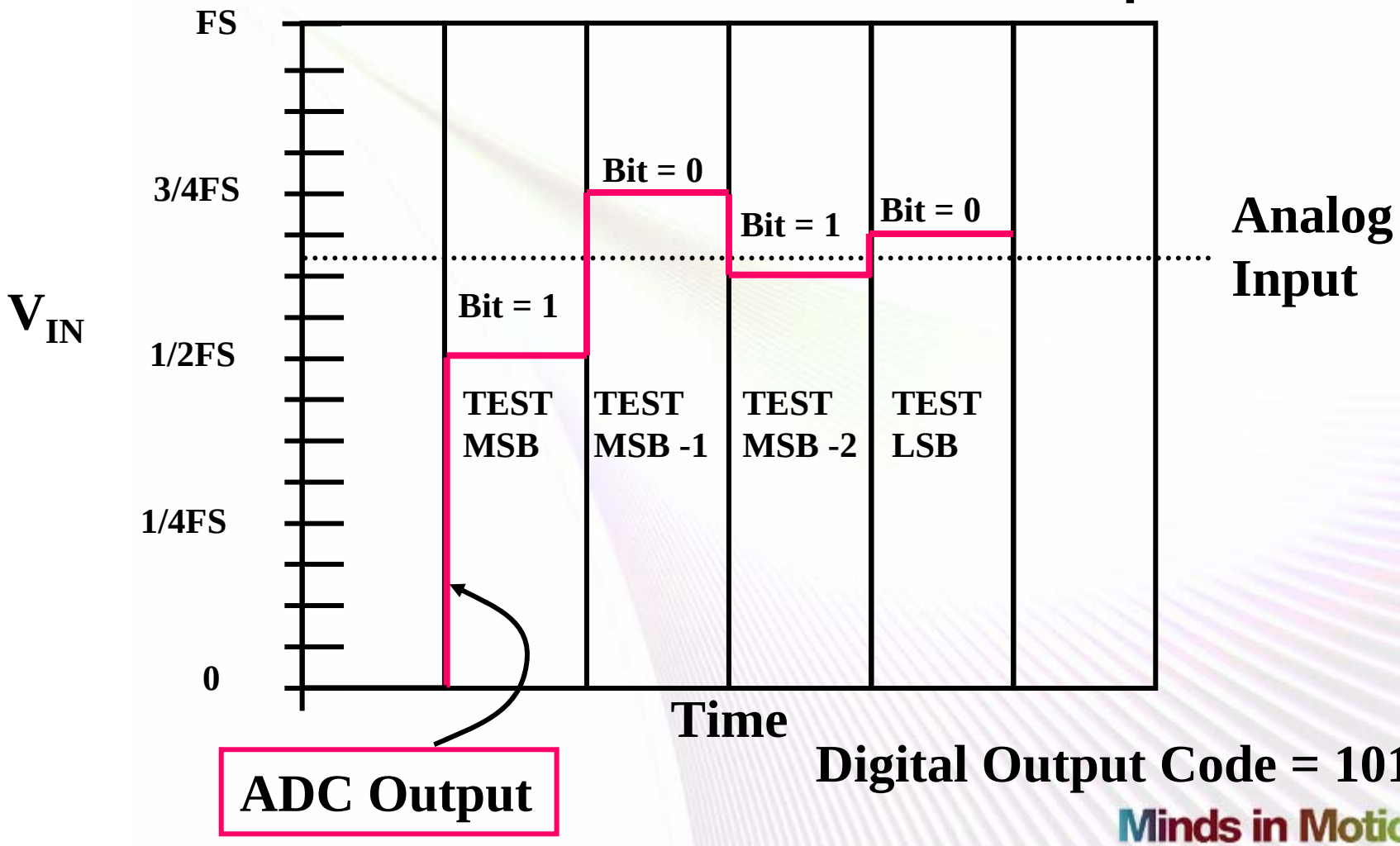
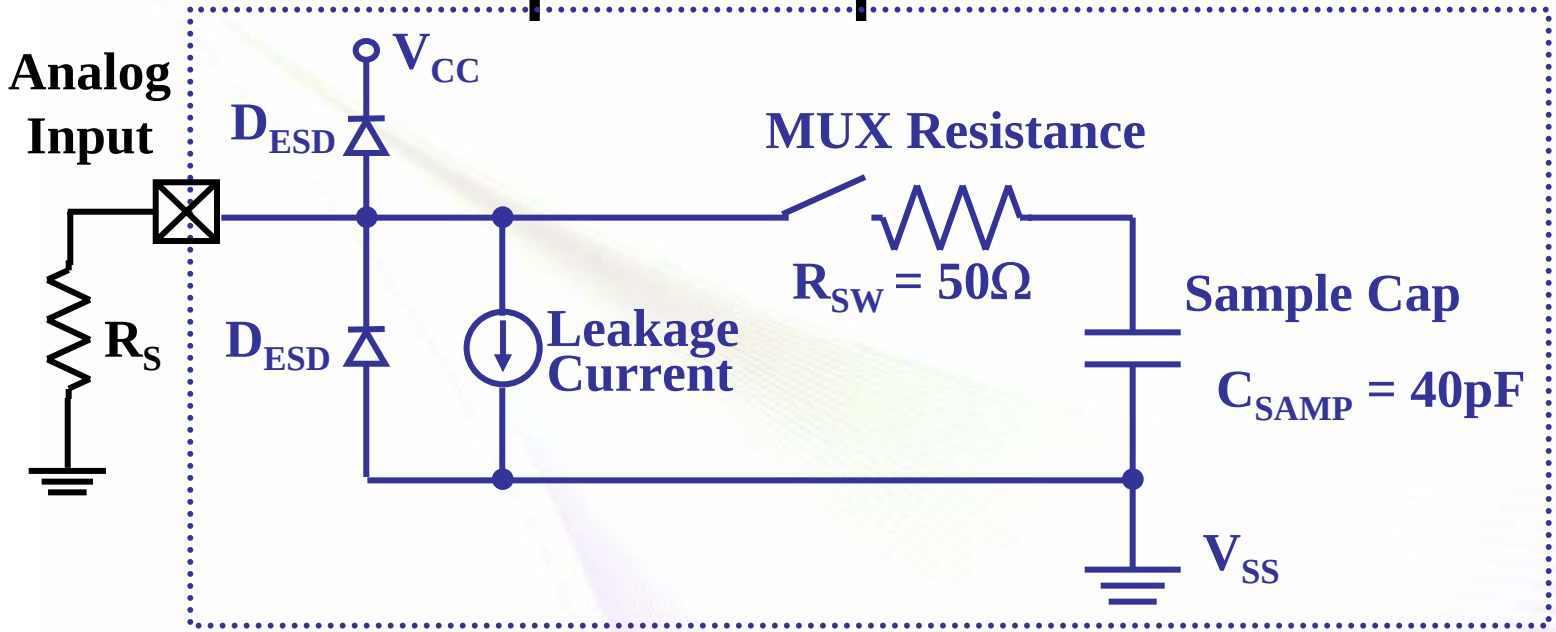
SAR Conversion Concept



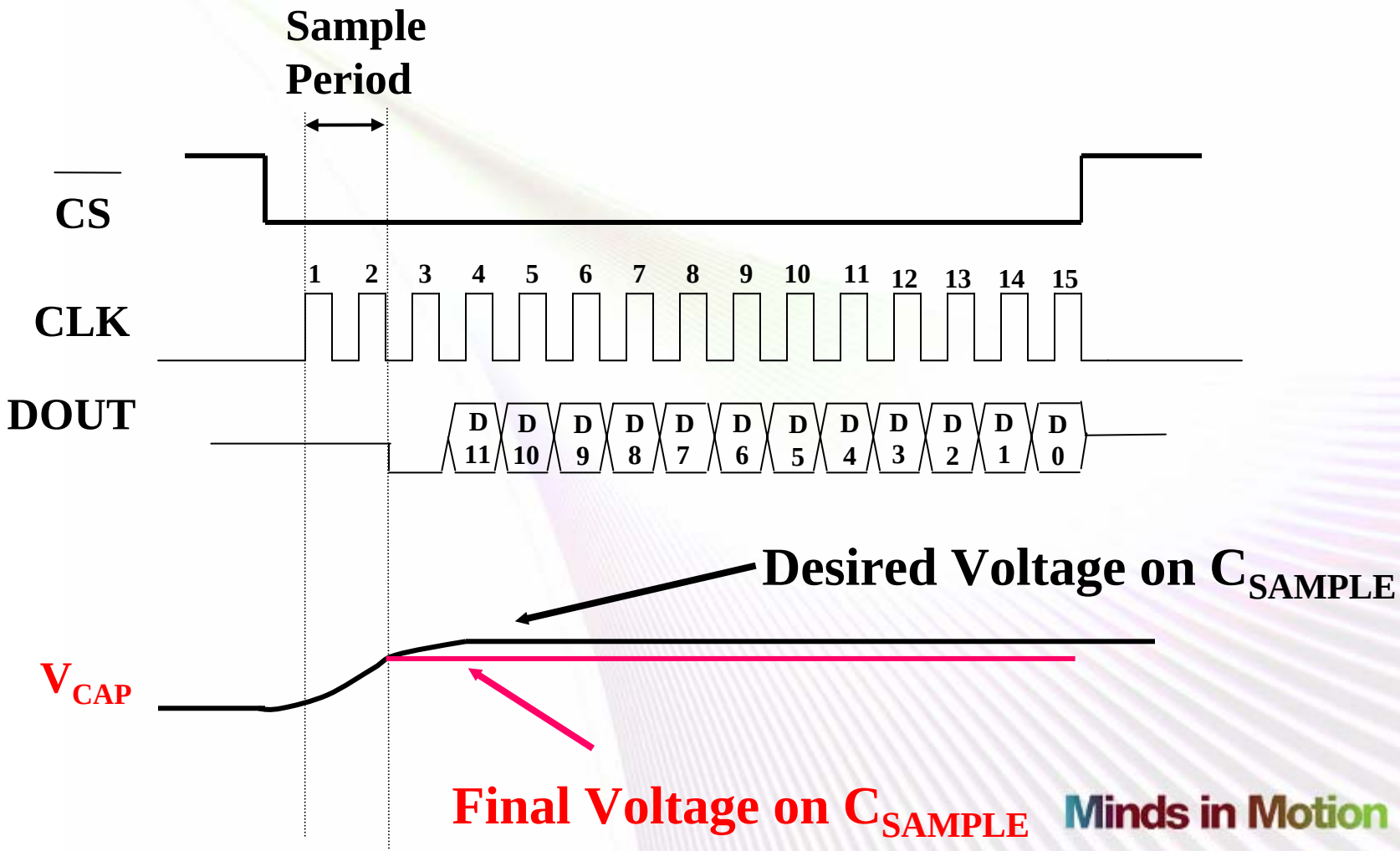
ADC Input Impedance



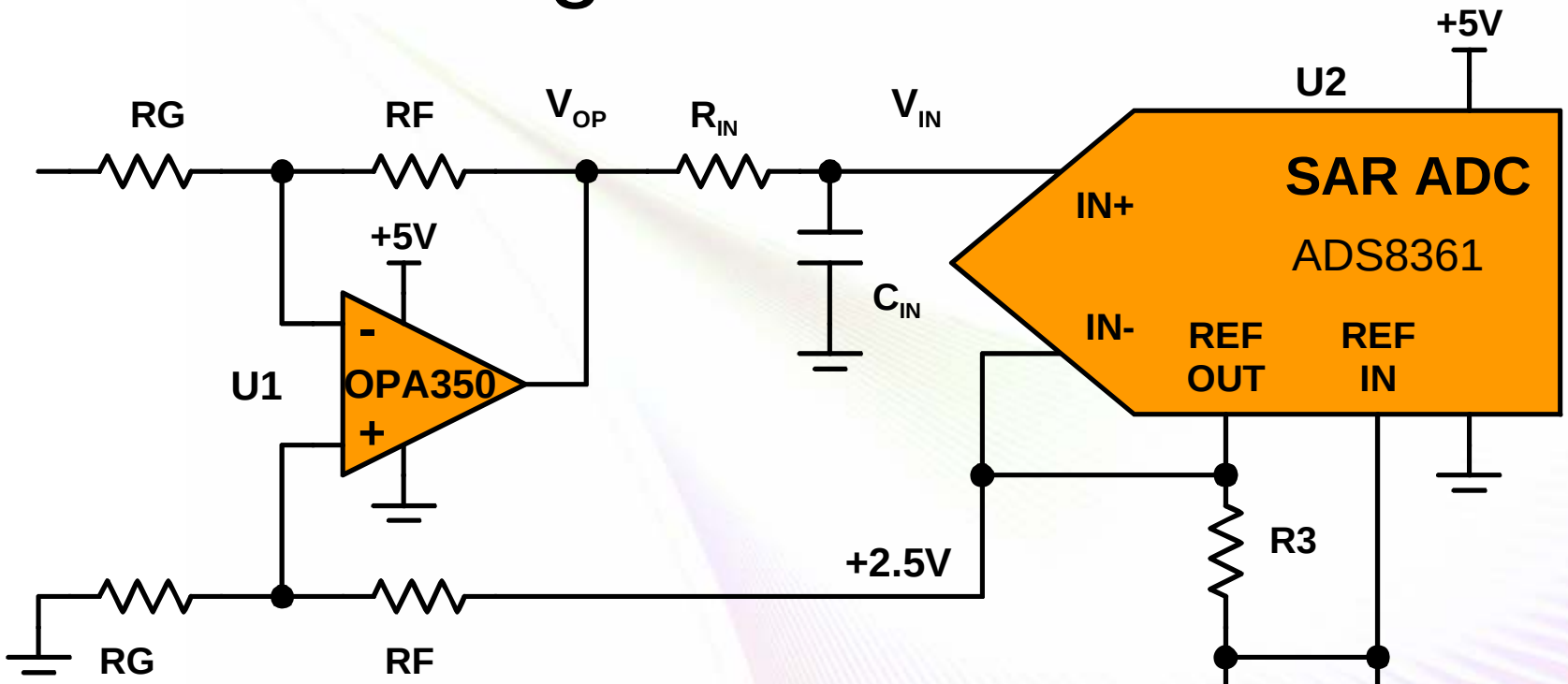
- Input internal impedance is relatively low.
- A high-impedance source increases sample cap charging time.
- Rise time of voltage on

$$C_{SW} \sim (R_S + R_{SAMP}) * C_{SW}$$

Sample Cap Charging Time



Driving SAR Converters



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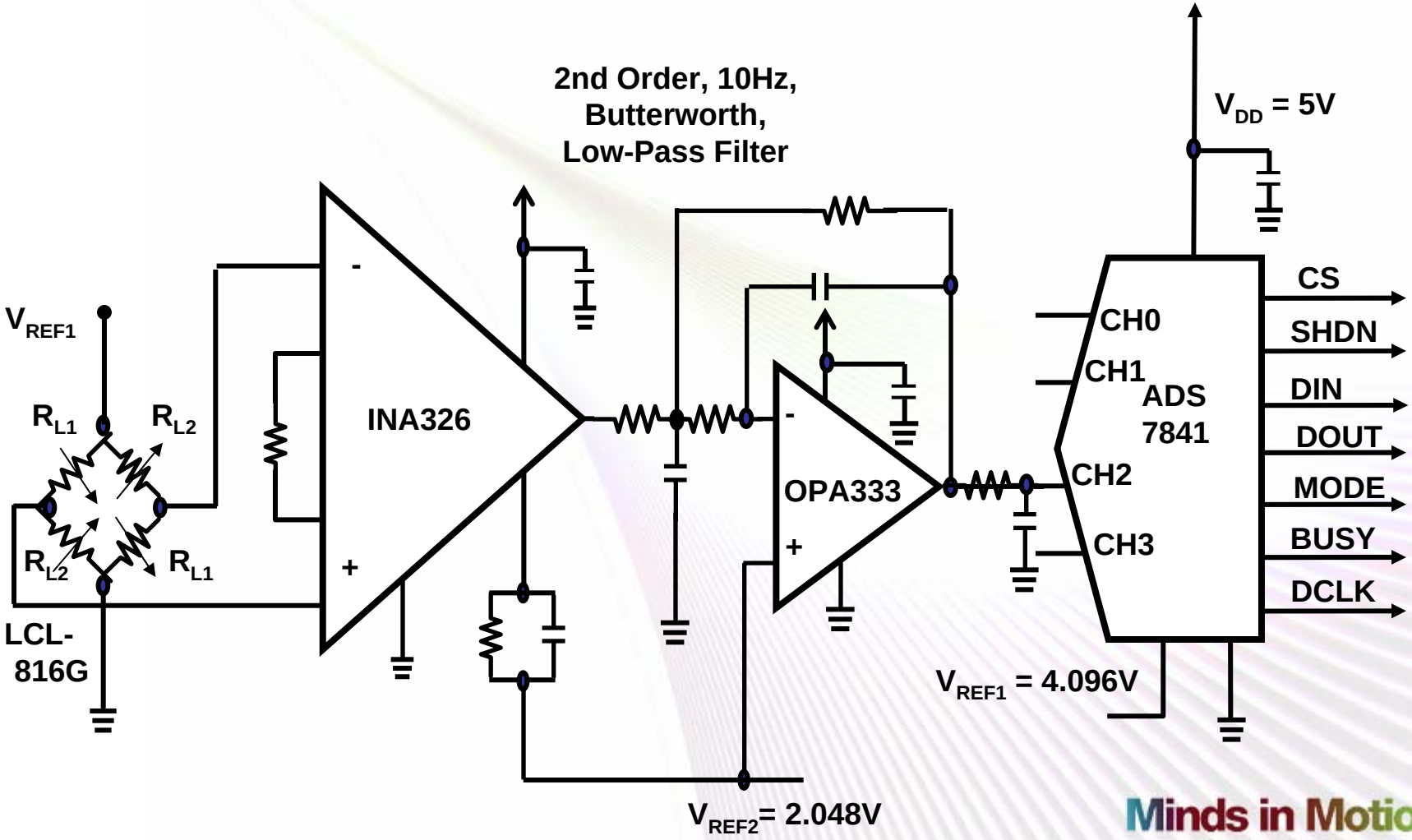
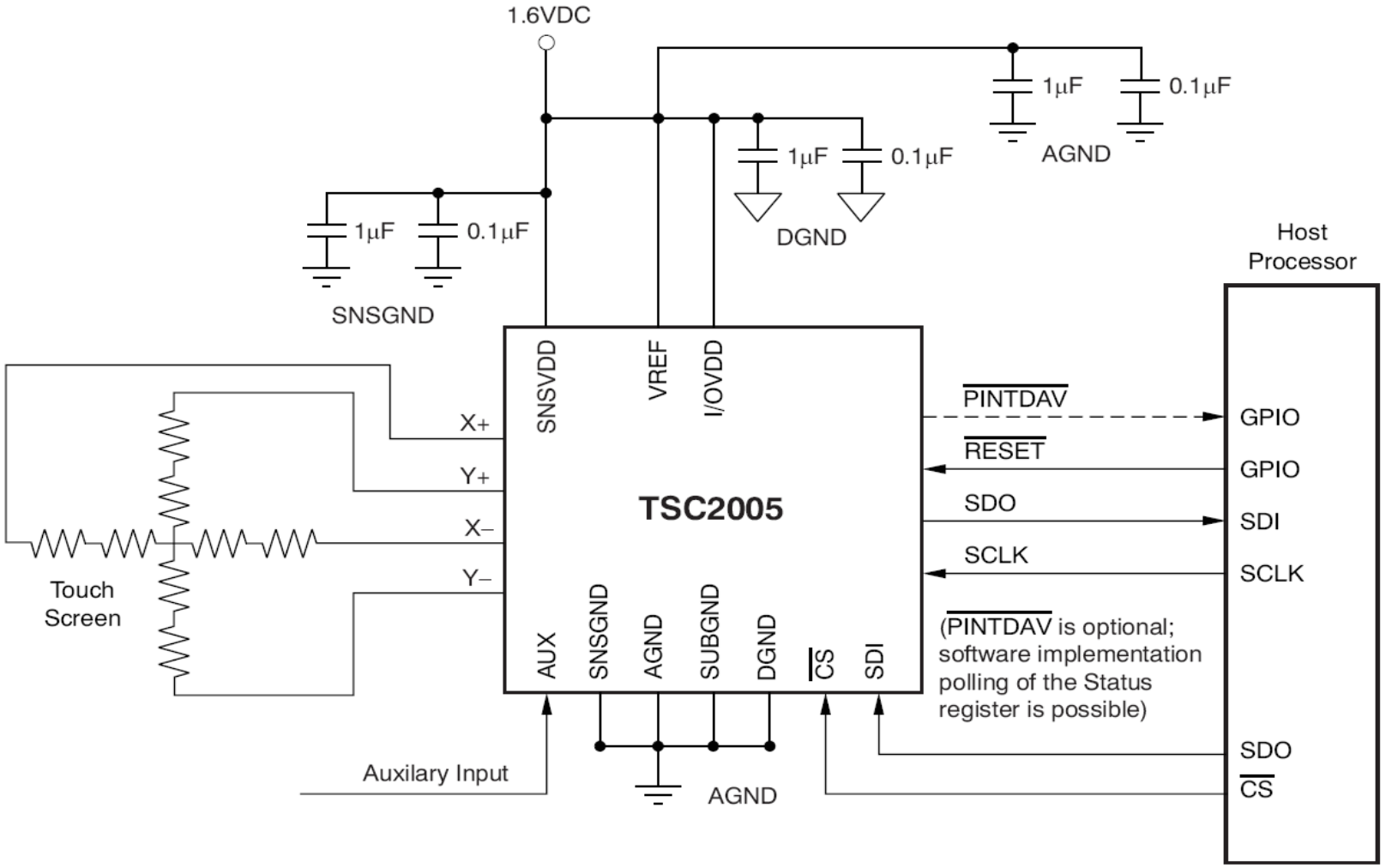
Load Cell Application



Touch-screen Controller



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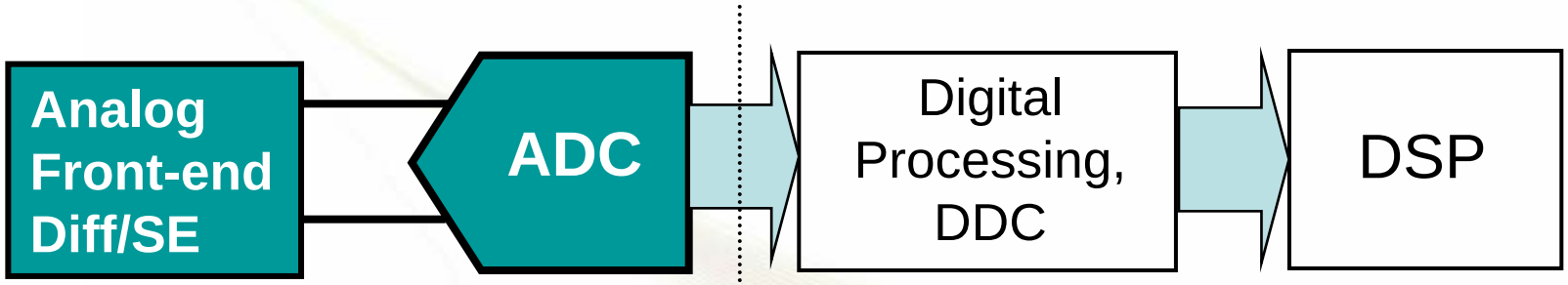
High Speed: Pipeline Topology

- Pipeline converters fit high-speed applications (5 MHz to 100+MHz).
- Applications where you typically find pipeline converters are:
  - Test and measurement instrumentation
  - Medical imaging
  - Radar systems
  - Data acquisition

System



Signal Conditioning
Band-pass Filtering
Gain to Match FSR of A/D
SE to Diff Conversion
DC-level Shifting

Conversion
Digitization
Mixing (alias)

Digital Processing
Frequency Translation
Decimation
Processing Gain (SNR)

DSP

Analog

Digital

What's the Application/EE ?

Time Domain

- Imaging (CCD)
  - Camcorders
  - Digital cameras
  - Scanners
  - RGB/comp. video
  - Test instrumentation
  - Medical
- Important Specs
  - SNR
  - Slew-rate/ tset
  - DNL
  - DC-accuracy/drift

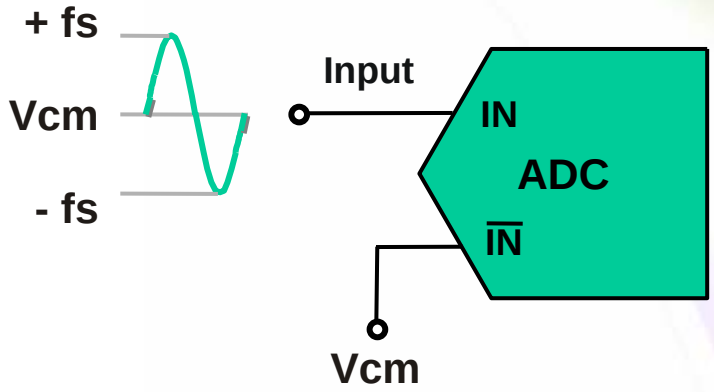
Frequency Domain

- Communications
  - Set-top boxes
  - Cable modems
  - Base stations
  - IF digitizers
  - GPS
  - Frequency synthesizers
- Important Specs
  - SFDR
  - ENOB
  - Analog input bandwith
  - Jitter

ADC Interface Solutions

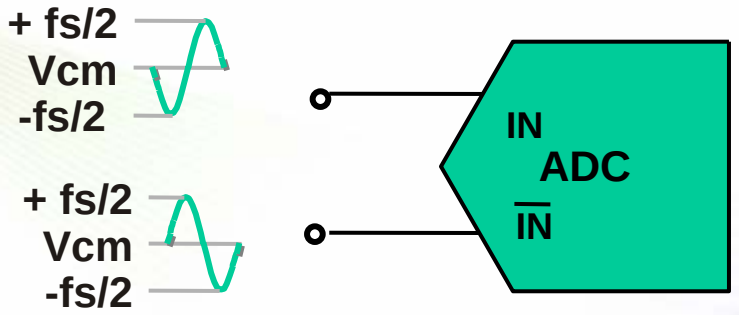
Principle Configuration Choices

Single-Ended Input (SE)



Requires full input swing from +fs to –fs.
2x the swing compared to differential.
Input signal at IN typically requires a common-mode voltage for bias.
Input IN\ also requires a Vcm for correct DC-bias.

Differential Input (DE)



Combined differential inputs result in full-scale input of +fs to –fs.
Each input only requires 0.5x the swing compared to single-ended.
Both inputs require a Vcm for correct DC-bias.

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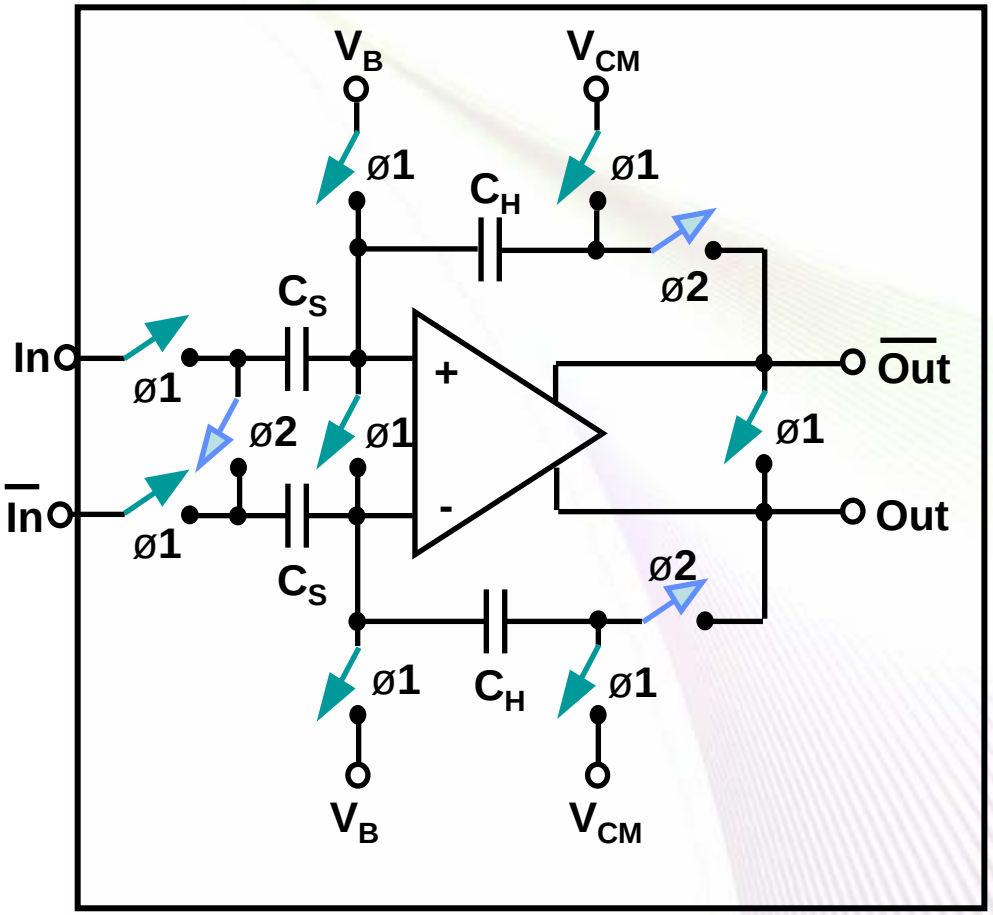
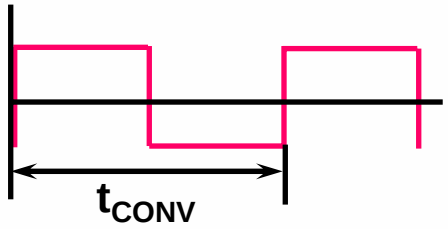
SE vs. DE Issues

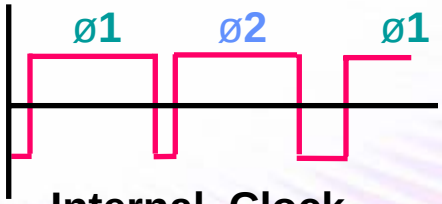
- *Single-ended Inputs (SEs)*
  - Degraded dynamic performance (larger FSR).
  - Common-mode voltage and op amp headroom may limit use for DC-coupling.
  - Best suited for **time-domain** applications.
- *Differential (DE)*
  - Optimized performance due to lower FSR, reduction of even-order and common-mode components.
  - Best for higher input frequencies (IFs).
  - More complex driver circuitry (consider diff-amps).
  - Best suited for **frequency-domain** applications.

HS-ADC Simplified Input Circuit





Input Clock



Internal Clock, non-overlapping

- Requires minimum clock frequency

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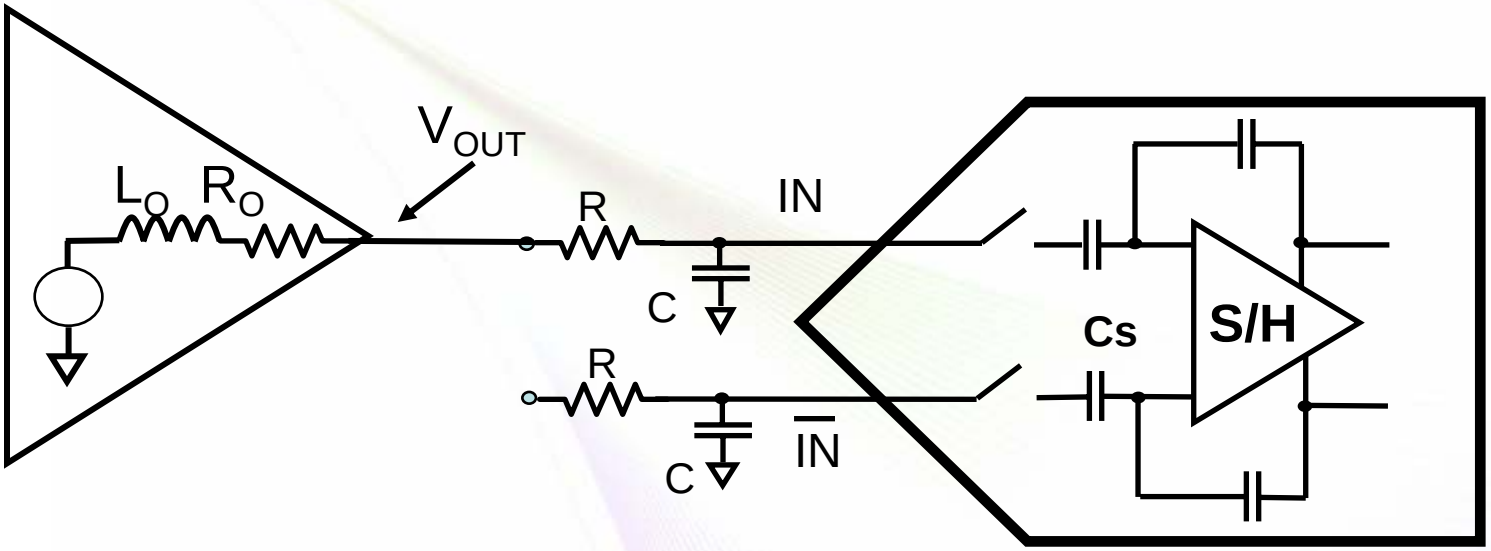
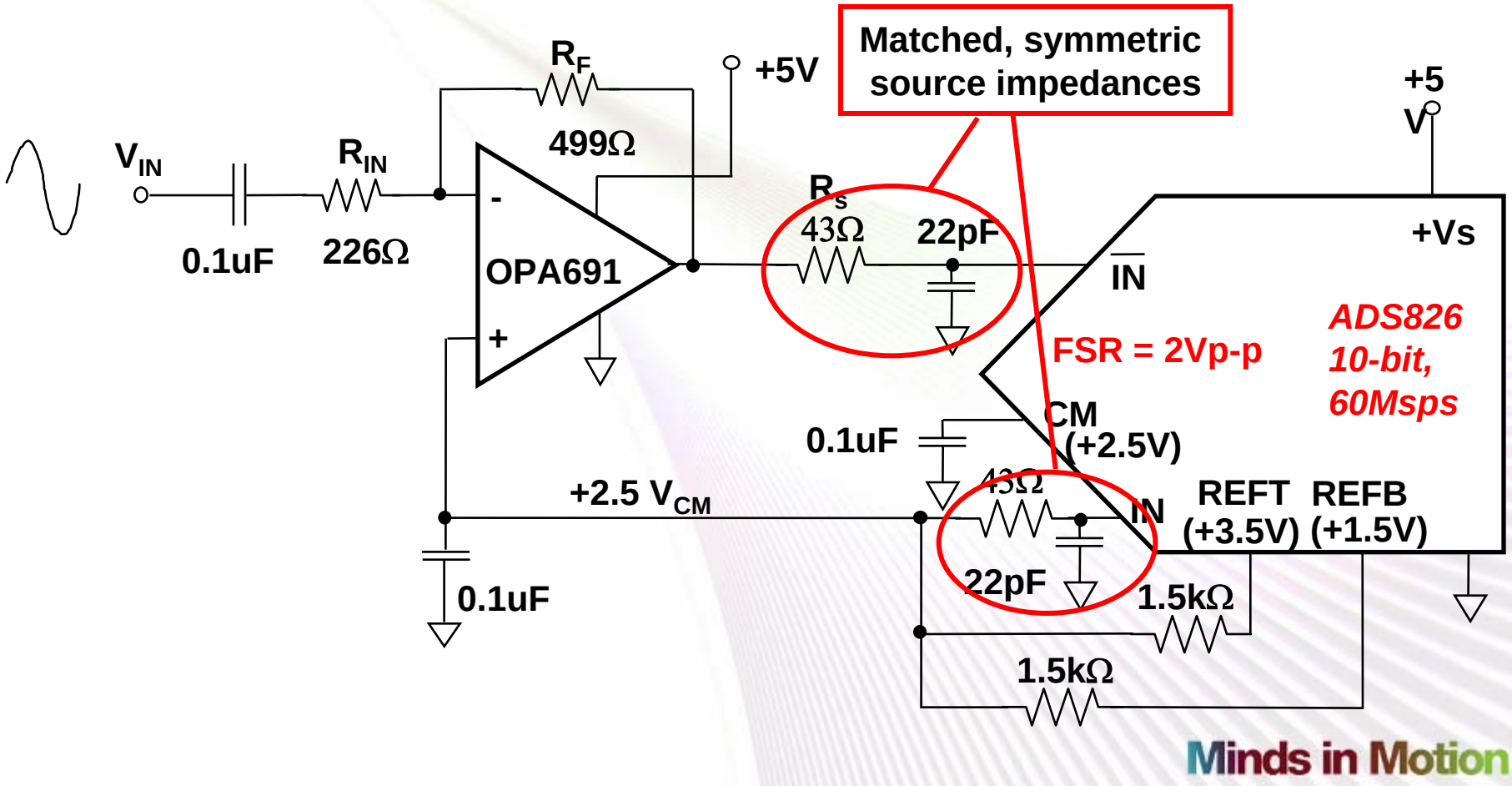
Driving Capacitive Input ADCs



- Due to Op amp's finite (R_O) output impedance, V_{OUT} will drop momentarily when cap load is switched.
- As the output recovers, ringing may occur, which results in increased settling time.
- Use external R: Isolates op amp output from capacitive load and improves settling.

SE: Interface

Single-ended, AC-coupled driver for single supply operation



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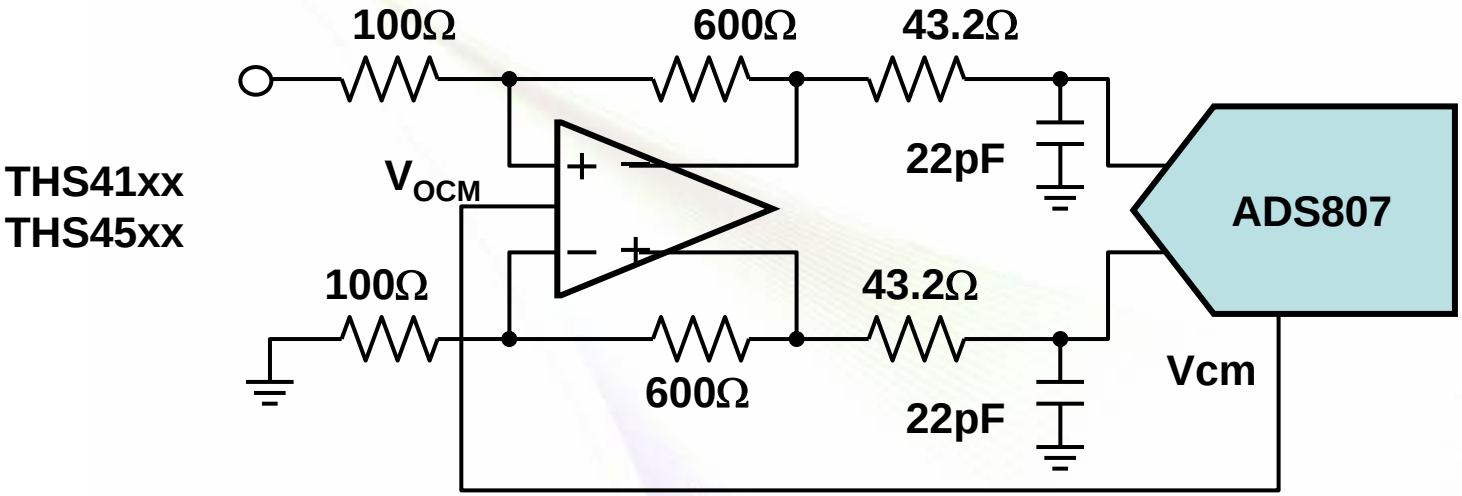
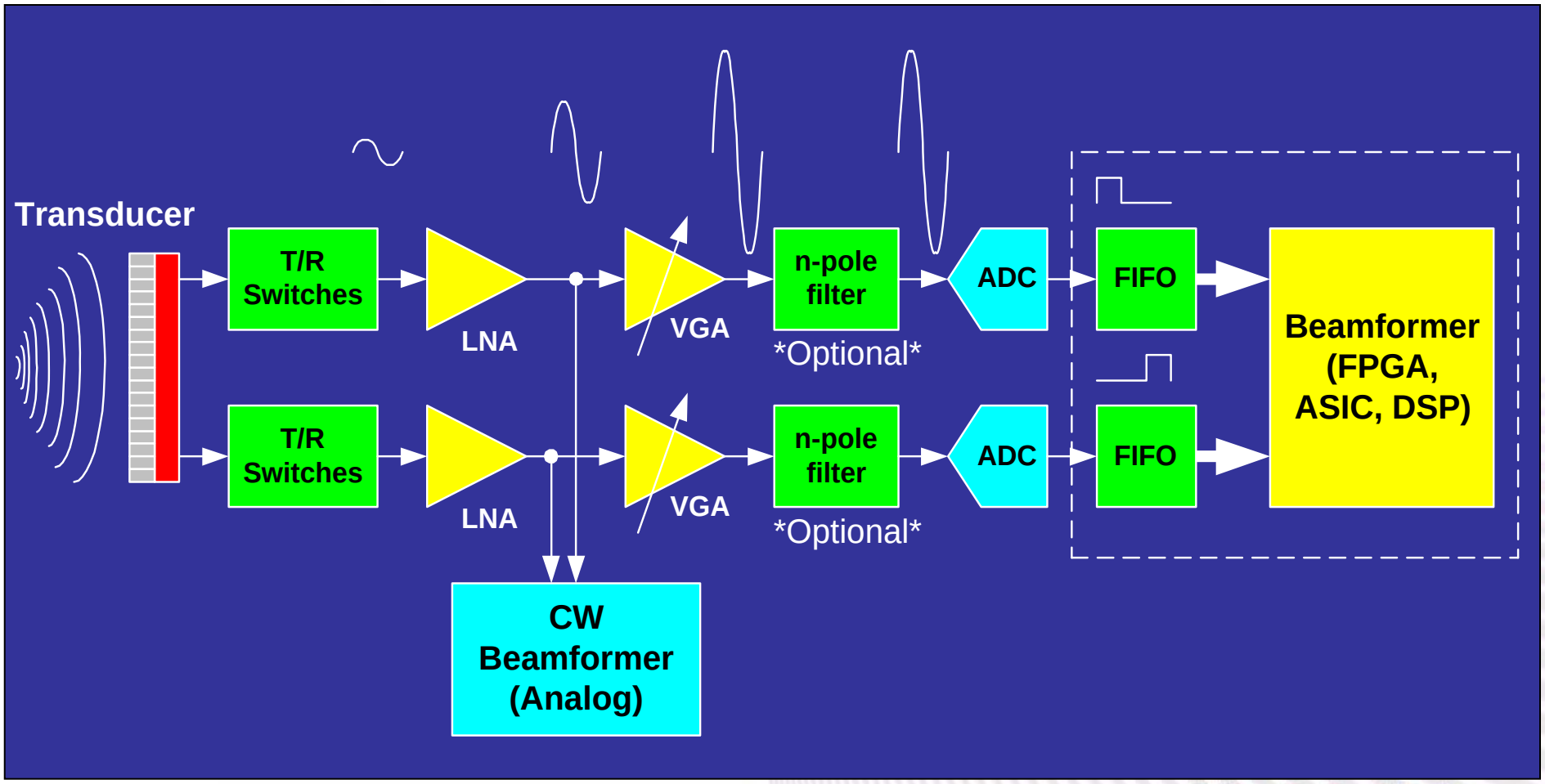
Differential ADC Driver



Ideal Baseband Driver Solution

- No transformer
- VCM matched to ADC
- Good even-order harmonic rejection
- Easily configured for gain and low-pass filter

Ultra-Sound Receive Chain



Conclusion
Delta-sigma, SAR, Pipeline ADCs

- Commonalities
  - Input stage
  - Input driving amplifier
- Differences
  - Sampling frequencies
- Appropriate Applications
  - Delta-Sigma: DC up to 30 ksps
  - SAR: 10 ksps up to 5 Msps
  - Pipeline: 1 Msps up to 500 Msps

TI Developer Conference
March 7-9, 2007 • Dallas, TX

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Real World Analog Solutions for Your Processor Applications

ADC: Delta-Sigma, SAR vs. Pipeline ADCs – When and Where to Use Them

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