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TMS320F28x Simulator Datasheet (v1.10)

FEATURES

- Integrated into the Code Composer Studio™
- Supports Pipeline Stall Analyzer on F28xx simulator
- Supports Full ISA for F2800
- Configurable Memory Simulation
- Cycle Accurate Simulation of CPU Hazards, On-Chip and External Memory
- Supports Memory Block Protection
- Supports external Data and Interrupt
 Simulation through Probe Points, Port
 Connect and Pin Connect on F28xx simulator

DESCRIPTION

 The TMS320F28x Instruction Set Simulator is available within the Code Composer Studio for TMS320F2000. This document was published earlier as TMS320C28x Instruction Set Simulator Technical Overview (SPRU608)

- The complete instruction set including the pipeline protection and memory block protection is modeled.
- Pipeline display plug-in provides a graphical display of instructions in various phases of the pipeline. This can be used for aggressive optimizations.
- The simulator can be configured to match the On-Chip SARAM spaces.
- The simulators for various memory configurations have been validated for correctness and cycle accuracy against hardware.
- External data inputs, not directly supported with the simulated peripherals, can be supported through the probe point or port connect feature(Code Composer Studio online help details the usage of probe point and port connect features).
- External control signals, like interrupts, can be modeled through the pin connect feature. (Code Composer Studio online help details the pins supported and the usage of pin connect feature)

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Summary of Architecture Features

Table 1. Architecture Features

FEATURE	F28xx	F283xx
Wait stated memory	Yes	No
Memory protection unit	Yes	No

Summary of Simulator Configurations

Table 2. Simulator Configuration

DEVICE SIMULATED	CODE COMPOSE STUDIO CONFIGURATION	CYCLE ACCURACY (1)	SPEED IN KCPS ⁽²⁾
F28xx Cycle Accurate Simulator	sim28xx.cfg	CPU Level	24
F283xx Simulator	simf283xx.cfg	CPU Level	952

Summary of Capabilities

Table 3. Capabilities of Simulator Configurations

CODE COMPOSER STUDIO CONFIGURATION	CYCLE ACCURACY	PROFILER	PIN CONNECT	PORT CONNECT
F28xx	Yes	Yes	Yes	Yes
F283xx	Yes	No	No	No

Pin Supported for Pin Connect

Table 4. Pins Supported

PIN NAME	F28xx	F283xx
INT1-INT14	Yes	No
DLOGINT	Yes	No
RTOSINT	Yes	No
NMI	Yes	No
EMUINT	Yes	No

Performance Numbers

Table 5. Performance Numbers

SIMULATOR CONFIGURATION	TEST CASE	KCPS
F28xx	GSMEFR	24
F283xx	GSMEFR	952

Measured against hardware using application suite.
Using GSMEFR application on 3.2 GHz PIV with 2 GB RAM running Windows® XP.



F283xx Simulator Cycle Accuracy

Table 6. F283xx Simulator Cycle Accuracy

Test Case	% Deviation
bdti_c28_lum.out	2.36
connor_c28_lum.out	1.11
dhry21_c28_lum.out	0.00
estone_c28_lum.out	1.39
pid16_c28_lum.out	0.62
pid32_c28_lum.out	0.00
pidiq_c28_lum.out	0.00
RS_c28_lum.out	-0.01
sea98_c28_lum.out	0.23

Glossary

TERM	DESCRIPTION
Cycle Accuracy	Correlation between cycles reported by simulator verses the real hardware.

Acronyms

ACRONYM	DESCRIPTION
CCS	Code Composer Studio
ISS	Instruction Set Simulator
RAM	Random Access Memory
KIPS	Kilo Instructions per Second

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