Application Note Achieve High SNR with the PGA855, Fully Differential Programmable-Gain Amplifier



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ABSTRACT

The PGA855 is a precision, wide-bandwidth programmable gain instrumentation amplifier with fully differential outputs optimized to drive high-performance analog-to-digital converters (ADCs) with fully differential inputs. The PGA855 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain-selection pins. The low-noise current-feedback front-end architecture offers excellent gain flatness, even at high frequencies, making the PGA855 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages up to ±40V beyond the power supply voltages. The PGA855 offers an excellent combination of AC performance and DC accuracy, making the PGA855 a versatile choice for a variety of sensors.

This application note shows the AC performance of the PGA855 driving the ADS127L11 and ADS127L21 delta-sigma ADCs. The focus of this document is on intrinsic noise, signal-to-noise ratio (SNR) and effective resolution performance. In particular, this application note provides guidelines of the analog filter selection and provides the performance of the PGA855 and ADS127Lx1 with different data rates and digital filter settings.

The document illustrates a step-by-step intrinsic noise analysis of the acquisition system, provides a calculator tool to estimate the system performance with different ADC digital filter and data rate settings, and shows the bench measurements of the PGA855 driving the ADS127Lx1.

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1 PGA855 and ADS127L21, 24-Bit, Delta-Sigma ADC Driver Circuit

Analog signal acquisition in industrial systems is a challenging problem. Sensor output signals often present full-scale signals in the millivolt range, requiring resolutions in the microvolt range or even nanovolt range. The system designer's challenge is optimizing the sensor amplifier front-end to achieve the best signal to noise performance. Hence, understanding and minimizing these sources of noise is essential.

The instrumentation amplifier (INA) and the programmable gain instrumentation amplifier (PGA) are essential in industrial acquisition systems. These components offer high accuracy, low noise signal-conditioning and level shifting, and versatile gain programmability. INAs and PGAs offer a high-impedance front-end and have evolved into excellent ADC drivers in the back-end, offering a complete integrated signal acquisition design. Applications include industrial analog input modules measuring a wide variety of bridge, pressure, and temperature sensors; data acquisition cards; surgical equipment; vibration analysis, and power metering/battery testing systems.

Figure 1-1 shows a circuit example for the PGA855 driving the ADS127Lx1, a fully-differential input, high resolution, wide-bandwidth, delta-sigma ADC.

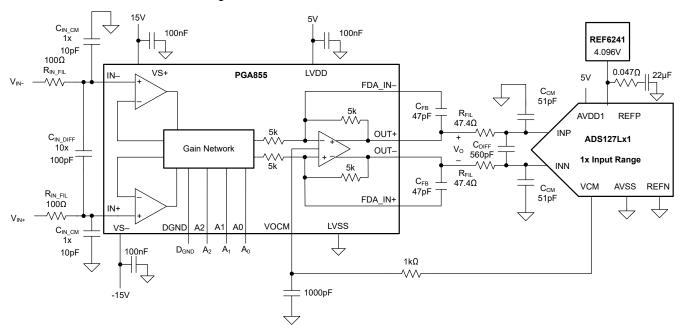


Figure 1-1. PGA855 and ADS127L21, 24-Bit, Delta-Sigma ADC Circuit

The PGA accepts single-ended or fully-differential input signals while driving the differential ADC inputs. Pincontrolled gains scale the input signal to the ADC input range. The super-beta input transistors offer a low input bias current, providing a very low input current noise density of 0.3pA/ \sqrt{Hz} , making the PGA855 a versatile choice for many sensor types.

The PGA855 offers independent input and output power supplies. In this example, ±15V input power supplies are used for the PGA input section, allowing a wide voltage input range. The output stage is powered with the ADC 5V power supply. The 5V output stage supply operation prevents overloading the ADC inputs during PGA overdrive conditions. The VCM output pin of the ADC drives the PGA855's VOCM pin setting the common mode voltage of the PGA outputs.

The goal of the circuit on Figure 1-1 is to provide a high level of SNR and total harmonic distortion (THD) performance for a given circuit bandwidth requirement. The effective bandwidth of the circuit is affected by the PGA855 analog front end bandwidth as well as the ADC digital filter.



2 PGA855 Analog Front-End Filters

The PGA855 analog-front-end circuit consists of three analog filters. Figure 2-1 shows the filters of the PGA855-ADS127Lx1 circuit.

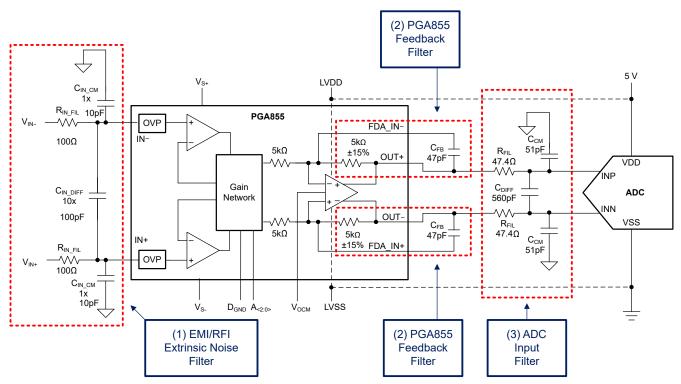


Figure 2-1. PGA855 Analog Filters

The first analog filter located at the input of the PGA helps reduce electromagnetic interference (EMI) and radio frequency interference (RFI) high-frequency extrinsic noise. This input filter can be customized per the application bandwidth and anti-aliasing requirements.

This circuit example uses a filter with the capacitor ratio of $C_{IN_DIFF} = 10 \times C_{IN_CM}$. Using the 10-to-1 ratio for differential capacitor C_{IN_DIFF} versus common-mode capacitors C_{IN_CM} offers good differential and common-mode noise rejection. This ratio of capacitor values also tends to be less sensitive to the tolerance variation and mismatch of the filter capacitors. When the C_{IN_DIFF} capacitor value is chosen to be 10 times larger than the common-mode capacitors, the resulting differential filter provides a corner frequency that is 20 times lower than the common-mode filter corner frequency. Therefore, differential signals are attenuated at a lower frequency than the common-mode signals. The instrumentation amplifier amplifies differential signals and rejects the common-mode voltage signals. Providing this ratio of capacitors helps to mitigate the effects due to the mismatch of the common-mode capacitors, where the asymmetric noise attenuation caused by the common-mode capacitor signals to insignificant levels. By simple inspection, derive Equation 1 and Equation 2 to calculate the corner frequencies:

EMI/RFI input filter differential-mode corner frequency:

$$f_{-3dB_DIFF} = \frac{1}{2\pi \times \left(R_{IN}_{FIL} + R_{IN}_{FIL}\right) \times \left(C_{IN}_{DIFF} + \frac{C_{IN}_{CM}}{2}\right)}$$
(1)

EMI/RFI input filter common-mode corner frequency:

$$f_{-3dB_CM} = \frac{1}{2\pi \times R_{IN}_{FIL} \times C_{IN}_{CM}}$$
(2)



(3)

Equation 1 provides an input differential filter f_{-3dB} corner frequency of 7.58MHz. When measuring bridge sensors with high-resistance, the sensor resistance can affect the corner frequency of the input filter.

The second filter helps to limit the PGA855 intrinsic noise contribution, and works as a low-pass anti-aliasing filter. Typically, the bandwidth of the feedback filter can be adjusted per the application bandwidth requirements. This filter is implemented with the feedback capacitor, C_{FB} , in parallel with the PGA855 output-stage 5k Ω feedback resistors forming a 1st order filter.

$$f_{-3dB_FB} = \frac{1}{2\pi \times R_{FB} \times C_{FB}}$$

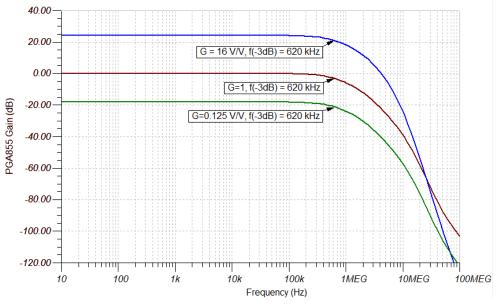
The PGA855 circuit bandwidth is limited by C_{FB} . In this example, C_{FB} is set to 47pF, in parallel with the output-stage 5k Ω feedback resistor providing a typical f_{-3dB} corner frequency of 677kHz.

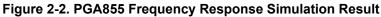
Note that the PGA855 internal fully differential amplifier output stage resistors, although precisely ratio-metrically matched among each other to provide very low gain error, can exhibit a ±15% absolute resistance over process and temperature variation, and this resistor variation must be taken in to account when implementing the noise filtering. The f_{-3dB} corner frequency for the feedback filter can vary in the range of approximately 589kHz to approximately 677kHz when accounting for the 5k Ω ±15% absolute resistance variation of the internal feedback resistors.

The third differential R-C-R filter at the ADS127Lx1 inputs serves two purposes. First, the filter provides a third pole to the overall filter response, thereby increasing the filter rolloff slope. The filter also works as a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise can degrade because of incomplete amplifier settling. The ADC input filter values are $R_{FIL} = 47.4\Omega$, $C_{DIFF} = 560$ pF, and $C_{CM} = 51$ pF. The ADS127Lx1 input precharge buffers significantly reduce the sample-and-hold input charge that raises the ADC input impedance to decrease gain error.

High-grade C0G (NP0) are used everywhere in the signal path (C_{IN_DIFF}, C_{IN_CM}, C_{FB}, C_{DIFF}, C_{CM}) for low distortion. Among ceramic surface-mount capacitors, the type of dielectric used in C0G (NP0) capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

The PGA855 analog front-end circuit, accounting for all three analog filters, provides a nominal f_{-3dB} bandwidth of 620kHz. On the high side of the internal $5k\Omega$ feedback resistor tolerance, the PGA855 f_{-3dB} bandwidth changes to 547kHz and the circuit maintains –0.1dB flatness to 85kHz. Figure 2-2 shows the TINA-TI simulated PGA855 AC frequency response.







3 ADS127Lx1 Delta-Sigma ADC and Digital Filter

The ADS127L11 and ADS127L21 is a family of wide-bandwidth, 24-bit, delta-sigma ($\Delta\Sigma$) ADCs offering an excellent combination of AC performance and DC precision. These $\Delta\Sigma$ ADCs offer configurable digital filters to optimize for wideband or low latency operation, allowing wideband ac performance or for data throughput dc signals. The ADS127L11 supports data rates up to 400kSPS using the wideband filter and up to 1067kSPS using the low-latency (sinc4) filter. The ADS127L21 supports data rates up to 512kSPS using the wideband filter and up to 1365kSPS using the low-latency (sinc4) filter. The ADS127L21 supports data rates up to 400kSPS using the wideband filter and up to 1365kSPS using the low-latency (sinc4) filter. The ADS127L21 supports data rates up to 512kSPS using the wideband and low latency filter options, it offers programmable infinite and finite impulse response (IIR and FIR) digital filters allowing custom filter profiles.

For a complete table of the available ADS127L21 and ADS127L11 digital filter (wideband, sinc4, sinc3, cascaded sinc3 + sinc1, and cascaded sinc4+sinc1) options, filter bandwidth specifications and noise performance, refer to the ADS127L21 and ADS127L11 device data sheets.

Table 3-1 shows an excerpt of the ADS127L21 sinc4 filter performance. In this example, the ADS127L21 is operated in high-speed mode, oversampling ratio, OSR = 64, sinc4 filter providing a data rate of 200kSPS. This corresponds to an input-referred noise of 5.53μ VRMS and a f_{-3dB} corner frequency of 45.5kHz for the sinc4 filter for these specific settings.

		.i – 4.000 v , ix input/								
DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	ADC Noise (E _{nADC}) (μVRMS)								
HIGH-SPEED MODE (f _{CLK} = 25.6MHz)										
1066.6	242.6	66.6								
833	182	24.5								
533.3	91.0	10.3								
400	45.5	8.06								
200	45.5	5.53								
100	22.75	3.89								
50	11.375	2.74								
25	5.687	1.93								
12.5	2.844	1.40								
6.25	1.422	0.995								
3.125	0.711	0.709								
	(kSPS) HIGH-SP 1066.6 833 533.3 400 200 100 50 25 12.5 6.25	(KSPS) (KHz) HIGH-SPEED MODE (f _{CLK} = 25.6MHz) 1066.6 242.6 833 182 533.3 91.0 400 45.5 200 45.5 100 22.75 50 11.375 25 5.687 12.5 2.844 6.25 1.422								

Table 3-1. ADS127L21 Sinc4 Filter Performance (VREF = 4.096V, 1x Input)



4 Approximate PGA855 Intrinsic Noise Analysis

This section illustrates the noise analysis of the PGA855 circuit example. The analysis includes the intrinsic noise sources of the instrumentation amplifier including the interaction of the input current noise of the device and source or sensor resistance.

4.1 Simplified Noise Model for the PGA855

The PGA855 architecture consists of a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, fully differential amplifier output stage. Eight preprogrammed binary gains, from 0.125V/V to 16V/V are selectable using gain-select pins A0, A1, and A2. Each amplifier in the circuit has a corresponding amplifier voltage noise and current noise contribution. In addition, each resistor in the gain resistor network has a thermal noise contribution element. Figure 4-1 shows a functional block diagram for the PGA855 and the noise sources.

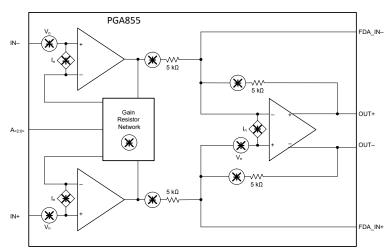


Figure 4-1. Noise Sources for PGA855

In the case of the PGA855, the voltage noise contribution of the internal amplifiers and the thermal noise contributions from the internal gain resistor network are lumped into a single voltage noise source e_{NI} . The input stage amplifier current noise is kept as a separate current noise source at the input of the PGA855. Since the resistor network changes of each gain setting, the PGA855 data sheet provides separate referred-to-input (RTI) voltage noise density specifications for each gain setting from 0.125V/V to 16V/V respectively. Figure 4-1 shows the simplified noise model of the PGA855.

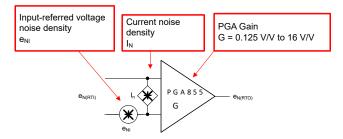


Figure 4-2. Simplified Noise Model for PGA855

The simplified PGA855 model uses a single stage model; where all the noise specifications are referred to the amplifier input. The input current noise remains constant across all gains. To refer the noise to the device output, the designer needs to multiply the input-referred noise by the PGA gain. Equation 4 provides the calculation of the output-referred noise, $e_{N(BTO)}$ as a function of the PGA gain, G.

$$e_{N(RTO)} = e_{NI} \times G$$

6

(4)



4.2 PGA855 Spectral Noise Density vs Frequency

Figure 4-3 shows the input referred voltage noise spectral density curve for the PGA855 for each gain setting.

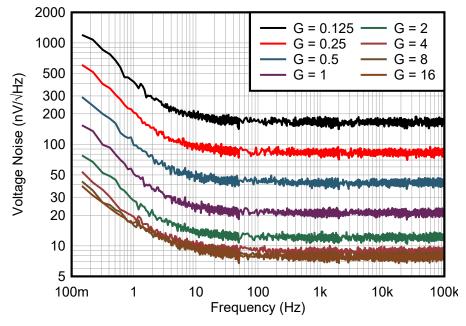


Figure 4-3. Voltage Noise Spectral Density of PGA855

The spectral noise density plot has two regions: the 1/f noise region and the broadband noise region. The left side of the spectral noise density plot, shows the 1/f noise, also known as flicker noise. 1/f noise is a category of noise in the low frequency range, typically at frequencies lower than 1kHz for most devices, and only showing at lower frequencies than 10Hz for the PGA855. The broadband noise region, at the right side of the curve, has a flat spectral density.

To convert the voltage spectral noise density (nV/\sqrt{Hz}) to RMS voltage noise, one must square the voltage spectral noise density, integrate across the desired bandwidth, and calculate the square root of the result. Equation 5 shows the calculation to convert the spectral noise into RMS noise.

$$E_{n}(V_{rms}) = \sqrt{\int_{f_{L}}^{f_{H}} (e_{n}(V/\sqrt{Hz}))^{2} df}$$
(5)

The following sections detail how to calculate the total PGA RMS noise associated with the 1/f noise region and the broadband noise region.

4.3 PGA855 Effective Noise Bandwidth

Before calculating the RMS noise, note the noise bandwidth of the circuit is not the same as the signal bandwidth given by the filter corner, therefore the noise bandwidth must be corrected. The amount of bandwidth correction depends on the filter order.

The effective noise bandwidth (ENBW) is the bandwidth of a designed for rectangular filter that allows the same amount of power to pass, as the cumulative bandwidth of the analog filters in the circuit. Also, the ENBW is the bandwidth of a rectangular filter, which produces the equivalent integrated noise power as that of the actual filters in the design. However, the frequency response of the analog filter has a roll-off low-pass response with the slope as shown in Figure 2-2.

One method to calculate a low-pass filter's ENBW is to calculate the noise curve using the direct-integration method of Equation 5. Alternatively, use Equation 6, which relates the Nth order low-pass filter response to the ENBW:

$$ENBW_{PGA855} = K_n \times f_{-3dB}$$

(6)



In Equation 6, the K_n constant is the brick-wall correction factor for a given Nth order low-pass filter. The K_n factor is 1.57 and 1.22 for a 1st order and 2nd order low-pass filter respectively. In this circuit, the PGA855 includes three low-pass filters, but the dominant pole occurs at 677-kHz, while the other poles occur at much higher frequencies; hence, the response can be roughly approximated to a 2nd order filter with a K_n correction factor of 1.22. For more information about how this formula was derived, see the TI Precision Labs training series on operational amplifier noise (Op-Amp Noise: Calculating RMS Noise).

The effective noise bandwidth of the system can be approximated if either Equation 7, or Equation 8, is true:

$$If f_{-3dB(ADC)} \le f_{-3dB(PGA855)} \to ENBW_{System} \cong f_{-3dB(ADC)}$$
(7)

If
$$f_{-3dB(ADC)} \ge 10 \times f_{-3dB(PGA855)} \rightarrow ENBW_{System} \cong ENBW_{PGA855}$$
 (8)

Note that in Equation 8, the system ENBW can be approximated to the PGA855 ENBW, but not the PGA855 circuit cutoff frequency.

If neither Equation 7 or Equation 8 is true, such that $f_{-3dB(ADC)}$ is between $f_{-3dB(PGA855)}$ and 10 × $f_{-3dB(ADC)}$, determine the combined system bandwidth using integration or other numerical methods.⁽²⁾

In this circuit, the bandwidth of the PGA855 front end is 677kHz typical, while the f_{-3dB} corner frequency of the ADS127L21 digital filter is 45.5kHz. Therefore, the system ENBW is limited by the ADC sinc4 digital-filter. Hence, an ENBW of the system of 45.5kHz can now be used to calculated the noise contribution of the analog front end circuit.

4.4 PGA855 Low Frequency (1/f) Noise Calculation

To calculate the 1/f noise contribution of the PGA855, obtain the noise density at the lowest given frequency on the voltage spectrum noise density curve (e_{nf}), and the lowest frequency (f_L) from Figure 4-3. The upper cutoff frequency f_H is set to the ENBW of 45.5kHz. Equation 9 calculates the 1/f noise normalized to 1Hz:

$$e_{nnormal} = e_{nf} \times \sqrt{f_L}$$
(9)

Equation 10 provides the total RMS noise from the 1/f region in μ VRMS. Table 4-1 shows the calculation results for the referred-to-input (RTI) 1/f noise.

$$E_{n1/f(RTI)} = e_{nnormal} \times \sqrt{\ln\left(\frac{f_H}{f_L}\right)}$$
 (10)

PGA GAIN (V/V)	f _L (Hz)	f _H (Hz)	e _{nf} (nV / √Hz)	e _{nnormal} (nV / √Hz)	E _{n1/f(RTI)} (µVRMS)
0.125	0.2	45500	1000	447.2	1.57
0.250	0.2	45500	500	223.6	0.79
0.50	0.2	45500	250	111.8	0.39
1	0.2	45500	130	58.1	0.20
2	0.2	45500	70	31.3	0.11
4	0.2	45500	45	20.1	0.07
8	0.2	45500	37	16.5	0.06
16	0.2	45500	35	15.7	0.05

Table 4-1. PGA855 Input-Referred 1/f Noise

4.5 PGA855 Voltage Broadband Noise

To calculate the broadband noise contribution of the PGA855, multiply the square-root of the PGA855 noise bandwidth with the input-referred voltage noise density (e_{NI}) specification. The PGA855 data sheet provides the broadband noise density at 1kHz as a function of the PGA gain on the electrical characteristics table.

Equation 11 solves the RTI broadband noise and Table 4-2 shows the calculated broadband noise contribution of the PGA855 as a function of gain.

$$E_{nBB(RTI)} = e_{ni} \times \sqrt{ENBW}$$

(11)

Table 4-2. PGA855 Input-Referred Voltage Broadband Noise							
PGA GAIN (V/V)	e _{ni} (nV / √Hz)	f _H (Hz)	Ε _{nBB(RTI)} (μVRMS)				
0.125	168	45500	35.8				
0.25	84	45500	17.9				
0.5	42	45500	9.0				
1	21.6	45500	4.6				
2	12.6	45500	2.7				
4	8.6	45500	1.8				
8	8	45500	1.7				
16	7.8	45500	1.7				

4.6 PGA855 Current Noise and Source Resistance

The PGA855 input current noise density interacts with the source resistance generating voltage noise. Consider an example where a bridge sensor is measured at the inputs of the amplifier. The resistive bridge sensor has a thermal noise contribution, and the combined resistance of the filter and bridge sensor scales with the PGA input current noise density.

Figure 4-4 shows the derivation of the equivalent input source resistance in the circuit:

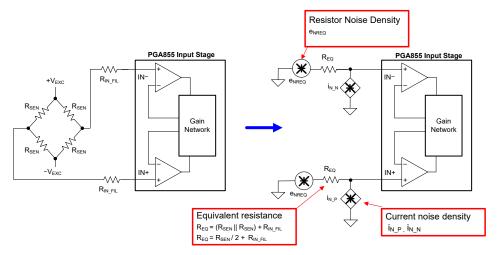


Figure 4-4. PGA855 Current Noise and Source Resistance

The circuit at the right of Figure 4-4 shows the simplified PGA855 noise model, where the equivalent input resistance (R_{EQ}) has a thermal noise density (e_{NR}) contribution, and the PGA input current noise density ($I_{N_{-}P}$, $I_{N_{-}N}$) interacts with R_{EQ} .

 R_{EQ} is a function of the bridge sensor resistance (R_{SEN}) and the input filter resistance (R_{IN_FIL}). Equation 12 solves for the equivalent input resistance at each input terminal of the PGA855:

$$R_{EQ} = (R_{SEN} \mid R_{SEN}) + R_{IN_{FIL}} = \frac{R_{SEN}}{2} + R_{IN_{FIL}}$$
(12)

Equation 13 provides the resistor thermal noise spectral density at each input terminal of the PGA855, where T is the absolute temperature in degrees Kelvin, and k is Boltzman's constant, 1.3807 x 10^{-23} Joule/°K:

$$e_{N_{REQ}} = \sqrt{4 \times k \times T \times R_{EQ}}$$
(13)

The equivalent source resistance interacts with the PGA855 current noise density, producing a voltage noise at the input of the instrumentation amplifier. Equation 14 calculates the resulting noise at each input terminal of the PGA855:

$$e_{iN} = i_N \times R_{EQ} \tag{14}$$

The total current and resistor noise is computed by combining the resistor thermal noise and current noise components at each amplifier input terminal, using the root-sum-of-squares. Equation 15 provides the total current and resistor noise density:

$$e_{iN_R} = \sqrt{\left(2 \times e_{iN}^2 + 2 \times e_{N_REQ}^2\right)}$$
(15)

Equation 16 calculates the RTI current and resistor noise as a function of the effective noise bandwidth in μ VRMS:

$$E_{iN R} = e_{iN R} \times \sqrt{ENBW}$$
(16)



Table 4-3 shows the RTI current and source resistance noise of the PGA circuit, for $R_{SEN} = 2 k\Omega$, $R_{IN_{FIL}} = 100\Omega$, and ENBW = 45.5kHz. The resistor and current noise contribution at the input remains constant with PGA gain. When referring this input noise contribution to the output, the input noise needs to be multiplied by the PGA gain.

i _N (pA / √Hz)	R _{EQ} (Ω)	e _{N_REQ} (nV / √Hz)	e _{iN} (nV / √Hz)	Ε _{iN_R(RTI)} (μVRMS)						
0.3	1.1 k	4.26	0.33	1.29						

Table 4-3. PGA855 Input-Referred Current and Source Resistance Noise
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4.7 PGA855 Total Noise

Calculate the PGA855 total noise by combining the 1/f voltage noise, voltage broadband noise, current noise and source resistance noise using the root-sum-of-squares (RSS). Equation 17 solves for the total referred-to-input PGA855 broadband noise and Equation 18 provides the total referred-to-output noise. Table 4-4 shows the total noise contribution of the PGA855 as a function of gain in μ VRMS.

$$E_{nPGA855(RTI)} = \sqrt{E_{n1/f(RTI)}^{2} + E_{nBB(RTI)}^{2} + E_{iN_{R}}^{2}}$$
(17)

 $E_{nPGA855(RTO)} = E_{nPGA855(RTI)} \times G$

(18)

Table 4-4.	PGA855 Total I	Noise
Engr/RTI)		EnDCARE

PGA GAIN (V/V)	E _{n1/f(RTI)} (µVRMS)	Ε _{nBB(RTI)} (μVRMS)	E _{iN_R(RTI)} (μVRMS))	E _{nPGA855(RTI)} (μVRMS)	E _{nPGA855(RTO)} (µVRMS)
0.125	1.57	35.8	1.29	35.89	4.49
0.25	0.79	17.9	1.29	17.98	4.50
0.5	0.39	9.0	1.29	9.06	4.53
1	0.20	4.6	1.29	4.79	4.79
2	0.11	2.7	1.29	2.98	5.96
4	0.07	1.8	1.29	2.24	8.97
8	0.06	1.7	1.29	2.14	17.11
16	0.05	1.7	1.29	2.10	33.67

5 PGA855 and ADS127Lx1 System Noise

Equation 19 computes the total noise in the system, as a function of the PGA855 noise, ADC noise and ADC voltage reference noise. The ADC circuit uses the REF6241 4.096V voltage reference. This reference includes an integrated wide bandwidth buffer that allows the REF6241 to directly drive the switched-capacitor reference input of the ADS127L21. The REF62xx High-Precision Voltage Reference With Integrated ADC Drive Buffer data sheet specifies a total integrated noise of 5 μ VRMS when using a 22 μ F bypass capacitor at frequencies higher than approximately1kHz. The uncorrelated noise sources are combined by computing the root-sum-of-squares:

$$E_{nSystem(RTO)} = \sqrt{E_{nPGA855(RTO)}^2 + E_{nADC}^2 + E_{nREF}^2}$$
(19)

Equation 20 converts RMS noise to effective resolution.

System Effective Resolution (Bits) =
$$\log_2 (FSR / E_{nSystem(RTO)})$$
 (20)

Where FSR is the full-scale range:

• FSR = 2 · VREF (1x input range)

Effective resolution is a figure of merit frequently used to specify the performance of delta-sigma ADCs. This specification is different than the effective number of bits (ENOB), which is a function of both noise and THD.

Equation 21 converts RMS noise to SNR.

System SNR (dB) =
$$20 \times \log \left(\frac{\text{FSR}(V_{\text{RMS}})}{E_{\text{nSystem}(\text{RTO})}(V_{\text{RMS}})} \right)$$
 (21)

Table 5-1 shows the PGA855 and ADS127L21 total system noise calculations vs PGA gain.

PGA GAIN (V/V)	PGA855 Noise E _{nPGA855 (RTO)} (µVRMS)	ADC Noise E _{nADC} (μVRMS)	Reference Noise E _{nREF} (μVRMS)	System Noise E _{nSystem(RTO)} (µVRMS)	System Effective Resolution (Bits)	System SNR (dB)
0.125	4.49	5.53	5.00	8.70	19.84	110.45
0.25	4.50	5.53	5.00	8.71	19.84	110.44
0.5	4.53	5.53	5.00	8.72	19.84	110.42
1	4.79	5.53	5.00	8.86	19.82	110.29
2	5.96	5.53	5.00	9.55	19.71	109.64
4	8.97	5.53	5.00	11.66	19.42	107.90
8	17.11	5.53	5.00	18.66	18.74	103.82
16	33.67	5.53	5.00	34.49	17.86	98.48

Table 5-1. Total System Noise





6 PGA855 and ADS127Lx1 SNR and Noise Calculator

The *PGA855 and ADS127Lx1 SNR and Noise Calculator* is a spreadsheet developed using Microsoft[®] Excel[®] that provides an estimate of the overall intrinsic noise performance of the acquisition system.

The tool calculates the noise contribution of the sensor resistance, PGA855, ADS127Lx1 ADC, REF6241 voltage reference and provides an estimate of the overall system noise bandwidth, SNR and effective resolution based on the data sheet noise specifications.

The delta-sigma ADC provides a trade-off between the output data rate and acquisition system bandwidth, against noise performance. The calculator facilitates selecting the ADC filter settings, and data rate or filter bandwidth, depending on the application required resolution, and sensor resistance.

The circuit designer enters the PGA855 circuit bandwidth, the RMS reference noise contribution at the ENBW, and selects the ADS127Lx1 digital filter settings and data rate. An optional field is available to enter the sensor equivalent resistance at each PGA855 input. Figure 6-1 shows the noise calculator inputs:

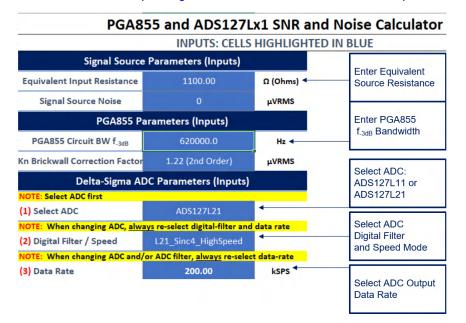
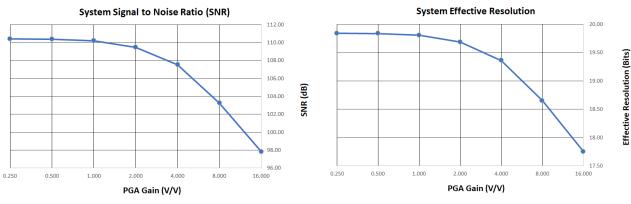


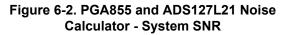
Figure 6-1. PGA855 and ADS127Lx1 Noise Calculator - Inputs

The calculator generates a plot of the system SNR and system effective resolution. Figure 6-2 shows the calculated SNR (dB) vs PGA gain in V/V, and Figure 6-3 shows the calculated system effective resolution in bits vs PGA gain in V/V.





High-Speed Mode, Sinc4, OSR = 64, Data Rate 200 kSPS



High-Speed Mode, Sinc4, OSR = 64, Data Rate 200 kSPS

Figure 6-3. PGA855 and ADS127L21 Noise Calculator - System Effective Resolution

The PGA855 and ADS127Lx1 SNR and Noise Calculator also generates a table with an estimate of the equivalent intrinsic noise of the acquisition system in μ VRMS, referred to the input of the PGA855 (RTI) or to the output of the PGA855 (RTO). In addition, it provides a separate table showing the noise contribution of the PGA855 circuit stand-alone, and the source or sensor noise contribution. Figure 6-4 and Figure 6-5 show a table with results as displayed in the tool, when selecting Sinc4 filter at 200-kSPS with R_{EQ} = 1.1k Ω .

n RT se MS)	Gain 'V)	No	m RTO bise RMS)	System (df		Effective Resolutic (Bits)
50	25	8.	70	110.	45	19.84
32	50	8.	70	110.	44	19.84
4	00	8.	72	110.	42	19.84
6		8.	86	110.	29	19.82
7		9.	54	109.	64	19.71
1	£	11	.66	107.	90	19.42
3	1	18	.65	103.	82	18.74
5	6	34	.47	98.4	19	17.86

High-Speed Mode, Sinc4, OSR = 64, Data Rate 200 kSPS

Figure 6-4. PGA855 and ADS127L21 - Noise Calculator, System Noise and Bandwidth

PGA855 Noise Contibution (Results) Req Noise Contibution RTI PGA855 RTI PGA855 Total Source RTO Reg Noise Req Noise PGA Gain Total Noise **RTO** Noise Noise (each Input) (Combined In+/In (V/V)(µVRMS) (µVRMS) (µVRMS) (nV/VHz) (nV/VHz) 0.125 35.84 8.65 0.16 4.26 6.02 0.250 17.92 4.48 0.32 tal Source 0.64 0.500 8 96 4.48 **RTI** Noise (µVRMS) 4.61 4.61 1.28 1 2.69 5.38 2.57 1.28 2 4 1.84 7.35 5.13 8 1.71 13.67 10.26 16 1.67 26.66 20.53 REF Noise @ Noise BW 4.911 **uVRMS**

High-Speed Mode, Sinc4, OSR = 64, Data Rate 200 kSPS

Figure 6-5. PGA855 and ADS127L21 Noise Calculator, PGA855 Noise Contribution

Note

The PGA855 calculator only accounts for the PGA855 and ADC intrinsic circuit noise to provide an estimate of noise performance based on the typical data sheet specifications. When measuring the SNR performance of the PGA-ADC acquisition system on the bench, the circuit designer must use a high-performance, very low noise, low distortion source. The bench measurement is sensitive to extrinsic noise sources, source distortion, as well as jitter in the signal.



7 PGA855 and ADS127Lx1 FFT Measured Performance

Figure 1-1 shows a block diagram for the PGA855-ADS127L21 circuit as tested on the bench.

A 1-kHz sine-wave test signal generates the SNR and THD data. The signal source must provide better noise performance and lower distortion than the circuit under test. The bench set up uses a low-pass filter between the signal source and PGA855 circuit to help reduce extrinsic noise injected into the circuit. The amplitude is adjusted to provide a –0.2-dBFS output from the ADC.

The bench set up uses an external low-jitter clock source of 25.6MHz as shown on Figure 7-1 to obtain a 200 kSPS data rate.

The PGA855 circuit is configured as shown in Figure 7-1. An equivalent resistance of $1k\Omega$ is added in series between the signal source and PGA855 circuit, to account for the noise contribution of the $2k\Omega$ bridge sensor resistance. The ADS127Lx1 GUI is configured with the ADC input buffers enabled and high-reference range selected.

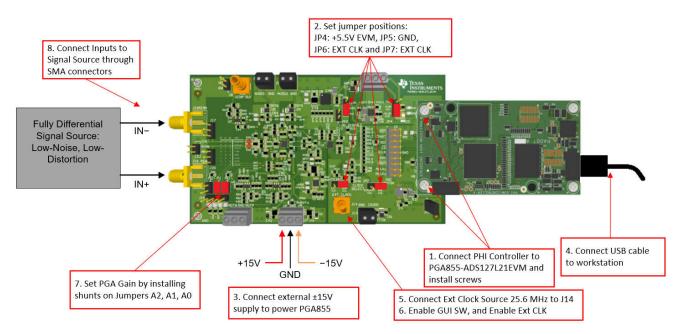


Figure 7-1. PGA855-ADS127L21 Bench Test

Table 7-1 lists the ADC settings, reference voltage on the PGA855-ADS127L21 bench measurements.

Table 7-1. PGA855-ADS127L21 Measurement Parameters					
PARAMETER	VALUE				
Input voltages (V _{PP} , differential)	20V, 16V, 8V, 4V, 2V, 1V, 0.5V, 0.25V				
ADC reference voltage	4.096				
Data rate	200.0 kSPS, OSR = 64				
Test frequency	1 kHz				
THD (gain = 1)	< –120dB typical				
SNR (gain = 1, wideband filter)	> 108dB typical				
SNR (gain = 1, sinc4 filter)	> 110dB typical				

Table 7-1. PGA855-ADS127L21 Measurement Parameters

Table 7-2 shows the SNR measurement of the PGA855 driving the ADS127L21 delta-sigma ADC using a sinc4 or wideband filter at 200kSPS. At gain = 1, the design achieves a 108.1-dB SNR for the wideband filter and 110.1-dB SNR for the sinc4 filter.



Table 7-2. PGA855 and ADS127L21 Calculated and Measured Performance Summary							
		WIDEBAN	D SNR (dB)	SINC4 SNR (dB)			
PGA GAIN (V/V)	INPUT (V _{PEAK})	Calculated	Measured	Calculated	Measured		
0.125	20	108.5	106.0 ⁽¹⁾	110.5	107.6 ⁽¹⁾		
0.25	16	108.4	108.4	110.4	110.4		
0.5	8	108.4	108.4	110.4	110.4		
1	4	108.3	108.1	110.3	110.1		
2	2	107.5	107.2	109.6	109.3		
4	1	105.5	105.0	107.9	107.1		
8	0.5	101.2	100.6	103.8	103.0		
16	0.25	95.7	95.0	98.5	97.2		

(1) The input signal amplitude is limited by the allowed input linear range of the PGA855 circuit at gain of 0.125, affecting the measured SNR.

Figure 7-2 and Figure 7-3 show the respective 1-kHz, full-scale FFT plots for the wideband and sinc4 filters at gain = 1. Because of the frequency roll-off of the sinc4 filter, SNR performance improves by an average of 2dB compared to the wideband filter. The filters provide identical THD results at -120-dB typical.

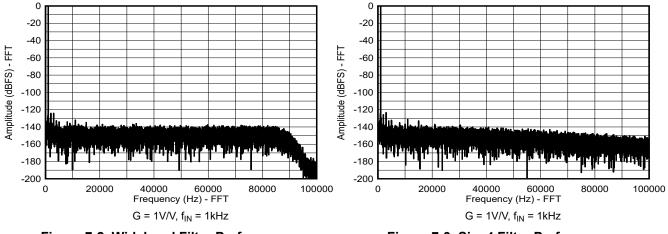


Figure 7-2. Wideband Filter Performance

Figure 7-3. Sinc4 Filter Performance

8 Summary

This document provides the information to assist the design engineer in implementing a low-noise, high-resolution, acquisition system with the PGA855-ADS127Lx1 according to the specific application needs.

The delta-sigma ADC provides a trade-off between the output data rate versus the system bandwidth and noise performance. The PGA855-ADS127Lx1 noise calculator provides an estimate of the intrinsic noise and SNR performance of the acquisition system, facilitating the design for data rate and digital filter settings selection per the bandwidth and resolution requirements.

9 References

- 1. Texas Instruments, Op-Amp Noise: Calculating RMS Noise, video training series.
- 2. Texas Instruments, ADC Noise: Calculating Amplifier + ADC Total Noise, video training series

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