Application Report
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# Using LVCMOS Input to the CDCM6100x

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**ABSTRACT**

This application report is a general guide for using LVCMOS inputs to the CDCM6100x series of ultra-low jitter clock generators from Texas Instruments. This document explains the basic connectivity of LVCMOS inputs to the CDCM6100x and recommends several methods for using the device that ensure proper operation.

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## 1 Introduction

A phase-locked loop (PLL) is a closed-loop system that generates a signal that is related to the frequency and phase of an input reference signal. Typically, a PLL involves locking the signal output (derived from a high-Q device) to the signal input (usually derived from a low-Q device). The PLL responds to variations in frequency and phase of the input by automatically raising or lowering the frequency of the controlled oscillator through feedback, until the output is aligned in the phase and frequency of the system. A practical phase PLL usually ensures a lock in phase, but a lock in frequency with a 0-ppm error has not yet been demonstrated. Generally, commercial PLLs ensure a frequency lock with a margin of error.

PLLs are widely used for synchronization purposes in several communication and consumer domains, radio transmissions, clock recovery and deskewing, spread spectrum, clock jitter reduction, and clock generation and distribution applications. The PLLs typically found in high-performance, high-speed systems are required to have low noise/jitter clock outputs, low clock skew, etc. among other requirements.

### *1.1 Past High-Performance PLL Trends*

High-performance, high-speed systems demand that the system components exhibit close to ideal characteristics, such that precision performance is not compromised while simultaneously ensuring that the systems themselves do not become overly complicated. In electronic systems, this exacting requirement has led to a move from the analog domain to the digital domain for all processing, while the signal transmission and reception are performed in the analog domain. This shift, consequently, means that high-performance systems generally have both analog and digital blocks and blocks to perform the analog-to-digital (A/D) and digital-to-analog (D/A) signal conversions. All the digital, A/D, and D/A blocks also require high-precision clocking that involves a clock generation and distribution circuitry which is typically a high-performance PLL. In the past, because of technology limitations in silicon, high-performance PLLs traditionally relied on off-chip, high-Q mechanical devices such as crystal oscillators to complete the feedback system in order to ensure high-quality output. Technology was simply not advanced enough to ensure a high-Q oscillator on silicon that was able to be successfully integrated with the rest of the PLL components.

However,crystal oscillators are not without drawbacks. Traditional fundamental-mode crystals are very difficult to cut, and thus tend to be very expensive at frequencies beyond 200 MHz. Moreover, long frequency lines produce undesirable effects such as electromagnetic interference (EMI); to reduce these interferences, then, multiple crystal oscillators are required at the point of clocking, which greatly increases system costs. Sometimes a programmable oscillator is also desired for applications that require a variety of high frequencies; using fixed-frequency crystal oscillators requires multiple components, and drives up the system costs even more.

### *1.2 Recent High-Performance PLL Trends*

Recent advances in silicon process technology have made possible the design of an on-chip, high-Q, inductor-based oscillator that costs a fraction of a similar crystal-based oscillator. The performance difference between the two components is negligible and insignificant for most applications. This new trend on silicon also allows for all PLL operations to be done on-chip, without the need for external components. Moreover, the use of a programming on-chip oscillator and dividers enables the PLL to track a wide range of frequencies that are useful for test applications.

Texas Instruments' CDCM6100x series of ultra-low jitter clock generators is such a family of devices: ; the PLL components are all on-chip and require no additional off-chip components for device operation. This series also includes a programming interface to enable the PLL to cover wide frequency ranges at its output as well as to operate at a wide range of PLL bandwidths, while ensuring very low noise/jitter over its entire operating range.

## 2 Functional Description

The CDCM6100x is a family of highly-versatile, low-jitter frequency synthesizers that can generate one, two, or four low-jitter clock outputs, selectable between LVPECL, LVDS or LVCMOS, from a low-frequency crystal or LVCMOS input for a variety of wireline and data communication applications. The CDCM61004 features an on-chip PLL that can be easily configured solely through control pins. The overall output jitter performance is less than 1 $ps_{RMS}$, thus making the device a perfect choice for use in demanding applications such as SONET, Ethernet, Fibre Channel, and SAN.

## 3 Input Stage of CDCM6100x

The input stage of the CDCM6100x is an oscillator circuit with a positive feedback loop that is designed to enable the attached crystal to oscillate at all times. In order for proper oscillation at all times, the following conditions are satisfied by design.

- Loop gain exceeds unity at the resonant frequency
- Phase shift around the loop is an integer multiple of $2\pi$ radians

The type of oscillator stage in the CDCM6100x is called the *Collpits oscillator*, which uses a parallel resonant-tuned circuit for fundamental mode parallel resonant crystals. Figure 1 shows the Collpits stage in the CDCM6100x, where the feedback is provided through the capacitive voltage divider with on-chip capacitors $C_1$ and $C_2$. When using a crystal input with the CDCM6100x, one leg of the crystal is connected to the XIN pin and the other leg of the crystal is connected to GND.

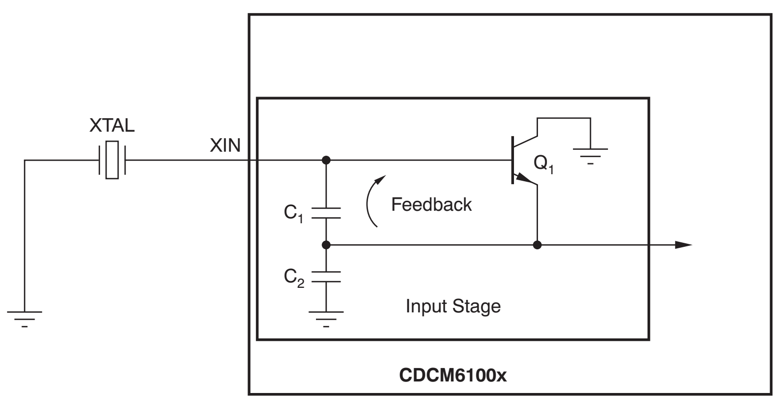


**Figure 1. Collpits Oscillator Input Stage of CDCM6100x**

## 4 Single-Ended LVCMOS Input to CDCM6100x

The CDCM6100x can be operated with an external LVCMOS reference input applied to the XIN pin, which has internal biasing of 1.9 V. As a result of the bias voltage, the recommended voltage swing for the LVCMOS input is 2.5 V ±30% in order to maintain low distortion and low jitter of the clock outputs from the CDCM6100x. The input duty cycle should be at least 40% to 60%, and the input slew rate should be at least 0.75 V/ns. Figure 2 shows the recommended method to interface an LVCMOS signal with the CDCM61004 (as an example) through an ac-coupling capacitor.

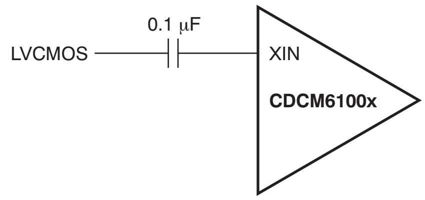


**Figure 2. LVCMOS Input Interface to CDCM61004**

## 5 Device Startup Mode with LVCMOS Input

When using an LVCMOS input, the CDCM6100x can start up with its PLL and output dividers/types loaded by control pins; thus, proper operation of the PLL ensures output at the correct frequency. The startup time depends on the power-supply ramp time. Once the supply voltage has crossed a pre-determined threshold voltage (2.27 V, in this case), the auto-calibration of the PLL kicks in which then sets the dividers and the VCO to the appropriate frequency as configured. The auto-calibration can also be restarted by toggling the RSTN pin of the CDCM6100x from high to low and back to high. The RSTN pin has an internal pull-up resistor of 150 kΩ. The calibration restarts after the RSTN pin crosses the pre-determined threshold voltage of 2.27 V as well. Thus, if the LVCMOS reference input to the CDCM6100x is unstable even after the power-supply voltage crosses the threshold voltage (and therefore, after the auto-calibration has been completed), the RSTN pin low-to-high transition on startup can be delayed through a low-pass filter using the internal pull-up resistor (creating a simple, first-order RC circuit) with a fairly high time constant. This time constant would depend on the average time before which the reference input stabilizes. For example, for a 10-ms delay before the input clock stabilizes, the RC circuit values are calculated as R (internal) = 150 kΩ and C = 0.1 µF. Figure 3 shows this recommended circuit.

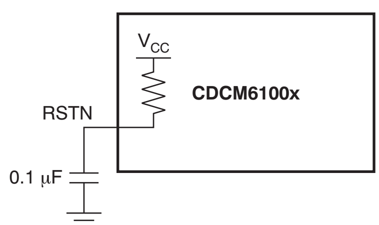


**Figure 3. Recommended Startup Circuit for LVCMOS Input Interface to CDCM6100x**

## 6 Conclusion

The CDCM6100x is a family of devices that is ideally suited to provide reference clocks for networking and wireless infrastructure baseband applications with challenging jitter requirements. While the CDCM6100x work well with a crystal as the reference input, it is also acceptable to provide an LVCMOS clock because the reference input and the methodology described in the report must be adopted for proper device operation.

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