TPS5625 Working With TMS320C6201 Applications Application Report

Feng Lin and Les Hodson

Literature Number: SLVA047
October 1998

TEXAS INSTRUMENTS

Contents

List of Figures

TPS5625 Working With TMS320C6201 Applications

ABSTRACT

This application report describes a design example that uses fast TPS5625 hysteretic controller and low-cost TL5001A PWM controller installed in SLVP105 and SLVP101 EVMs for a TMS320C6201 DSP application. This design converts 5 V to 2.5 V at 8 A and 3.3 V at 3 A for high-current DSP applications.

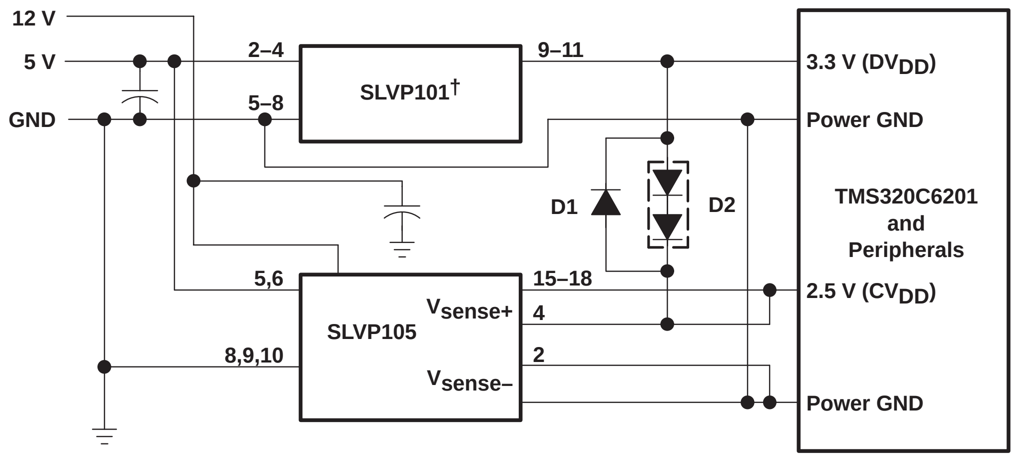
Introduction

Texas Instruments' TMS320C6x Digital Signal Processors (DSP) require two power supply voltages. For example, the TMS320C6201 core requires 2.5 V at 2 A, and the I/O interface requires 3.3 V at 500 mA. In most DSP applications, and especially in multiple-DSP applications, the power requirement is much higher to supply the whole application board. In addition, high efficiency, fast transient response, and protection between two outputs are characteristics increasingly required of the power supply system. The Texas Instruments TPS5210 controller and its spinoffs, like the TPS5625, meet these requirements. These synchronized rectifier type controllers provide the required high efficiency and, more importantly, they use hysteresis control to speed up the feedback response. Hysteresis control keeps the maximum time delay to less than 250 ns from output voltage feedback to drive signal. This control is much faster than conventional current or voltage mode control methods. Consequently, with the same ESR and ESL, the output capacitance can be greatly reduced to save board space and cost. Also, peak-to-peak output voltage ripple can be controlled by setting the hysteresis range so that the noise that affects DSP functions can be minimized.

This application report describes a design example that uses fast TPS5625 hysteretic controllers and low-cost TL5001A PWM controllers installed in SLVP105 and SLVP101 EVMs for a TMS320C6201 DSP application. This design converts 5 V to 2.5 V at 8 A and 3.3 V at 3 A for high-current DSP applications.

Circuit Description

Figure 1 shows the example design circuit.



† Two resistor values are changed in SLVP101: R7 is changed to 820 kΩ, and R10 is changed to 560 kΩ.
NOTE: Check references for more details.

Figure 1. Example Circuit

The SLVP101 EVM is a nominal 5-V-input-to-3.3-V-output regulator designed by Texas Instruments. The EVM supplies 3.3-V I/O power and satisfies all requirements for powering this high performance DSP such as low cost, low parts count, good transient response, and excellent output voltage accuracy. Two resistors in SLVP101 are changed from the original design to further soften the soft-start start-up sequence. The SLVP108, a new version of the SLVP101 that has fewer components, will be available soon.

The SLVP105 is a nominal 5-V-input-to-2.5-V-output regulator also designed by Texas Instruments; it uses hysteresis control to provide fast transient response for core voltage (2.5 V). The time delay from the output voltage feedback signal to the MOSFET driver output is less than 250 ns. With this module, the external capacitance can be reduced. The output control compensation is easier to design in terms of load type variation, compared with the conventional voltage and current control. The control voltage for the SLVP105 is 12 V to achieve high efficiency of the TPS5625 controller. A 5-V control voltage version will also be available soon.

Diodes D1 and D2 are protection diodes to prevent damage caused by excessive voltage difference (>2 V) between two outputs under any conditions. During normal operation, the forward voltage across each section of D2 will be only 0.4 V, not enough to conduct.

The TMS320C6201 requires start-up sequencing. Since the SLVP105 uses 12-V input logic, the 12-V input must be brought up first, or simultaneously with the 5-V input. After the inputs are up, the 3.3-V and 2.5-V output voltages must be brought up, preferably the 2.5-V output first, but at least simultaneously. To achieve this sequence, the SLVP101 soft-start is slowed down. Resistors R7 and R10 in the SLVP101 are changed to 820 kΩ and 560 kΩ, respectively. The start-up waveforms in Figure 6 show that the 2.5-V output reaches the 90% nominal voltage first.

Toggling the input voltages resets both regulators after a fault condition.

The EVMs should be positioned as close to the DSP as possible to minimize trace resistance and inductance and ground-loop current between the two output grounds. Ground-loop current can generate large amounts of radiated EMI noise that can adversely affect any circuitry within the loop. Make the ground connection right on the DSP to minimize the problem.

Specifications

This section provides the operating conditions and characteristics for the EVMs. Figures 2 through 7 show data and waveforms for the example design circuit.

Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
V_{IN}	4.5	5	5.5	V
V_{CC} for SLVP105	11	12	14	V
Operating ambient temperature, T_A	0		85	°C

Electrical Characteristics Over Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage setpoint 1	Over all conditions	2.425	2.5	2.575	V
Output voltage setpoint 2	Over all conditions	3.201	3.3	3.399	V
Load regulation	Over all conditions		0.02%	1%	
Line regulation	Over all conditions		0.01%	0.1%	
Output current	T_A = 25°C	0		8	A
Output current	T_A = 25°C	0		3	A
Efficiency	T_A = 25°C, both full load		89%		
Switching frequency	T_A = 25°C		200		kHz
Turn on input voltage	T_A = 25°C	4.20		4.49	V
Under voltage lock out	T_A = 25°C, 50% load	4.10		4.48	V
Over voltage setpoint 1	T_A = 25°C, V_{IN} = 5 V		3		V
Over voltage setpoint 2	T_A = 25°C, V_{IN} = 5 V		4		V
Over current inception 1	T_A = 25°C, V_{IN} = 5 V		9		A
Over current inception 2	T_A = 25°C, V_{IN} = 5 V		3.25		A
Short circuit current 1†	T_A = 25°C, V_{IN} = 5 V		0		A
Short circuit current 2†	T_A = 25°C, V_{IN} = 5 V		0		A

† Under short circuit condition, the outputs are turned off. Toggling the inputs resets the circuitry.

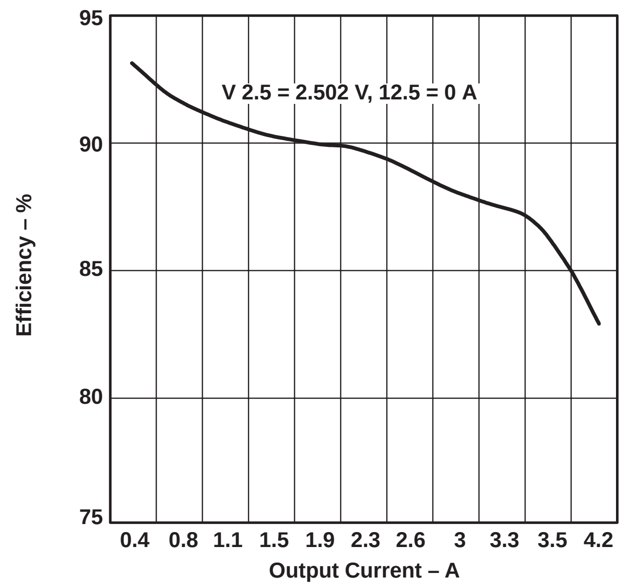


Figure 2. Efficiency of 3.3-V Output at 2.5 V/0 A

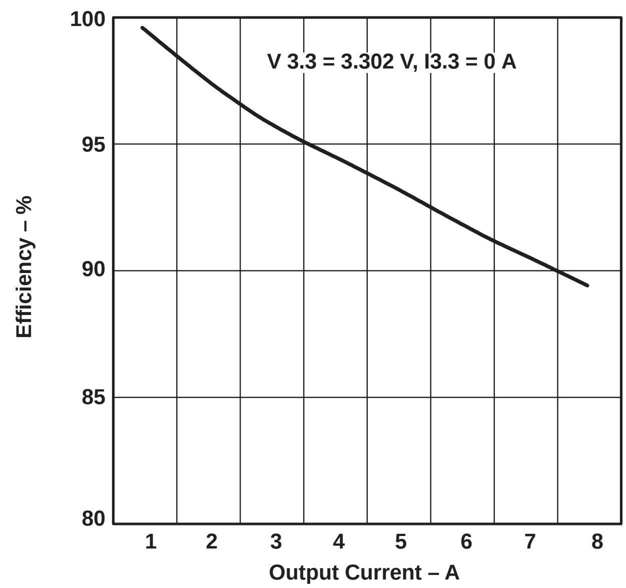


Figure 3. Efficiency of 2.5-V Output at 3.3 V/0 A

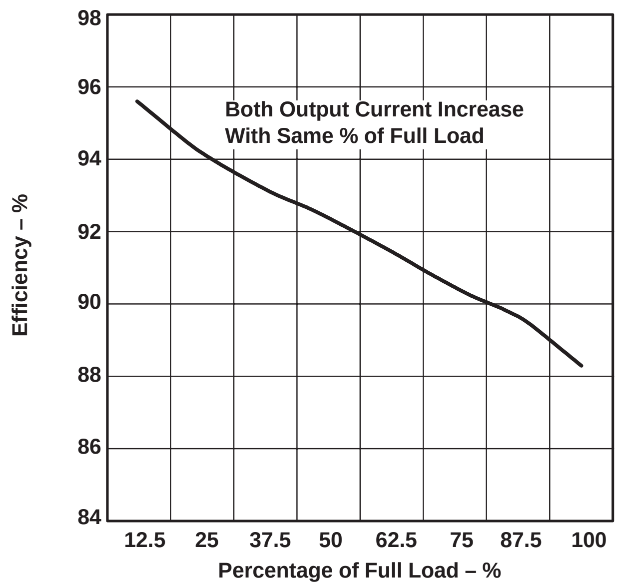


Figure 4. Efficiency of Both Outputs at Same Output Current Increasing Rate

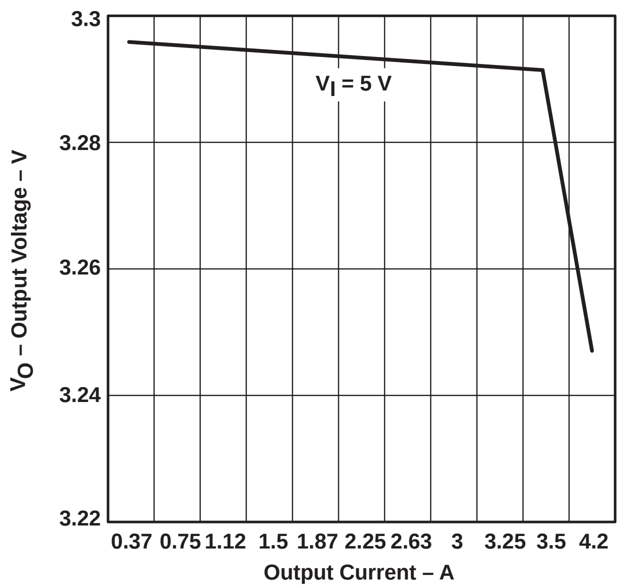


Figure 5. Load Regulation on 3.3-V Output

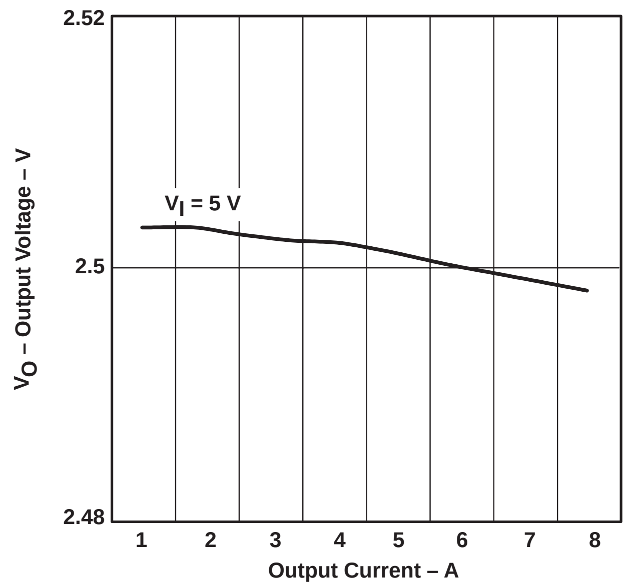


Figure 6. Load Regulation of 2.5-V Output

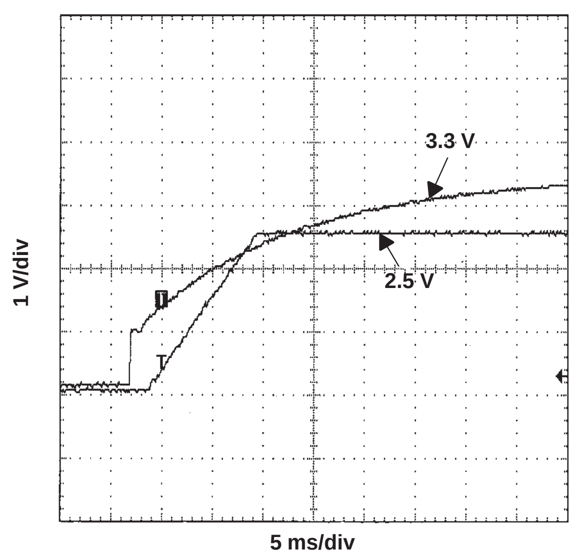


Figure 7. Output Voltage Start-Up Waveforms

Summary

The SLVP105 and SLVP101 EVMs, equipped with TPS5625 hysteretic controller and TL5001A PWM controller, provide a power supply solution for high-performance DSP applications.

References

1. *SLVP101, SLVP102, and SLVP103 Buck Converter Design Using the TL5001 User's Guide*, Texas Instruments, 1998, Literature No. SLVU005.
2. *TPS5615, TPS5618, TPS5625, and TPS5633 Synchronous Buck Hysteretic Regulator Controller*, Texas Instruments, 1998.
3. *TL5001, TL5001A, TL5001Y Pulse-Width-Modulation Control Circuits*, Texas Instruments, Revised 1998, Literature No. SLVS084D.
4. *Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMS,* Texas Instruments, September, 1998, Literature No. SLVU007.