

# ***TPS25751 Technical Reference Manual***

## ***Technical Reference Manual***

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Literature Number: SLVUCR8A  
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## Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

## Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## Related Documents

- USB Power Delivery Specification Revision 3.1 [www.usb.org/developers/docs](http://www.usb.org/developers/docs)
- USB Type-C Cable and Connector Specification Revision 2.0. [www.usb.org/developers/docs](http://www.usb.org/developers/docs)

## Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 1.1 Introduction

### 1.1.1 Purpose and Scope

This document describes the Host Interface for the TPS25751S and TPS25751D Type-C Port Switch / Power Delivery (PD) Controller devices.

## 1.2 PD Controller Host Interface Description

### 1.2.1 Overview

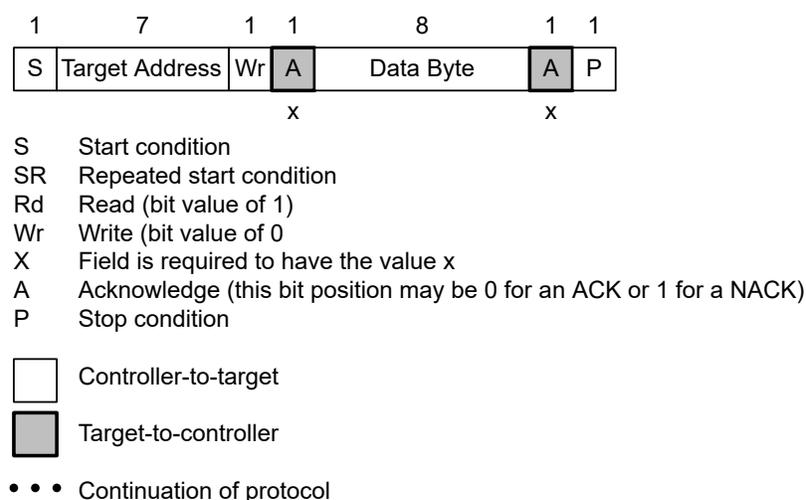
The PD Controller provides one I2C target. The I2C target is meant to be connected to an Embedded Controller (EC).

The Host Interface defines how the registers are accessed from I2C target port and target addresses. Target Address #1 is selected by the customer using the ADCIN1 and ADCIN2 pins on the PD controller. See also [Table 5-1](#) for more details about the target addresses.

The Host Interface provides general status information to the controller of these I2C interfaces about the PD Controller, ability to control the PD Controller, status of USB Type-C® Port and communications to/from a connected device (Port Partner) and/or cable plug through USB PD messages. All Host Interface communication that uses the Unique I2C address is referred to as Unique Address Interface.

The PD Controller supports a register-based Unique Address Interface. [Chapter 3](#) lists the Unique Address Interface registers and provides detailed Unique Address Interface register descriptions.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 and is repeated here in part in [Figure 1-1](#).



**Figure 1-1. I2C Read/Write Protocol Key**

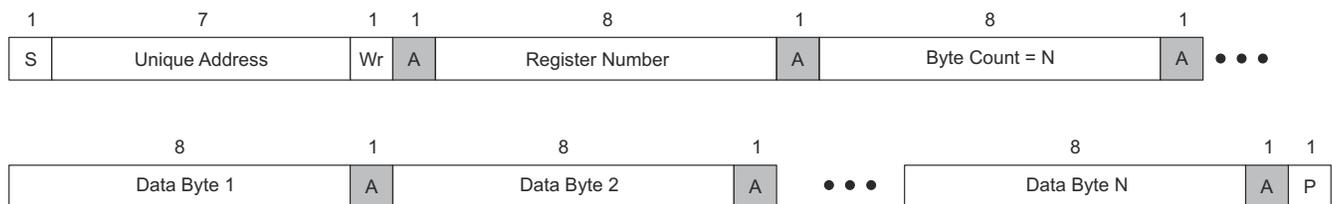
## 1.2.2 Register and Field Notation

In this document the register names use an ALL CAPS notation, and the field names use a CamelBack notation. For example `TX_SOURCE_CAPS` refers to register 0x32, and `TX_SOURCE_CAPS.numValidPDOs` refers to a specific field in Byte 1 of that register. In this document I2C1 denotes I2Ct.

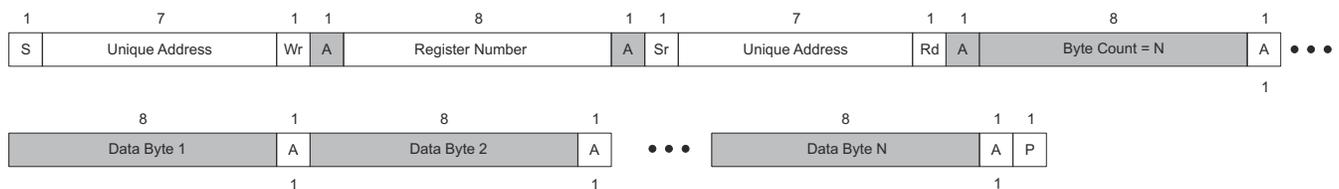
## 1.3 Unique Address Interface

### 1.3.1 Unique Address Interface Protocol

The Unique Address Interface allows for complex interactions between an I2C controller and a single PD Controller. The I2C target unique address is used to receive or respond to Host Interface protocol commands. [Figure 1-2](#) and [Figure 1-3](#) show the write and read protocols, respectively. The Byte Count used during a register write can be longer than the number of bytes actually written, in other words the controller can issue the stop bit without writing N bytes. Similarly, during a register read, the controller can issue the stop bit before reading all N bytes. N bytes refers to the number of bytes to be read or written.



**Figure 1-2. I2C Unique Address Write Register Protocol**



**Figure 1-3. I2C Unique Address Read Register Protocol**



## 2.1 Overview

The PD Controller implements modes for "SRC Policy" (handing out Source contracts) and modes for "SNK Policy" (issuing Requests for Sink contracts). Certain fields are referred to differently, the [table](#) below summarizes the naming conventions assumed.

**Table 2-1. Naming Conventions**

Reference Name	TPS25751S Reference	TPS25751D Reference
PP_5V1, PP1 Switch	PP5V	PP5V
PP_EXT1, PP3 Switch	PP_EXT	PP_HV

## 2.2 Source Policy Mode

The PD Controller uses the *TX\_SOURCE\_CAPS* register (0x32) to know what PDO(s) to advertise. The PD Controller will automatically respond to Request messages as appropriate, and each port acts independently. The host can dynamically change the *TX\_SOURCE\_CAPS* register, then issue the 'SSrC' 4CC Task and the PD controller will advertise the new PDOs.

## 2.3 Sink Policy Mode

The PD Controller will always prepare its own Request message based on the settings in the *AUTO\_NEGOTIATE\_SINK* register (0x37) and the *TX\_SINK\_CAPS* register (0x33). The PD Controller will send its prepared Request message as soon as it is ready. The host can change the *AUTO\_NEGOTIATE\_SINK* register and/or the *TX\_SINK\_CAPS* register, then issue the 'GSrC' 4CC Task and the PD controller will re-negotiate the PD contract based on the updated values.

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Table 3-1 lists the memory-mapped registers for the TPS25751 registers. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

**Table 3-1. TPS25751 Registers**

Offset	Acronym	Register Name	Section
3h	Mode	Mode	<a href="#">Section 3.1</a>
6h	Customer Use	Customer Use	<a href="#">Section 3.2</a>
8h	Command Register for I2C1	Command Register for I2C1	<a href="#">Section 3.3</a>
9h	Data Register for CMD1	Data Register for CMD1	<a href="#">Section 3.4</a>
14h	Interrupt Event for I2C1	Interrupt Event for I2C1	<a href="#">Section 3.5</a>
16h	Interrupt Mask for I2C1	Interrupt Mask for I2C1	<a href="#">Section 3.6</a>
18h	Interrupt Clear for I2C1	Interrupt Clear for I2C1	<a href="#">Section 3.7</a>
1Ah	Status	Status	<a href="#">Section 3.8</a>
26h	Power Path Status	Power Path Status	<a href="#">Section 3.9</a>
28h	Port Configuration	Port Configuration	<a href="#">Section 3.10</a>
29h	Port Control	Port Control	<a href="#">Section 3.11</a>
2Dh	Boot Flags	Boot Flags	<a href="#">Section 3.12</a>
30h	Received Source Capabilities	Received Source Capabilities	<a href="#">Section 3.13</a>
31h	Received Sink Capabilities	Received Sink Capabilities	<a href="#">Section 3.14</a>
32h	Transmit Source Capabilities	Transmit Source Capabilities	<a href="#">Section 3.15</a>
33h	Transmit Sink Capabilities	Transmit Sink Capabilities	<a href="#">Section 3.16</a>
34h	Active PDO Contract	Active PDO Contract	<a href="#">Section 3.17</a>
35h	Active RDO Contract	Active RDO Contract	<a href="#">Section 3.18</a>
37h	Autonegotiate Sink	Autonegotiate Sink	<a href="#">Section 3.19</a>
3Fh	Power Status	Power Status	<a href="#">Section 3.20</a>
40h	PD Status	PD Status	<a href="#">Section 3.21</a>
5Ch	IO Config	IO Config	<a href="#">Section 3.22</a>
69h	Type C State	Type C State	<a href="#">Section 3.23</a>
6Ah	ADC Results	ADC Results	<a href="#">Section 3.24</a>
70h	Sleep Control Register	Sleep Control Register	<a href="#">Section 3.25</a>
72h	GPIO Status	GPIO Status	<a href="#">Section 3.26</a>
98h	Liquid Detection Config	Liquid Detection Config	<a href="#">Section 3.27</a>

Complex bit access types are encoded to fit into small table cells. Table 3-2 shows the codes that are used for access types in this section.

**Table 3-2. TPS25751 Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read

**Table 3-2. TPS25751 Access Type Codes (continued)**

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 3.1 Mode Register (Offset = 3h) [Reset = 0000000h]

Mode is shown in [Table 3-3](#).

Return to the [Summary Table](#).

Indicates the operational state of the port. The PD controller has limited functionality in some modes.

**Table 3-3. Mode Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	Mode	R	0h	The mode described in 4 ASCII characters. 'APP ' indicates that the PD controller is fully functioning in the application firmware where all registers are available. 'BOOT' indicates that the PD controller is booting in dead battery. 'PTCH' indicates that the PD controller is in patch mode. Any other values indicates that the PD controller is functioning in limited capacity. In 'BOOT' and 'PTCH' only the follow register addresses are accessible, Mode, Command, Data, Int Event, Int Mask, Int Clear, and Boot Flags.

### 3.2 Customer Use Register (Offset = 6h) [Reset = 000000000000000h]

Customer Use is shown in [Table 3-4](#).

Return to the [Summary Table](#).

These 8 bytes are allocated for customer use as needed. The PD controller does not use this register. This register may be changed during application customization.

**Table 3-4. Customer Use Register Field Descriptions**

Bit	Field	Type	Reset	Description
63-0	Customer Use	R	0h	These 8 bytes are allocated for customer use as needed. The PD controller does not use this register. This register may be changed during application customization.

### 3.3 Command Register for I2C1 (Offset = 8h) [Reset = 0000000h]

Command Register for I2C1 is shown in [Table 3-5](#).

Return to the [Summary Table](#).

Command register for the primary command interface. Cleared to 0x0000\_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

**Table 3-5. Command Register for I2C1 Field Descriptions**

Bit	Field	Type	Reset	Description
31-0	Command	R/W	0h	Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".



### 3.5 Interrupt Event for I2C1 Register (Offset = 14h) [Reset = 00000000000002000008h]

Interrupt Event for I2C1 is shown in [Table 3-7](#).

Return to the [Summary Table](#).

Interrupt event bit field for IRQ. If any bit in this register is 1, then the IRQ pin is pulled low. Bytes 1 to 10 of this register are port-specific, but Byte 11( Bits 80-87) is common to all ports in the PD controller.

**Table 3-7. Interrupt Event for I2C1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
87-83	RESERVED	R	0h	Reserved
82	I2C Controller NACKed	R	0h	A transaction on the I2C Controller was NACKed.
81	Ready for Patch	R	0h	Device ready for a patch bundle from the host.
80	Patch Loaded	R	0h	Patch was loaded to the device.
79	RESERVED	R	0h	Reserved
78	RESERVED	R	0h	Reserved
77	RESERVED	R	0h	Reserved
76	RESERVED	R	0h	Reserved
75-74	RESERVED	R	0h	Reserved
73	RESERVED	R	0h	Reserved
72	RESERVED	R	0h	Reserved
71	RESERVED	R	0h	Reserved
70	RESERVED	R	0h	Reserved
69-67	RESERVED	R	0h	Reserved
66	MBRD Buffer Ready	R	0h	Receive memory buffer full and ready to be read using the 'MBRd' command.
65	TX Memory Buffer Empty	R	0h	Transmit memory buffer empty.
64	RESERVED	R	0h	Reserved
63	RESERVED	R	0h	Reserved
62	RESERVED	R	0h	Reserved
61	RESERVED	R	0h	Reserved
61	RESERVED	R	0h	Reserved
60	Liquid Detection	R	0h	Asserted when Liquid Detection is detected or removed. Read 0x98 to determine the state of Liquid Detection.
60	RESERVED	R	0h	Reserved
59	RESERVED	R	0h	Reserved
62-59	RESERVED	R	0h	Reserved
58	RESERVED	R	0h	Reserved
57	Ext DCDC Source Safe State	R	0h	Used for EC controlled battery charger or DC/DC applications to indicate when the PD controller is no longer going to act as a source. This interrupt will be set when acting as a source and receiving/sending an Accept message to a Power Role Swap.
56	Ext DCDC Sink Safe State	R	0h	Used for EC controlled battery charger or DC/DC applications to indicate when the PD controller is no longer going to act as a sink. This interrupt will be set when acting as a sink and receiving/sending an Accept message to a Power Role Swap. This interrupt will also be set when acting as a sink and receiving an Explicit PD Contract Accept from the connected source.
55	RESERVED	R	0h	Reserved
54	RESERVED	R	0h	Reserved
53	RESERVED	R	0h	Reserved
52	RESERVED	R	0h	Reserved

**Table 3-7. Interrupt Event for I2C1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
51	RESERVED	R	0h	Reserved
50	RESERVED	R	0h	Reserved
49	RESERVED	R	0h	Reserved
48	RESERVED	R	0h	Reserved
47	RESERVED	R	0h	Reserved
46	Unable to Source Error	R	0h	The Source was unable to increase the voltage to the negotiated voltage of the contract.
45	RESERVED	R	0h	Reserved
44	RESERVED	R	0h	Reserved
43	Plug Early Notification	R	0h	A connection has been detected but not debounced.
42	Sink Transition Completed	R	0h	This event only occurs when in source mode (PD_STATUS.PresentPDRole = 1b). It occurs tSrcTransition (ms) after sending an Accept message to a Request message, just before sending the PS_RDY message.
41-40	RESERVED	R	0h	Reserved
39	Message Data Error	R	0h	An erroneous message was received.
38	Protocol Error	R	0h	An unexpected message was received from the partner device.
37	RESERVED	R	0h	Reserved
36	Missing Get Capabilities Message Error	R	0h	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
35	Power Event Occurred Error	R	0h	An OVP, or ILIM event occurred on VBUS. Or a TSD event occurred.
34	Can Provide Voltage or Current Later Error	R	0h	The USB PD Source can provide acceptable voltage and current, but not at the present time. A "wait" message was sent or received.
33	Cannot Provide Voltage or Current Error	R	0h	The USB PD Source cannot provide an acceptable voltage and/or current. A Reject message was sent to the Sink or a Capability Mismatch was received from the Sink.
32	Device Incompatible Error	R	0h	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
31	RESERVED	R	0h	Reserved
30	CMD1 Complete	R	0h	Set whenever a non-zero value in CMD1 register is set to zero or ! CMD.
29-28	RESERVED	R	0h	Reserved
27	PD Status Updated	R	0h	Set whenever contents of PD_STATUS register (0x40) change.
26	Status Updated	R	0h	Set whenever contents of STATUS register (0x1A) change.
25	RESERVED	R	0h	Reserved
24	Power Status Updated	R	0h	Set whenever contents of POWER_STATUS register (0x3F) change.
23	Power Path Switch Changed	R	0h	Set whenever contents of POWER_PATH_STATUS register (0x26) changes.
22	RESERVED	R	0h	Reserved
21	USB Host No Longer Present	R	0h	Set when STATUS.UsbHostPresent transitions to anything other than 11b.
20	USB Host Present	R	0h	Set when STATUS.UsbHostPresent transitions to 11b.
19	RESERVED	R	0h	Reserved
18	Data Swap Requested	R	0h	A DR swap was requested by the Port Partner.
17	Power Swap Requested	R	0h	A PR swap was requested by the Port Partner.
16	RESERVED	R	0h	Reserved
15	Sink Cap Message Received	R	0h	

**Table 3-7. Interrupt Event for I2C1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
14	Source Capabilities Message Received	R	0h	This is asserted when a Source Capabilities message is received from the Port Partner.
13	New Contract as Provider	R	0h	An RDO from the far-end device has been accepted and the PD Controller is a Source. This is asserted after the PS_RDY message has been sent. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
12	New Contract as Consumer	R	0h	Far-end source has accepted an RDO sent by the PD Controller as a Sink. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	Overcurrent	R	0h	Set whenever an Overcurrent field (VBUS or VCONN) in the POWER_PATH_STATUS register (0x26) changes.
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	Data Swap Complete	R	0h	A Data Role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
4	Power Swap Complete	R	0h	A Power role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
3	Plug Insert or Removal	R	1h	USB Plug Status has Changed. See Status register for more plug details.
2	RESERVED	R	0h	Reserved
1	PD Hardreset	R	0h	A PD Hard Reset has been performed. See PD_STATUS.HardResetDetails for more information.
0	RESERVED	R	0h	Reserved

### 3.6 Interrupt Mask for I2C1 Register (Offset = 16h) [Reset = 00000000000000003000h]

Interrupt Mask for I2C1 is shown in [Table 3-8](#).

Return to the [Summary Table](#).

Interrupt mask bit field for INT\_EVENT1. A bit in INT\_EVENT1 cannot be set if it is cleared in this register. Bytes 1 to 10 of this register are port-specific, but Byte 11( Bits 80-87) is common to all ports in the PD controller.

**Table 3-8. Interrupt Mask for I2C1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	RESERVED	R/W	0h	
78	RESERVED	R/W	0h	
77	RESERVED	R/W	0h	
76	RESERVED	R/W	0h	
75	RESERVED	R/W	0h	
74	RESERVED	R/W	0h	
73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	
71	RESERVED	R/W	0h	
70	RESERVED	R/W	0h	
69	RESERVED	R/W	0h	
68	RESERVED	R/W	0h	
67	RESERVED	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	RESERVED	R/W	0h	
63	RESERVED	R/W	0h	
62	RESERVED	R/W	0h	
61	RESERVED	R/W	0h	Reserved
60	Liquid Detection	R/W	0h	Liquid Detection
59	RESERVED	R/W	0h	
58	RESERVED	R/W	0h	
57	Ext DCDC Source Safe State	R/W	0h	
56	Ext DCDC Sink Safe State	R/W	0h	
55	RESERVED	R/W	0h	
54	RESERVED	R/W	0h	
53	RESERVED	R/W	0h	
52	RESERVED	R/W	0h	
51	RESERVED	R/W	0h	
50	RESERVED	R/W	0h	
49	RESERVED	R/W	0h	
48	RESERVED	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	

**Table 3-8. Interrupt Mask for I2C1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
45	RESERVED	R/W	0h	Reserved
44	RESERVED	R/W	0h	
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	RESERVED	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabilities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	RESERVED	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	RESERVED	R/W	0h	
24	Power Status Updated	R/W	0h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	1h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	RESERVED	R/W	0h	
10	RESERVED	R/W	0h	
9	Overcurrent	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	

**Table 3-8. Interrupt Mask for I2C1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

### 3.7 Interrupt Clear for I2C1 Register (Offset = 18h) [Reset = 00000000000000000000h]

Interrupt Clear for I2C1 is shown in [Table 3-9](#).

Return to the [Summary Table](#).

Interrupt clear bit field for INT\_EVENT1. Writing 1 to a specific bit will clear that specific event in INT\_EVENT1. Bits set in this register are cleared from INT\_EVENT1. Bytes 1 to 10 of this register are port-specific, but Byte 11( Bits 80-87) is common to all ports in the PD controller.

**Table 3-9. Interrupt Clear for I2C1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	RESERVED	R/W	0h	
78	RESERVED	R/W	0h	
77	RESERVED	R/W	0h	
76	RESERVED	R/W	0h	
75	RESERVED	R/W	0h	
74	RESERVED	R/W	0h	
73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	
71	RESERVED	R/W	0h	
70	RESERVED	R/W	0h	
69	RESERVED	R/W	0h	
68	RESERVED	R/W	0h	
67	RESERVED	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	RESERVED	R/W	0h	
63	RESERVED	R/W	0h	
62	RESERVED	R/W	0h	
61	RESERVED	R/W	0h	Reserved
60	Liquid Detection	R/W	0h	Liquid Detection
59	RESERVED	R/W	0h	
58	RESERVED	R/W	0h	
57	Ext DCDC Source Safe State	R/W	0h	
56	Ext DCDC Sink Safe State	R/W	0h	
57-55	RESERVED	R/W	0h	Reserved
56-55	RESERVED	R/W	0h	
56-54	RESERVED	R/W	0h	Reserved
55-54	RESERVED	R/W	0h	Reserved
53	RESERVED	R/W	0h	
52	RESERVED	R/W	0h	
51	RESERVED	R/W	0h	
50	RESERVED	R/W	0h	
49	RESERVED	R/W	0h	

**Table 3-9. Interrupt Clear for I2C1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
48	RESERVED	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	
45	RESERVED	R/W	0h	Reserved
44	RESERVED	R/W	0h	
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	RESERVED	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabilities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	RESERVED	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	RESERVED	R/W	0h	
24	Power Status Updated	R/W	0h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	RESERVED	R/W	0h	
10	RESERVED	R/W	0h	
9	Overcurrent	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved

**Table 3-9. Interrupt Clear for I2C1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
6	RESERVED	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

### 3.8 Status Register (Offset = 1Ah) [Reset = 000000000h]

Status is shown in [Table 3-10](#).

Return to the [Summary Table](#).

Status bit field for non-interrupt events.

**Table 3-10. Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
39-34	RESERVED	R	0h	Reserved
33-32	RESERVED	R	0h	Reserved
31	RESERVED	R	0h	Reserved
30	SOC Ack Timeout	R	0h	Indicates whether the attached SoC has responded timely. 0h = SoC has responded timely 1h = SoC has not responded timely
29-28	RESERVED	R	0h	Reserved
27	BIST	R	0h	Indicates if a BIST procedure is in progress. 0h = No BIST in progress 1h = BIST in progress
26	RESERVED	R	0h	Reserved
25-24	Acting as Legacy	R	0h	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device. It can take approximately 10 seconds for the PD controller to determine that it is attached to a legacy source or sink. 0h = PD Controller is not in a legacy (non PD) mode 1h = PD Controller is acting like a legacy sink 2h = PD Controller is acting like a legacy source 3h = Acting as legacy sink due to dead-battery.
23-22	USB Host Present	R	0h	USB host attachment status. 0h = No host present 1h = Attached source is not data capable 2h = Attached source is not USB PD capable 3h = Host present
21-20	VBUS Status	R	0h	Indicates the present state of VBUS. 0h = At vSafe0V (less than 0.8V) 1h = At vSafe5V (4.75V to 5.5V) 2h = Within expected limits 3h = Not within any of the other specified ranges
19-7	RESERVED	R	0h	Reserved
6	Data Role	R	0h	PD controller data role. This is only valid once there is a connection. 0h = Upward-facing port (UFP) 1h = Downward-facing port (DFP)
5	Port Role	R	0h	Current state of PD Controller CCx terminations. This also indicates the PD Controller Power Role, once connected. This bit does not toggle during Unattached.* state transitions. 0h = PD Controller is in the Sink role 1h = PD Controller is Source (CCx pull-up active)
4	Plug Orientation	R	0h	Plug orientation indicator. Indicates port orientation when known (requires connection). 0h = Upside-up orientation (plug CC on CC1) 1h = Upside-down orientation (plug CC on CC2)
3-1	Connection State	R	0h	Details of a connected plug. 0h = No connection 1h = Port is disabled 2h = Audio connection (Ra/Ra) 3h = Debug connection (Rd/Rd) 4h = No connection Ra detected (Ra but no Rd) 5h = Reserved (may be used for Rp/Rp Debug connection) 6h = Connection present no Ra detected 7h = Connection present Ra detected

**Table 3-10. Status Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
0	Plug Present	R	0h	Status of the plug 0h = No plug is connected 1h = A plug is connected

### 3.9 Power Path Status Register (Offset = 26h) [Reset = 000000000h]

Power Path Status is shown in [Table 3-11](#).

Return to the [Summary Table](#).

Power Path Status.

**Table 3-11. Power Path Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
39-38	Power Source	R	0h	Indicates current PD Controller power source. NOTE: Since the Dead Battery flag forces PD Controller to be powered from VBUS, only 10b is valid when this flag is set. Any other setting indicates that the Dead Battery flag is not set. 0h = Reserved 1h = PD Controller is powered from VIN_3V3 2h = PD Controller is powered from VBUS 3h = Reserved
37-35	RESERVED	R	0h	Reserved
34	PPCable1 Overcurrent	R	0h	PP_CABLE1 overcurrent indicator. Asserted if an overcurrent condition exists on PP_CABLE1 (VCONN).
33-29	RESERVED	R	0h	Reserved
28	PP1 Overcurrent	R	0h	PP_5V1 overcurrent indicator. Asserted if an overcurrent conditions exists on PP1 switch (PP_5V1).
27-21	RESERVED	R	0h	Reserved
20-18	RESERVED	R	0h	Reserved
17-15	RESERVED	R	0h	Reserved
14-12	PP3 Switch	R	0h	Indicates current state of PP3 (PP_EXT1). 0h = PP3 switch disabled 1h = PP3 switch currently disabled due to fault 2h = PP3 switch enabled (system output) 3h = PP3 switch enabled (system input)
11-9	RESERVED	R	0h	Reserved
8-6	PP1 Switch	R	0h	Indicates current state of PP1 switch (PP_5V1). 0h = PP1 switch disabled 1h = PP1 switch currently disabled due to fault 2h = PP1 switch enabled (system output)
5-2	RESERVED	R	0h	Reserved
1-0	PPCable1 Switch	R	0h	Indicates current state of PP_CABLE1 switch. 0h = PP_CABLE1 switch disabled 1h = PP_CABLE1 switch currently disabled 2h = PP_CABLE1 switch CC1 enabled (system output) 3h = PP_CABLE1 switch CC2 enabled (system output)

### 3.10 Port Configuration Register (Offset = 28h) [Reset = 000000000000000000000000002F4802h]

Port Configuration is shown in [Table 3-12](#).

Return to the [Summary Table](#).

Configuration for port-specific hardware. This register configures hardware that is specific for each port and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by Application Customization.

**Table 3-12. Port Configuration Register Field Descriptions**

Bit	Field	Type	Reset	Description
127-96	RESERVED	R/W	0h	Reserved
95-80	RESERVED	R/W	0h	Reserved
79-73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	Reserved
71-64	RESERVED	R/W	0h	Reserved
63-48	VBUS For Valid PPS Status	R/W	0h	
47-32	APDO VBUS Uvp TripPoint Offset	R/W	0h	
31	RESERVED	R/W	0h	Reserved
30-29	APDO ILIM Over Shoot	R/W	0h	
28-27	APDO VBUS UVP Threshold	R/W	0h	
26-24	VBUS Sink UVP Trip HV	R/W	0h	VBUS disconnect when power role is sink. The disconnect threshold is set to $(1 - \text{VBUS\_SinkUvpTripHV}) * (\text{min expected VBUS})$ . The 000b setting follows the USB-C specification requirements. Use a non-zero value for additional margin. 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 50%
23-22	RESERVED	R/W	0h	Reserved
21-20	OVP for PP5V	R/W	2h	VBUS OVP settings while sourcing from PP5V. This applies while sourcing through PP1 or PP2. See data-sheet for voltage range. 0h = Use setting 0: 5.25 V (typical) 1h = Use setting 1: 5.5 V (typical) 2h = Use setting 2: 5.8 V (typical) 3h = Use setting 3: 6.1 V (typical)
19-18	RESERVED	R/W	0h	Reserved
17-16	VBUS OVP Usage	R/W	3h	OVP configuration settings. These two bits are used to select the OVP trip-point. The PD controller automatically computes the lowest threshold that does not overlap with the expected maximum voltage (including maximum tolerance allowed by USB PD specification). The OVP trip-point will be set at the selected percentage of the computed threshold. 0h = 100% 1h = 105% 2h = 111% 3h = 114%
15	RESERVED	R/W	0h	Reserved
14-13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	

**Table 3-12. Port Configuration Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
11	RESERVED	R/W	0h	Reserved
10	Disable PD	R/W	0h	Assert this bit to disable USB PD.
9-8	TypeC Support Options	R/W	0h	Configuration for optional features. This register controls whether optional Type-C state machine states are supported. NOTE: These states are mutually-exclusive and these options only exist when specific Type-C state machines are used. 0h = No Type-C optional states are supported 1h = Try.SRC state is supported as a DRP 3h = Reserved
7-2	RESERVED	R/W	0h	Reserved
1-0	TypeC State machine	R/W	2h	Port Configuration. 0h = Sink state machine only 1h = Source state machine only 2h = DRP state machine 3h = Disabled

### 3.11 Port Control Register (Offset = 29h) [Reset = 03915052h]

Port Control is shown in [Table 3-13](#).

Return to the [Summary Table](#).

Configuration bits affecting system policy. These bits may change during normal operation and are used for controlling the respective port. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. Initialized by Application Customization.

**Table 3-13. Port Control Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-30	Charger Detect Enable	R/W	0h	Configure the types of legacy chargers to detect. 0h = Do not detect any legacy chargers 1h = Detect BC 1.2 chargers 2h = Reserved do not use 3h = Detect BC 1.2 and proprietary legacy chargers
29	RESERVED	R/W	0h	Reserved
28-26	Charger Advertise Enable	R/W	0h	Configure the types of legacy chargers to emulate. 0h = Do not emulate any legacy charger 1h = BC 1.2 CDP only 2h = BC 1.2 DCP only 3h = Reserved 4h = Reserved 5h = DCP Auto 1 (2.7V and DCP) 6h = DCP Auto 2 (1.2V 2.7V and DCP) 7h = Reserved
25	RESERVED	R/W	0h	Reserved
24	Resistor 15k Present	R/W	1h	Configure D+ and D- termination. Assert this bit if there is a 15kOhm pull-down on D+ and D- (USB2.0 Host Phy pull-downs enabled). This should not be used for DCP or DCP Auto modes. 0h = System does NOT have 15 kOhm pull-down 1h = System has 15 kOhm pull-down
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	0h	Reserved
20	Enable Current Monitor	R/W	1h	Assert this bit to enable the current monitor (peak and average) that are read from the ADC_RESULTS register. While asserted the PD controller will remain in the active power mode.
19	Unconstrained Power	R/W	0h	External power configuration. This also sets the Unconstrained Power bit defined by USB PD. When this bit is changed from 1 to 0 the PD controller will not attempt a power role swap with the Port Partner. If a power role swap is desired the host should issue a 'SWSr' 4CC command. 0h = No external power 1h = External power present
18	RESERVED	R/W	0h	Reserved
17	RESERVED	R/W	0h	Reserved
16	RESERVED	R/W	0h	Reserved
15	Initiate Swap to DFP	R/W	0h	Configure DR_Swap to DFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as UFP.
14	Process Swap to DFP	R/W	1h	Configure response to DR_Swap to DFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a DFP. Otherwise, the PD Controller will reject such a request.
13	Initiate Swap to UFP	R/W	0h	Configure DR_Swap to UFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as DFP.

**Table 3-13. Port Control Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
12	Process Swap to UFP	R/W	1h	Configure response to DR_Swap to UFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a UFP. Otherwise, the PD Controller will reject such a request.
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	Initiate Swap to Source	R/W	0h	Configure PR_Swap to source initiation. If this bit is asserted, the PD Controller automatically initiates and sends PR_Swap requests to the Port Partner when appropriate if presently operating as Sink (C/P).
6	Process Swap to Source	R/W	1h	Configure response to PR_Swap to source. If this bit is asserted, the PD Controller will automatically accept a PR_Swap request to become a Source. Otherwise, the PD Controller will reject such a request.
5	Initiate Swap to Sink	R/W	0h	Configure PR_Swap to sink initiation. If this bit is asserted, the PD Controller automatically initiates and sends PR_Swap requests to the Port Partner when appropriate if presently operating as Source (P/C).
4	Process Swap to Sink	R/W	1h	Configure response to PR_Swap to sink. If this bit is asserted, the PD Controller will automatically accept a PR_Swap request to become a Sink. Otherwise, the PD Controller will reject such a request.
3-2	RESERVED	R/W	0h	Reserved
1-0	TypeC Current	R/W	2h	Type-C Current advertisement. This setting is ignored if a Source role is not enabled and active. This setting is also ignored during an explicit USB PD contract, where the Rp value is used for collision avoidance as required by the USB PD specification. Note that when PP5V is low, the FW will only use the default Type-C current regardless of the value in this field. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Reserved

### 3.12 Boot Flags Register (Offset = 2Dh) [Reset = 00000000h]

Boot Flags is shown in [Table 3-14](#).

Return to the [Summary Table](#).

Detailed status of boot process. This register provides details on PD Controller boot flags, Customer OTP configuration, and silicon revision

**Table 3-14. Boot Flags Register Field Descriptions**

Bit	Field	Type	Reset	Description
39-32	Revision ID	R	0h	Revision ID for the PD controller.
31-29	Patch Config Source	R	0h	Source of patch configuration. This field indicates the source of the configuration patch that has been successfully loaded. 0h = No configuration has been loaded 4h = Reserved 5h = A configuration has been loaded from EEPROM 6h = A configuration has been loaded from I2C 7h = Reserved
28-27	RESERVED	R	0h	Reserved
26-25	RESERVED	R	0h	
24	RESERVED	R	0h	Reserved
23-20	RESERVED	R	0h	Reserved
19	System TSD	R	0h	System thermal shut-down indicator. This bit is asserted if the PD controller is rebooting after the system thermal sensor caused a reset.
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16-14	RESERVED	R	0h	Reserved
13	Region 1 CRC Fail	R	0h	Region 1 CRC status indicator. This bit is asserted when the CRC of data read from Region 1 of EEPROM memory failed.
12	Region 0 CRC Fail	R	0h	Region 0 CRC status indicator. This bit is asserted when the CRC of data read from Region 0 of EEPROM memory failed.
11	RESERVED	R	0h	Reserved
10	Patch Download Error	R	0h	Asserted when a patch download error occurs.
9	Region 1 EEPROM Error	R	0h	Region 1 status indicator. This bit is asserted when an error occurred attempting to read Region 1 of EEPROM memory. A retry may have been successful.
8	Region 0 EEPROM Error	R	0h	Region 0 status indicator. This bit is asserted when an error occurred attempting to read Region 0 of EEPROM memory. A retry may have been successful.
7	Region 1 Invalid	R	0h	Region 1 header status indicator. This bit is asserted when Region 1 header of the EEPROM memory was invalid.
6	Region 0 Invalid	R	0h	Region 0 header status indicator. This bit is asserted when Region 0 header of the EEPROM memory was invalid.
5	Region 1	R	0h	Region 1 attempted indicator. This bit is asserted when Region 1 of the EEPROM memory was attempted.
4	Region 0	R	0h	Region 0 attempted indicator. This bit is asserted when Region 0 of the EEPROM memory was attempted.
3	I2C EEPROM Present	R	0h	EEPROM presence indicator. This bit is asserted when an EEPROM device was discovered during boot.
2	Dead Battery Flag	R	0h	Dead Battery flag indicator. This bit is asserted when the PD Controller booted in dead-battery mode.
1	RESERVED	R	0h	Reserved
0	Patch Header Error	R	0h	Asserted when a patch bundle header errors.







**Table 3-17. Transmit Source Capabilities Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-0	Number Valid PDOs	R/W	1h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)



### 3.17 Active PDO Contract Register (Offset = 34h) [Reset = 00000000000h]

Active PDO Contract is shown in [Table 3-19](#).

Return to the [Summary Table](#).

Power data object for active contract. This register stores PDO data for the current explicit USB PD contract, or all zeroes if no contract.

**Table 3-19. Active PDO Contract Register Field Descriptions**

Bit	Field	Type	Reset	Description
47-42	RESERVED	R	0h	Reserved
41-32	First PDO Control Bits	R	0h	Contains bits 29:20 of the first PDO. It does not matter which PDO was selected, this field is always drawn from the first PDO.
31-0	Active PDO	R	0h	Power data object. This field contains the contents of the PDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

### 3.18 Active RDO Contract Register (Offset = 35h) [Reset = 000000000000000000000000h]

Active RDO Contract is shown in [Table 3-20](#).

Return to the [Summary Table](#).

Power data object for the active contract. This register stores the RDO of the current explicit USB PD contract, or all zeroes if no contract.

**Table 3-20. Active RDO Contract Register Field Descriptions**

Bit	Field	Type	Reset	Description
95-32	RESERVED	R	0h	Reserved
31-28	Object Position	R	0h	As defined by USB PD.
27	Give Back Flag	R	0h	As defined by USB PD.
26	Capability Mismatch	R	0h	As defined by USB PD.
25	USB Communication Capable	R	0h	As defined by USB PD.
24	No USB Suspend	R	0h	As defined by USB PD.
23	Unchunked Supported	R	0h	As defined by USB PD.
22-20	RESERVED	R	0h	Reserved
19-10	Operating Current	R	0h	As defined by USB PD.
9-0	Max Min Operation Current	R	0h	As defined by USB PD.



**Table 3-21. Autonegotiate Sink Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
41-32	Auto Neg Max Voltage	R/W	190h	Maximum voltage to request. During PD power contract negotiation, the PD controller will only select voltages that are less than or equal to the value specified in this field. Not used unless AutoComputeSinkMinVoltage=0. (50mV per LSB)
31-22	Auto Neg Sink Min Required Power	R/W	104h	Minimum operating power required by the Sink. The PD Controller will always attempt to receive this power level from the Source. (250mW per LSB) See description in AutoComputeSinkMinPower field
21-12	RESERVED	R/W	0h	Reserved
11-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	Auto Disable Sink Upon Capability Mismatch	R/W	0h	Sink path and capability mismatch settings. If this bit is asserted, then any time the implicit or explicit power contract would cause the Capability Mismatch bit to be set the PD controller will disable the sinking path. The 'SRDY' 4CC task can override and enable the sink path. However, if the contract changes after the 'SRDY' has completed, the PD controller will disable the sink path if the contract causes a capability mismatch. This bit should only be asserted if the NoCapabilityMismatch bit is set to 0.
5	Auto Compute Sink Max Voltage	R/W	1h	Configuration for maximum voltage. The PD controller can automatically compute ANMaxVoltage, or allow the host to specify it. 0h = Provided by host 1h = Computed by PD controller
4	Auto Compute Sink Min Voltage	R/W	1h	Configuration for minimum voltage. The PD controller can automatically compute ANMinVoltage, or allow the host to specify it. 0h = Provided by host 1h = Computed by PD controller
3	No Capability Mismatch	R/W	1h	Configuration for capability mismatch in RDO. There are two conditions that will trigger a capability mismatch: <ul style="list-style-type: none"> <li>If the attached source does not offer a PDO whose power is greater or equal to the ANSinkCapMismatchPower field in this register.</li> <li>PPS is enabled in this register and the attached source did not offer a PPS PDO that matches the requirements in TX_SINK_CAPS.</li> </ul> <p>If either condition is true, then the PD controller will assert the capability mismatch bit in its request unless this bit is asserted. 0h = Capability mismatch enabled 1h = Capability mismatch disabled.</p>
2	Auto Compute Sink Min Power	R/W	1h	Minimum power sink requires. The minimum sink power is the largest power reported in any valid PDO in the TX_SINK_CAPS (0x33). The power for a particular PDO from the TX_SINK_CAPS follows for each supply type: <ul style="list-style-type: none"> <li>Battery Supply: OperatingPower</li> <li>Variable Supply: MaxVoltage*OperatingCurrent</li> <li>Fixed Supply: Voltage*OperatingCurrent.</li> </ul> <p>However, if the TX_SINK_CAPS register includes Battery supply type PDO(s), then ANSinkMinRequiredPower = maximum OperatingPower in a Battery supply type PDO. 0h = Provided by host 1h = Computed by PD controller</p>
1	No USB Suspend	R/W	1h	Value used for the NoUSBSusp Flag in the RDO. This is as defined by USB PD.

**Table 3-21. Autonegotiate Sink Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
0	Auto Neg RDO Priority	R/W	0h	Configuration for tie-breaker in PDO selection. The PD controller will find the set of PDOs that fulfill the voltage requirements. From that set of PDOs it will pick the one with higher power. If two acceptable PDOs have the same power, Fixed Supply Type is preferred, and then Variable Supply has second preference. If two PDOs have the same power and the same type, then this bit determines which PDO is selected. 0h = Higher voltage 1h = Lower voltage

### 3.20 Power Status Register (Offset = 3Fh) [Reset = 0000h]

Power Status is shown in [Table 3-22](#).

Return to the [Summary Table](#).

Details about the power of the connection. This register reports status regarding the power of the connection.

**Table 3-22. Power Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-8	Charger Advertise Status	R	0h	Charger Advertise Status 0h = Charger advertise disabled or not run 1h = Charger advertisement in process 2h = Charger advertisement complete 3h = Reserved
7-4	Charger Detect Status	R	0h	0h = Charger detection disabled or not run 1h = Charger detection in progress 2h = Charger detection complete none detected 3h = Charger detection complete SDP detected 4h = Charger detection complete BC 1.2 CDP detected 5h = Charger detection complete BC 1.2 DCP detected 6h = Charger detection complete Divider1 DCP detected 7h = Charger detection complete Divider2 DCP detected 8h = Charger detection complete Divider3 DCP detected 9h = Charger detection complete 1.2V DCP detected
3-2	TypeC Current	R	0h	This field is redundant with PD_STATUS.CCPullUp in register 0x40 when SourceSink is 1b. This field is redundant with PORT_CONTROL.TypeCCurrent in register 0x29 when SourceSink is 0b. In the future, this redundant field may be removed. This field is intended for Type-C Sink operation. If the port is connected as source, the field is updated upon initial connection only. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Explicit PD contract sets current
1	SourceSink	R	0h	Source / Sink indicator. This bit is equivalent to PresentPDRole in register 0x40. It is replicated in this register for convenience. In the future, this redundant bit may be removed. 0h = Connection requests power 1h = Connection provides power (PD Controller as sink)
0	Power Connection	R	0h	Asserted if there is a connection. This bit is asserted when PlugPresent is TRUE and ConnState is greater than 5h. So it is redundant with information from register 0x1A. It is replicated in this register for convenience. In the future this redundant bit may be removed. 0h = No connection 1h = Connection present

### 3.21 PD Status Register (Offset = 40h) [Reset = 0000000h]

PD Status is shown in [Table 3-23](#).

Return to the [Summary Table](#).

Status of PD and Type-C state-machine. This register contains details regarding the status of PD messages and the Type-C state machine.

**Table 3-23. PD Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	RESERVED	R	0h	Reserved
27-22	RESERVED	R	0h	Reserved
21-16	Hard Reset Details	R	0h	Reason for Hard Reset 0h = Reset value no hard reset 1h = Received from Port Partner 2h = Requested by host 3h = Invalid DR_Swap request during Active Mode 4h = DischargeFailed. 5h = NoResponseTimeOut. 6h = SendSoftReset. 7h = Sink_SelectCapability. 8h = Sink_TransitionSink. 9h = Sink_WaitForCapabilities. Ah = SoftReset. Bh = SourceOnTimeout. Ch = Source_CapabilityResponse. Dh = Source_SendCapabilities. Eh = SourcingFault. Fh = UnableToSource. 10h = FRS failure 11h = Unexpected message 12h = Failure to to complete the VCONN recovery sequence within 200ms after PP5V rising edge
15-13	RESERVED	R	0h	Reserved
12-8	Soft Reset Details	R	0h	Reason for Soft Reset 0h = Reset value no soft reset 1h = Soft reset received from Port Partner 2h = Reserved 3h = Reserved 4h = Received source capabilities message was invalid 5h = Message retries were exhausted 6h = Received an accept message unexpectedly 7h = Received a control message unexpectedly 8h = Received a GetSinkCap message unexpectedly 9h = Received a GetSourceCap message unexpectedly Ah = Received a GotoMin message unexpectedly Bh = Received a PS_RDY message unexpectedly Ch = Received a Ping message unexpectedly Dh = Received a Reject message unexpectedly Eh = Received a Request message unexpectedly Fh = Received a Sink Capabilities message unexpectedly 10h = Received Source Capabilities message unexpected 11h = Received a Swap message unexpectedly 12h = Received a Wait Capabilities message unexpectedly 13h = Received an unknown control message 14h = Received an unknown data message 15h = To initialize SOP' controller in plug 16h = To initialize SOP" controller in plug 17h = Received an Extended message unexpectedly 18h = Received an unknown Extended message 19h = Received a data message unexpectedly 1Ah = Received a Not Supported message unexpectedly 1Bh = Received a Get_Status message unexpectedly

**Table 3-23. PD Status Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	Present PD Role	R	0h	Present PD power role. The PD Controller is acting under this PD power role. 0h = Sink 1h = Source
5-4	Port Type	R	0h	Present Type-C power role. The PD Controller is acting under this Type-C power role. 0h = Sink/Source 1h = Sink 2h = Source 3h = Source/Sink
3-2	CC Pullup	R	0h	CC Pull-up value. The pull-up value detected by PD Controller when in CC Pull-down mode. 0h = Not in CC pull-down mode / no CC pull-up detected 1h = USB Default current 2h = 1.5 A (SinkTxNG) 3h = 3.0 A (SinkTxOK)
1-0	RESERVED	R	0h	Reserved



**Table 3-24. IO Config Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
76-64	Initial Value	R	0h	Controls default output level for each GPIO enabled as output (0=Drive Low, 1=Drive High)
63-45	RESERVED	R	0h	Reserved
44-32	GPIO Interrupt Enable	R	400h	Controls interrupt enable for each GPIO (1=Interrupt Enabled, 0=Interrupt Disabled). Note that all GPIO pins may not be configured as inputs (see the data-sheet).
31-13	RESERVED	R	0h	Reserved
12-0	GPIO Output Enable	R	14CFh	Controls output enable for each GPIO (1=Output Enabled, 0=Hi-Z). Note that all GPIO may not be configurable as an output (see data-sheet).

### 3.23 Type C State Register (Offset = 69h) [Reset = 0000000h]

Type C State is shown in [Table 3-25](#).

Return to the [Summary Table](#).

Contains current status of both CCn pins.

**Table 3-25. Type C State Register Field Descriptions**

Bit	Field	Type	Reset	Description
31-24	TypeC Port State	R	0h	Present state of Type-C state-machine. 0h = Disabled 5h = ErrorRecovery 24h = Unattached.Accessory 2Bh = AttachWait.Accessory 45h = Try.SRC 4Eh = TryWait.SNK 4Fh = Try.SNK 50h = TryWait.SRC 60h = Attached.SRC 61h = Attached.SNK 62h = AudioAccessory 63h = DebugAccessory 64h = AttachWait.SRC 65h = AttachWait.SNK 66h = Unattached.SNK 67h = Unattached.SRC
23-16	CC2 Pin State	R	0h	State of CC2 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (Sink only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
15-8	CC1 Pin State	R	0h	State of CC1 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (Sink only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
7-0	CC Pin for PD	R	0h	CC pin used for PD communication. 0h = Not connected 1h = CC1 is used for USB PD communication 2h = CC2 is used for USB PD communication

### 3.24 ADC Results Register (Offset = 6Ah) [Reset = 000000000000000000000000h]

ADC Results is shown in [Table 3-26](#).

Return to the [Summary Table](#).

Provides access to measurements from the internal ADC. The PD controller periodically measures the pins mentioned in this register and updates the register accordingly. The frequency of the update depends upon the mode of the PD controller. For example, in Unconnected Sleep the PD controller will not update these registers.

**Table 3-26. ADC Results Register Field Descriptions**

Bit	Field	Type	Reset	Description
103-96	RESERVED	R	0h	Reserved
95-88	IVBUS1_Mean	R	0h	Most recent current peak estimate through PP_5V1. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent mean current. It is cleared upon attach for a new connection.(16.5mA per LSB)
87-80	GPIO2	R	0h	Most recent voltage on the GPIO2 pin. (14mV per LSB)
79-72	GPIO0	R	0h	Most recent voltage on the GPIO0 pin. (14mV per LSB)
71-64	GPIO5	R	0h	Most recent voltage on the GPIO5 pin. (14mV per LSB)
63-56	GPIO4	R	0h	Most recent voltage on the GPIO4 pin. (14mV per LSB)
55-48	RESERVED	R	0h	Reserved
47-40	IVBUS1	R	0h	Most recent current measurement through PP_5V1. (16.5mA per LSB)
39-32	RESERVED	R	0h	Reserved
31-24	VBUS1	R	0h	Most recent voltage on the PA_VBUS pin. (98mV per LSB)
23-16	LDO3V3	R	0h	Most recent voltage on the LDO_3V3 pin. (14mV per LSB)
15-8	ADCIN2	R	0h	Most recent voltage on the ADCIN2 pin. (14mV per LSB)
7-0	ADCIN1	R	0h	Most recent voltage on the ADCIN1 pin. (14mV per LSB)

### 3.25 Sleep Control Register (Offset = 70h) [Reset = 01h]

Sleep Control Register is shown in [Table 3-27](#).

Return to the [Summary Table](#).

Sleep configurations.

**Table 3-27. Sleep Control Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-1	Sleep Time	R/W	0h	Minimum time the PD controller waits before entering sleep mode. 0h = Reserved 1h = 100 ms 2h = 1200 ms 3h = Reserved
0	Sleep Mode Allowed	R/W	1h	If this bit is asserted the PD controller will enter sleep modes after device is idle for Sleep Time.

### 3.26 GPIO Status Register (Offset = 72h) [Reset = 000000000000000h]

GPIO Status is shown in [Table 3-28](#).

Return to the [Summary Table](#).

Captures status and settings of all GPIO pins. Check the device-specific datasheet for the available GPIO because it may vary by device type.

**Table 3-28. GPIO Status Register Field Descriptions**

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39	GPIO 7 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
38	GPIO 6 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
37	GPIO 5 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
36	GPIO 4 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
35	GPIO 3 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
34	GPIO 2 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
33	GPIO 1 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
32	GPIO 0 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
31-13	RESERVED	R	0h	Reserved
12	GPIO 12 Data	R	0h	Asserted if a logic high is detected on the GPIO.
11-8	RESERVED	R	0h	Reserved
7	GPIO 7 Data	R	0h	Asserted if a logic high is detected on the GPIO.
6	GPIO 6 Data	R	0h	Asserted if a logic high is detected on the GPIO.
5	GPIO 5 Data	R	0h	Asserted if a logic high is detected on the GPIO.
4	GPIO 4 Data	R	0h	Asserted if a logic high is detected on the GPIO.
3	GPIO 3 Data	R	0h	Asserted if a logic high is detected on the GPIO.
2	GPIO 2 Data	R	0h	Asserted if a logic high is detected on the GPIO.
1	GPIO 1 Data	R	0h	Asserted if a logic high is detected on the GPIO.
0	GPIO 0 Data	R	0h	Asserted if a logic high is detected on the GPIO.

### 3.27 Liquid Detection Config Register (Offset = 98h) [Reset = 00000000000000000000h]

Liquid Detection Config is shown in [Table 3-29](#).

Return to the [Summary Table](#).

Liquid Detection Configuration

**Table 3-29. Liquid Detection Config Register Field Descriptions**

Bit	Field	Type	Reset	Description
82	Enable Liquid Detection	R/W	0h	Enables liquid detection on the SBU pins connected to the GPIO on the PD Controller. In order for this to function correctly the proper external liquid detection circuitry must be in place.
81	Enable Corrosion Mitigation	R/W	0h	Enable corrosion mitigation. Corrosion mitigation will disconnect the port, disabled the port, and pull down CC pins.
80	Liquid Detection State	R/W	0h	Liquid Detection State
79-76	Sample Time in 10ms Liquid	R/W	0h	Sample Time in multiples of 10ms (10ms per LSB as ms)
75-72	Sample Time in 10ms No Liquid	R/W	0h	Sample Time in multiples of 10ms (10ms per LSB as ms)
71-64	High Threshold ADC Liquid	R/W	0h	High Threshold ADC Liquid (14mV per LSB as mV)
63-56	Low Threshold ADC Liquid	R/W	0h	Low Threshold ADC Liquid (14mV per LSB as mV)
55-48	High Threshold ADC No Liquid	R/W	0h	High Threshold ADC No Liquid, provides hysteresis for exit out of Liquid Detected. (14mV per LSB as mV)
47-40	Low Threshold ADC No Liquid	R/W	0h	Low Threshold ADC No Liquid, provides hysteresis for exit out of Liquid Detected. (14mV per LSB as mV)
39-32	Number of Samples	R/W	0h	Number of samples (must be 2 <sup>N</sup> ) to take average
31-16	Sleep Time In Sec Liquid	R/W	0h	Sleep in multiples of 1s when liquid is detected (1000ms per LSB as ms)
15-0	Sleep Time In Sec No Liquid	R/W	0h	Sleep in multiples of 1s when liquid is not detected. (1000ms per LSB as ms)

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Chapter 4  
**4CC Task Detailed Descriptions**

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## 4.1 CPU Control Tasks

### 4.1.1 'Gaid' - Return to Normal Operation

**Table 4-1. 'Gaid' - Return to Normal Operation**

<b>Description</b>	The 'Gaid' Task causes a warm restart of the PD Controller processor.
<b>INPUT DATAx</b>	None
<b>OUTPUT DATAx</b>	None
<b>Task Completion</b>	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete.
<b>Side Effects</b>	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
<b>Additional Information</b>	The PD controller is in the 'APP ' mode, then it immediately goes to the Error Recovery state then after delaying 1 second (typical) it does a warm restart.

### 4.1.2 'GAID' - Cold Reset Request

**Table 4-2. 'GAID' - Cold Reset Request**

<b>Description</b>	The 'GAID Task causes a cold restart of the PD Controller processor.
<b>INPUT DATAx</b>	None
<b>OUTPUT DATAx</b>	None
<b>Task Completion</b>	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete. This Task forces the PD Controller to reboot its OTP bootloader.
<b>Side Effects</b>	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
<b>Additional Information</b>	The PD controller immediately goes to the Error Recovery state, then after delaying 1 second (typical) it does a cold restart.

## 4.2 PD Message Tasks

### 4.2.1 'SWSk' - PD PR\_Swap to Sink

**Table 4-3. 'SWSk' - PD PR\_Swap to Sink**

<b>Description</b>	The 'SWSk' Task instructs PD Controller to attempt to become a Sink through PR_Swap at the first opportunity while maintaining policy engine compliance.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'SWSk' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Source. The 'SWSk' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>The Source indicated through Source Capabilities that it does not support Dual-Role Power.</li> <li>The PR_Swap is Rejected.</li> </ul> <p>The 'SWSk' Task shall be considered timed-out if:</p> <ul style="list-style-type: none"> <li>The PR_Swap is Accepted but failed to complete per the PD spec.</li> </ul> <p>The 'SWSk' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>PD Controller is already in the Sink power role.</li> <li>The PR_Swap is Accepted and completes normally.</li> </ul>
<b>Side Effects</b>	When the 'SWSk' Task completes successfully PD Controller will have transitioned to the Sink power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
<b>Additional Information</b>	None

### 4.2.2 'SWSr' - PD PR\_Swap to Source

**Table 4-4. 'SWSr' - PD PR\_Swap to Source**

<b>Description</b>	The 'SWSr' Task instructs PD Controller to attempt to become a Source through PR_Swap at the first opportunity while maintaining policy engine compliance.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code
<b>Task Completion</b>	<p>The 'SWSr' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Sink. The 'SWSr' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>The Sink previously indicated through Sink or Source Capabilities that it does not support Dual-Role Power.</li> <li>The PR_Swap is Rejected.</li> </ul> <p>The 'SWSr' Task shall be considered timed-out if:</p> <ul style="list-style-type: none"> <li>The PR_Swap is Accepted but failed to complete per the PD spec.</li> </ul> <p>The 'SWSr' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>PD Controller is already in the Source power role.</li> <li>The PR_Swap is Accepted and completes normally.</li> </ul>
<b>Side Effects</b>	When the 'SWSr' Task completes successfully PD Controller will have transitioned to the Source power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
<b>Additional Information</b>	None

### 4.2.3 'SWDF' - PD DR\_Swap to DFP

**Table 4-5. 'SWDF' - PD DR\_Swap to DFP**

<b>Description</b>	The 'SWDF' Task instructs PD Controller to attempt to become a DFP through DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a UFP PD Controller will attempt to exit those Modes first before sending the DR_Swap.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'SWDF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the DFP. The 'SWDF' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>The UFP indicated through Source or Sink Capabilities that it does not support Data Role Swap.</li> <li>The DR_Swap is Rejected.</li> </ul> <p>The 'SWDF' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>PD Controller is already in the DFP data role.</li> <li>The DR_Swap is Accepted and completes normally.</li> </ul>
<b>Side Effects</b>	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
<b>Additional Information</b>	None

### 4.2.4 'SWUF' - PD DR\_Swap to UFP

**Table 4-6. 'SWUF' - PD DR\_Swap to UFP**

<b>Description</b>	The 'SWUF' Task instructs PD Controller to attempt to become a UFP through DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a DFP PD Controller will exit those Modes first before attempting the DR_Swap.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'SWUF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the UFP. The 'SWUF' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>The DFP indicated through Source or Sink Capabilities that it does not support Data Role Swap.</li> <li>The DR_Swap is Rejected.</li> </ul> <p>The 'SWUF' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>PD Controller is already in the UFP data role.</li> <li>The DR_Swap is Accepted and completes normally.</li> </ul>
<b>Side Effects</b>	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
<b>Additional Information</b>	None

#### 4.2.5 'GSKC' - PD Get Sink Capabilities

**Table 4-7. 'GSKC' - PD Get Sink Capabilities**

<b>Description</b>	The 'GSKC' Task instructs PD Controller to issue a <code>Get_Sink_Cap</code> message to the Port Partner at the first opportunity while maintaining policy engine compliance.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'GSKC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails.</p> <ul style="list-style-type: none"> <li>The Port Partner is a Source and indicated it was not Dual-Role Power.</li> <li>The Port Partner responds to the <code>Get_Sink_Cap</code> message with a <code>Reject</code> or <code>Not_Supported</code> message.</li> </ul> <p>The 'GSKC' Task shall be considered timed-out if:</p> <ul style="list-style-type: none"> <li>The Port Partner fails to respond within the time required by the PD spec.</li> </ul> <p>The 'GSKC' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>The <code>Get_Sink_Cap</code> message is sent, GoodCRC'ed and a Sink Capabilities response is received and processed.</li> </ul>
<b>Side Effects</b>	When the 'GSKC' Task completes successfully the <code>RX_SINK_CAPS</code> register (0x31) will have been updated.
<b>Additional Information</b>	None

#### 4.2.6 'GSrC' - PD Get Source Capabilities

**Table 4-8. 'GSrC' - PD Get Source Capabilities**

<b>Description</b>	The 'GSrC' Task instructs PD Controller to issue a <code>Get_Source_Cap</code> message to the Port Partner device at the first opportunity while maintaining policy engine compliance.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'GSrC' Task completes either when the Source Capabilities message is received or the Task otherwise fails. The 'GSrC' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>The Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power.</li> <li>The Port Partner responds to the <code>Get_Source_Cap</code> message with a <code>Reject</code> or <code>Not_Supported</code> message.</li> </ul> <p>The 'GSrC' Task shall be considered timed-out if:</p> <ul style="list-style-type: none"> <li>The Port Partner fails to respond within the time required by the PD spec.</li> </ul> <p>The 'GSrC' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>The <code>Get_Source_Cap</code> message is sent, GoodCRC'ed and a Source Capabilities response is received and processed.</li> </ul>
<b>Side Effects</b>	When the 'GSrC' Task completes successfully the <code>RX_SOURCE_CAPS</code> register (0x30) will have been updated.
<b>Additional Information</b>	None

#### 4.2.7 'GPPI' - PD Get Port Partner Information

The 'GPPI' Task can be used to cause the PD controller to issue these types of USB PD Get messages:

- Get\_Source\_Cap\_Extended (control message)
- Get\_Sink\_Cap\_Extended (control message)
- Get\_Country\_Codes (Control message)
- Get\_Country\_Info (Data message)
- Get\_Manufacturer\_Info (Extended message)

The PD controller does not have dedicated registers to store the response to these messages. The host must get that response from the DATAX register associated with this Task.

The host must NOT use 'GPPI' to send Get\_Sink\_Capabilities or Get\_Source\_Capabilities messages, because the USB PD spec requires specific actions be taken by the PD controller any time those messages are received. While executing the 'GPPI' Task, the PD controller does not parse the returned message to carry out those checks. Instead, the host must use 'GSkC' to send Get\_Sink\_Capabilities and 'GSrC' to send Get\_Source\_Capabilities messages.

This Task is defined to enable supporting any new Get message that can be defined by USB PD in the future.

**Table 4-9. 'GPPI' - Send a USB PD Get\* Message**

Description	The 'GPPI' Task instructs PD Controller to issue a specific USB PD message to the Port Partner at the first opportunity while maintaining policy engine compliance.			
<b>INPUT DATAX</b>	Bit	Name	Description	
	15	Reserved		
	14:13	FrameType	00b	SOP
			01b	SOP'
			10b	SOP"
			11b	Reserved
	12:8	NumBytes		
	7	Reserved		
	6:5	MessageCategory	00b	Control message (no payload)
			01b	Data message (requires payload)
10b			Extended message (requires payload)	
11b			Reserved	
4:0	MessageType	This field must be the MessageType as defined in the USB PD specification. It specifies the Type of message the PD controller will send.		
<b>OUTPUT DATAX</b>	Byte 1: Standard Task Return Code.			

**Table 4-9. 'GPPI' - Send a USB PD Get\* Message (continued)**

Description	The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.
<b>Task Completion</b>	<p>The 'GPPI' Task completes either when the appropriate message is received or the Task otherwise fails. The 'GPPI' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>• Sending the requested message can violate the USB PD spec. For example, the Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power.</li> <li>• The PortPartner replies with a Reject or Not_Supported message.</li> <li>• The USB PD spec revision (PlugPartnerNegSpecRev or PortPartnerNegSpecRev in PD3_STATUS register (0x41) does not allow sending the requested message.</li> </ul> <p>The 'GPPI' Task shall be considered timed-out if:</p> <ul style="list-style-type: none"> <li>• The requested message is sent, GoodCRC'ed and the recipient (Port Partner or Cable Plug) fails to respond within the time required by the PD spec.</li> <li>• A PD Hard Reset or a disconnection happens before the Task completes.</li> </ul> <p>The 'GPPI' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>• The requested message is sent, GoodCRC'ed and an appropriate response is received and processed.</li> </ul> <p>The 'GPPI' Task shall be aborted when the Rx Buffer is locked. The Rx Buffer is locked after data from a receive message is placed in the DATAx register. The Rx Buffer is unlocked after disconnect and by the 'MBRd' Task.</p>
<b>Side Effects</b>	<p>If necessary, the PD controller can issue a VCONN_Swap in order to send the requested message to a Cable Plug. If the PD controller is in the sink power role and it reads Rp = SinkTxNG, it will wait until Rp = SinkTxOK before initiating the atomic message sequence requested by this 'GPPI' Task. This can cause a non-deterministic delay in completing the Task.</p>
<b>Additional Information</b>	<p>The PD controller will continue trying to execute this Task until it times out or aborts as described above. The host can want to issue the 'ABRT' Task if the process takes too long. Some scenarios where this can happen are:</p> <ul style="list-style-type: none"> <li>• The PD controller is required to be the VCONN_Source in order to send any message on SOP or SOP'. The PD controller will continue trying to become the VCONN provider until it is successful.</li> <li>• The PD controller with a sink power role (that is PresentRole = Sink) is required to wait for Rp = SinkTxOK before initiating an Atomic Message Sequence. The PD controller will continue waiting for Rp = SinkTxOK until it is able to send the appropriate message required for this 'GPPI' Task.</li> </ul> <p>The host must wait until CMDx reads as 0 or INT_EVENT1.CmdComplete is asserted before issuing the 'MBRd' 4CC Task to read the Rx Buffer after issuing this 'GPPI' Task.</p> <p>While executing the 'GPPI' Task, the PD controller uses the same shared buffer that is used to store other extended messages. Therefore, the host must not use the 'GPPI' Task when any other atomic message sequence is ongoing.</p> <p>To read the PD response received as a result of issuing the 'GPPI' Task after it is completed, the host must use the 'MBRd' 4CC command. The 'MBRd' Task must also be used to unlock the Rx Buffer for other incoming message.</p>

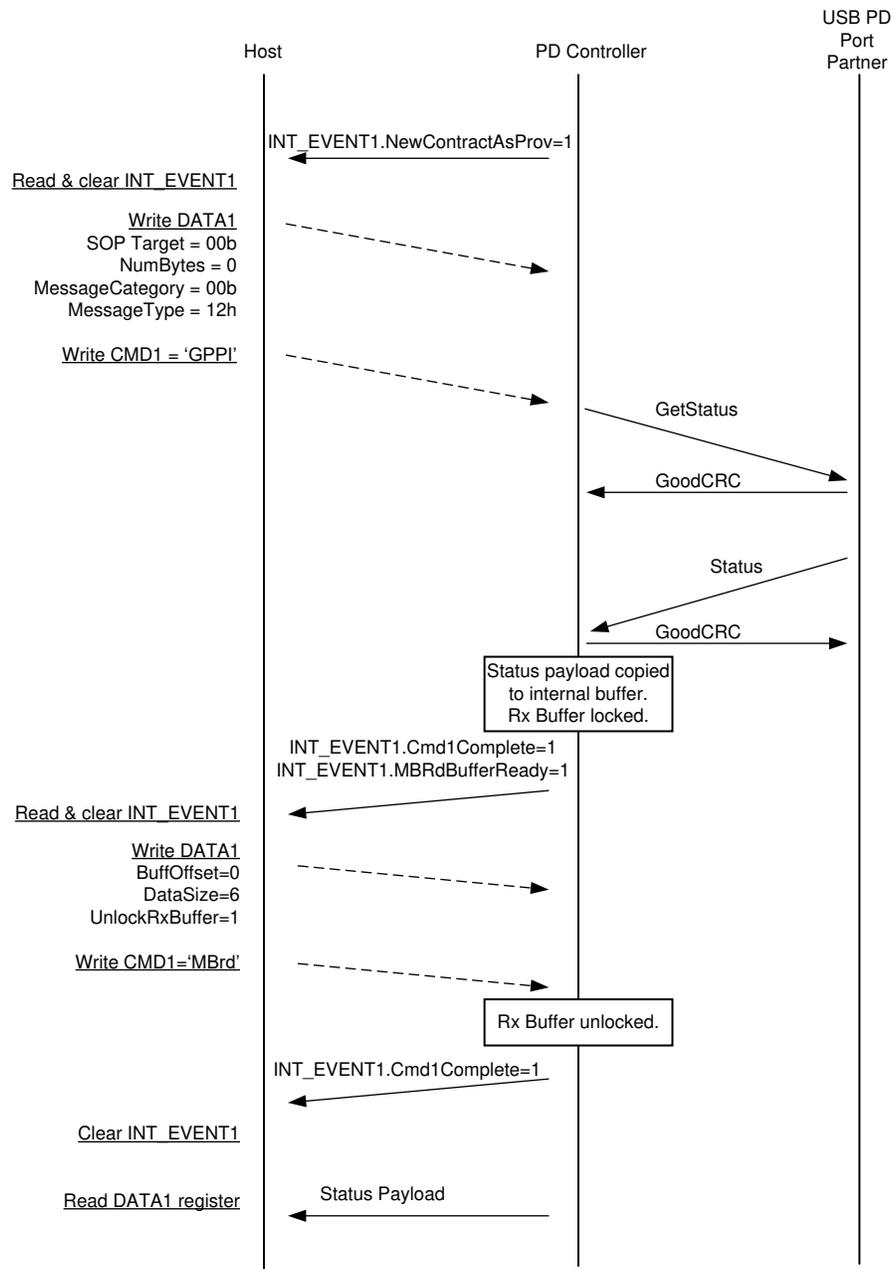


Figure 4-1. Example Sequence for 'GPPI' Task When Host Uses INT\_EVENT1

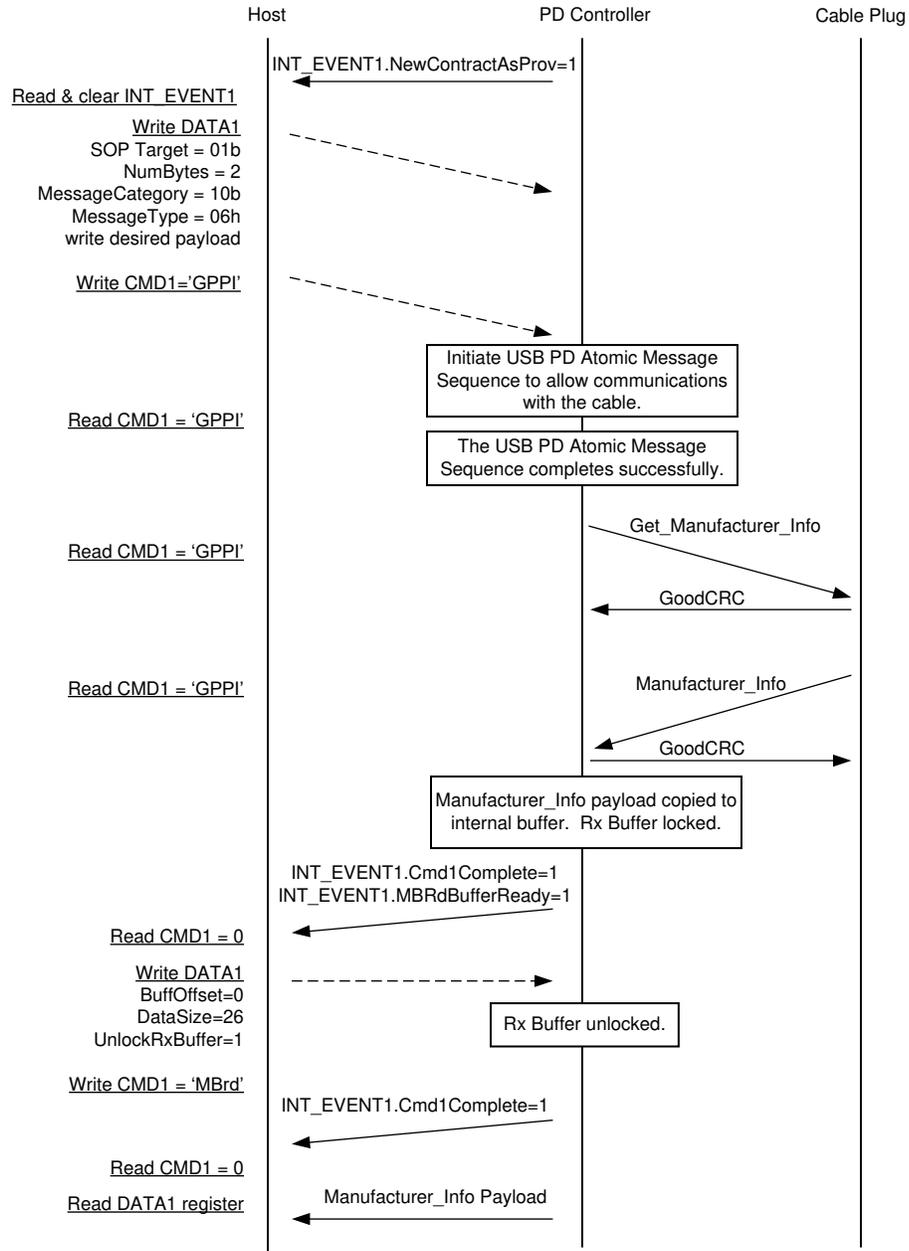


Figure 4-2. Example Sequence for 'GPPI' Task When Host Uses CMD1 Polling

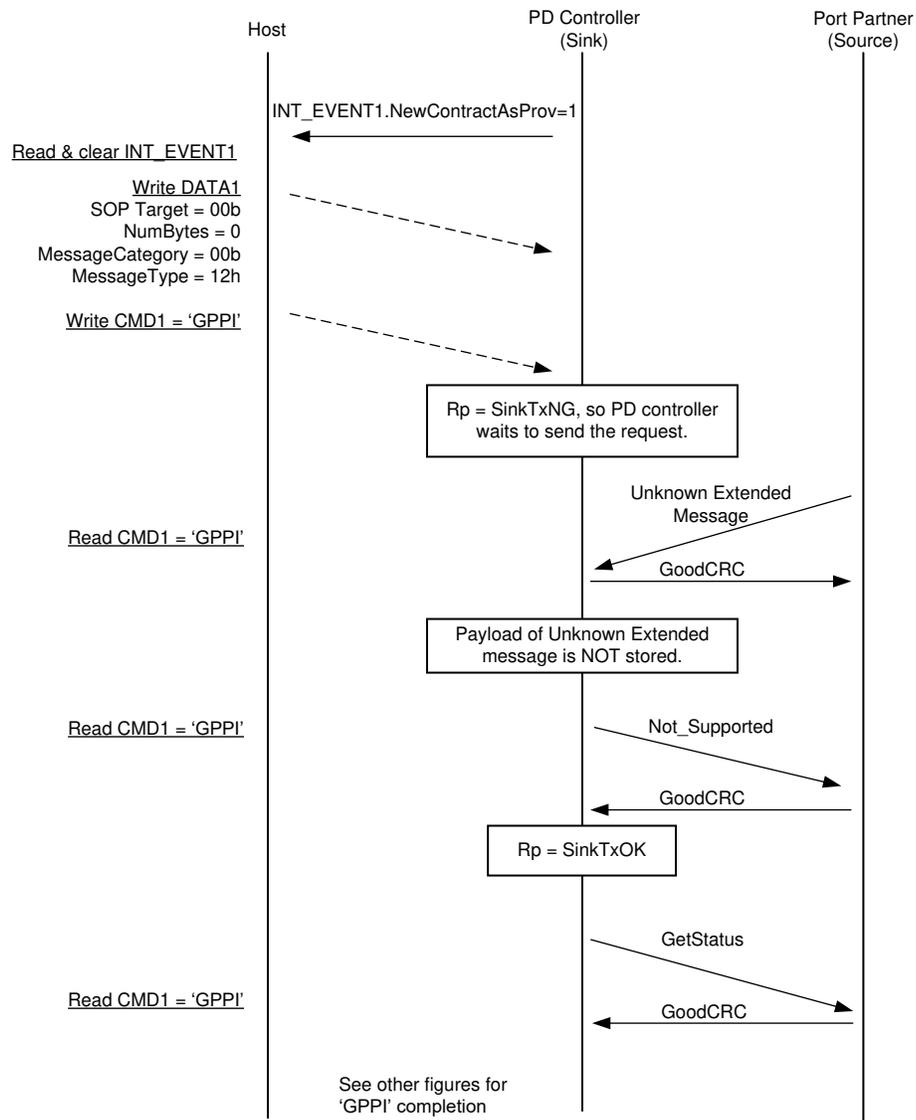


Figure 4-3. 'GPPI' Interrupted by an Unknown Message

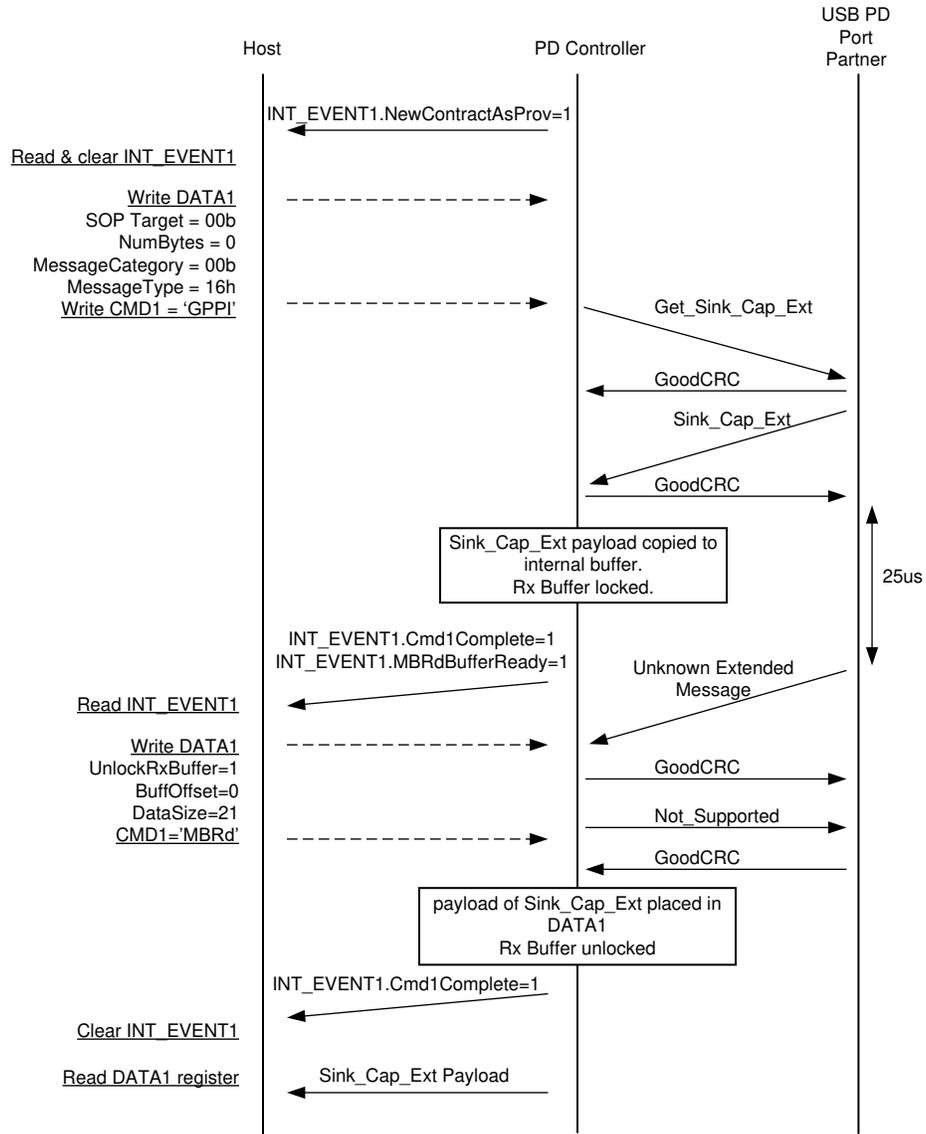


Figure 4-4. 'GPPI' Interrupted by an Unknown Extended Message

## 4.2.8 'SSrC' - PD Send Source Capabilities

**Table 4-10. 'SSrC' - PD Send Source Capabilities**

<b>Description</b>	The 'SSrC' Task instructs the PD Controller to send a SourceCapabilities message at the first opportunity while maintaining policy engine compliance.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'SSrC' Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails. The 'SSrC' Task shall be considered rejected if:</p> <ul style="list-style-type: none"> <li>• PD Controller is not in a Source role.</li> </ul> <p>The 'SSrC' Task shall be considered timed-out if:</p> <ul style="list-style-type: none"> <li>• The Source Capabilities message was sent but no GoodCRC was received.</li> </ul> <p>The 'SSrC' Task shall be considered successful if:</p> <ul style="list-style-type: none"> <li>• The Source Capabilities message was sent and a GoodCRC is received.</li> </ul>
<b>Side Effects</b>	Other registers can change as a result of the contract negotiation that begins with the new Source Capabilities message.
<b>Additional Information</b>	None

#### 4.2.9 'MBRd' - Message Buffer Read

**Table 4-11. 'MBRd' - Read from PD message buffer.**

Description	The MBRd Task instructs the PD Controller to read data from the extended message buffer previously received from the Port Partner.			
<b>INPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>	
	23	Reserved	Reserved (Write as 0).	
	22	UnlockRxBuffer	This input controls whether or not the PD controller unlocks its internal buffer after this Task is completed. It is recommended to unlock the internal buffer as soon as possible to make room for other incoming messages. It is important that the host only set this bit to 1 after it has received an alert that the Rx Buffer is locked (that is INT_EVENTx.MBRdBufferReady asserted).	
			0b	Do not clear the internal buffer, another 'MBRd' Task can be used later.
			1b	Clear the internal buffer after this Task completes and the requested data is in the DATAx register.
	21:16	DataSize	Number of data bytes to be read in from the message buffer. Up to 62 bytes can be read at after.	
15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible.		
<b>OUTPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>	
	511:16	DataByte1	First Byte of data read at BuffOffset.	
	15:0	MessageSize	Size of message in bytes.	
<b>Task Completion</b>	The MBRd Task completes after buffer data of DataSize at BuffOffset has been read from the message buffer.			
<b>Side Effects</b>	None			
<b>Additional Information</b>	This Task is required for the host to obtain the information from the response due to the usage of the 'GPPI' Task . The PD controller has a single buffer per port that is shared for these messages.			

### 4.3 Patch Bundle Update Tasks

The following tasks are used for updating a Patch Bundle.

#### 4.3.1 'PBMs' - Start Patch Burst Mode Download Sequence

**Table 4-12. 'PBMs' - Start Patch Burst Download Sequence**

Description	The 'PBMs' Task starts the patch loading sequence. This Task initializes the firmware in preparation for a patch bundle load sequence and indicates what the patch bundle will contain.			
<b>INPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>	
	Byte 6: Burst Mode Timeout			
	7:6	Reserved		
	5:0	Timeout value	Timeout value for this task. A non-zero value must be used, it is recommended to always use 0x32 in this field (5 seconds) (LSB of 100ms).	
	Byte 5: I2C target for downloading patch.			
	7	Reserved		
	6:0	I2C Target Address	The following target addresses are not valid: <ul style="list-style-type: none"> <li>• 0x00</li> <li>• The I2Ct target address of any port selected using the ADCINx pins. Refer to data-sheet.</li> </ul>	
	Bytes 0-3: Low Region Binary bundle size in of bytes: [ Byte4, Byte3, Byte2, Byte1]			
	39:32	Byte4 of bundle size		
	31:24	Byte3 of bundle size		
	23:16	Byte2 of bundle size		
	15:8	Byte1 of bundle size		
	<b>OUTPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>
7:0		PatchStartStatus	Status of the patch start.	
			0x00	Patch start success
			0x04	Invalid bundle size
			0x05	Invalid target address
0x06	Invalid Timeout value			
<b>Task Completion</b>	The 'PBMs' Task completes after output has a valid PatchStartStatus. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			
<b>Side Effects</b>	When the 'PBMs' is successful, the second target address will be set to the input value.			
<b>Additional Information</b>	The host can only issue a 'PBMs' Task to the I2Ct port of the PD controller. If the host issues 'PBMs' a second time, then the PD controller ignores the DATAx input, restarts the burst-mode timer, and resets the pointer to the beginning of the patch space in RAM. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMs' Task.			

### 4.3.2 'PBMc' - Patch Burst Mode Download Complete

**Table 4-13. 'PBMc' - Patch Burst Download Complete**

Description	The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.			
INPUT DATA	None			
OUTPUT DATA	Bit	Name	Description	
	319:288	acCalculatedCRC	The CRC calculated in FW for the configuration data.	
	287:256	acTransferredCRC	The CRC transferred along with the configuration data	
	255:240	Reserved	reads as 0	
	239:224	acIndicatedDataSize	The indicated DataSize in the transferred configuration data.	
	223:216	acHeaderVersion	The indicated header version in the transferred configuration data.	
	215:208	acFailCode	An error code indicating why the app config data failed to apply, if it failed to apply	
			0x00	AC_FAIL_NONE: No failure
			0x01	AC_FAIL_WRONG_HEADER_VERSION: The header version is expected to be 1 and was not
			0x02	AC_FAIL_TOO_MUCH_DATA: The DataSize field indicates that you are trying to load more configuration data that there is allocated SRAM for
	207:200	acState	The current internal state of the AppConfig state machine	
			0x00	AC_NODATA: No configuration data found yet, because we haven't started looking
			0x01	AC_LOADING_DEFAULT: Attempting to load configuration data from a factory default
			0x02	AC_LOADING_SRAM: Attempting to load configuration data from SRAM
			0x03	AC_LOADING_FLASH: Attempting to load configuration data from Flash
			0x04	AC_LOADING_I2C: Attempting to load configuration data from I2C
			0x05	AC_LOADING_DONE: Done loading configuration data, we found valid data
			0x06	AC_ERROR: A generic error state
			0x07	AC_DONE_SUCCESS: Completely done with the app customization process and the records were applied successfully.
	0x08	AC_DONE_FAIL: Completely done with the app customization process and the records were not applied		
199:192	configBundleGood	1 if the top-level state machine found a valid configuration bundle, otherwise 0.		
191:160	rpRomVersionExpected	The romVersionExpected in the transferred bundle's patch header		
159:144	rpBundleTotalSize	The bundleTotalSize in the transferred bundle's patch header		
143:128	rpBundleFlags	The bundleFlags in the transferred bundle's patch header		
127:96	rpPatchBodyCrc	The patchBodyCrc in the transferred bundle's patch header		
95:64	rpPatchHeaderCrc	The patchHeaderCrc in the transferred bundle's patch header		

**Table 4-13. 'PBMc' - Patch Burst Download Complete (continued)**

Description	The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.			
<b>OUTPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>	
	55:48	rpBundleSignature	The bundleSignature in the transferred bundle's patch header	
	47:40	rpState	The current internal state of the RomPatch state machine.	
			0x00	RP_NOPATCH: No patch has been loaded
			0x01	RP_LOADING: In the process of loading patch data
			0x02	RP_LOADINGDONE: All patch data has been received
			0x03	RP_RUNNING: A patch has been loaded and is running. Could also indicate that a NULL patch is active.
			0x04	RP_EARLYLOAD_SKIPPED: Indicates that the early boot process does not need to wait for a patch over I2C
			0x05	RP_UARTBOOTED: Checking for a patch in RAM
	0x06	RP_ERROR: A generic error state		
	39:32	patchBundleGood	0x01 if the top-level state machine found a good ROM patch, otherwise 0x00.	
	31:24	AppConfigPatchCompleteStatus	0x00	
			0x40	Warning
			0x80	Failure
	23:16	DevicePatchCompleteStatus	A return code indicating whether the RomPatch state machine executed successfully. This value is always valid, and reflective of the internal state of the RomPatch mechanism, but must only be considered if the bundle transferred did in fact include patch data.	
			0x00	Success
			0x20	Not ready
			0x40	Not a patch
			0x41	Patch header checksum mismatch
			0x42	Patch not compatible with this version of ROM
0x43			Patch code checksum mismatch	
0x44			Null patch received	
0x45	Error patch received			
15:8	cpReturn	Always returns success, there is no way for it to fail.		
Byte 1: Return Code				
7:4	rpReturnIndicator	The most significant nibble of the rpReturn value.		
		0x0	Success	
		0x2	Informational	
		0x4	Warning	
		0x8	Error	
3:0	acReturnIndicator	The most significant nibble of the acReturn value.		
		0x0	Success	
		0x2	Informational	
		0x4	Warning	
		0x8	Error	
<b>Task Completion</b>	The 'PBMc' Task completes as output has a valid DevicePatchCompleteStatus and AppConfigPatchCompleteStatus. This Task is rejected if the DATAx input does not contain the total patch size. If MODE register (0x03) is equal to 'APP', then this Task will be rejected.			

**Table 4-13. 'PBMc' - Patch Burst Download Complete (continued)**

<b>Description</b>	The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.
<b>Side Effects</b>	Before this Task completes it will change the I2C target address from the patch address back to the normal value. Upon successful completion of this Task the PD controller will change the MODE register (0x03) to 'APP ' and move to the application mode.
<b>Additional Information</b>	When the CMD1 register goes to 0 check the Output DATA register for status. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMc' Task.

### 4.3.3 'PBMe' - End Patch Burst Mode Download Sequence

**Table 4-14. 'PBMe' - Patch Burst Mode Exit**

<b>Description</b>	The 'PBMe' Task ends the patch loading sequence. This Task instructs the PD controller to complete the patch loading process.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	The 'PBMe' Task completes after it has ended the patch loading sequence. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.
<b>Side Effects</b>	When the 'PBMe' is successful, the second target address will be restored to the value configured by the ADCINx pins. The PD controller leaves the MODE register (0x03) as 'PTCH' and will wait for the patching process to restart.
<b>Additional Information</b>	If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMe' Task.

### 4.3.4 'GO2P' - Go to Patch Mode

**Table 4-15. 'GO2P' - Forces PD Controller to Return to 'PTCH' Mode and Wait for Patch Over I2C**

<b>Description</b>	The 'GO2P' Task causes the PD controller to re-enter the patch mode (MODE = 'PTCH').
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	Byte 1: Standard Task Return Code.
<b>Task Completion</b>	<p>The 'GO2P' Task completes after the PD controller has re-entered the patch mode.</p> <ul style="list-style-type: none"> <li>If the PD controller has re-entered the patch mode and the MODE register reads as 'PTCH'.</li> </ul> <p>The 'GO2P' Task is considered rejected if:</p> <ul style="list-style-type: none"> <li>The PD controller did not enter the 'APP ' mode without receiving a patch over I2C.</li> <li>BOOT_STATUS.PatchConfigSource does not read as 3h or 4h.</li> </ul>
<b>Side Effects</b>	When the 'GO2P' Task is successful, the MODE register will read as 'PTCH' and the USB PD PHY will be disabled. The PD Controller can temporarily NAK I2C transactions. The host must wait for the IRQ signal to assert (because INT_EVENT1.ReadyForPatch is asserted), and then push the patch as soon as possible.
<b>Additional Information</b>	The 'GO2P' Task must only be used when the ADCINx configuration option NegotiateHighVoltage is used.

## 4.4 System Tasks

#### 4.4.1 'DBfg' - Clear Dead Battery Flag

**Table 4-16. 'DBfg' - Clear Dead Battery Flag**

<b>Description</b>	The 'DBfg' Task is used to clear the dead battery flag. This Task does not disable the PP_EXT input switch that can have been enabled during dead battery operation.
<b>INPUT DATA</b>	None
<b>OUTPUT DATA</b>	None
<b>Task Completion</b>	The 'DBfg' Task completes after the effects of clearing the Dead Battery Flag are complete.
<b>Side Effects</b>	The Dead Battery Flag causes the PD Controller to take specific actions, so clearing this flag will have side effects. PD Controller 's power input is forced to VBUS until the Dead Battery Flag is cleared, so executing this Task will change PD Controller 's power input.
<b>Additional Information</b>	None

There are several limitations placed on the PD controller while the Dead-Battery Flag is asserted (PowerPathStatus.PowerSource = 10b).

- A Hard Reset will not be transmitted while in the sink role (on either port).
- VBUS is selected as the main supply for the PD controller, even if the 3.3 V input is present.
- The PD controller will reject PR\_Swap requests to become source (on either port).
- A port connected to a source will only act as a Type-C sink regardless of the configuration.
- If no Source Capabilities message is received after the boot process is complete (Status.ActingAsLegacy=11b), the PD controller will not send a Hard Reset until the Dead-Battery Flag is cleared even if the SinkWaitCapTimer expires.

#### 4.4.2 'I2Cr' - I2C Read Transaction

**Table 4-17. 'I2Cr' - Executes I2C Read Transaction on I2Cc**

<b>Description</b>	The 'I2Cr' task can be used to cause the PD controller to read from a specified target address and register offset using a I2C read transaction through the I2Cc_SDA and I2Cc_SCL pins.		
<b>INPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>
	Byte 3: Number of bytes to read from the target.		
	7:0	NumBytes	
	Byte 2: Register offset to use in the I2C read transaction.		
	7:0	RegisterOffset	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
<b>OUTPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>
	Bytes 2-65: Data Bytes read from the target (in order received)		
	511:0	Data	
	Byte 1: Standard Task Return Code.		
<b>Task Completion</b>	The PD controller completes after it has successfully read the specified number of bytes, or the I2C transaction terminated for some other reason.		
<b>Side Effects</b>	This task causes the PD controller to issue a command on the I2Cc port. It can result in INT_EVENTx.I2CControllerNACKed being asserted.		
<b>Additional Information</b>	The 'I2Cr' command cannot be sent within 5s from sending a previous 'I2Cr' command. This allows the PD controller to complete all I2C transactions.		

#### 4.4.3 'I2Cw' - I2C Write Transaction

**Table 4-18. 'I2Cw' - Executes I2C Write Transaction on I2Cc**

<b>Description</b>	The 'I2Cw' task can be used to cause the PD controller to write a particular I2C transaction using I2Cc_SDA and I2Cc_SCL.		
<b>INPUT DATAx</b>	<b>Bit</b>	<b>Name</b>	<b>Description</b>
	Bytes 5-14: Payload for the I2C transaction		
	Byte 4: Register Offset for the I2C transaction		
	7:0	Register offset	
	Bytes 2-3: Length		
	15:8	Reserved	
	7:0	Number of bytes in the transaction payload.	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
<b>OUTPUT DATAx</b>	Byte 1: Standard Task Return Code		
<b>Task Completion</b>	The PD controller maintains a queue of transactions to send on the I2Cc port. If the PD controller has been configured to send transactions upon certain events, it is possible there is a transaction in the queue when the 'I2Cw' task is received. In that case the task will complete successfully after the transaction is inserted into the queue. If the PD controller fails to insert the task into the queue for any reason, the task is rejected. Therefore, when this task is completed successfully it does not guarantee that the I2C transaction is complete. If possible, the host must use the 'I2Cr' 4CC task to confirm the write was successful.		
<b>Side Effects</b>	When successful, this task will cause the PD controller to issue a command on the I2Cc port. This can result in INT_EVENTx.I2CControllerNACKed being asserted.		
<b>Additional Information</b>	If the DATAx register is written with more than 14 bytes, all bytes beyond byte 14 are ignored. The PD controller has a limit on the maximum length of the I2C write transaction. The 'I2Cw' command cannot be sent within 5s from sending a previous 'I2Cw' command. This allows the PD controller to complete all I2C transactions.		

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## 5.1 PD Controller Application Customization

The PD Controller application binary can be pushed over I2C using the I2Ct port, or the PD controller can read it from an external EEPROM at target address 0x50 on the I2Cc port. The PD Controller application binary provides a way to customize and initialize the settings of the PD Controller. It allows for any register bit accessible through the Host Interface to be changed *before* the PD Controller application starts normal operation, to configure system-related settings that must be correct before any application decision is made. TI provides a GUI tool to create the PD Controller application binary.

## 5.2 Loading a Patch Bundle

The patch bundle can contain Application Customization data and a Patch binary that modifies the default application firmware in the PD controller. This section will describe how the host can load the patch bundle. The host uses the I2Ct bus for all transactions related to loading the patch bundle. As noted in the flow diagram below, the I2C target address varies depending upon which mode the PD controller is in. The Patch Burst Mode allows the host to push the Patch Bundle to multiple PD controllers simultaneously.

The following flow diagram illustrates the normal successful patch loading process. Other error handling steps can be necessary depending upon the nature of the errors encountered for a particular system. The EC can reset and restart the patch process by issuing a 'PBMe' 4CC Task.

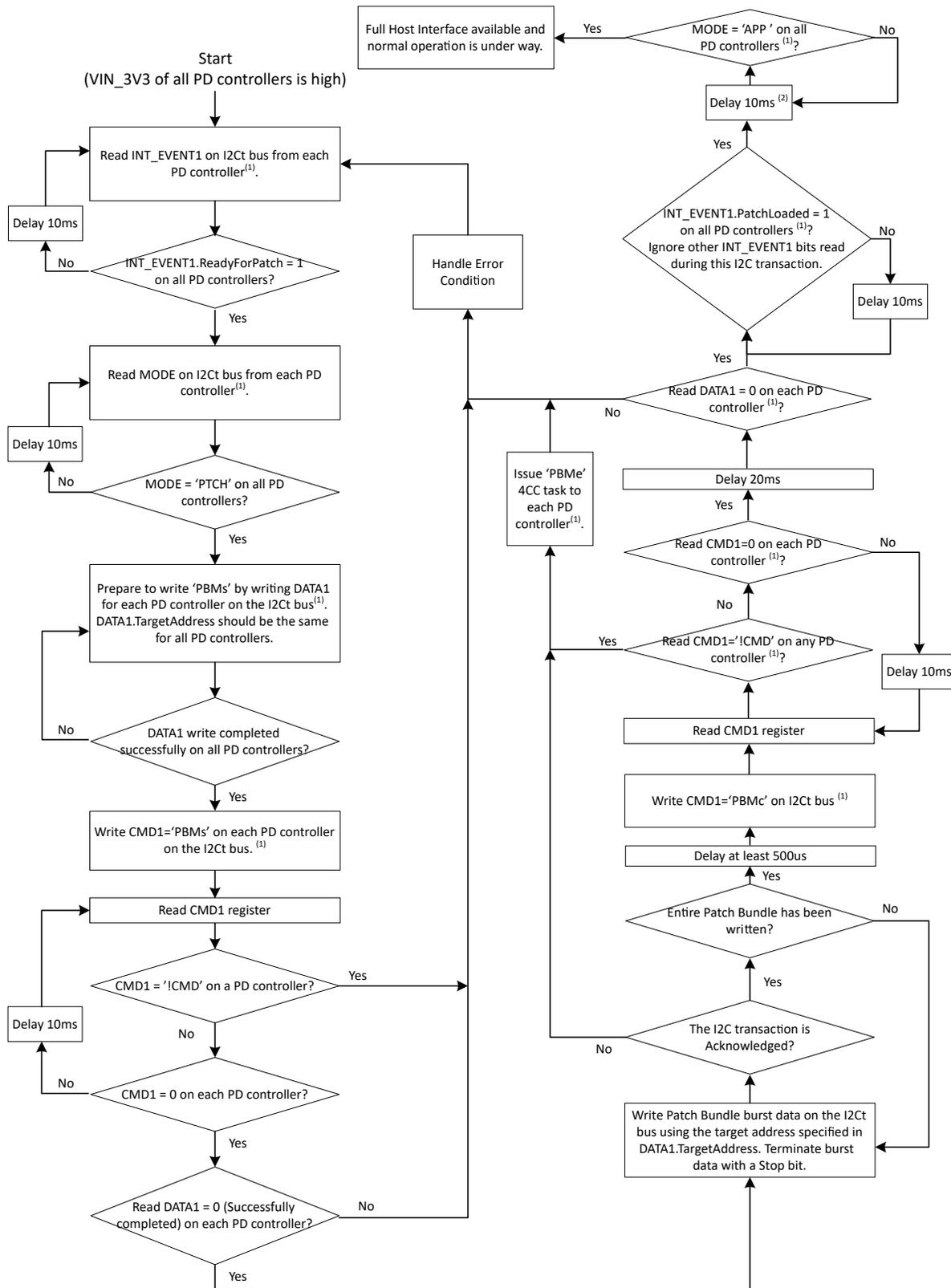
The following table summarizes the target addresses in the different modes of operation.

**Table 5-1. Use of Target Addresses During Different Modes of Operation**

MODE Register Read-Back Value	I2Ct
	Target Address 1
'BOOT'	As configured by ADCINx pins. This is the "Fundamental" I2C target address. BOOT indicates that the PD controller is in the boot stage due to a bad firmware image or incorrect ADCINx settings. APP indicates that the firmware has successfully loaded and is in normal operation. PTCH indicates that the PD controller is waiting for a patch or is in the patch process using the PBMx commands.
'PTCH' <sup>(1)</sup>	
'APP' <sup>(2)</sup>	

(1) A successful 'PBMs' Task puts the PD controller into the 'PTCH' mode.

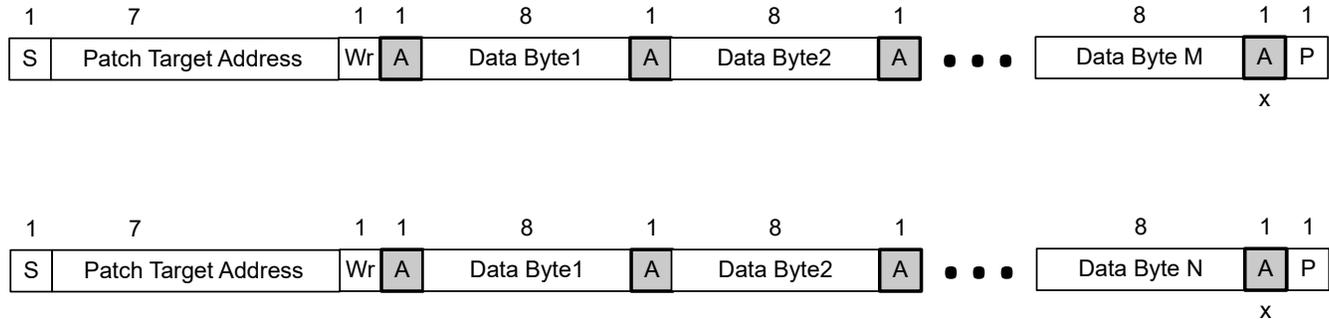
(2) A successful 'PBMc' Task puts the PD controller into the 'APP' mode.



<sup>(1)</sup> Use the fundamental I2C target address of each PD controller.  
<sup>(2)</sup> This delay before reading the MODE register, is optional but recommended.

**Figure 5-1. Flow for Pushing a Patch Bundle Over the I2C Bus to Multiple PD Controllers at the Same Time**

While the host is writing the Patch Bundle burst data, the I2C protocol in the following figure must be followed. The host can send the entire Patch Bundle in a single I2C transaction, or it can break it up into multiple transactions. The PD controller increments the pointer into its patch memory space with each byte received on the Patch Target address that was configured by DATA1.TargetAddress as part of the 'PBMs' 4CC Task. The EC can re-issue a 'PBMs' 4CC Task or it can issue a 'PBMe' 4CC Task in order to reset the pointer.



**Figure 5-2. Protocol of Patch Bundle Burst Data Assuming it is Broken Into Two Transactions**

### 5.3 GPIO Events

**Table 5-2. GPIO Events**

Event #	Event Name	I/O	Description
158	WAIT_nPG	I	GPIO from battery charger to indicate to the PD controller can communicate over I2C during a dead battery power up condition.
157	LIQUID_DETECTED	O	GPIO is asserted when liquid is detected on the SBU1/2 pins. When liquid is no longer detected on the SBU1/2 pins the GPIO will be de-asserted.
156	LIQUID_NMOS_CONTROL	O	GPIO used to enable the NMOS in the external liquid detection circuit. The GPIO will toggle during liquid detection.
155	LIQUID_PMOS_CONTROL	O	GPIO used to enable the PMOS in the external liquid detection circuit. The GPIO will toggle during liquid detection.
76	PdNegotiationInProgress	Output	When in source mode, this GPIO is asserted after a Request message is received, before sending the Accept message. The GPIO is de-asserted after the PS_RDY message is sent. When in sink mode, this GPIO is asserted right before sending a Request message, and de-asserted after a PS_RDY message is received. In either mode, the GPIO is de-asserted when a detach occurs.
75	AttachedAsSink	Output	When the PD controller has a port that is connected to a Source, this GPIO will be asserted. The GPIO is de-asserted upon disconnect, hard reset, during power-role swap and during fast-role swap only if none of the ports in the PD controller are connected to a source.
73	EnableSource	Output	PD controller will assert this GPIO when acting as a source (implicit or explicit contract)
65	Load_Switch_Drive	Output	When the PD controller enables the PP_EXT1 sinking path, it will pull the selected GPIO low to enable a load-switch. When the PD controller disables the PP_EXT1 sinking path, it will drive the selected GPIO high.
61	Dp_Dm_Mux_Enable_Event	Output	This GPIO must be used to enable/disable a USB 2.0 D+ /D-mux. The GPIO is driven high upon connection, and low upon disconnect on the port.
50	Debug_Accessory_Mode_Event	Output	Output: This GPIO is asserted high when a Debug Accessory is attached on the port.

**Table 5-2. GPIO Events (continued)**

Event #	Event Name	I/O	Description
45	Prevent_DRSwap_To_UFP_Event	Input	When the GPIO is high, the PD controller will reject any DR_Swap messages from the Port Partner requesting to change the data-role from DFP to UFP.
44	UFP_Indicator_Event	Output	The GPIO is driven high when the data role of any port in the PD controller is UFP.
43	Barrel_Jack_Event	Input	When this GPIO is high, the PD controller interprets it to mean that a barrel-jack adaptor is connected and the system has Unconstrained power. A falling edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 0 and TX_SCEDB.SourceInputs[0] to 0. A rising edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 1 and TX_SCEDB.SourceInputs[0] to 1.
35	Fault_Condition_Active_Low_Event	Output	Asserts low on an overcurrent event on the port.
33	Fault_Input_Event	Input	When set low by the system, the port enters the Type-C Error Recovery State. When set high, no action is taken.
29	UFP_DFP_Event	Output	Output: Asserted high when the port is operating as UFP. Asserted low when port is operating as DFP.
13	SourcePDOContractBit2	Output	Output: Bit2 of binary encoded outputs indicating when a Source PDO1 through PDO7 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
12	SourcePDOContractBit1	Output	Output: Bit1 of binary encoded outputs indicating when a Source PDO1 through PDO7 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
11	SourcePDOContractBit0	Output	Output: Bit0 of binary encoded outputs indicating when a Source PDO1 through PDO7 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
10	SourcePDO4Contract	Output	Output: Asserted high when a Source PDO4 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
9	SourcePDO3Contract	Output	Output: Asserted high when a Source PDO3 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
8	SourcePDO2Contract	Output	Output: Asserted high when a Source PDO2 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
7	SourcePDO1Contract	Output	Output: Asserted high when a Source PDO1 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO1 has been negotiated.
3	Cable_Orientation_Event	Output	Output: Indicates the plug orientation on the port. Low when the plug is connected upside-up (CC1 connected to CC in cable) or disconnected. High when plug is connected upside-down (CC2 connected to CC in cable).
1	PlugEvent	Output	Output: Asserted high when plug event (attached state) has occurred on the port, otherwise low.
0	NullEvent	NA	No event associated with this GPIO.

## 5.4 AUTO\_NEGOTIATE\_SINK Register

In general, writing to AUTO\_NEGOTIATE\_SINK register while a sink contract is in place does not cause an automatic renegotiation, and changes take effect the next time a contract is negotiated. The ANeg command forces a re-evaluation of this register and a new Request message is issued if appropriate.

However, if a Sink PPS Explicit Contract is already in place there are some fields that do cause the PD controller to automatically reevaluate the register and send a new Request message if appropriate:

- PPSOutputVoltage
- PPSOperatingCurrent
- PPSEnableSinkMode
- PPSRequestInterval
- RequireFullVoltageRange
- PPSSourceMode

If PPSEnableSinkMode is changed while a Sink PPS Explicit Contract is not already in place the PD controller also automatically re-evaluates the register and sends a new Request message if appropriate.

If the first four bytes of this register are written as zero, then the PD controller will always request a 5V Fixed Supply contract at 100mA ; unless PPSEnableSinkMode is asserted in which case an APDO can be selected.

To implement Sink PPS features in this register, the host shall provide an APDO in the TX\_SINK\_CAPS register. If the PD controller is evaluating a PPS supply type, it only uses the first APDO in the TX\_SINK\_CAPS register to determine when to assert the Capability Mismatch bit. Therefore, it is recommended that the host only have one APDO in the TX\_SINK\_CAPS register. In order to not assert the Capability Mismatch bit, the source APDO advertised by the source must meet these conditions:

- RX\_SOURCE\_CAPS.APDO.MinVoltage <= TX\_SINK\_CAPS.APDO.MinVoltage
- RX\_SOURCE\_CAPS.APDO.MaxVoltage >= TX\_SINK\_CAPS.APDO.MaxVoltage
- RX\_SOURCE\_CAPS.APDO.MaxCurrent >= TX\_SINK\_CAPS.APDO.MaxCurrent

If the source fails any of the conditions above, a sink PPS contract is still requested if one of the source APDOs meets these conditions:

- RX\_SOURCE\_CAPS.APDO.MinVoltage <= AUTO\_NEGOTIATE\_SINK.PPSOutputVoltage
- RX\_SOURCE\_CAPS.APDO.MinVoltage >= AUTO\_NEGOTIATE\_SINK.PPSOutputVoltage
- RX\_SOURCE\_CAPS.APDO.MaxCurrent >= AUTO\_NEGOTIATE\_SINK.PPSOperatingCurrent

During PPS operation, if the host sets the PPSOutputVolage field to a value outside what the source APDO can deliver as reported in the RX\_SOURCE\_CAPS register, then a Fixed Supply PDO is selected and the sink path can be automatically disabled (see AUTO\_NEGOTIATE\_SINK.PPSDisableSinkUponNonAPDOContract).

If PPS is enabled, then an APDO that fulfills the requirements is given highest priority.

The following is a high-level summary of how this register drives the PDO selection when PPS is disabled or no matching APDO is found.

- Parse the received PDOs in the register RX\_SOURCE\_CAPS. Discard any PDO whose voltage range is below ANMinVoltage or above ANMaxVoltage.
- Calculate the PDO power for each received PDO (RX\_SOURCE\_CAPS.SourcePdoX). Rank all PDOs according to the PDO power.
  - PDO Power = Voltage × MaximumCurrent (Fixed Supply)
  - PDO Power = MinimumVoltage × MaximumCurrent (Variable Supply)
  - PDO Power = MaximumPower (Battery Supply)
- The PDO with maximum PDO Power that also passes the voltage check is selected. In case there are multiple PDOs that pass the voltage check and have the same maximum PDO Power, tie breakers are applied as described below:
  - A Fixed supply type is preferred, and Variable supply type is preferred over Battery supply type.

- If the PDOs being compared have the same supply type, then ANRDOPriority specifies how to break the tie.

#### 5.4.1 AUTO\_NEGOTIATE\_SINK Usage Example 1

When attached to a 36W source the PD controller has RX\_SOURCE\_CAPS:

- PDO1: 5V at 3A
- PDO2: 9V at 3A
- PDO3: 15V at 2.4A
- PDO4: 20V at 1.8A

The PD controller has TX\_SINK\_CAPS set as:

- PDO1: 5V at 3A (fixed)
- PDO2: 20V at 3A (fixed)

The PD controller has AUTO\_NEGOTIATE\_SINK set as:

- AUTO\_NEGOTIATE\_SINK = 0
- AUTO\_NEGOTIATE\_SINK.ANSinkCapMismatchPower = 240d (60W)
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinPower = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinVoltage = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO\_NEGOTIATE\_SINK.NoCapabilityMismatch = x (see table below)
- AUTO\_NEGOTIATE\_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 60 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

**Table 5-3. AUTO\_NEGOTIATE\_SINK Usage Example 1**

AUTO_NEGOTIATE_SINK		ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	0	1.8A	3.0A	4	1
1	0	1.8A	1.8A	4	0
1	1	2.4A	2.4A	3	0

#### 5.4.2 AUTO\_NEGOTIATE\_SINK Usage Example 2

When attached to a 36W source the PD controller has RX\_SOURCE\_CAPS:

- PDO1: 5V at 3A
- PDO2: 9V at 3A
- PDO3: 15V at 2.4A

The PD controller has TX\_SINK\_CAPS set as:

- PDO1: 5V at 0.1A (fixed)
- PDO2: 20V at 3A (fixed)

The PD controller has AUTO\_NEGOTIATE\_SINK set as:

- AUTO\_NEGOTIATE\_SINK = 0
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinPower = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinVoltage = 0
- AUTO\_NEGOTIATE\_SINK.ANMinVoltage = 20V
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO\_NEGOTIATE\_SINK.NoCapabilityMismatch = x (see table below)
- AUTO\_NEGOTIATE\_SINK.ANRDOPriority = 0

The settings give the results in the table below. Note that ANMaxVoltage computed as 20V, but it does not affect the result. Because the ANMinVoltage was set to 20V, and the source is not offering 20V none of the source PDOs fulfill the sink requirements. Even though ANSinkCapMismatchPower=0 in this example, because the voltages offered are insufficient, the capability mismatch bit can still be set.

**Table 5-4. AUTO\_NEGOTIATE\_SINK Usage Example 2**

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	3.0A	3.0A	1	1
1	3.0A	3.0A	1	0

### 5.4.3 AUTO\_NEGOTIATE\_SINK Usage Example 3

When attached to a 45W source the PD controller has RX\_SOURCE\_CAPS:

- PDO1: 5V at 3A
- PDO2: 9V at 3A
- PDO3: 15V at 3A
- PDO4: 20V at 2.25A

The PD controller has TX\_SINK\_CAPS set as:

- PDO1: 5V at 3A (fixed)
- PDO2: 20V at 2.25A (fixed)

The PD controller has AUTO\_NEGOTIATE\_SINK set as:

- AUTO\_NEGOTIATE\_SINK = 0
- AUTO\_NEGOTIATE\_SINK.ANSinkCapMismatchPower = 180d (45W)
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinPower = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinVoltage = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO\_NEGOTIATE\_SINK.NoCapabilityMismatch = 0
- AUTO\_NEGOTIATE\_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 45W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

**Table 5-5. AUTO\_NEGOTIATE\_SINK Usage Example 3.**

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	2.25A	2.25A	4	0
1	3.0A	3.0A	3	0

### 5.4.4 AUTO\_NEGOTIATE\_SINK Usage Example 4

When attached to a 100W source the PD controller has RX\_SOURCE\_CAPS:

- PDO1: 5V at 3A
- PDO2: 9V at 3A
- PDO3: 15V at 3A
- PDO4: 20V at 5A

The PD controller has TX\_SINK\_CAPS set as:

- PDO1: 5V at 3A (fixed)
- PDO2: 20V at 5A (fixed)

The PD controller has AUTO\_NEGOTIATE\_SINK set as:

- AUTO\_NEGOTIATE\_SINK = 0
- AUTO\_NEGOTIATE\_SINK.ANSinkCapMismatchPower = 240d (60W)
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinPower = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMinVoltage = 1
- AUTO\_NEGOTIATE\_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO\_NEGOTIATE\_SINK.NoCapabilityMismatch = 0
- AUTO\_NEGOTIATE\_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 100W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

**Table 5-6. AUTO\_NEGOTIATE\_SINK Usage Example 3.**

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	5A	5A	4	0
1	5A	5A	4	0

## Revision History

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (September 2023) to Revision A (March 2024)</b>	<b>Page</b>
• Added 'GPPI' - PD Get Port Partner Information section.....	62
• Added 'MBRd' - Message Buffer Read section.....	69
• 'I2Cr' - I2C Read Transaction timing clarification in Addition Information.....	77
• 'I2Cw' - I2C Write Transaction timing clarification in Additional Information .....	77
• GPIO Events updates and clarifications.....	81
• Added AUTO_NEGOTIATE_SINK Register section.....	83

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