Test Report
June 2016

PMP15018 –Industrial 24Vin Dual output with 1.2V and 1V at 10A

ABSTRACT

PMP15018 is a power Evaluation Module to showcase the implementation of TPS56C215 and TPS54541 to power two rails of a Processor from 24 V DC bus. This design also displays the trade-off between efficiency and solution size while operating at low and high frequencies. This design is made on a 2.5 inch X 2.5 inch board demonstrating the small printed-circuit-board areas that may be achieved while using TPS56C215. All the converters on the board are designed for a DC regulation of +/- 2% and DC+AC regulation of +/- 5%.

Contents

1. Introduction

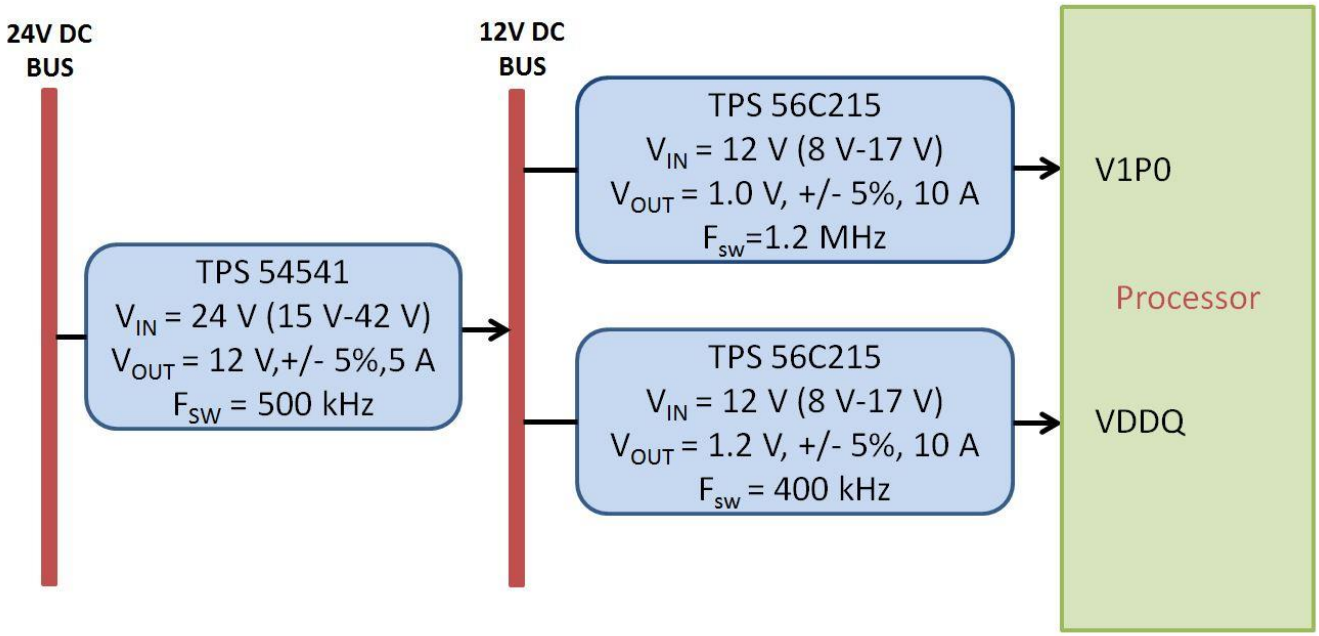
1.1 Description

The TPS56C215 dc/dc converter is a synchronous buck converter designed to provide up to a 14 A output. The input (V_{IN}) is rated for 4.5 V to 17 V. The TPS56C215 uses a proprietary DCAP3 Control mode and a MODE pin is used to select output current limit, switching frequency, and Forced Continuous Conduction Mode (FCCM)/Discontinuous Conduction Mode (DCM) operation. The high-side and low-side MOSFETs are incorporated inside the TPS56C215 package along with the gate drive circuitry. The low drain-to source on-resistance of the MOSFET allows the TPS56C215 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS56C215 provides adjustable slow start and undervoltage lockout inputs and a power good output.

The TPS54541 device is a 42 V, 5 A step-down regulator with an integrated high-side MOSFET. The device survives load dump pulses up to 45 V per ISO 7637. Current mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no-load supply current to 152 µA. When the enable pin is pulled low, the shutdown supply current is reduced to 2 µA. Cycle-by-cycle current limit, frequency foldback, and thermal shutdown protect internal and external components during an overload condition. The output voltage startup ramp is controlled by the soft-start pin that can also be configured for sequencing and tracking. An opendrain power-good signal indicates the output is within 93% to 106% of the nominal voltage.

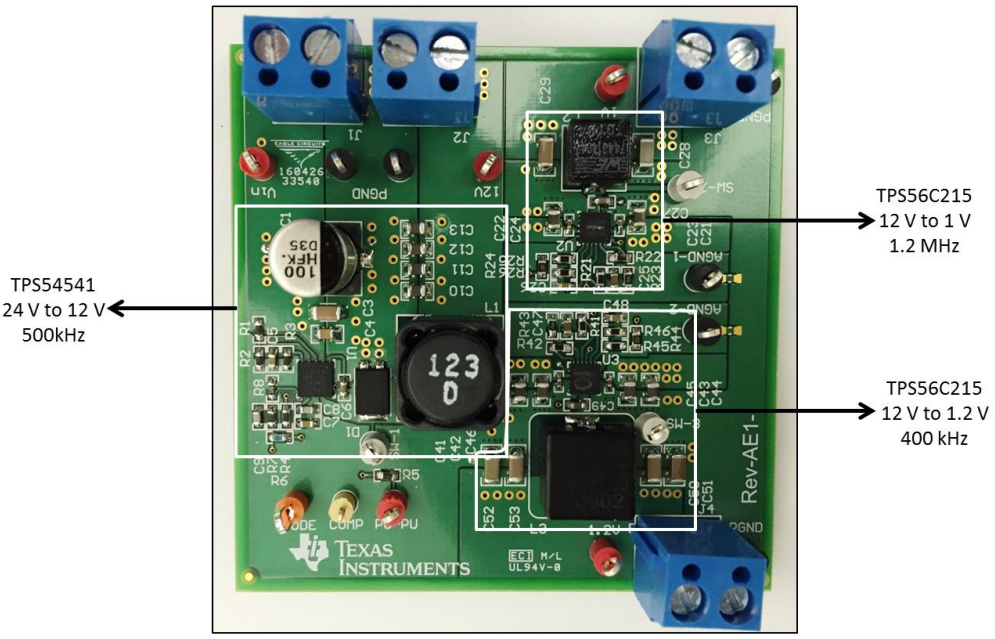
This design uses TPS54541 to step-down 24 V dc to 12 V dc at a frequency of 500 kHz. The converter is designed to operate with an input range of 15 V to 42 V and supports a load current of 5 A. To step down 12 V to processor level voltages of 1 V and 1.2 V, two TPS56C215 converters operating at different frequencies are used. The TPS56C215 converter which steps down 12 V to 1 V is designed to operate at a frequency of 1.2 MHz and the other TPS56C215 converter steps down 12 V to 1.2 V operates at a frequency of 400 kHz. Both the converters are configured to a maximum output current of 10 A, DCM mode, output DC regulation less than +/- 2% and DC+AC regulation less than +/- 5%.

The block diagram of the design is as shown below.



1.2 Board Photo

The board dimensions are 2.5 inch X 2.5 inch. The top view of the board is as shown below. The three converters on the board are marked for identification.



1.3 Test Setup

This section describes how to properly connect, set up, and use the evaluation module. The PMP15018 is provided with input/output connectors and test points as shown in Table 1. A power supply capable of supplying voltage greater than 24V and 3 A must be connected to J1 through a pair of 20-AWG wires or better. J2 can be used to load the TPS54541 converter up to 5 A, if the converter is to be tested alone without loading on J3 and J4. A maximum load of 10 A each can be connected to J3 and J4 through a pair of 20-AWG wires or better. Wire lengths must be minimized to reduce losses in the wires.

As EN of TPS56C215 has internal pull up, the converter starts up with a PGOOD high from TPS54541 even without external pull up. The PG-PU may be used if user wants to use external pull up source for EN.

Table 1. Connectors and Test Points

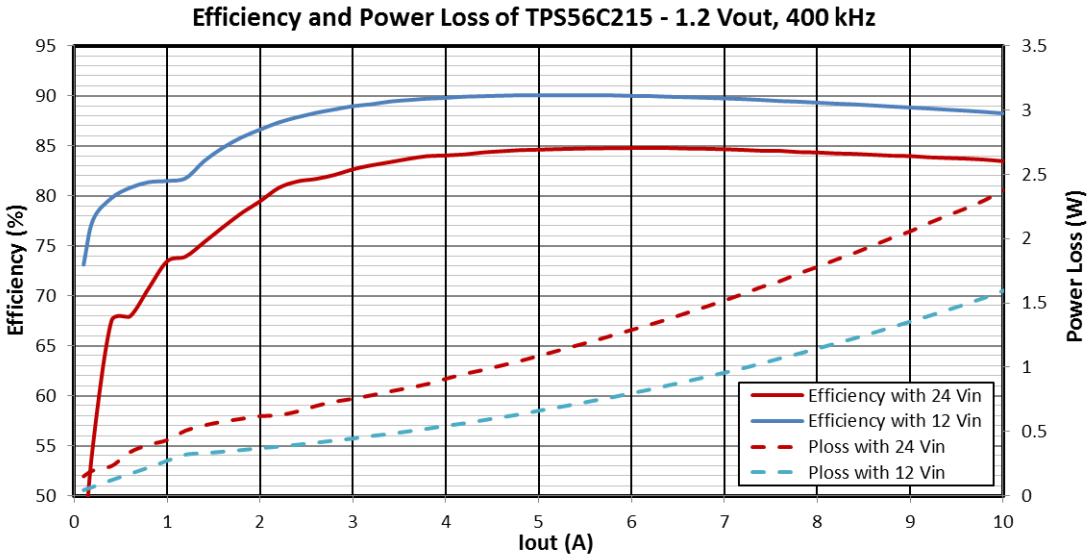
Reference Designator	Function
J1	V_{IN} input voltage connector. Range 15 V to 40 V
J2	V_{OUT}, 12 V at 5 A maximum
J3	V_{OUT}, 1 V at 10 A maximum
J4	V_{OUT}, 1.2 V at 10 A maximum
Vin	V_{IN} test point
12V	12 V test point
1V	1 V test point
1.2V	1.2 V test point
PGND	GND test point
AGND-1	AGND test point of 12 V to 1 V converter
AGND-2	AGND test point of 12 V to 1.2 V converter
SW-1	SW node test point of 24 V to 12 V, TPS54541 converter
SW-2	SW node test point of 12 V to 1 V, TPS56C215 converter
SW-3	SW node test point of 12 V to 1.2 V, TPS56C215 converter
BODE	Test point between voltage divider network and output of TPS54541 converter. Used for loop response measurements
COMP	COMP test point of TPS54541 converter. Used for loop response measurements
PG-PU	PGood Pull up to enable 12 V to 1 V, TPS56C215 converter. Maximum 5 V

2. TPS56C215 – 12 V to 1.2 V at 400 kHz

2.1 Efficiency and Power Loss

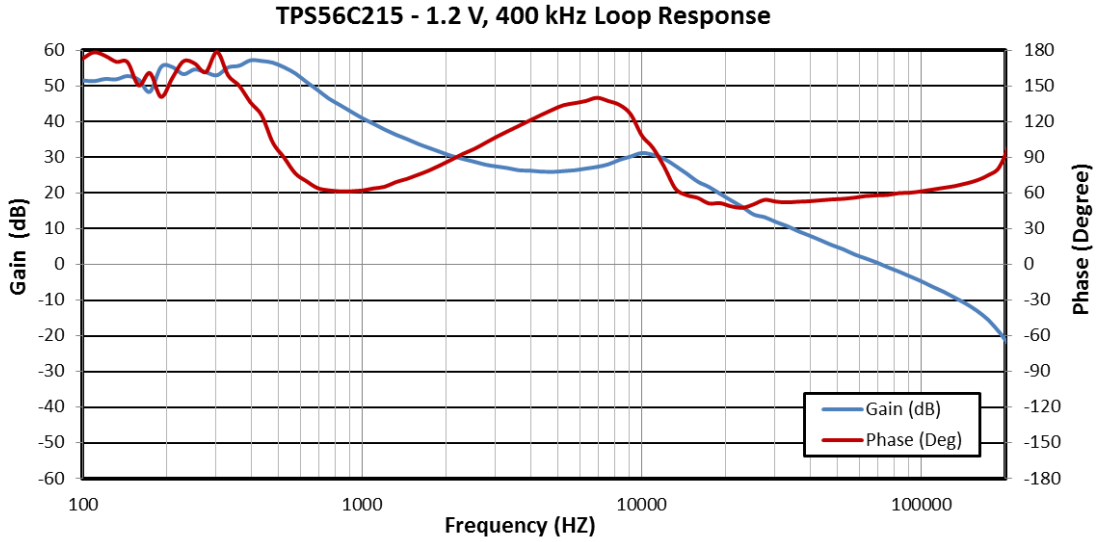
The efficiency and power loss tests on the entire system by applying 24 V_{IN} to TPS54541 at J1 and obtaining 1.2 V_{OUT} of TPS56C215 at J4 is done. The performance of TPS56C215 converter alone is

done by applying 12 V_{IN} at J2 and disabling TPS54541. The efficiency and power loss for both cases are shown below.



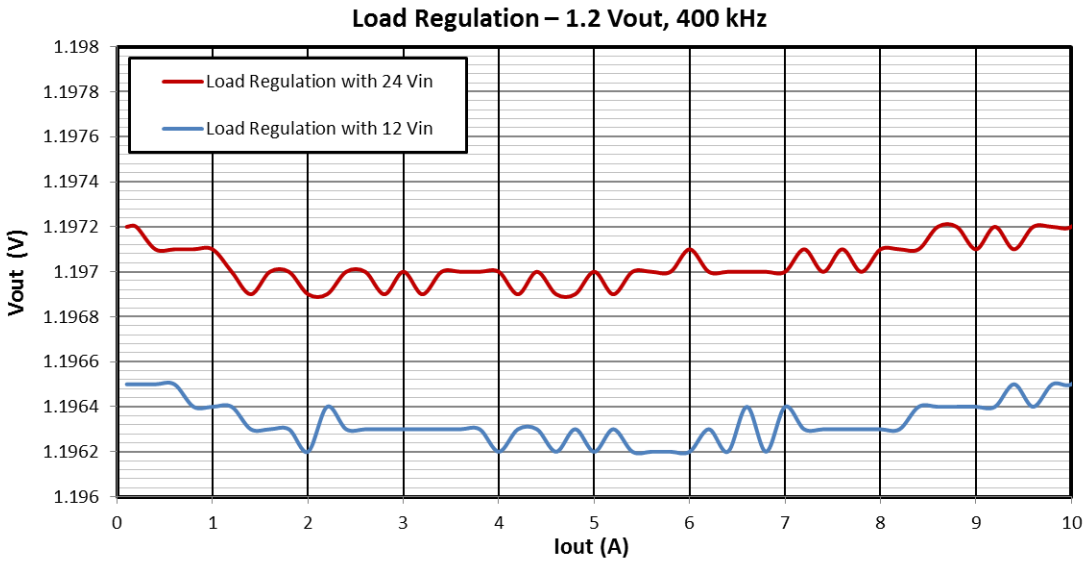
2.2 Loop Response

The plot below shows the loop-response characteristics of TPS56C215 – 1.2 V, 400 kHz converter. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 7 A. The phase margin measured is 59 degrees.



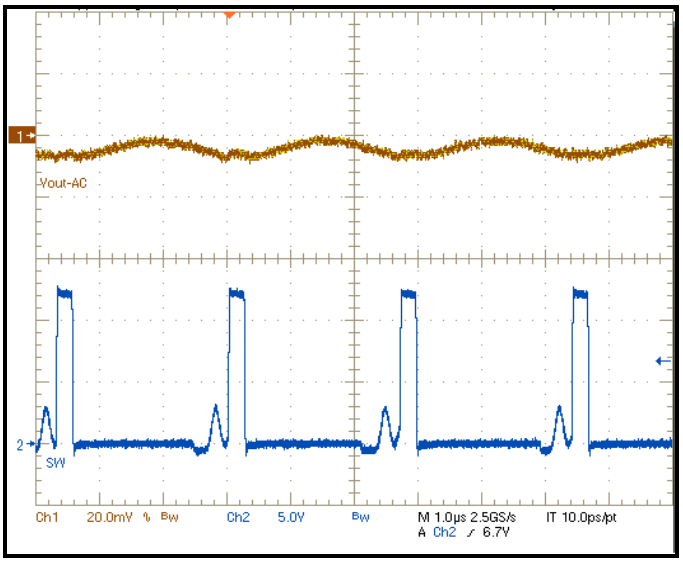
2.3 Load regulation

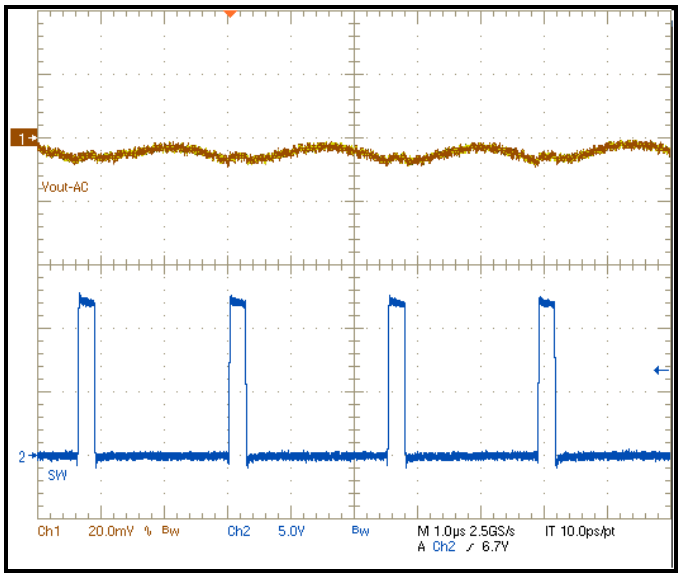
The Load regulation of TPS56C215 – 1.2 V, 400 kHz converter in both cases with 24 V_{IN} applied to TPS54541 at J1 and 12 V_{IN} applied at J2 is shown below.



2.4 Output Ripple

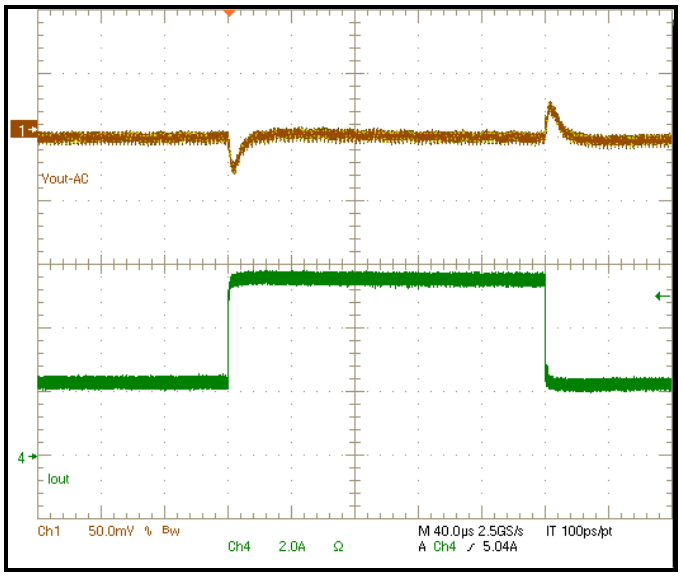
The output Voltage graphs of TPS56C215 – 1.2 V, 400 kHz converter shown below are AC coupled for 1A and 7A load respectively. The output voltage is measured across output capacitors by tip and barrel method. The length of the ground wire should be as small as possible to avoid switching noise getting coupled.





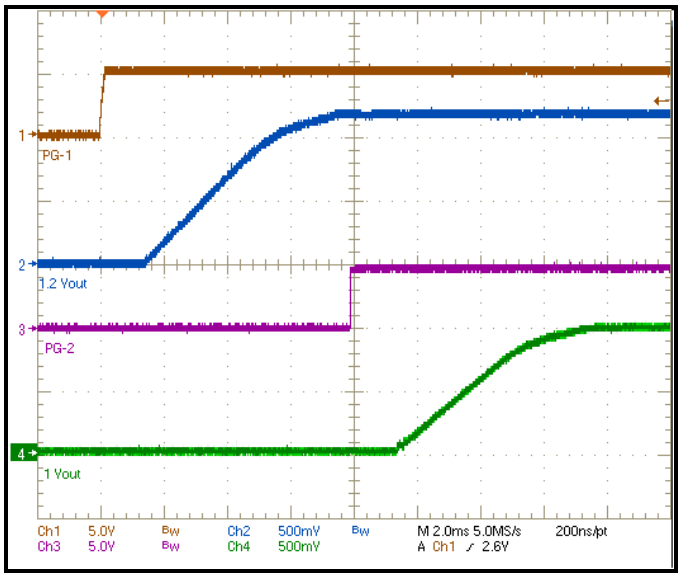
2.5 Transient Response

The figures below show TPS56C215 – 1.2 V, 400 kHz converter's response to load transients. The current step is from 2 A to 6 A. The current step slew rate is 2.5 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

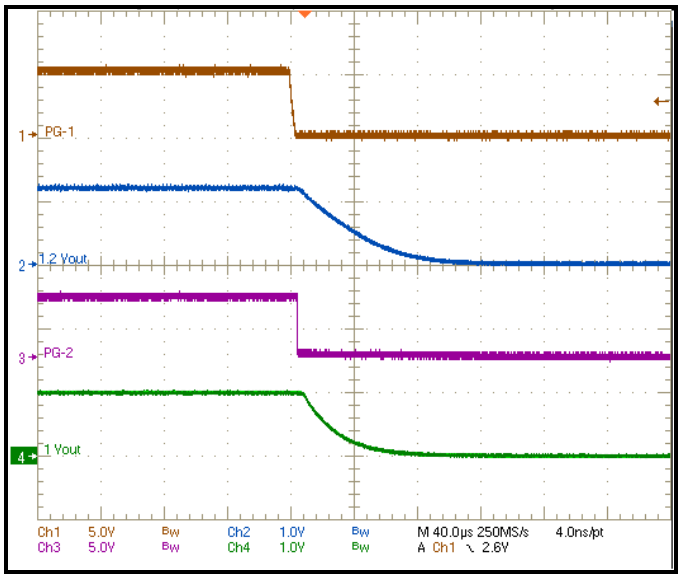


2.6 Start Up and Shut Down

The Start Up of the converters is designed to be sequential. The TPS56C215 – 1.2 V, 400 kHz converter powers up immediately after the PGOOD signal from TPS54541 (PG-1) goes high. Once the output voltage reaches 93% the PGOOD (PG-2) is de-asserted and floats after a 200 µs de-glitch time which is pulled high by EN of TPS56C215 – 1 V, 1.2 MHz. The soft start capacitor is selected to set a soft start time of 4.7 µs for both the converters. Start Up sequence of converters with full load is shown below.

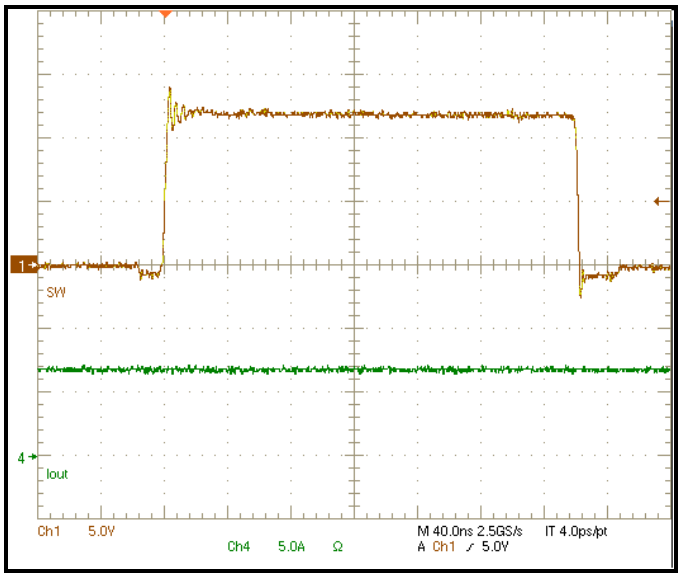


The Shut Down is also sequential. Shut Down of TPS54541 pulls the PG-1 low which causes the Shut Down of TPS56C215 – 1.2 V, 400 kHz converter. The TPS56C215 – 1 V, 1.2 MHz converter follows immediately upon PG-2 going low. Shut Down sequence of converters operating at their full load is shown below.



2.7 Switch Node

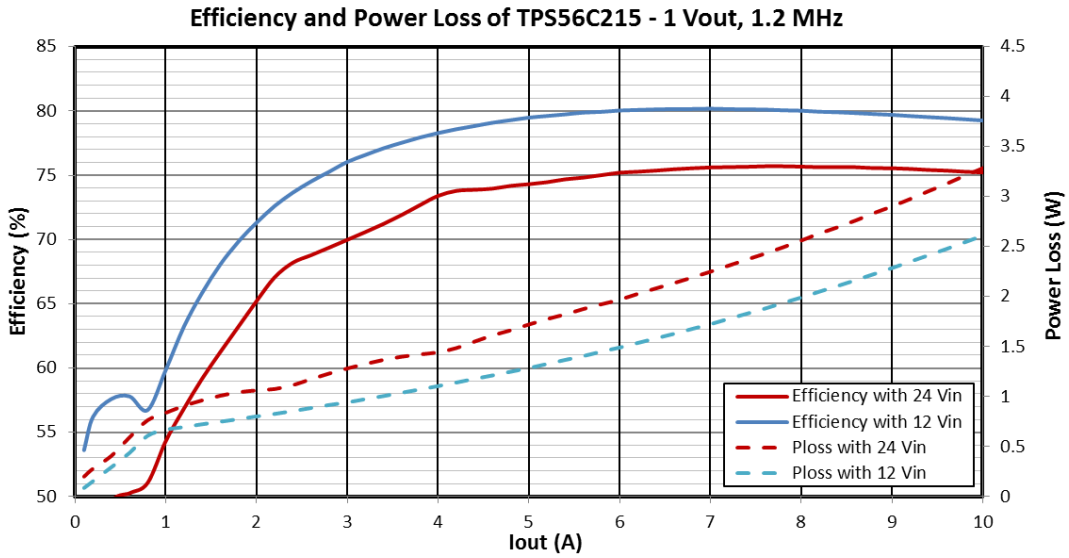
The switch node waveform of the TPS56C215 – 1.2 V, 400 kHz converter operating at 7A load is shown below.



3. TPS56C215 – 12 V to 1 V at 1.2 MHz

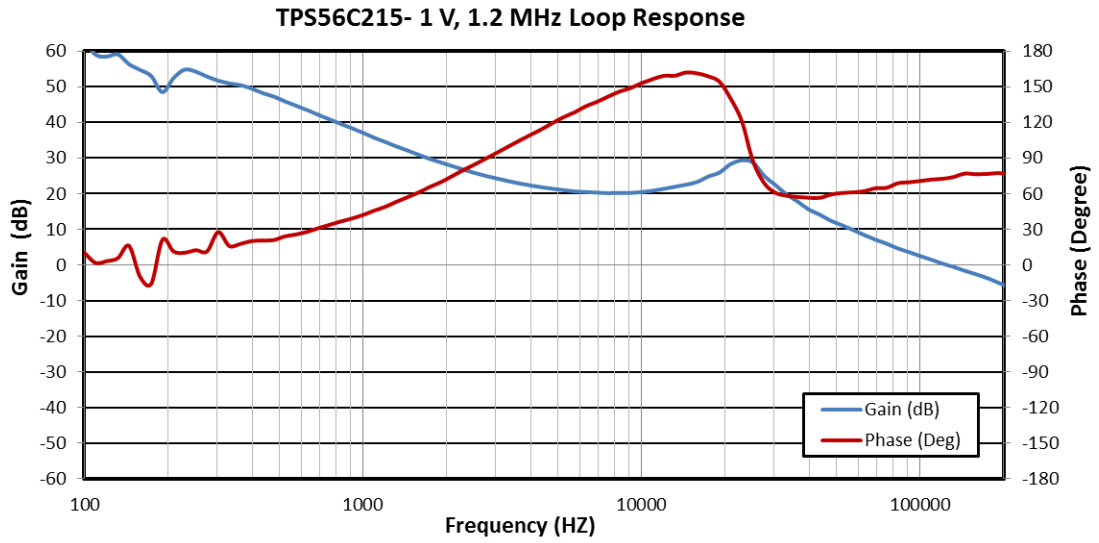
3.1 Efficiency and Power Loss

The efficiency and power loss tests on the entire system by applying 24 V_{IN} to TPS54541 at J1 and obtaining 1 V_{OUT} of TPS56C215 at J3 is done. The performance of TPS56C215 converter alone is done by applying 12 V_{IN} at J2 and disabling TPS54541. The efficiency and power loss for both cases are shown below.



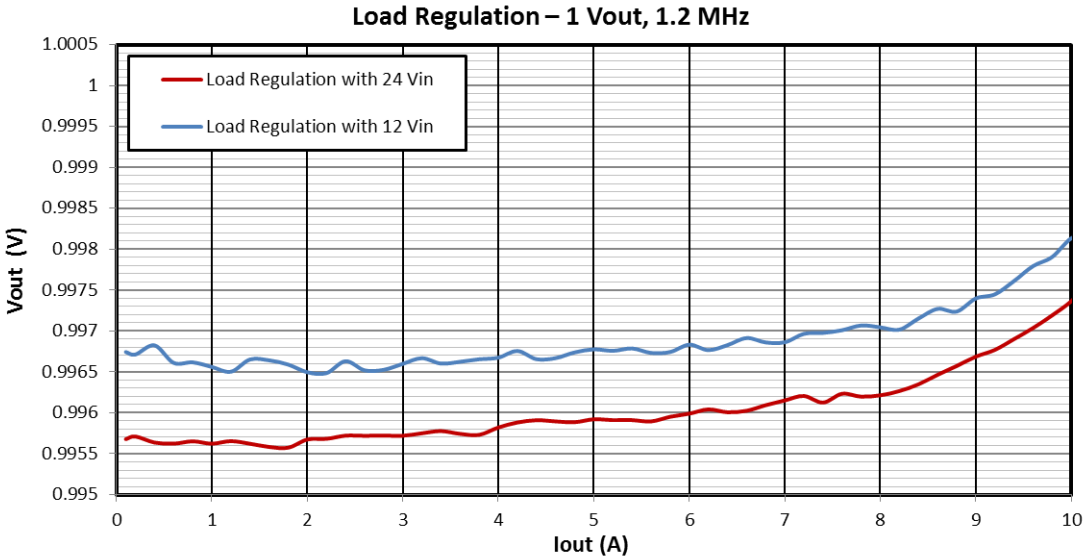
3.2 Loop Response

The plot below shows the loop-response characteristics of TPS56C215 – 1 V, 1.2 MHz converter. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 7 A. The phase margin measured is 73 degrees.



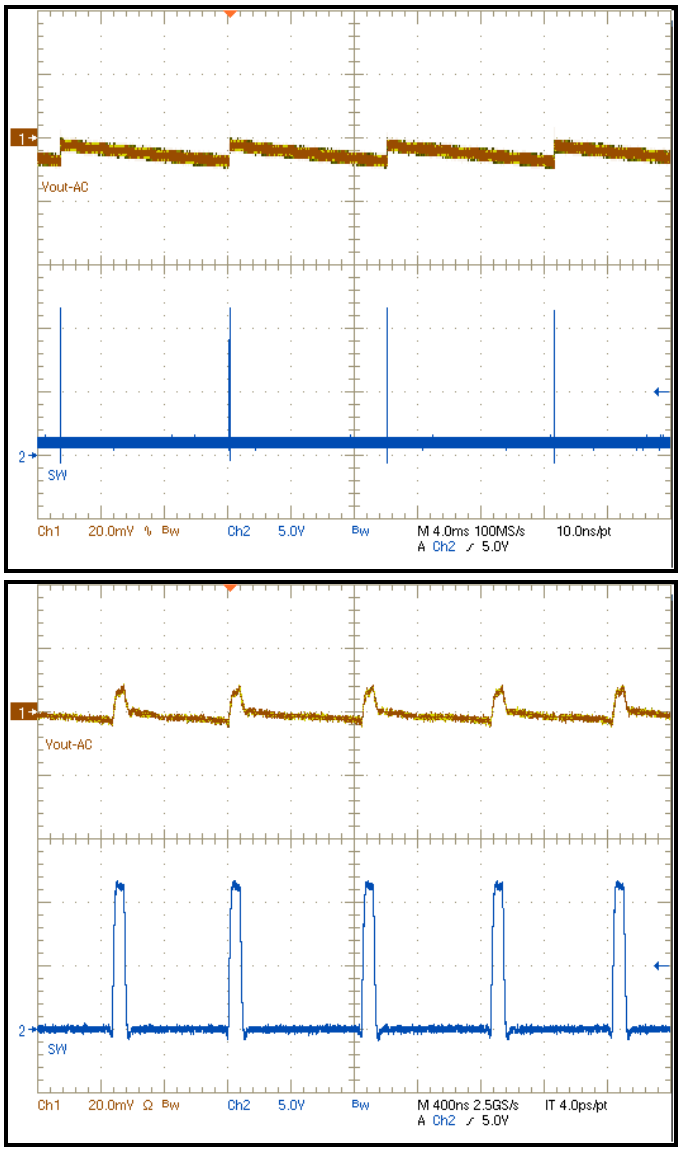
3.3 Load regulation

The Load regulation of TPS56C215 – 1 V, 1.2 MHz converter in both cases with 24 V_{IN} applied to TPS54541 at J1 and 12 V_{IN} applied at J2 is shown below.



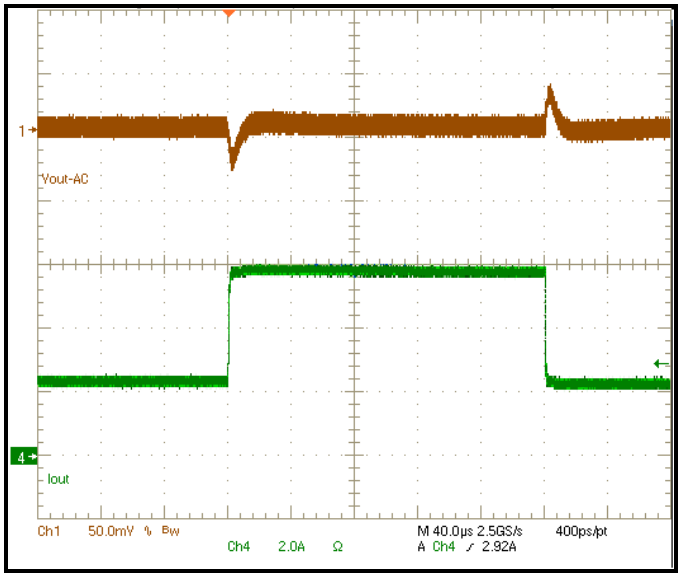
3.4 Output Ripple

The output Voltage graphs of TPS56C215 – 1 V, 1.2 MHz converter shown below are AC coupled for 0A and 7A load respectively. The output voltage is measured across output capacitors by tip and barrel method. The length of the ground wire should be as small as possible to avoid switching noise getting coupled.



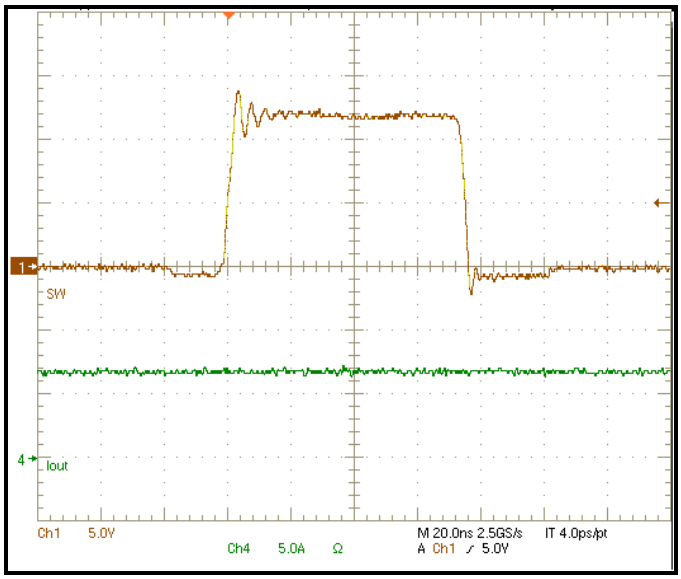
3.5 Transient Response

The figures below show TPS56C215 – 1 V, 1.2 MHz converter's response to load transients. The current step is from 2 A to 6 A. The current step slew rate is 2.5 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.



3.6 Switch Node

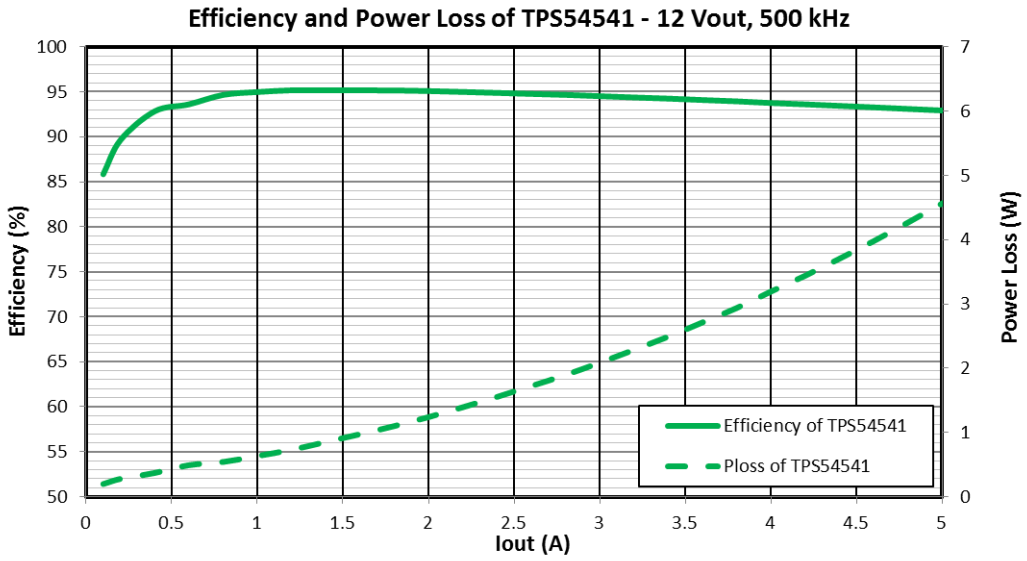
The switch node waveform of the TPS56C215 – 1 V, 1.2 MHz converter operating at 7 A load is shown below.



4. TPS54541 – 24 V to 12 V at 500 kHz

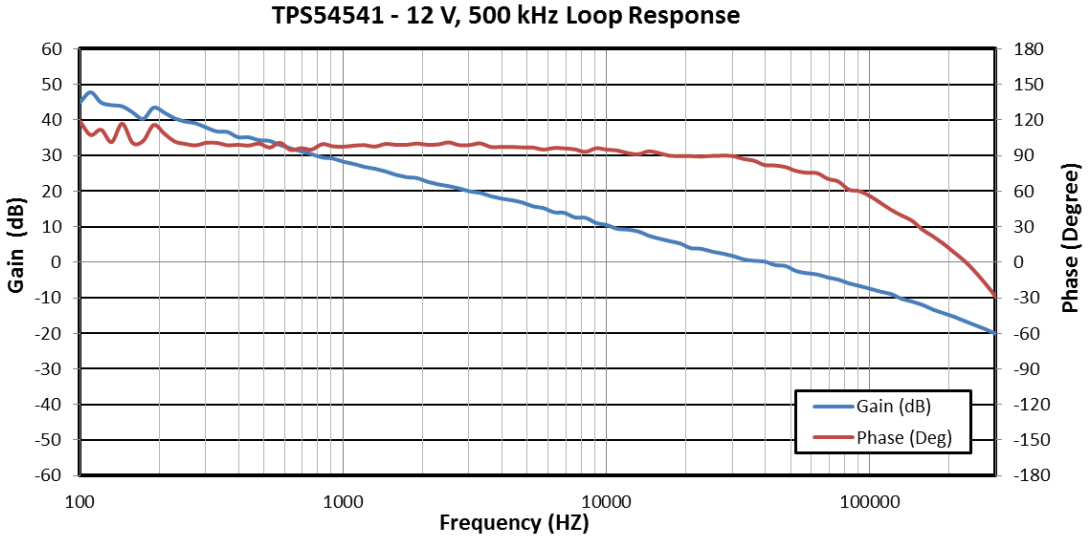
4.1 *Efficiency and Power Loss*

The efficiency and power loss tests of TPS54541 are done at 24 V_{IN} applied to J1 and 12 V_{OUT} obtained from J2. The results obtained are shown below.



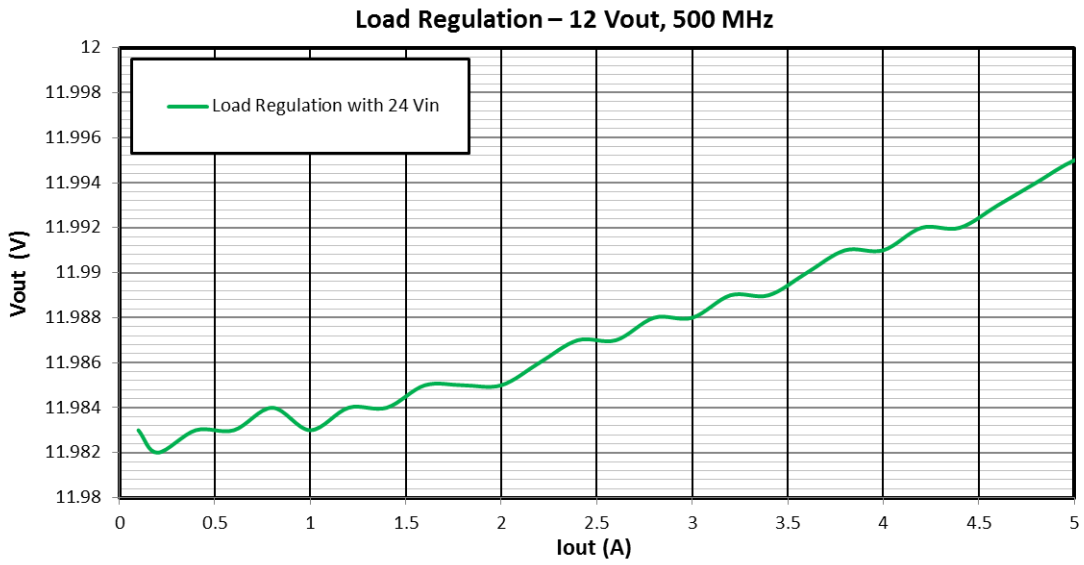
4.2 Loop Response

The plot below shows the loop-response characteristics of TPS54541 – 12 V, 500 MHz converter. Gain and phase plots are shown for V_{IN} voltage of 24 V. Load current for the measurement is 5 A. The phase margin measured is 82 degrees.



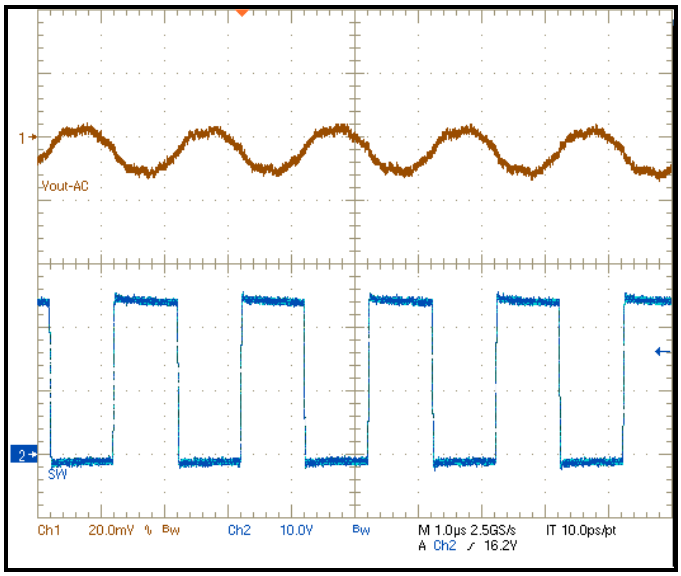
4.3 Load Regulation

The Load regulation of TPS54541 – 12 V, 500 MHz converter with 24 V_{IN} applied at J1 and 12 V_{OUT} obtained at J2 is shown below.



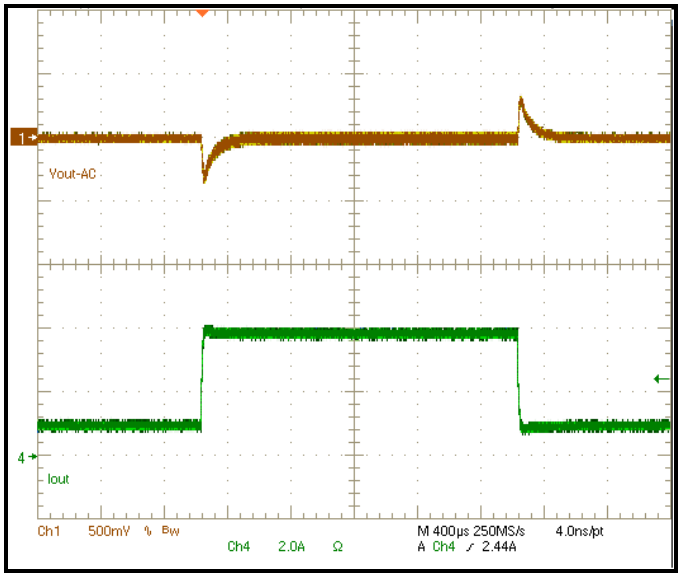
4.4 Output Ripple

The output Voltage graph of TPS54541 – 12 V, 500 kHz converter shown below is AC coupled at a load of 5 A. The output voltage is measured across output capacitors by tip and barrel method. The length of the ground wire should be as small as possible to avoid switching noise getting coupled.



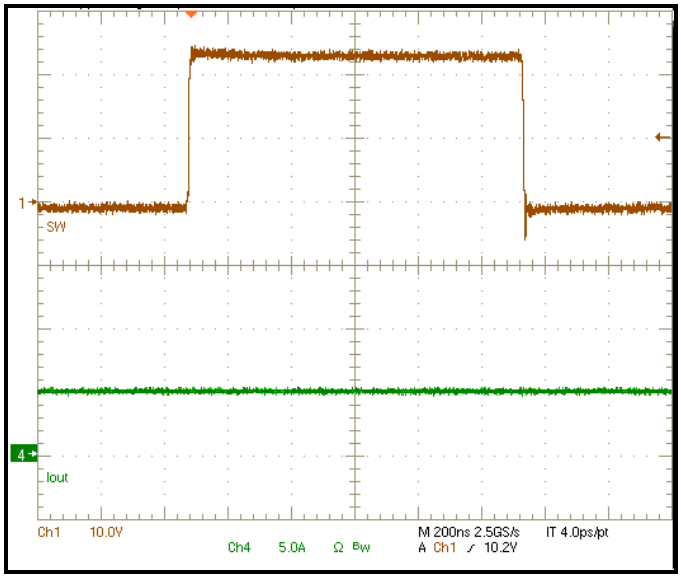
4.5 Transient Response

The figures below show TPS54541 – 12 V, 500 kHz converter's response to load transients. The load step is from 1 A to 4 A. The current step slew rate is 2.5 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.



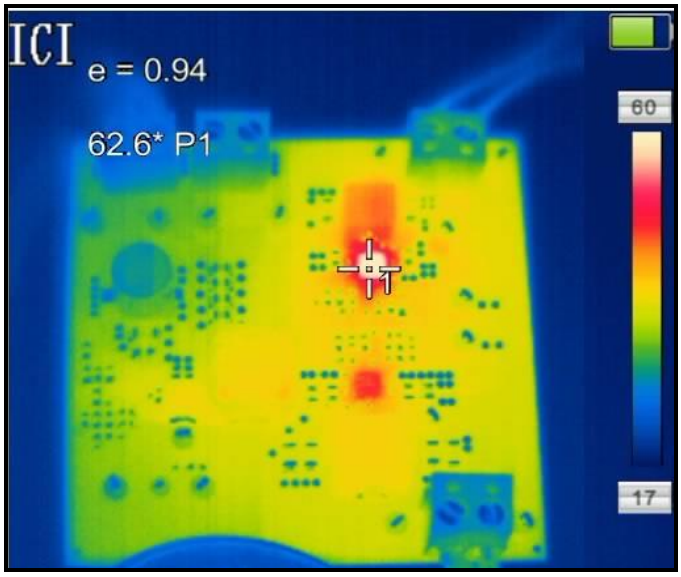
4.6 Switch Node

The switch node waveform of the TPS54541 – 12 V, 500 kHz converter operating at 5A load is shown below.



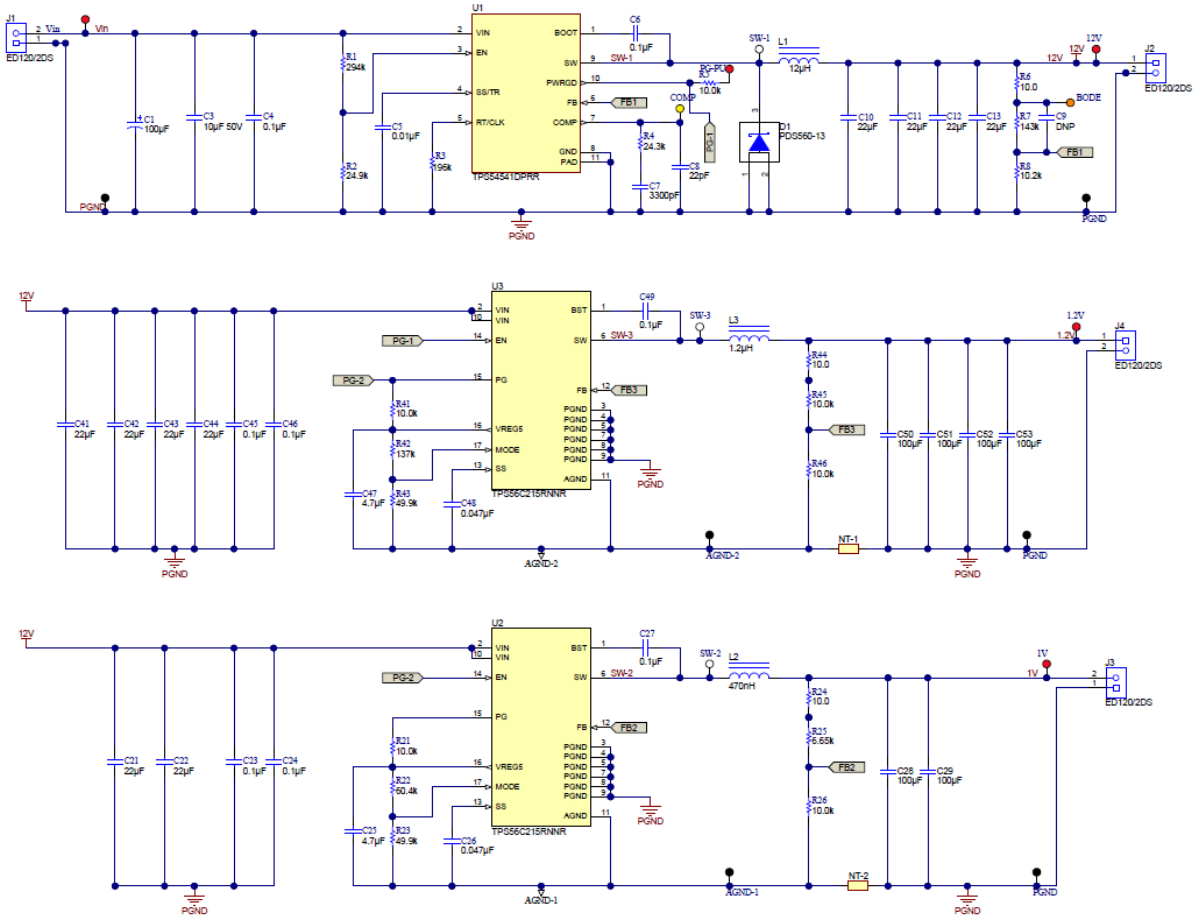
5. Thermal Image

The thermal Image of the board when the TPS56C215 1.2 V, 400 kHz and TPS56C215 1 V, 1.2 MHz converters are operating at their respective full loads is shown below. The cursor in the image is pointed on the TPS56C215 1 V, 1.2 MHz converter which is the hottest IC on the board for its high switching losses.



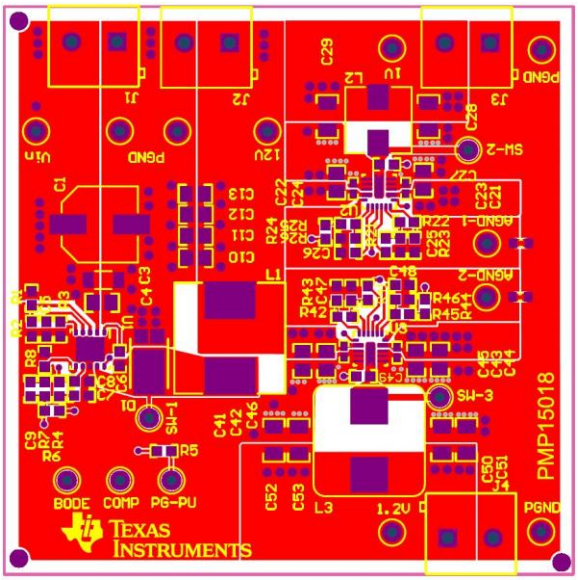
6. Schematic and Layout

The schematic of PMP15018 is shown below.

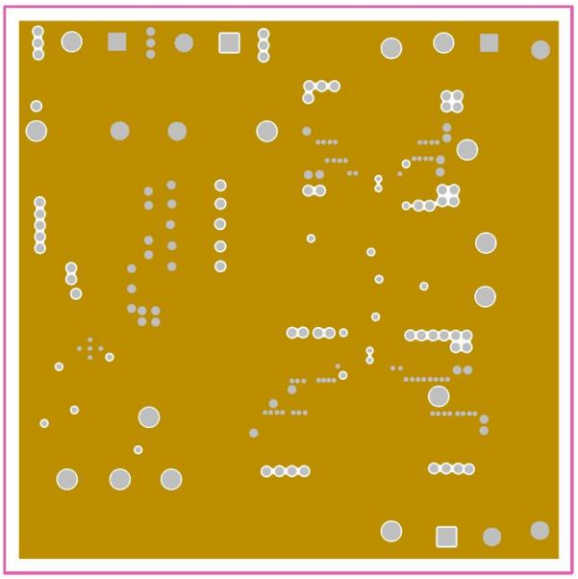


In board layout of PMP15018, the top, bottom, and internal layers are 2-oz. copper. The top layer contains the main power traces for VIN, VOUT, and SW. The quite analog ground planes of TPS56C215, 1.2 V, 400 kHz converter and TPS56C215, 1 V, 1.2 MHz converter on the top layer are tied to power ground at single points. The top-side ground traces are connected to the bottom ground planes with multiple vias on the board. The input decoupling capacitors are all located as close to the IC's as possible. Additionally, the voltage set point resistor divider components are kept close to the IC's.

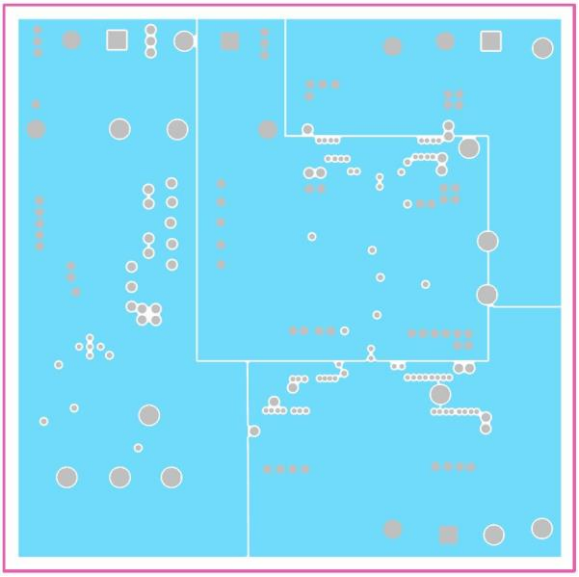
The top layer along with top overlay and top Solder is shown below.



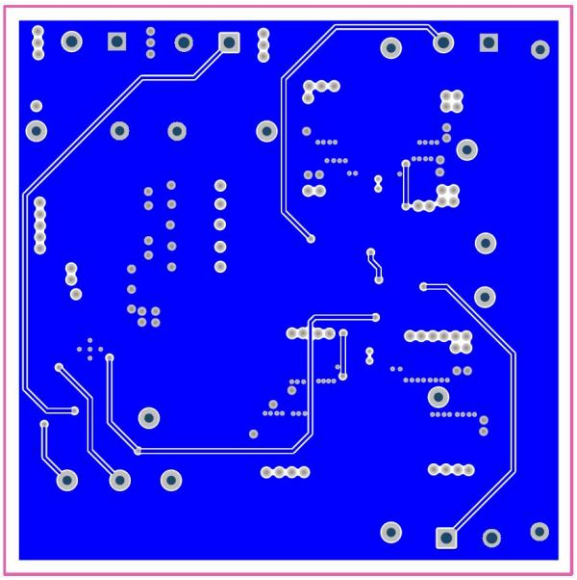
The inner layer-1 is a ground plane and is shown below.



The inner layer-2 is having copper fills of V_{IN} and V_{OUT} and is shown below.

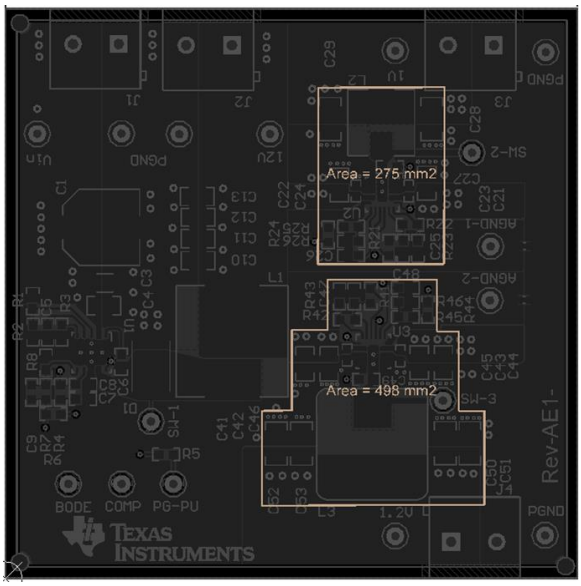


The Bottom Layer is an additional ground plane with output feedbacks, PGOOD and EN signal routings.



7 Efficiency vs Solution Size with different Switching Frequencies

Since the two converters used to step down 12 V_{IN} to 1 V_{OUT} and 1.2 V_{OUT} are operating at close specifications they can be used to compare their efficiency and Board area for 400 kHz and 1.2 Mhz. The peak efficiency of by the converter operating at 400 kHz is 90% when compared to 80% of the converter operating at 1.2 MHz. On the other hand the Solution size occupied by the converter operating at 400 kHz is 495mm^2 which is much higher when compared to 275mm^2 that of the converter operating at 1.2 MHz. The figure below shows the difference in solution size of each converter. So the trade-off between efficiency and Solution Size with low and high solution size can be seen.


Area = 275 mm2
Area = 498 mm2
PGND
SW-2
AGND-1
AGND-2
SW-3
Rev-AE1-
BODE
COMP
PG-PU
1.2V
PGND

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