

# Design Guide: TIDA-010052

## Safety Power Supply for Motor Drives Reference Design



### Description

This reference design implements a safe power supply for powering up microcontrollers in a two-MCU architecture. The TIDA-010052 has several protection features including overvoltage protection and short circuit protection to prevent the MCUs from getting damaged. The DC/DCs, LMR36520, and LMR36015 convert the 5-V and 12-V rail into 3.3 V, which is monitored by the TPS3703 and TPS3702 voltage monitors respectively.

### Resources

<a href="#">TIDA-010052</a>	Design Folder
<a href="#">TPS2660</a>	Product Folder
<a href="#">LMR36520</a>	Product Folder
<a href="#">TPS3703-Q1</a>	Product Folder
<a href="#">TPS7A16</a>	Product Folder
<a href="#">LMR36015</a>	Product Folder
<a href="#">TPS3702</a>	Product Folder
<a href="#">TPS2400</a>	Product Folder
<a href="#">TLV6002</a>	Product Folder

### Features

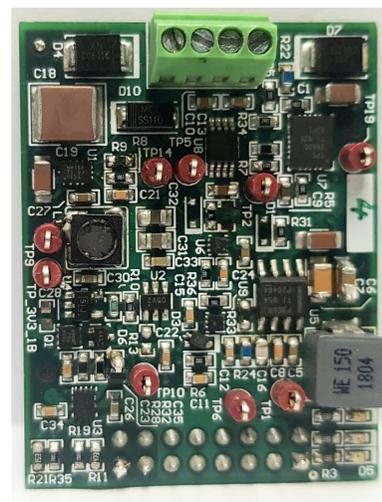
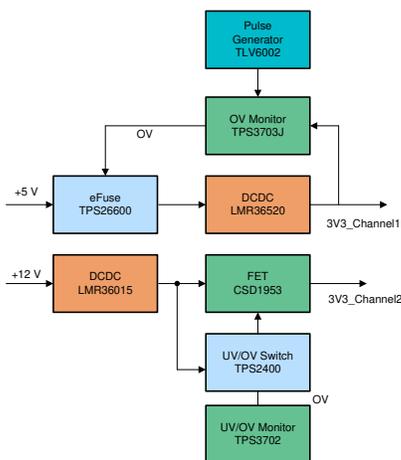
- Overvoltage, overcurrent, and short circuit protection of the 3.3-V rail for powering the MCU
- Protection of the power supply input from an overvoltage of up to 60 V
- Small form factor for space-critical applications
- Synchronous buck DC/DC converter with integrated switch optimized for > 90% efficiency and compact size

### Applications

- [Motor drives](#)
- [Elevator main control panel](#)



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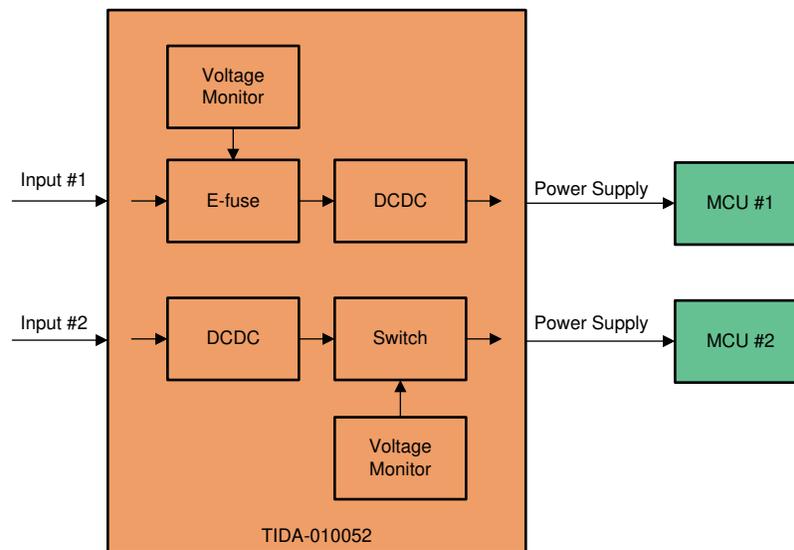


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## 1 System Description

Motor drive systems are widely used in a range of industrial applications including robots, machine tools, process lines, fan control, and so forth. Safe operation of machinery is a major concern in a factory setting to prevent casualty to human personnel and destruction of machines during fault conditions, as well as for reducing factory downtime. A typical motor drive system consists of a control module, communication module, power stage, and input/output module. The control module performs the signal processing and overall command algorithm using single or multiple MCUs based on the complexity of the drive. A two-MCU architecture becomes particularly significant in safety-critical applications where the MCUs are installed in a lockstep configuration. These two MCUs must be powered from two separate supplies so as to increase reliability. This reference design implements two redundant power supplies for powering the MCUs as shown in Figure 1. The two power rails are generated using different architectures to reduce the chances of failure in the two paths. A voltage monitor circuit is used to protect the circuit in case of an overvoltage condition. Both of the inputs can withstand up to 60 V, and each rail is protected against an overvoltage, overcurrent, and short circuit condition.

**Figure 1. System Block Diagram**



## 1.1 Key System Specifications

The key system specifications are highlighted in [Table 1](#).

**Table 1. Key System Specifications**

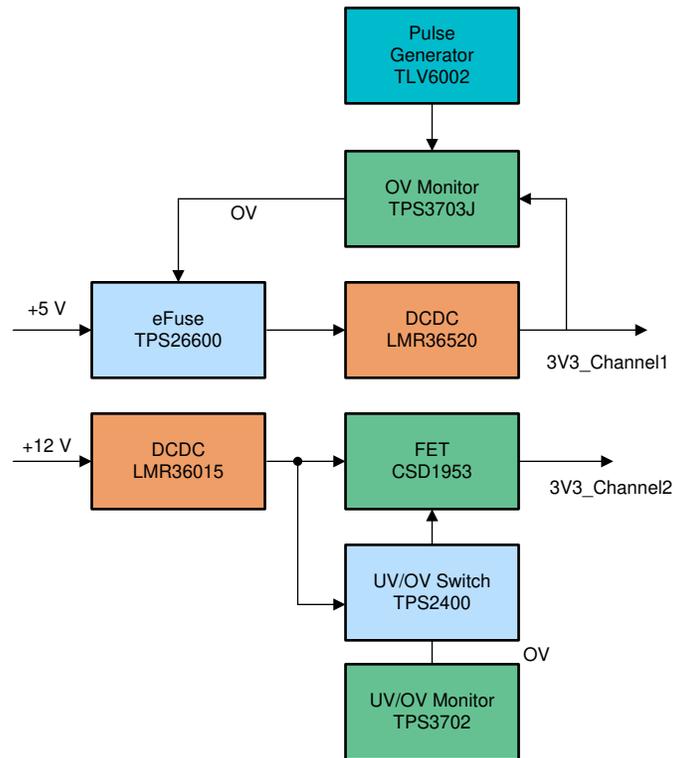
PARAMETER	TYPICAL VALUE
Power supply A	
Input voltage, VIN	5 V
Output voltage, VOUT	3.3 V
Input UVLO	4.2 V
Output current	1 A
Input overvoltage protection	up to 60 V
Switching frequency	400 kHz
Protection	Short circuit protection, overvoltage protection, thermal protection, overcurrent protection
Power supply B	
Input voltage, VIN	12 V
Output voltage, VOUT	3.3 V
Input UVLO	4.2 V
Output current	1 A
Input overvoltage protection	up to 60 V
Switching frequency	400 kHz
Protection	Short circuit protection, overvoltage protection, thermal protection, overcurrent protection

## 2 System Overview

### 2.1 Block Diagram

Figure 2 shows the block diagram of the TIDA-010052.

**Figure 2. TIDA-010052 Block Diagram**



Power rail A performs input current limit, inrush current control, overcurrent, and thermal protections using a 5-V input and the TPS26600 eFuse. Together with the TLV6002 operational amplifier (op amp) and the TPS3703J voltage monitor, the 3.3-V output voltage rail is monitored for overvoltage protection. The LMR36520 DC/DC regulates output to 3.3 V and has integrated overcurrent and thermal protections. Power rail B takes a 12-V input and converts it to 3.3 V using the LMR36015. The TPS2400 switch controller and TPS3702 overvoltage monitor together disconnect rail B in case of overvoltage.

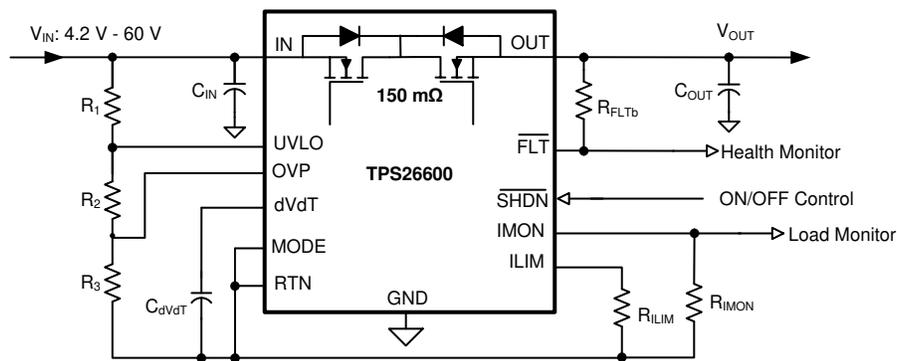
## 2.2 Highlighted Products

This reference design features the following devices, selected based on their specifications and relevance for this design. For more information on each of these devices, see their respective product folders at TI.com.

### 2.2.1 TPS26600

Figure 3 shows the block diagram of the TPS26600. It is a compact, feature-rich, high-voltage eFuse with a full suite of protection features. The TPS26600 integrates overcurrent, output slew rate, overvoltage, and undervoltage protections, which enable load, source, and device protections. An integrated back-to-back FET provides reverse blocking features. In a current-limiting status, the TPS26600 offers different protection modes including circuit breaker, latch off, and auto-retry. The device supports shutdown pin, fault, and precise current-monitor output.

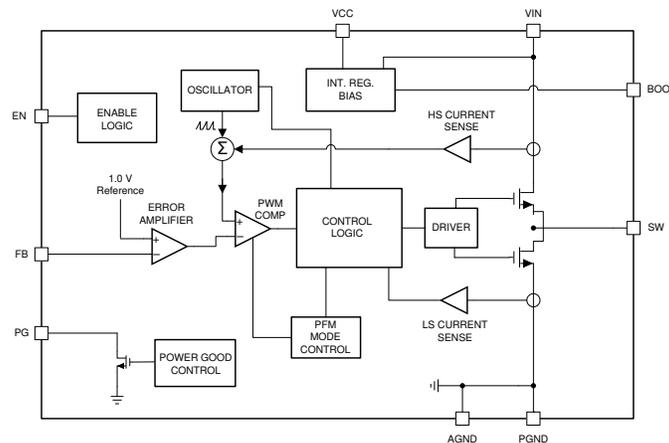
Figure 3. TPS26600 Block Diagram



### 2.2.2 LMR36015

Figure 4 shows the block diagram of the LMR36015. This regulator is an easy-to-use, synchronous, step-down DC/DC converter. With integrated high-side and low-side power MOSFETs, up to 1.5 A of output current is delivered over a wide input voltage range of 4.2 V to 60 V. The LMR36015 uses peak-current-mode control to provide optimal efficiency and output voltage accuracy. Load transient performance is improved with the FPWM feature in the 1-MHz regulator. The device requires few external components and has a pinout designed for simple PCB layout. The small solution size and feature set of the LMR36015 are designed to simplify implementation.

Figure 4. LMR36015 Block Diagram

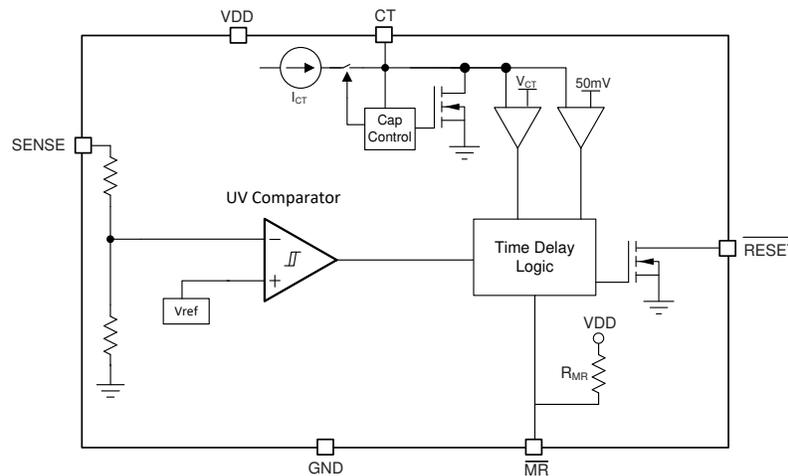


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### 2.2.3 TPS3703

Figure 5 shows the block diagram of the TPS3703. The TPS3703 device is an integrated overvoltage (OV) and undervoltage (UV) monitor or reset IC in the industry's smallest 6-pin DSE package. This highly accurate voltage supervisor is ideal for systems that operate on low-voltage supply rails and have narrow-margin supply tolerances. The Capacitor Time (CT) pin is used to select between the two available reset time delays designed into each device and also to adjust the reset time delay by connecting a capacitor. The device can be configured as auto recovery and latch mode in an OV/UV status.

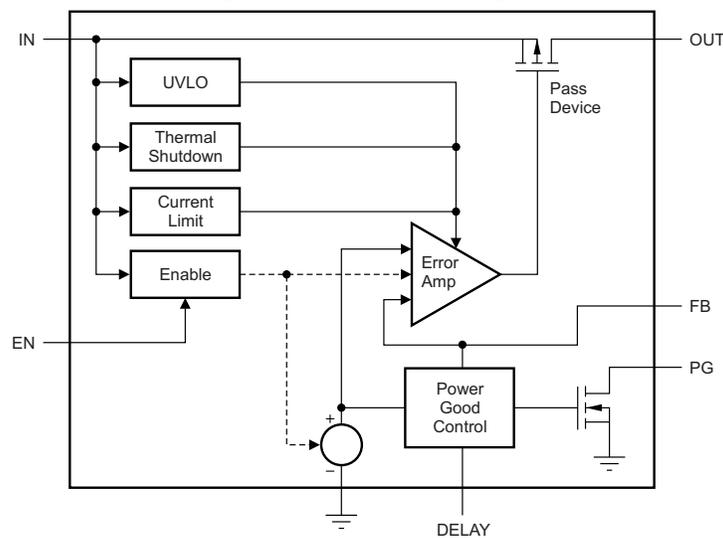
**Figure 5. TPS3703 Block Diagram**



### 2.2.4 TPS7A16

Figure 6 shows the block diagram of the TPS7A16. The TPS7A16 family of ultra-low power, low-dropout voltage regulators offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16 family integrates enable pin (EN) compatible with CMOS logic and power good pin (PG) with user-programmable delay. The TPS7A16 can withstand and maintain regulation during voltage transients.

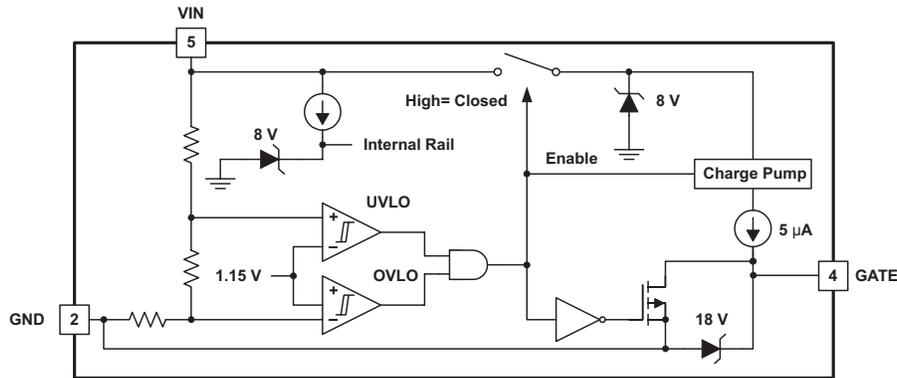
**Figure 6. TPS7A16 Block Diagram**



### 2.2.5 TPS2400

Figure 7 shows the block diagram of the TPS2400. The TPS2400 overvoltage protection controller is used with an external MOSFET to isolate sensitive electronics from destructive voltage spikes and surges. The internal circuit includes a charge pump, band-gap reference oscillator, and Zener diode.

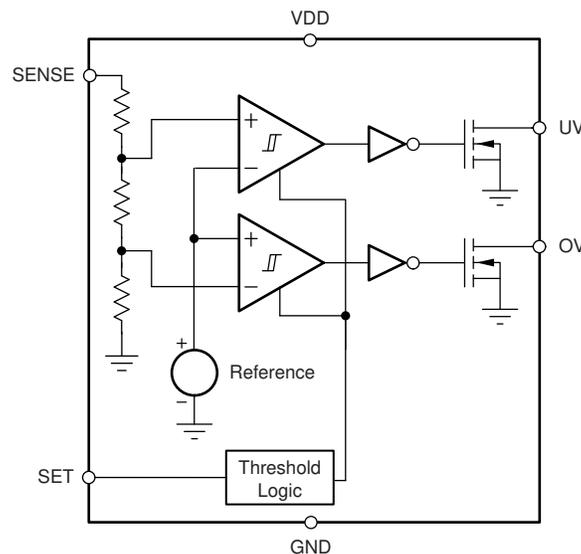
Figure 7. TPS2400 Block Diagram



### 2.2.6 TPS3702

Figure 8 shows the block diagram of the TPS3702. The TPS3702 is an integrated overvoltage and undervoltage window comparator in a small SOT-6 package. Low-threshold hysteresis options of 0.55% and 1.0% prevent false reset signals when the monitored voltage supply is in its normal range of operation. Internal glitch immunity and noise filters further eliminate false resets resulting from erroneous signals. The SET pin is used to select between the two available threshold voltages designed into each device. The device has a low typical quiescent current specification of 7 µA.

Figure 8. TPS3702 Block Diagram



### 2.2.7 TLV6002

The TLV600x family of single-channel and dual-channel operational amplifiers is specifically designed for general-purpose applications. Featuring rail-to-rail input and output (RRIO) swings, low quiescent current (75 µA, typical), wide bandwidth (1 MHz) and low noise (28 nV/√Hz at 1 kHz), this family is attractive for a variety of general-purpose applications that require a balance between cost and performance. The low-input-bias current (±1 pA, typical) enables the TLV600x-Q1 to be used in applications with megaohm source impedances. The devices are optimized for operation at voltages as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and are specified over the extended temperature range of -40°C to +125°C.

## 2.3 System Design Theory

This reference design generates two independent 3.3-V power rails. Each of the subsystem modules in the design are explained in the subsequent sections.

### 2.3.1 Design Theory of Power Rail A

#### 2.3.1.1 eFuse Circuit Design - TPS26600

Figure 9. Schematic of the TPS26600

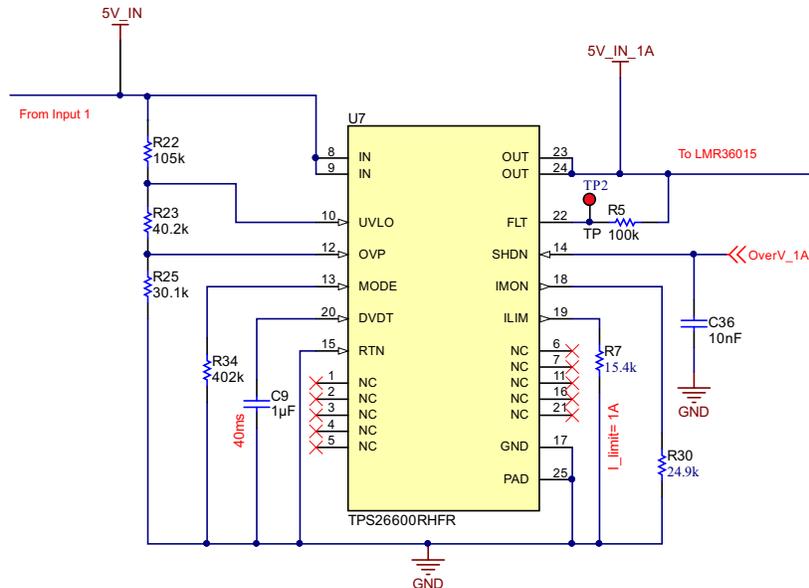


Figure 9 shows the block diagram of the TPS26600. The TPS26600 is used for input current limiting, input overvoltage protection, and output slew rate control. The SHDN pin of the TPS26600 is used to shut down power rail A in case of overvoltage of the 3.3-V rail. To limit the input current and inrush current, a programmable resistor must be determined properly. 15.4kΩ selected for 0.8-A current limiting is used as shown in Equation 1.

$$R_{ILIM} = \frac{12}{I_{OL}} = \frac{12}{0.8A} = 15 \text{ k}\Omega$$

where

- $I_{OL}$  is the overload current limit in Ampere
  - $R_{ILIM}$  is the current limit programmable resistor in kΩ
- (1)

The dVdT pin can be set to program the output ramp rate with a proper capacitor. For a 40-ms start up time, the required capacitor should be 1µF as shown in Equation 2. The inrush current can be determined by Equation 3.

$$C_{dVdT} = \frac{t_{(dVdT)}}{8 \times 10^3 \times V_{IN}} = \frac{40 \times 10^{-3} \text{ s}}{8 \times 10^3 \times 5 \text{ V}} = 1 \mu\text{F}$$
(2)

$$I_{(INRUSH)} = C_{OUT} \times \frac{V_{IN}}{t_{dVdT}} = 4.7 \mu\text{F} \times \frac{5 \text{ V}}{40 \text{ ms}} = 0.58 \text{ mA}$$
(3)

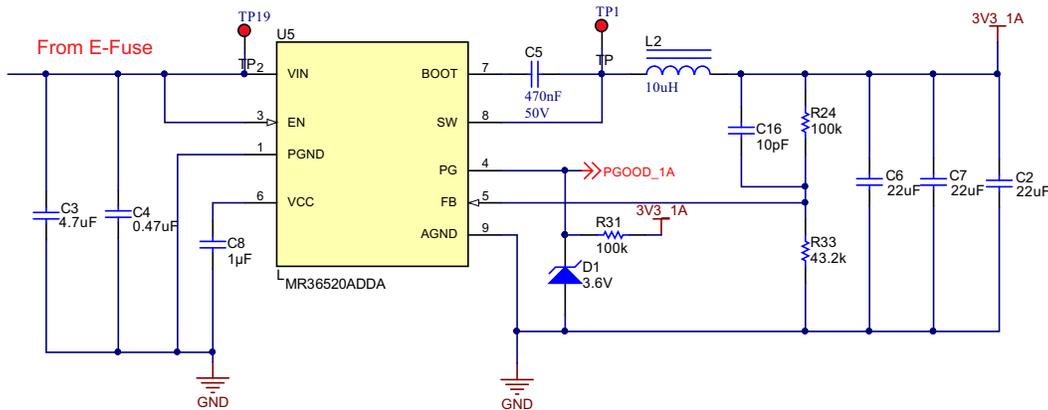
The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network in R22, R23, and R25. The values required for setting the ULVO and overvoltage are calculated using Equation 4 and Equation 5. By setting R25 to 30 kΩ, the calculated values of R22 and R23 are 40 kΩ and 105 kΩ .

$$V_{(OVPR)} = \frac{R_{25}}{R_{22} + R_{23} + R_{25}} \times V_{(OV)} \quad (4)$$

$$V_{(OVPR)} = \frac{R_{23} + R_{25}}{R_{22} + R_{23} + R_{25}} \times V_{(UV)} \quad (5)$$

### 2.3.1.2 DC/DC Design - LMR36520

Figure 10. Schematic of the LMR36520



The LMR36520 is a 65-V, 2-A DC/DC converter. Figure 10 shows the schematic of the LMR36520. The main parameters are shown in Table 2.

Table 2. TPS36520 Design Parameters

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	SWITCHING FREQUENCY
5 V	3.3 V	1 A	400 kHz

The ripple current coefficient is chosen as 30%. Accordingly, the inductor value can be calculated from Equation 6. An inductor value of 10 uH is selected accordingly.

$$L = \frac{(V_{IN} - V_{OUT}) V_{OUT}}{f_{SW} K I_{OUT} V_{IN}} = \frac{(5 V - 3.3 V) \times 3.3 V}{400 \times 10^3 \text{Hz} \times 0.3 \times 1 A \times 5 V} = 9.3 \mu\text{H} \quad (6)$$

The output filter capacitor can be calculated by the ripple voltage, which is caused by the ripple current. To limit the voltage ripple to 30 mV, a capacitor above 50 uF is used as calculated by Equation 7. Three capacitors of 22 μF each are used at the output.

$$C > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 0.09 A}{400 \times 10^3 \times 20 \times 10^{-3}} = 46 \mu\text{F} \quad (7)$$

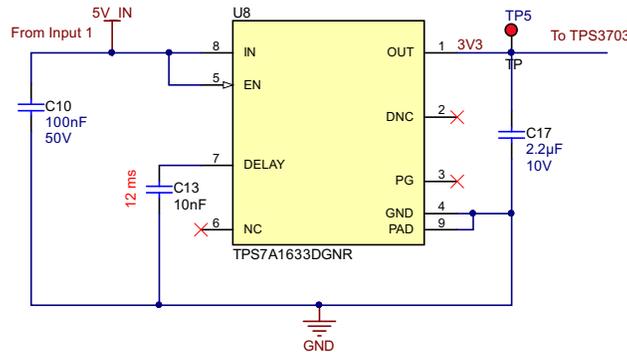
The internal reference is set as 1.2 V for the LMR36520. The feedback resistors that generate an output voltage of 3.3 V can be calculated using Equation 8. R23 and R24 are calculated as 43.2 kΩ and 100 kΩ respectively.

$$V_{OUT} = V_{REF} \frac{R_{24} + R_{33}}{R_{33}} \quad (8)$$

### 2.3.1.3 Linear Voltage Regulator - TPS7A1633

The TPS7A1633 is used to power the voltage monitor TPS3703 as shown in Figure 11. The TPS7A1633 is capable of withstanding 60 V at the input, therefore no external overvoltage protection is implemented in the circuit.

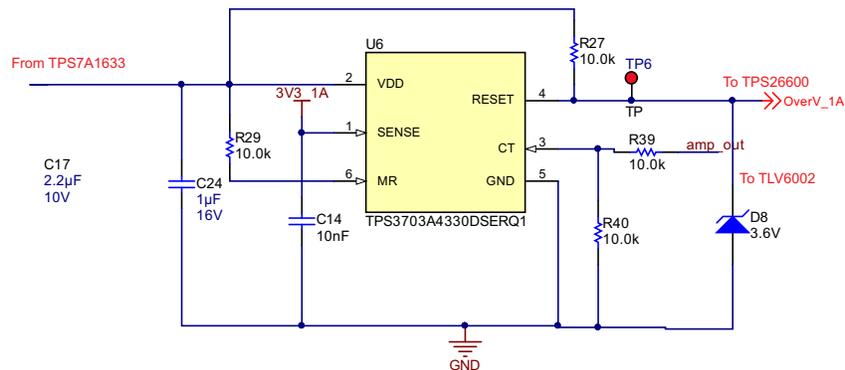
Figure 11. Schematic of the TPS7A1633



### 2.3.1.4 Voltage Monitor Circuit - TPS3703

The TPS3703 is used as a reset IC to power off power rail A in case of overvoltage. The TPS3703 can set the overvoltage threshold without a divider resistor, so the SENSE pin can be connected to monitor the 3.3-V rail directly. The schematic of the TPS3703 is shown in Figure 12.

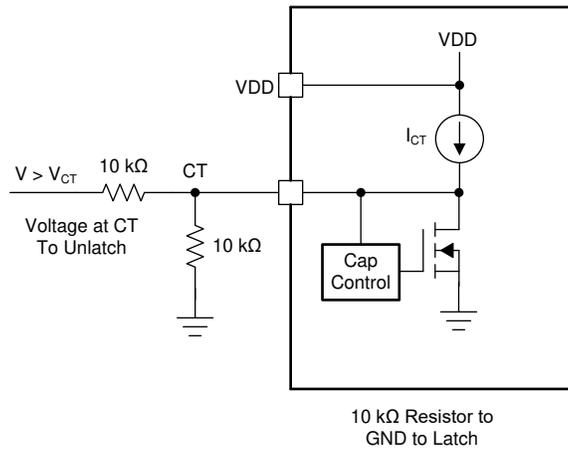
Figure 12. Schematic of the TPS3703



The TPS3703 features two options of RESET signal, including auto recovery mode and latch mode, when overvoltage happens. In auto recovery mode, the RESET goes low when overvoltage happens and can return to normal in case overvoltage disappears. In latch mode, the RESET is pulled low once overvoltage happens regardless of the SENSE pin status. The TPS3703 is set to operate in latch mode because power rail A should remain turned off once it goes abnormal.

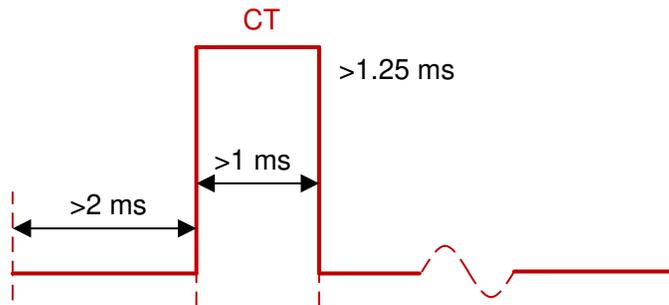
For latch mode connection, a pull down resistor on the CT pin is recommended as shown in [Figure 13](#).

**Figure 13. Latch Mode of the TPS3703**



For operating the device in latch mode, an initial pulse should be given at the CT pin at start up to ensure the device is unlatched. The specifications of the desired initial pulse are highlighted in [Figure 14](#). A pulse generator circuit, discussed in the following section, uses the TLV6002 to generate this pulse when the circuit powers up.

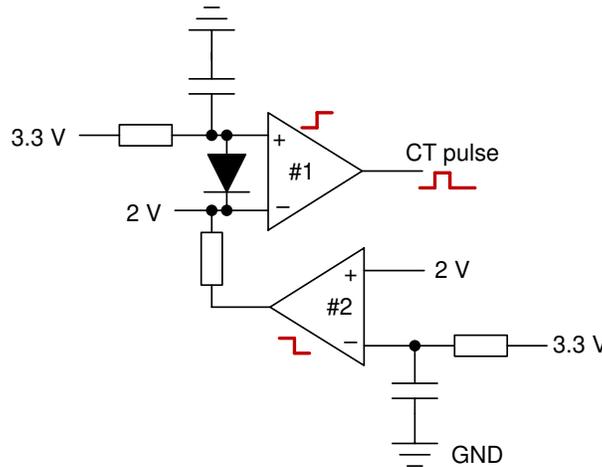
**Figure 14. Pulse to Initially Unlatch the TPS3703**



### 2.3.1.5 Pulse Generator Circuit - TLV6002

To generate pulse for unlatching the TPS3703, a pulse generator circuit is designed as shown in Figure 15. Opamp1 produces the rising edge of the pulse with programmable delay implemented by R38 and C25 as shown in Equation 9. Opamp2 produces the falling edge of the pulse using R42 and R43 as shown in Equation 10.

Figure 15. Pulse Generator Circuit

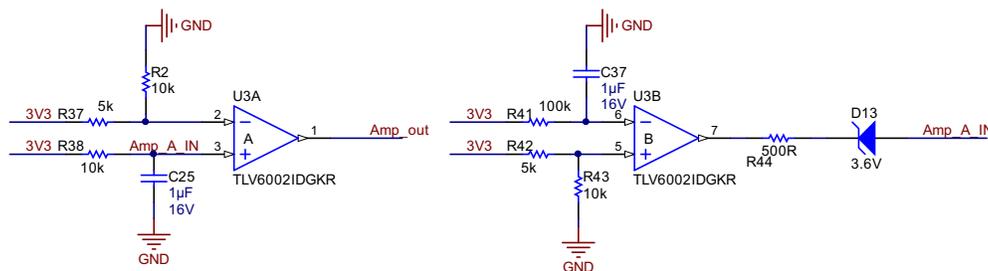


$$t_1 = R_{38} C_{25} = 10 \times 10^3 \times 1 \times 10^{-6} = 10 \text{ ms} \tag{9}$$

$$t_2 = R_{41} C_{37} = 100 \times 10^3 \times 1 \times 10^{-6} = 100 \text{ ms} \tag{10}$$

The filter capacitor can be calculated by the ripple voltage, which is caused by the ripple.

Figure 16. Schematic of the Pulse Generator Circuit



## 2.3.2 Design Theory of Power Rail B

### 2.3.2.1 DC/DC Design - LMR36015

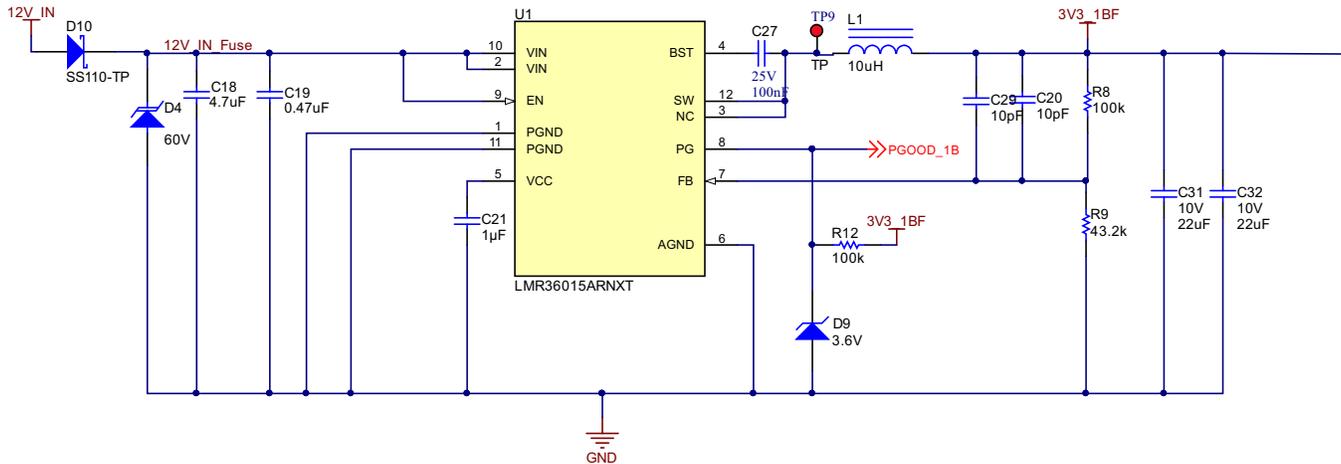
The LMR36015 is used to convert 12 V to 3.3 V with 1-A output current. For the DC/DC converter, the inductor and capacitor must be carefully selected to meet the output current rating and voltage ripple. The main parameters are shown in Table 3.

Table 3. TPS36015 Design Parameters

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	SWITCHING FREQUENCY
12 V	3.3 V	1 A	400 kHz

Figure 17 shows the schematic of the LMR36015.

Figure 17. Schematic of the LMR36015



The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current. A ripple current coefficient of 40% was chosen to balance the ripple and inductance. Equation 11 is used to determine the value of inductance. The constant, K, is the percentage of inductor current ripple. For this application, 10 uH is recommended.

$$L = \frac{(V_{IN} - V_{OUT}) V_{OUT}}{f_{SW} K I_{OUT} V_{IN}} = \frac{(12 \text{ V} - 3.3 \text{ V}) \times 3.3 \text{ V}}{1000 \times 10^3 \text{ Hz} \times 0.3 \times 1 \text{ A} \times 12 \text{ V}} = 8 \mu\text{H} \quad (11)$$

The filter capacitor can be calculated by the ripple voltage, which is caused by the ripple current. To limit the voltage ripple to 10 mV, a capacitor above 40 uF is required in Equation 12. Two capacitors of 22 uF each were selected at the output.

$$C > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 0.2 \text{ A}}{1000 \times 10^3 \text{ Hz} \times 10 \times 10^{-3}} = 40 \mu\text{F} \quad (12)$$

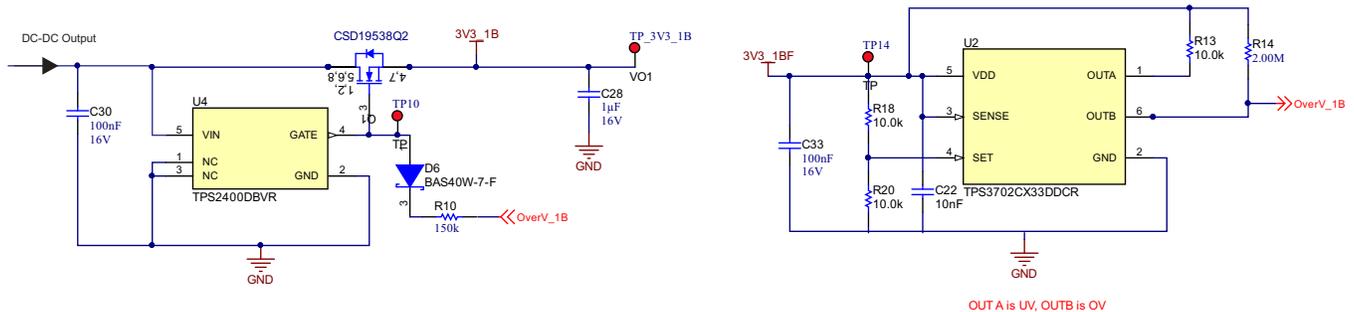
With a 1.2-V internal reference, R9 and R8 are calculated as 43.2k and 100k using Equation 13.

$$V_{OUT} = V_{REF} \frac{R_8 + R_9}{R_9} \quad (13)$$

### 2.3.2.2 Overvoltage Monitor Circuit - TPS3702 and TPS2400

In coordination with the voltage monitor circuit of the TPS3702, the TPS2400 switch controller can turn off the FET, Q1, in case of an overvoltage. The TPS2400 has an integrated charge pump circuit which provides 5 uA to turn on the gate of Q1 during normal operation. In case of overvoltage, the OUTB pin of the TPS3702 is pulled low and diode D6 discharges the gate of Q1 and turns off power supply B. The schematic is shown in Figure 18.

Figure 18. Schematic of the Overvoltage Monitor Circuit

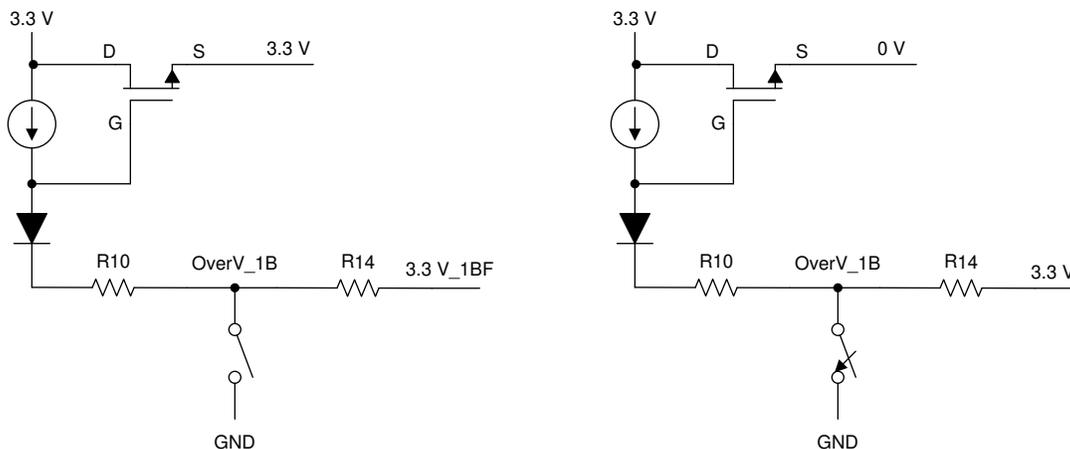


The equivalent circuit under normal and overvoltage condition can be represented as shown in Figure 19. R10 must be selected, noting the minimum threshold voltage of Q1 (2.8 V). R10 is chosen as 150 kΩ based on Equation 14, where,  $I_{source}$  is the maximum current driven from the gate pin of the TPS2400. The gate pin can source a minimum of 3 uA to charge the gate of Q1 during normal operation. To maintain the  $V_{gs}$  of 6 V for low  $R_{ds-on}$  operation of Q1, the gate voltage should be 9.3 V (as the source will be at 3.3 V under normal operation). The value of R14 is calculated as 2000 kΩ using Equation 15.

$$R10 < \frac{V_{g\_off} - 0.2 V}{I_{max}} = \frac{1.8 V - 0.2 V}{10 \mu A} = 160 k\Omega \quad (14)$$

$$R10 + R14 > \frac{V_{g\_on} - 0.2 V - 3.3 V}{I_{min}} = \frac{9.3 V - 0.2 V - 3.3 V}{3 \mu A} = 1933 k\Omega \quad (15)$$

Figure 19. Equivalent Circuit for Overvoltage Monitoring



### 3 Hardware, Testing Requirements, and Test Results

#### 3.1 Required Hardware and Software

##### 3.1.1 Hardware

Figure 20 shows the top view of the TIDA-010052 board.

**Figure 20. TIDA-010052 PCB**



The TIDA-010052 board is very compact, with 45.00-mm x 35.00-mm dimensions. J2 is a 4-pin connector, which supplies 5-V and 12-V input voltages. J1 is the output connector, giving a 3.3-V power supply for external use respectively.

## 3.2 Testing and Results

### 3.2.1 Normal Operation

Figure 21 shows the normal operation of rail A. Once the TIDA-010052 is powered on, a start pulse is generated at the CT pin, and the output rail goes up to 3.3 V without any overshoot.

Figure 22 shows the output of rail B. The rail provides a stable 3.3-V supply without overshoot.

Figure 21. Normal Operation of Rail A

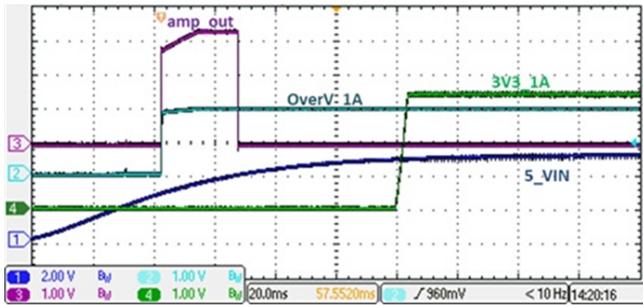
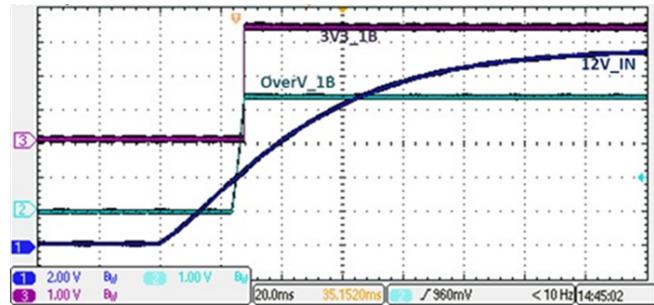


Figure 22. Normal Operation of Rail B



### 3.2.2 Load Transient Behavior

Figure 23 and Figure 24 show the load transient of rail A and rail B, which is measured with 10% load to 90% load. The figures show that only a small amount overshoot/undershoot is caused by load transient.

Figure 23. Load Transient Behavior of Rail A With 10% Load to 90% Load

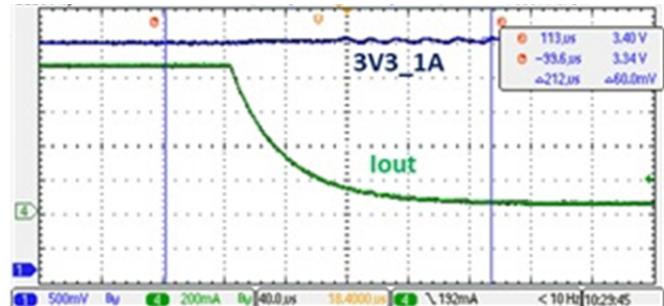
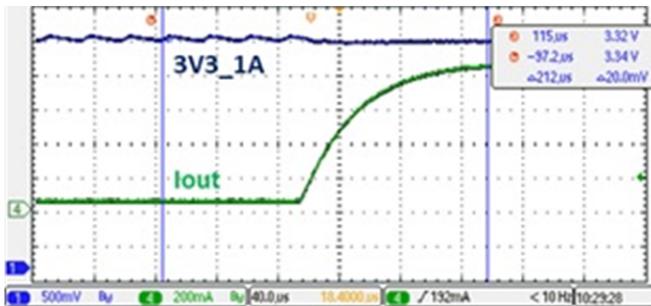
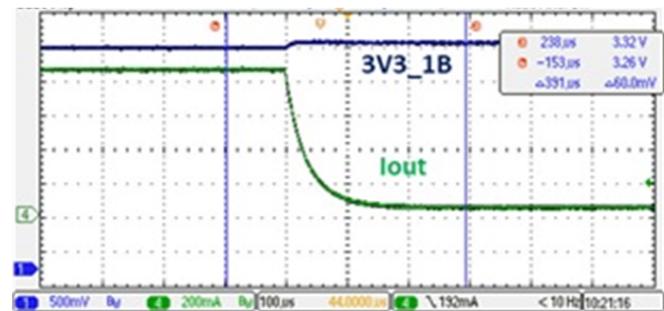
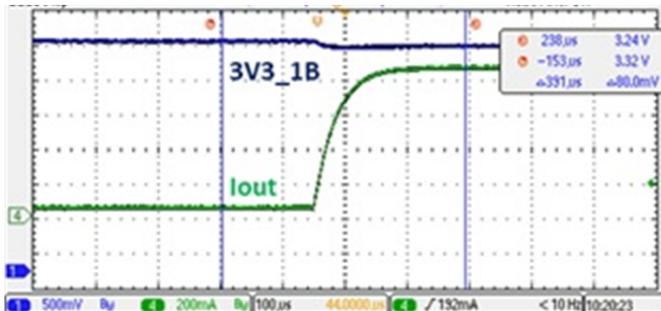


Figure 24. Load Transient Behavior of Rail B With 10% Load to 90% Load



### 3.2.3 Overvoltage Protection

As Figure 25 and Figure 26 show, overvoltage protection is implemented to shut down the power supply in case of overvoltage.

Figure 25. Overvoltage Protection of Rail A

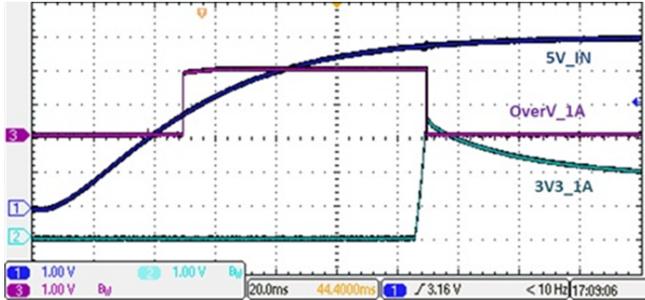
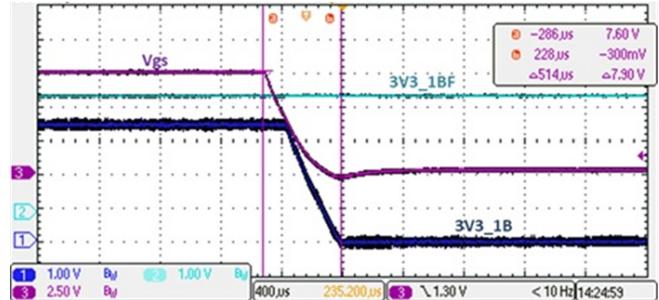


Figure 26. Overvoltage Protection of Rail B



### 3.2.4 Short Circuit Protection

Power rail A and power rail B have integrated short circuit protection with cycle-by-cycle current limiting. Figure 27 and Figure 28 highlight the protection when short circuit occurs. There is no ring and oscillation in short circuit status.

Figure 27. Short Circuit Protection of Rail A

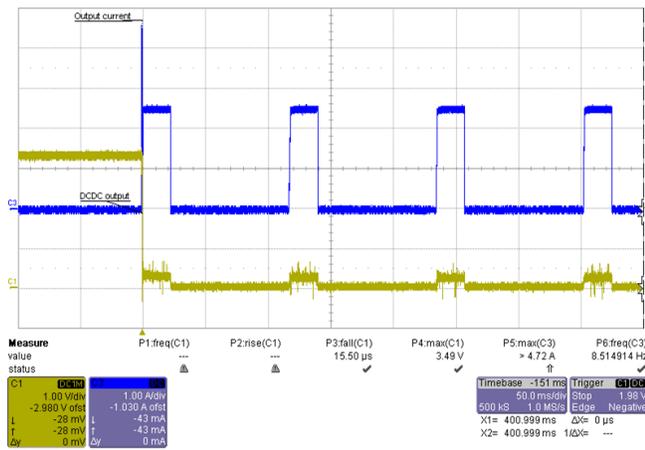
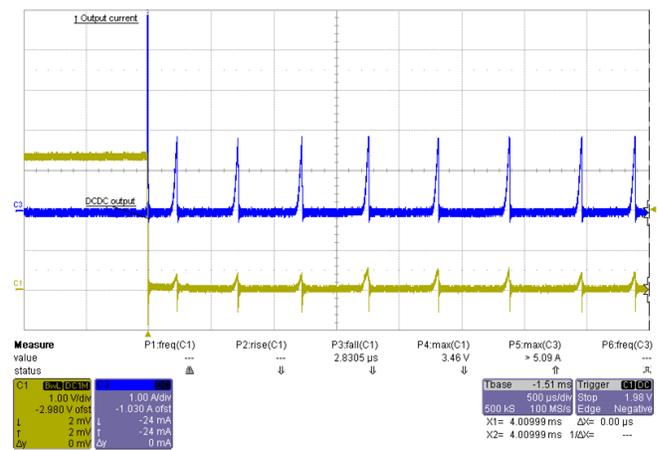


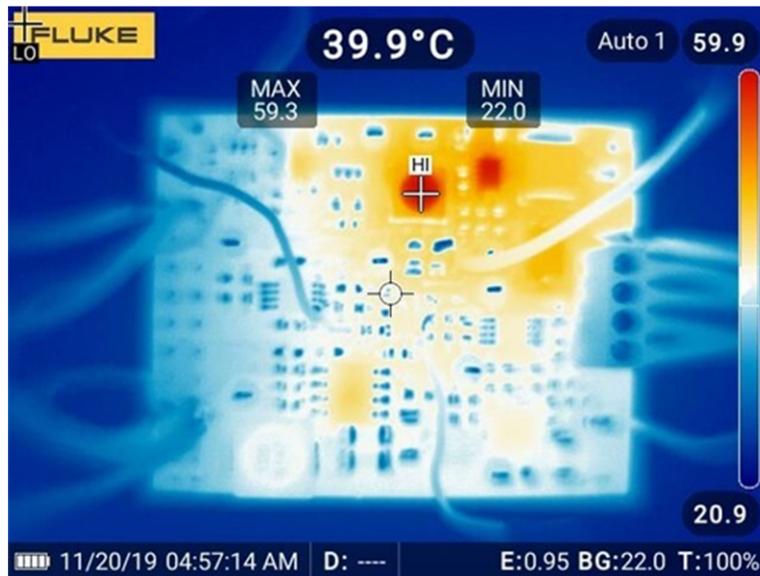
Figure 28. Short Circuit Protection of Rail B



### 3.2.5 Temperature Results

The thermal performance under full load is shown in Figure 29. Power rail A and power rail B have a 1-A output. The maximum temperature point is 59.3°C with an environment temperature of 22°C.

Figure 29. Thermal Image of the Board



## 4 Design Files

### 4.1 Schematics

To download the schematics, see the design files at [TIDA-010052](#).

### 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-010052](#).

### 4.3 PCB Layout Recommendations

#### 4.3.1 Minimizing Area of Switching Loop

The PCB layout of the DC/DC converter is critical to the optimal performance of the design. A smaller loop means smaller leakage inductance, which causes smaller transient voltage at the switching joint. Smaller transient will lead to less EMI.

#### 4.3.2 Layout Prints

To download the layer plots, see the design files at [TIDA-010052](#).

### 4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-010052](#).

### 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-010052](#).

### 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-010052](#).

## 5 Related Documentation

1. Texas Instruments, [TPS2660x 60-V, 2-A Industrial eFuse With Integrated Reverse Input Polarity Protection data sheet](#)

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## 6 About the Author

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