

FEATURES

- PROVIDES FAST AND EASY PERFORMANCE TESTING FOR DAC1220
- OPTIONAL OUTPUT BUFFER
- PC PRINTER PORT CONTROL
- WINDOWS® 95/98 SOFTWARE

NOTE: Shipped with 16-bit components.

DESCRIPTION

The DEM-DAC1220 evaluation fixture is designed for ease of use when evaluating the high resolution digital-to-analog converter DAC1220. The DAC1220 offers 20-bit monotonic performance with settling to 0.003% in 15ms typical. It also can be programmed for 16-bit settling to 0.012% within 2ms maximum.

The DAC1220 features a synchronous serial interface. It has been designed for closed-loop control applications in the industrial process market and high-resolution applications in the test and measurement market. It is also ideal for remote applications, battery powered instruments and isolated systems.

INITIAL CONFIGURATION

The DEM-DAC1220 is designed to be operational without any user configuration except connecting power supplies and the communications cable to the PC printer port.

POWER SUPPLY

The analog and digital supplies should be connected together at the power supply. That means that a pair of wires should go from the V_{CC} and AGND to the power supply and a separate pair of wires should go from V_{DD} and DGND to the same +5V power supply.

If a single pair of wires are used, then connect them to the analog connectors. A 10Ω resistor will source the current for the digital supply from the analog supply and the digital can get the ground reference from the computer interface.

VOLTAGE REFERENCE

The REF1004C-25 is used for the 2.5V reference. It is buffered using an OPA336 low current precision op amp. Another reference can be used by wiring it to the appropriate points in the breadboard area and removing the REF buffer.

CLOCK

A 2.5MHz crystal is connected to the XIN and XOUT pins to provide the maximum operating speed for the DAC1220.

PC BOARD LAYOUT

The DEM-DAC1220 evaluation fixture consists of a two-layer PC board. To achieve the highest level of performance, surface-mount components are used wherever possible. This reduces the trace length and minimizes the effects of parasitic capacitance and inductance. The evaluation fixture has a divided ground with all the analog signals over one portion and the digital signals in the other. Keep in mind that this approach may not necessarily yield optimum performance results when designing the DAC1220 into different individual applications. In any case, thoroughly bypassing the power supply and reference pins of the converter is strongly recommended.

The breadboard area is provided so that output filters can be added. Additionally an output op amp U4 can be used as a buffer to increase the output drive. The DAC1220 can source $500\mu A$. When an output buffer is used, remove the wire (R5) that connects the DAC1220 output to the output BNC.

A high performance voltmeter can be connected to the BNC to measure the output of the DAC1220. The software provides a means to drive the DAC1220 for checking linearity, monotonicity, offset and gain performance.

WINDOWS SOFTWARE

This software provides a convenient method (Figure 1) for writing or reading the Command (CMR), Data (DIR), Offset (OCR) and Gain (FCR) registers. The Instruction Register (INSR) is a write only register that controls the operations with the other registers. The formatting of information for the INSR is all handled by the program.

The Command Register is the most involved with most of the bits having specific control functions. The Demo software shows the bits that can be changed and shows the function that is associated with each bit. Of the two options for each bit, the top selection is equivalent to a zero and the bottom to a one. The 4 hex digits that represent the selection are shown as the bits are changed. When the correct options are selected they can be written to the DAC1220 with the "Write to Command Register" button. The current state of the Command Register can also be read with the "Read Command Register" button.

The Data, Offset, and Gain registers are all handled the same. Enter the 6 Hex Digits (3 bytes) that you want to write in the fields provided. Then select the Write button and the values will be written to the DAC1220. You can also read the current value of the same registers. The result of the read operation will be displayed in both hex and decimal format.

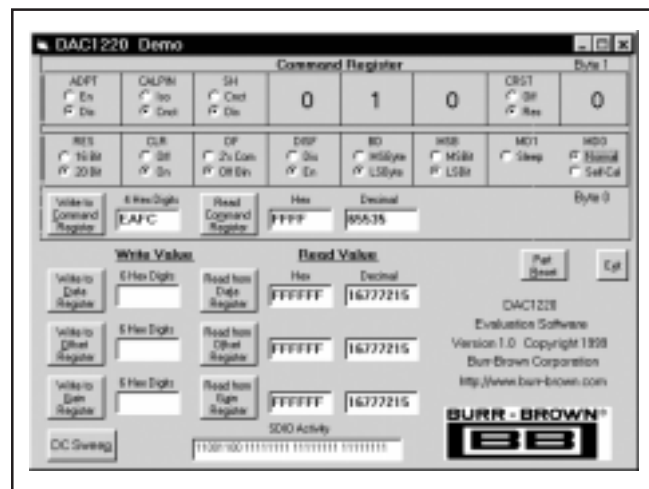


FIGURE 1. Demo Program Screen Display.

The SDIO Activity field will show the bits transferred to and from the DAC1220. This is very helpful when trying to understand the effect of changing the bit order or byte order. When non-default ordering is selected, that will not change the way data is entered or displayed. But you will observe a change in the bit patterns sent and received from the DAC1220. It can be very instructive to examine the details of the commands as they appear in the SDIO Activity display field.

The reset button sets the CLR (Clear Data Register) and CRST (Reset Calibration Registers) bits TRUE (1) and sends the command to the command register. After execution, these bits return to the default condition.

The DAC1220 Demo program can be terminated with either the X in the upper-right corner, or with the Exit button.

DC SWEEP

The DC Sweep button opens another window (Figure 2) that allows the user to enter the information for making a linearity test. There are two methods for generating a sweep: Step Size and End Point. For the Step Size method you enter the start code and the Step Size. Monotonicity can be checked by observing single bit changes. Use a value of 100_{HEX} for 16 bit steps and 10_{HEX} for 20 bit steps. The End Point method provides a convenient way to check linearity. By entering the Start, Stop and number of points.

20-BIT PERFORMANCE

The DEM-DAC1220 board is built as a 16-bit board with 2ms settling time. If 20-bit performance is desired then capacitors C1 and C2 must be changed; C1 = 10nF, C2 = 3.3nF. With the capacitor changes the monotonicity improves to 20 bits, the settling time is 15ms and the power consumption increases.

There are two methods of execution for the sweep. The Auto method waits after each step for at least the minimum selected delay. Depending on the PC, the time could be slightly longer. For the Manual sweep, the user hits the enter key between each DAC voltage step.

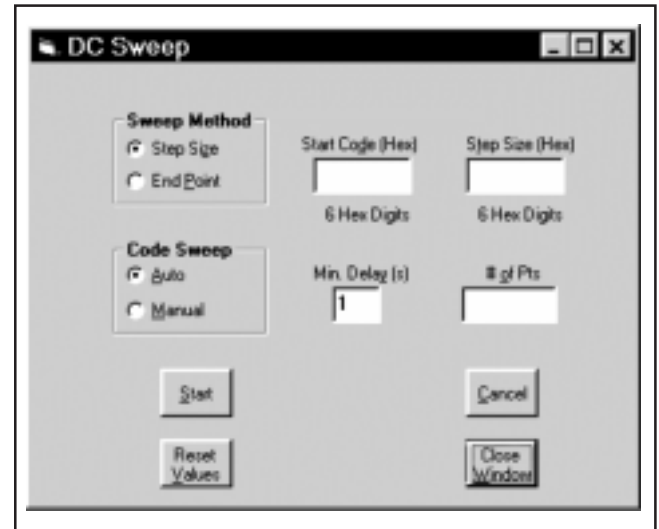


FIGURE 2. Screen Display of Sweep Control.

COMPONENT LIST

REFERENCE	QTY	COMPONENT	DESCRIPTION	MANUFACTURER
R4	1	CRCW120610R0F	RES, 10.0Ω, 0.125W, 1%	Dale
R3	1	CRCW120649R9F	RES, 49.9Ω, 0.125W, 1%	Dale
R2	1	CRCW12062002F	RES, 20.0kΩ, 0.125W, 1%	Dale
R1	1	CRCW12062492F	RES, 24.9kΩ, 0.125W, 1%	Dale
C11, C14	2	C315C569D2G5CA	CAP, 5.6pF, 200V, 0.5%, CERAMIC COG	Kemet
C2	1	C320C221J2G5CA	CAP, 220pF, 200V, 5%, CERAMIC COG	Kemet
C1	1	C320C222J2G5CA	CAP, 2200pF, 200V, 5%, CERAMIC COG	Kemet
C3, C4, C9, C10, C17	5	C1206C104K5RAC	CAP, 0.10μF, 50V, 10%, CHIP-CERAMIC X7R	Kemet
C12	1	C1210C103K5GAC	CAP; 0.01μF; 10%; 50V; COG	Kemet
C7, C13	2	C1210C104K5RAC	CAP, 0.10μF, 50V, 10%, CHIP-CERAMIC X7R	Kemet
DUT1	1	DAC1220E	Serial DAC; 16-Pin SSOP Package	Burr-Brown
Y1	1	ECS_V2.50-S	CRYSTAL; 2.5MHz	ECS
R5	1	FRJ-55	RES, 0.0Ω, 0.125W, 0%, METAL-FILM-JUMPER	Dale
U3	1	OPA336P	IC, OPAMP LOW POWER, RAIL-TO-RAIL I/O	Burr-Brown
U4	1	Any	IC, OPAMP	
U2	1	REF1004C-2.5	IC, VOLTAGE REFERENCE; 2.5V; CELL 8SO	Burr-Brown
R6	1	RN55C1001F	RES, 1.0kΩ, 0.125W, 1%, METAL-FILM	Dale
C6	1	T491A105K010AS	CAP, 1μF, 10V, 10%, TANTALUM CHIP-MOLDED	Kemet
C5, C8, C15, C16	4	T491D106K035AS	CAP, 10μF, 35V, 10%, TANTALUM CHIP-MOLDED	Kemet
CR1, CR2	2	1N5820	DIODE, SCHOTTKY BARRIER RECTIFIER 3 AMP	
U1	1	74hc367d	IC, Bus Driver, hex, 3-state outputs	Burr-Brown
J2	1	227161-2	RA BNC: VALOX CONNECTOR	AMP
J1	1	747842-6	25-Pin Right Angle Male D Conn	AMP
P1, P2	2	31165102	2 PIN TERM BLK	RIRCON
P1, P2	2	31024102	2 PIN HEADER; 3mm SPACING	RIRCON
FOR CABLE ASSY	1	8225-6060	3M 25 PIN D CONN-MALE-RIBBON	3M
FOR CABLE ASSY	1	8325-6060	3M 25 PIN D CONN-FEMALE-RIBBON	3M
VOR CABLE ASSY	6FT	3302/25	3M RIBBON CABLE-25 POSITION	3M

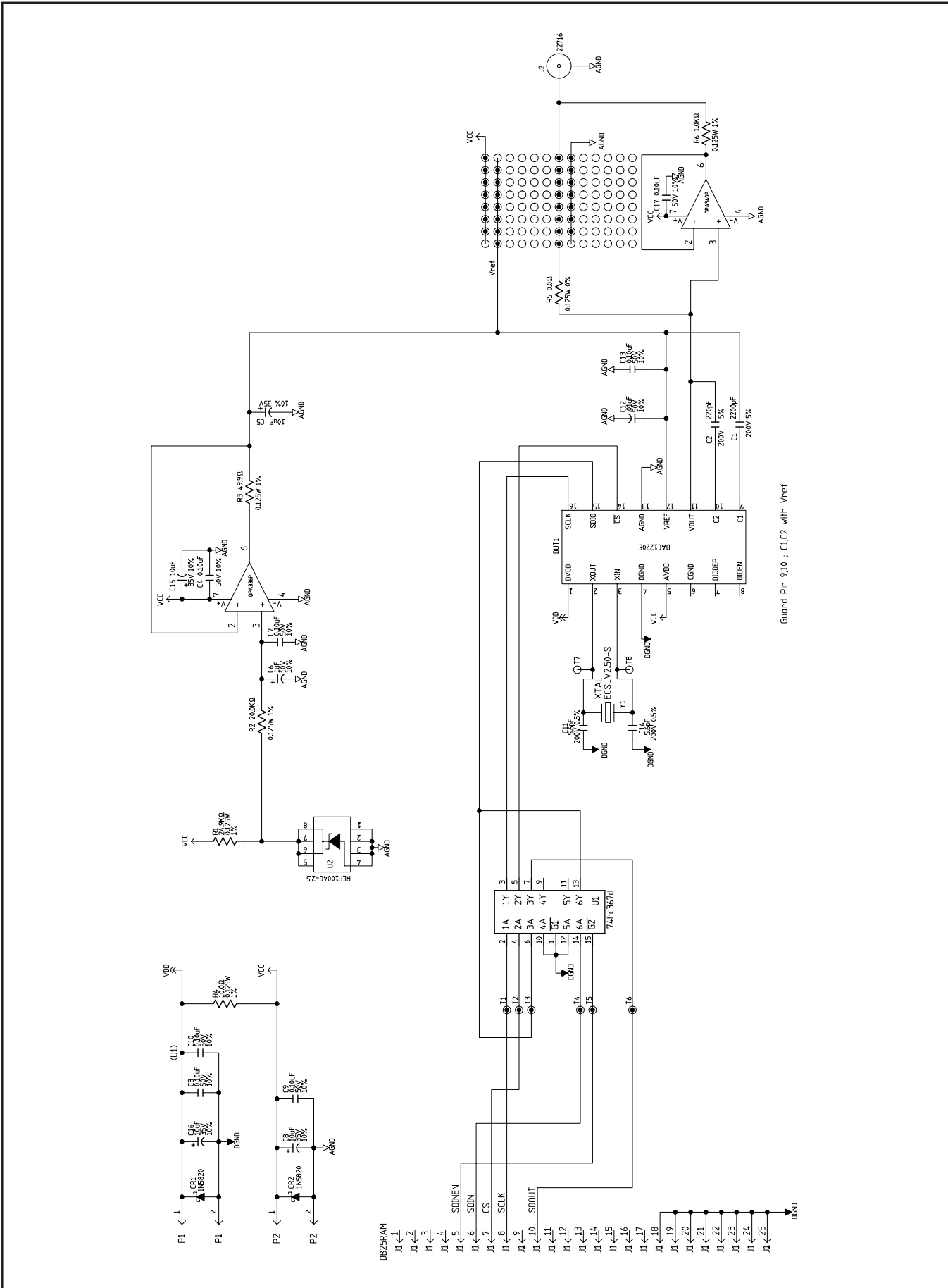


FIGURE 3. DEM-DAC1220.

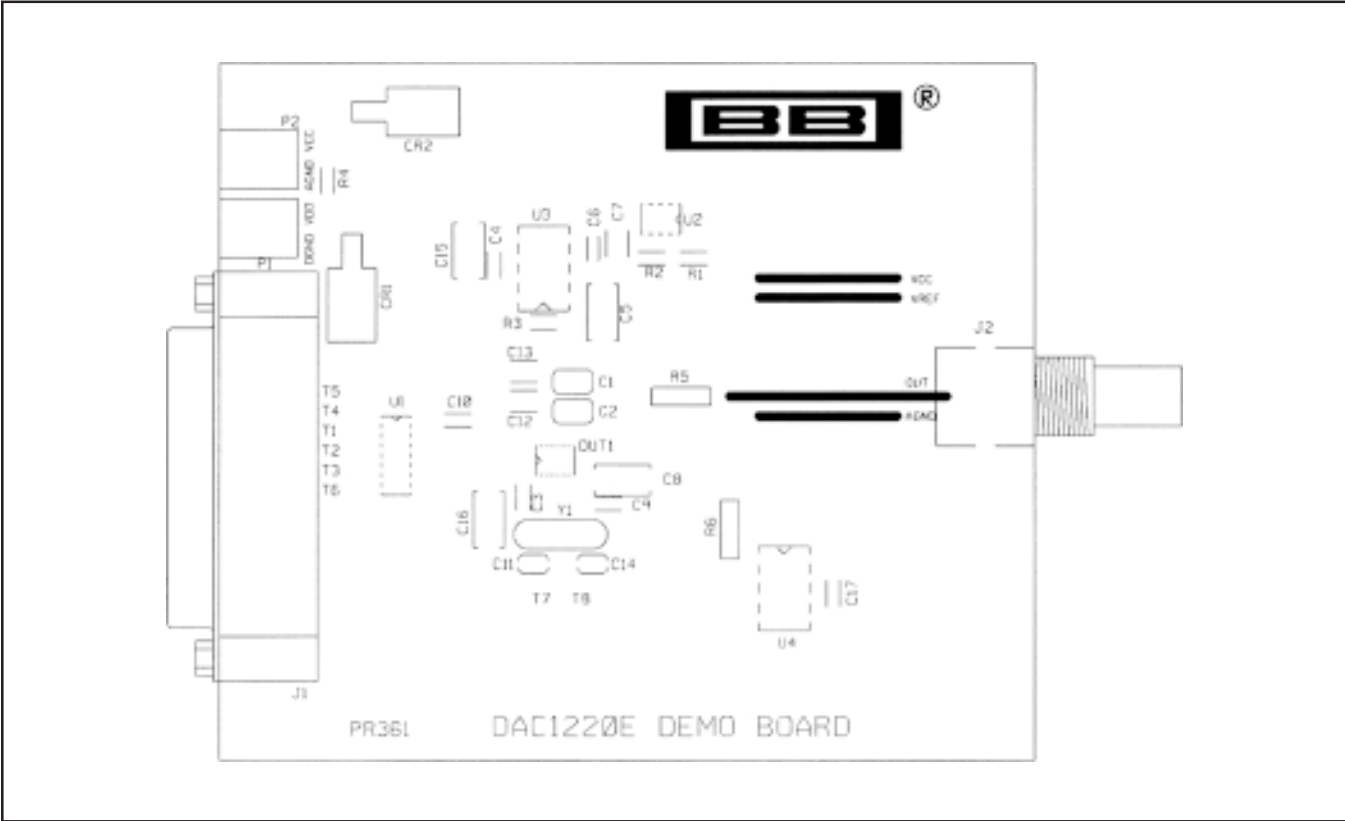


FIGURE 4. Top Layer Silk Screen.

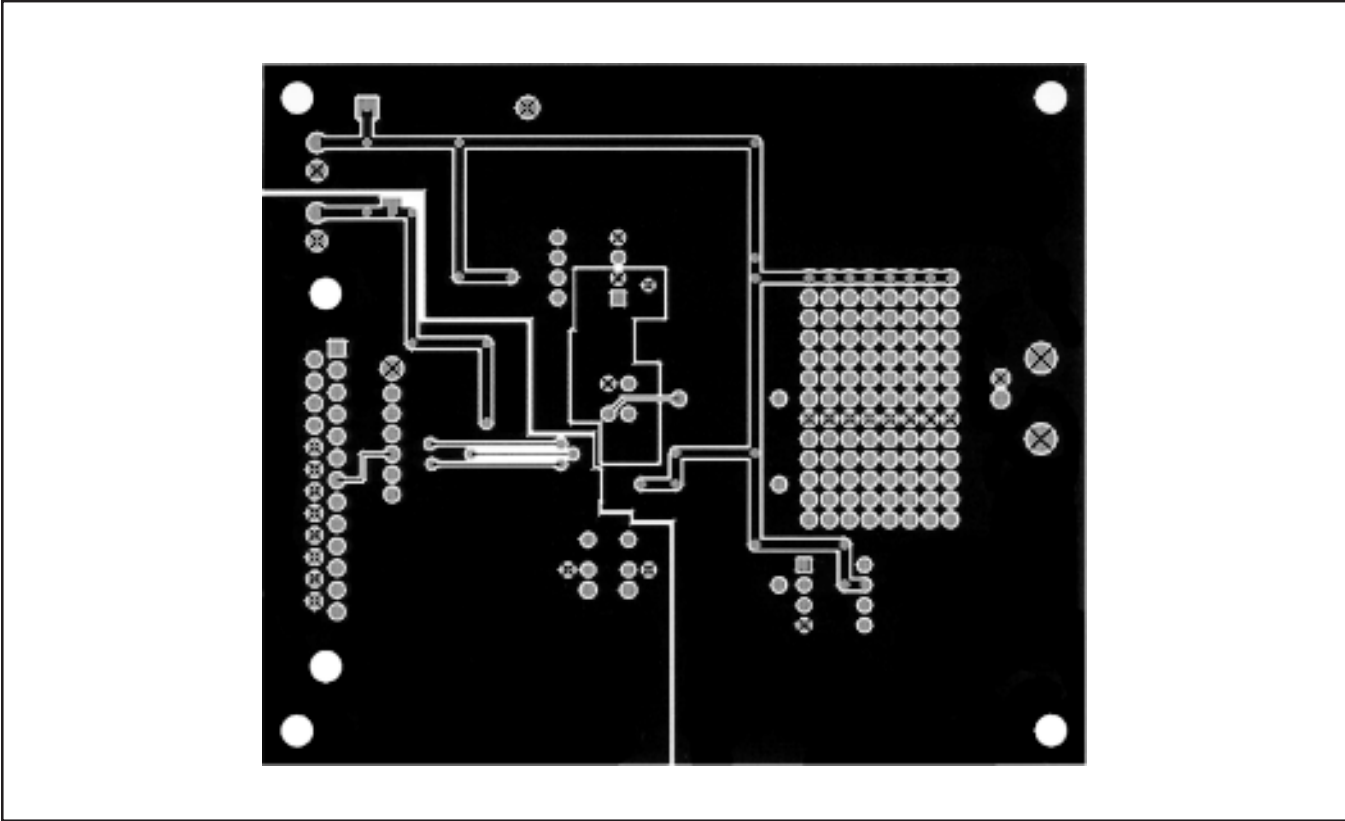


FIGURE 5. Top Layer.

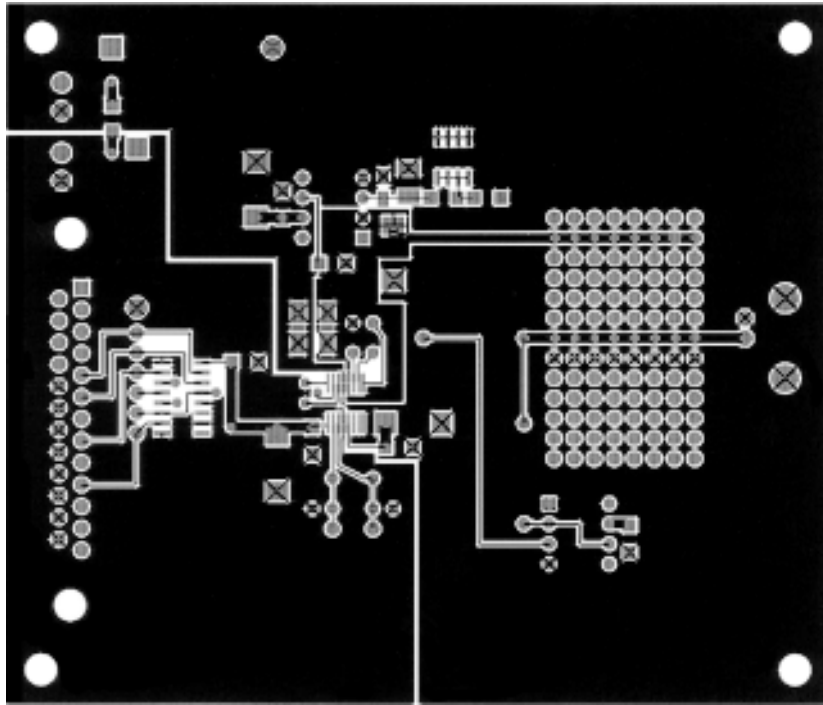


FIGURE 6. Bottom Layer.

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