Texas Instruments

5–6K Interface Board EVM

User's Guide

May 2004

Data Acquisition Products

SLAU104A

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±15 V and the output voltage range of ±15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 23°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

The 5−6K Interface Board provides a complete system development platform using evaluation modules from the Data Acquisition Products Group. This board passes signals from TMS320C5000™ and TMS320C6000™ DSK platforms featuring the 80-pin daughtercard connectors defined in the TMS320 Cross-Platform Daughtercard Interface (SPRA711), to a variety of analog-to-digital and digital-to-analog converters. When combined with sensor or amplifier boards, it can provide a complete data acquisition system for a variety of applications.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Signal Conditioning Sites
- Chapter 3—Serial EVM Sites
- Chapter 4—Parallel EVM Site
- Chapter 5—5−6K Interface Board Assembly and Schematics

Related Documentation From Texas Instruments

- TMS320 Cross-Platform Daughtercard Specification – SPRA711
- SN74CBT3257, 4-Bit 1-Of-2 FET Multiplexer/Demultiplexer – SCDS017
- SN74AHC1G04, Single Inverter Gate – SCLS318
- SN74AHC1G32, Single 2-Input Positive-OR Gate − SCLS317

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Tables

Chapter 1

Introduction

The 5−6K Interface Board provides data converter customers with the greatest amount of flexibility for the evaluation of data acquisition products from Texas Instruments. The Interface Board maintains a compatible interface with the TMS320™ DSP family according to the guidelines set forth in the *TMS320 Cross-Platform Daughtercard Specification* (SPRA711). Signal names and references to the multichannel buffered serial port (McBSP) found throughout this document are common to those found in the SPRA711 document.

The Interface Board consists of two signal conditioning sites, two serial EVM sites, and a parallel EVM site. Regardless of the interface type, all EVMs compatible with the 5−6K Interface Board have a standard analog interface and standard power connector. Three-position screw terminals J1 and J2 and two-position screw terminals J6, J8, J9, and J11 provide access to a common power bus routed to all sites.

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1.1 Power Connections to the Interface Card

The screw terminals along the bottom edge of the Interface Board give access to the common power bus. Three-port terminals J1 and J2 provide analog power. Two-port terminals J6, J8, J9, and J11 provide the digital voltages. Two jumpers, W2 and W3, located on the Interface Board give the user the option of using DSK +5 V and +3.3 V for the digital power. Analog power must be supplied from an external source. Table 1−1 shows the typical external power connections.

Table 1−1. External Power Connections

Screw Terminal	Applied Voltage	Typical Function
J1	±VA (±18 V Max)	Analog Voltage—provides analog power for signal conditioning, sensor boards, amplifiers, etc.
J2	±5V (±5.5 V Max)	Analog Voltage—provides analog power for signal conditioning, sensor boards, amplifiers, etc.
J6	+5 (5.5 V Max)	Digital Voltage—power to digital logic − ADCs, DACs, etc.
J8	+VD (undefined)	Digital Voltage—Reserved for future use
J9	+1.8 V (2.3 V Max)	Digital Voltage—core logic voltage for Codecs etc.
J11	+3.3 V (3.7 V Max)	Digital Voltage—power to digital logic – ADCs, DACs, etc.

Chapter 2

Signal Conditioning Sites

The signal conditioning sites provide a 20-pin analog I/O header and a 6-pin header for the analog power supply connections.

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2.1 Signal Conditioning Analog I/O Connection

The analog I/O connectors, J3 and J4, provide up to eight single-ended or four differential channels to/from the data converter. External reference voltages can also be applied to the data converter through the analog I/O connector. Because the reference requirements vary by converter type, no restrictions are placed on the input voltage levels. Be sure to check the documentation for the EVM before applying any input signals. Single- and dual-channel converters leave the unused pins open. Table 2−1 shows the standard analog connector pinout. See Section 3.3 for details on applying differential signals.

Table 2−1. Signal Conditioning I/O Connections

Signal	Pin Number		Signal
A0−	**1**	**2**	A0
A1−	**3**	**4**	A1
A2−	**5**	**6**	A2
A3−	**7**	**8**	A3
AGND	**9**	**10**	A4
AGND	**11**	**12**	A5
AGND	**13**	**14**	A6
VCOM	**15**	**16**	A7
AGND	**17**	**18**	REF−
AGND	**19**	**20**	REF+

The 20-pin headers located beside JP1 and JP2 provide stability for the signal conditioning boards—no signals are routed to or from these connectors. These connectors are labeled *Analog 1* and *Analog 2* in the assembly drawing found in Chapter 5.

2.2 Signal Conditioning Power Connector

The Interface Board provides a common power bus to both signal conditioning sites. The power connector used on the Interface Board is a 6-pin male header. Four power connectors JP1, JP2, JP3, and JP4 are provided—each with the same pinout. This allows an analog-to-digital (ADC) converter to use the same signal conditioning board as a digital-to-analog (DAC) converter, simply by rotating the signal conditioning board 180 degrees.

Table 2−2 shows the power connector voltages supplied to the signal conditioning module.

Table 2−2. Signal Conditioning Power Connections—JP1, JP2, JP3, and JP4

Signal	Pin Number		Signal
+VA	**1**	**2**	−VA
+5VA	**3**	**4**	−5VA
AGND	**5**	**6**	AGND

Chapter 3

Serial EVM Sites

The serial interface consists of two digital I/O connectors (J15 and J16), two power connectors (JP5 and JP6), and two analog I/O connectors (J10 and J12). The analog I/O connectors are configured as *pass through* connections from/to the signal conditioning sites. See section 2.1 for more information.

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3.1 Serial Digital I/O Connections

The serial site digital I/O connectors are 20-pin headers that provide access to the serial interface signals defined in the *TMS320 Cross-Platform Daughtercard Specification* (SPRA711). These signals are based on the multichannel buffered serial port (McBSP) interface found on most Texas Instruments DSPs. Table 3−1 shows the standard serial connector pinout.

Table 3−1. Digital I/O Connections—J15 and J16

Signal		Pin Number		Signal	
Site 1 (J16)	**Site 2 (J15)**			**Site 1 (J16)**	**Site 2 (J15)**
DC_CNTLb	DC_CNTLa	**1**	**2**	TP Access	TP Access
DC_CLKXb	DC_CLKXa	**3**	**4**	DGND	DGND
DC_CLKRb	DC_CLKRa	**5**	**6**	TP Access	TP Access
DC_FSXb	DC_FSXa	**7**	**8**	TP Access	TP Access
DC_FSRb	DC_FSRa	**9**	**10**	DGND	DGND
DC_DXb	DC_DXa	**11**	**12**	TP Access	TP Access
DC_DRb	DC_DRa	**13**	**14**	TP Access	TP Access
DC_INTc	DC_INTa	**15**	**16**	TP Access	TP Access
DC_TOUTb	DC_TOUTa	**17**	**18**	DGND	DGND
TP Access	TP ACcess	**19**	**20**	TP Access	TP Access

Note: Revision B boards include pulldown resistors at all points listed as TP Access via 6-position slide switches SW1 and SW2.

3.2 Chip Select, Frame Sync and Interrupt Options

The TMS320 Cross−Platform Daughtercard Specification defines the DC_CNTLx signals as alternate chip select sources. DC_CNTLx is a GPIO signal controlled by the CPLD located on the C5000 and C6000 DSK boards. DC_CNTLa and DC_CNTLb are routed directly to pin 1 of the Digital I/O connectors (J15 and J16 respectively) on Revision A Interface Boards. Revision B interface boards include jumpers W12 and W13 which apply the DC_CNTLx signal (default) or digital ground (shunt pins 2−3) to pin 1 of the digital I/O connectors.

Revision B interface boards also include jumpers W10 and W11 which allow the user to apply the FSX signal (default) or DC_CNTLx signal (shunt pins 2−3) to pin 7 of the digital I/O connectors. W10 controls the application of DC_FSXa or DC_CNTLa on J15, while W11 controls the application of DC_FSXb or DC_CNTLb on J16.

Jumpers W8 and W9 allow the signals applied to DC_INTa or DC_INTc to be directly sourced from the data-converter EVM when the shunts are installed on pins 1-2 (default). Moving the shunt on W8 to pins 2-3 sends the EVM interrupt signal through a single-gate inverter (U5) before being sent to DC-INTa on the DSK. W9 controls the polarity of the signal applied to DC-INTc via U6.

3.3 EVM Power Connector

The Interface Board provides a common power bus to both serial sites. The power connector used on the Interface Board is a 10-pin male header. Two power connectors JP5 and JP6 are provided—each with the same pinout. JP5 services serial Site 2, while JP6 services serial Site 1. Table 3−2 shows the power-connector voltages supplied to the EVM.

Table 3−2. EVM Power Connections—JP5 and JP6

Signal	Pin Number		Signal
+VA	**1**	**2**	−VA
+5VA	**3**	**4**	−5VA
DGND	**5**	**6**	AGND
+1.8VD	**7**	**8**	VD1
+3.3VD	**9**	**10**	+5VD

3.4 EVM Analog I/O Connector

As mentioned previously, the analog I/O connectors act as *pass-through* connectors to the signal conditioning sites. Table 3−3 shows the analog I/O connections to the serial and parallel EVM sites.

Table 3−3. EVM Analog I/O Connections—J10 and J12

Signal	Pin Number		Signal
A0−	**1**	**2**	A0
A1−	**3**	**4**	A1
A2−	**5**	**6**	A2
A3−	**7**	**8**	A3
AGND	**9**	**10**	A4
AGND	**11**	**12**	A5
AGND	**13**	**14**	A6
VCOM	**15**	**16**	A7
AGND	**17**	**18**	REF−
AGND	**19**	**20**	REF+

Note: J10 and J12 are also used for the parallel EVM site.

When applying differential signals to a data converter EVM, the signal pairs may be applied between pin pairs 1-2, 3-4, 5-6, and 7-8, or pin pairs 2-4, 6-8, 10-12, and 14-16. The pin assignment for the signal pair is determined by the EVM being used. See the specific EVM user's guide for implementation details.

Chapter 4

Parallel EVM Site

The parallel interface consists of a 48-pin header (J17), which provides access to up to 24 parallel data bits and a 20-pin parallel control header (J18). The parallel control header provides four multiplexed address lines, configurable read and write strobes, configurable interrupts, and chip-select and clock signals. Analog I/O and power is also provided.

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4.1 Parallel Analog I/O and Power Connections

The parallel site uses the same analog I/O and power connections described in the serial interface section of this manual. Typically, a parallel-ADC EVM uses the analog interface connector located at J10 and the power connector located at JP5. See Chapter 3 for pinout details. A parallel-DAC EVM typically uses the analog interface connector J12, presenting the opportunity to stack certain EVMs.

4.2 Parallel Control Connector—J18

The parallel control connector feeds chip-select, read, write, and address lines to the parallel EVMs. The address decoding for most parallel EVMs is done on the EVM card itself, allowing the possibility of *stacking* several cards together. Table 4−1 shows the typical signals found on parallel interface EVMs, designed to be used with the 5−6K Interface Board

Table 4−1. Parallel Control Connections

Signal	Pin Number		Signal
DC_CSx	**1**	**2**	DGND
$\overline{\text{WR}}$ (R/W)	**3**	**4**	DGND
$\overline{\text{RD}}$	**5**	**6**	DGND
EVM_A0	**7**	**8**	DGND
EVM_A1	**9**	**10**	DGND
EVM_A2	**11**	**12**	DGND
EVM_A3	**13**	**14**	DGND
GPIO (SPARE−NC)	**15**	**16**	DGND
TOUTa	**17**	**18**	DGND
INT	**19**	**20**	DGND

DC_CSx is defined in the *TMS320 Cross-Platform Daughtercard Specification*. This signal is intended to act as a chip-select to the EVM, not necessarily the actual data converter being evaluated. Carefully read the documentation that came with your EVM for details on how this signal is used. Revision-B Interface boards include jumper W16 which applies DC_CSa (default) or DC_CSb (shunt pins 2−3) to J18 pin 1.

The write and read strobes can be controlled through jumpers W4 and W5 on the Interface Card. With W4 and W5 in their default positions (shunt on pins 2−3), $\overline{\text{WR}}$ and $\overline{\text{RD}}$ are defined as in the *TMS320 Cross-Platform Daughtercard Specification.* With the shunts on W4 and W5 in positions 1−2, combination logic located on the interface card can provide a simple strobing arrangement which may be useful with the TMS320C5402 DSK.

The EVM address lines EVM_A0 through EVM_A3 are fed from a four-bit 2:1 bus switch, U1. Typically, this provides access to DSP address lines A2..A5, or A14..A17. A shunt on W1 (default) applies the DSK address lines A2..A4 to the parallel control connector; removing the shunt from W1 applies address lines A14..A17. The actual address lines vary depending on the DSK used; see your DSK documentation for the exact address locations.

The interface card provides four options for a clock source to the parallel EVM interface with use of a 2-mm shunt on J14.

Table 4−2. Parallel EVM Clocking Options via J14

Shunt on Pins	Clock Source
1−2	DC_TOUTa
3−4	DC_TOUTa
5−6	DC_CLKXa
7−8	DC_CLKXb

The interface card provides two options for an external interrupt source to the DSP with use of a 2-mm shunt on J15.

Table 4−3. External Interrupt Source via J13

Shunt on Pins	Connects To:	
	Rev A PWB	Rev B PWB
1−2	DC_INTa	DC_INTb
3−4	DC_INTb	DC_INTb
5−6	DC_INTc	DC_INTd
7−8	DC_INTd	DC_INTd

Note: External interrupts shown in this table are based on the TMS320C6711 DSK.

4.3 Inverted Interrupts

Jumper W7 on the 5−6K Interface Board revision B expands the interrupt capabilities of certain data-converter EVMs. W7 controls the signal applied to J13 via single-gate inverter U7. When a shunt is installed on W7-pins 1-2 (default), the interrupt signal is applied directly to J13. Installing the shunt on W7-pins 2-3 provides an interrupt inverted signal to J13 via U7.

4.4 Parallel Data Bus Connector—J17

The parallel data connector used on the Interface Card is a 48-pin male header. Typical parallel EVMs have a data bus that is a minimum of 16 bits wide and a maximum of 24 bits. Bus expansion is done in 4-bit increments. Data is aligned LSB to LSB.

Table 4−4 shows the parallel data bus connections.

Table 4−4. Parallel Data Connections

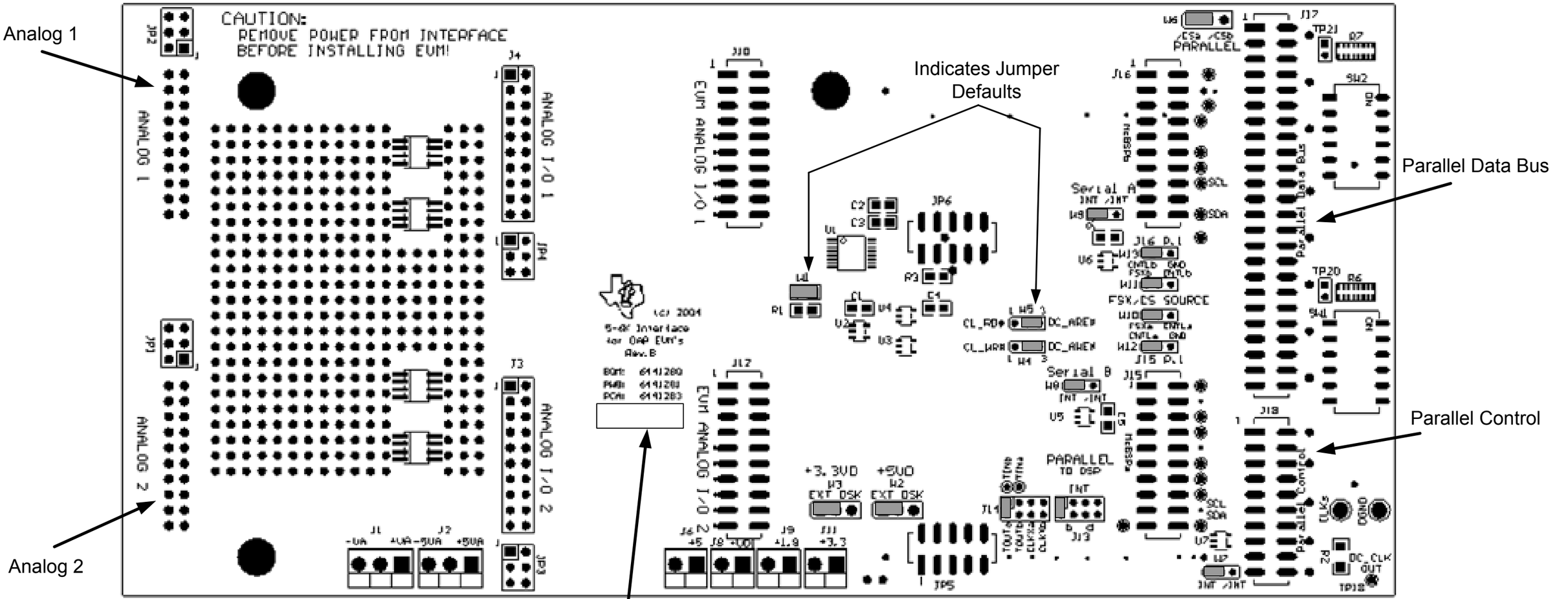
Signal	Pin Number		Signal
D0	**1**	**2**	DGND
D1	**3**	**4**	DGND
D2	**5**	**6**	DGND
D3	**7**	**8**	DGND
D4	**9**	**10**	DGND
D5	**11**	**12**	DGND
D6	**13**	**14**	DGND
D7	**15**	**16**	DGND
D8	**17**	**18**	DGND
D9	**19**	**20**	DGND
D10	**21**	**22**	DGND
D11	**23**	**24**	DGND
D12	**25**	**26**	DGND
D13	**27**	**28**	DGND
D14	**29**	**30**	DGND
D15	**31**	**32**	DGND
D16	**33**	**34**	DGND
D17	**35**	**36**	DGND
D18	**37**	**38**	DGND
D19	**39**	**40**	DGND
D20	**41**	**42**	DGND
D21	**43**	**44**	DGND
D22	**45**	**46**	DGND
D23	**47**	**48**	DGND

Chapter 5

5–6K Interface Board Assembly and Schematics

The board assembly and schematics are attached on the following pages.

5-6K Interface Board (Rev. B) - Top View



Analog 1

Analog 2

Indicates Jumper Defaults

Signal Conditioning Site 1

Analog I/O = J4
Power = JP2 or JP4

Signal Conditioning Site 2

Analog I/O = J3
Power = JP1 or JP3

Assy. Revison Label

Serial Site 1

Analog I/O = J10
Digital I/O = J16
Power = JP6

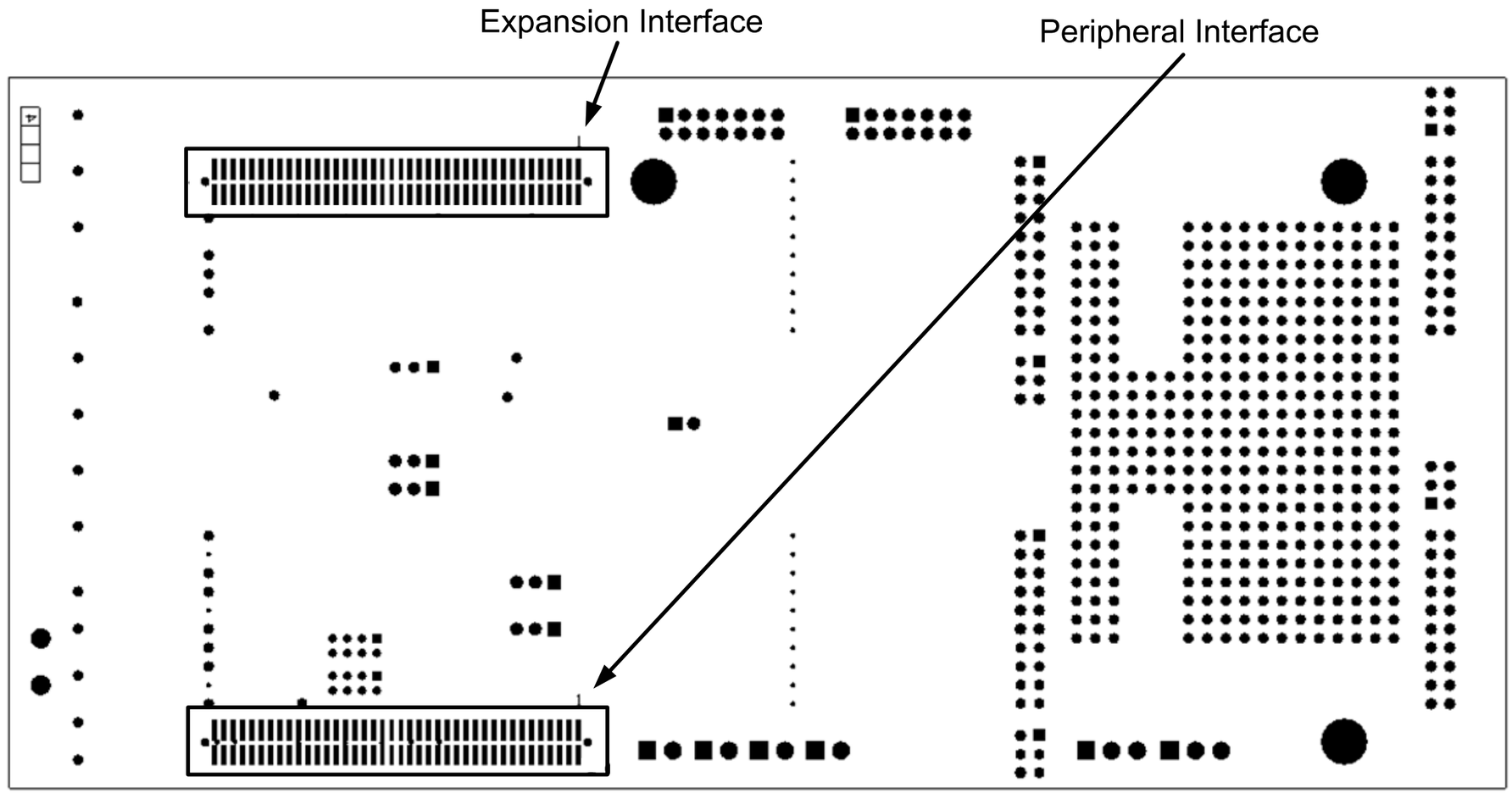
Serial Site 2

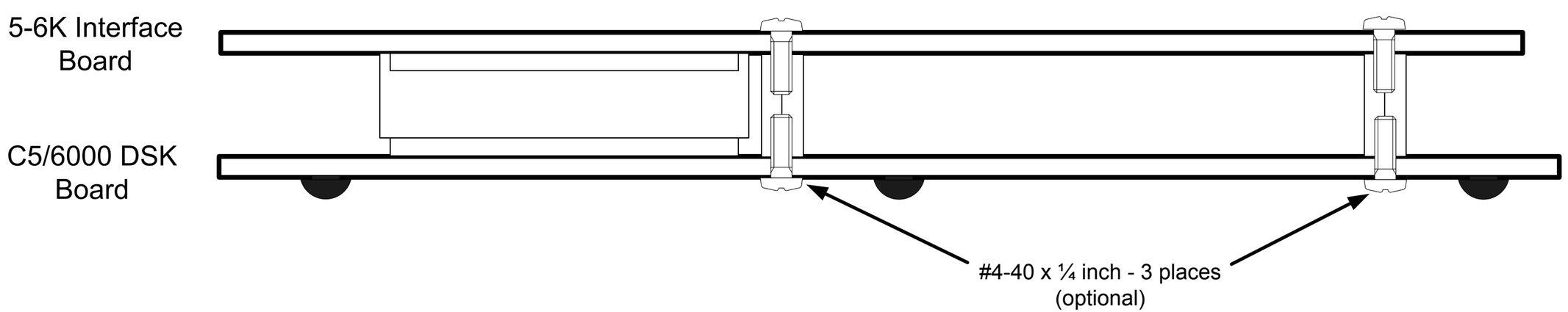
Analog I/O = J12
Digital I/O = J15
Power = JP5

Parallel Interface

Analog I/O = J10 (ADC's) or J12 (DAC's)
Parallel Data Bus = J17
Parallel Control = J18
Power = JP5

5-6K Interface Board - Bottom View

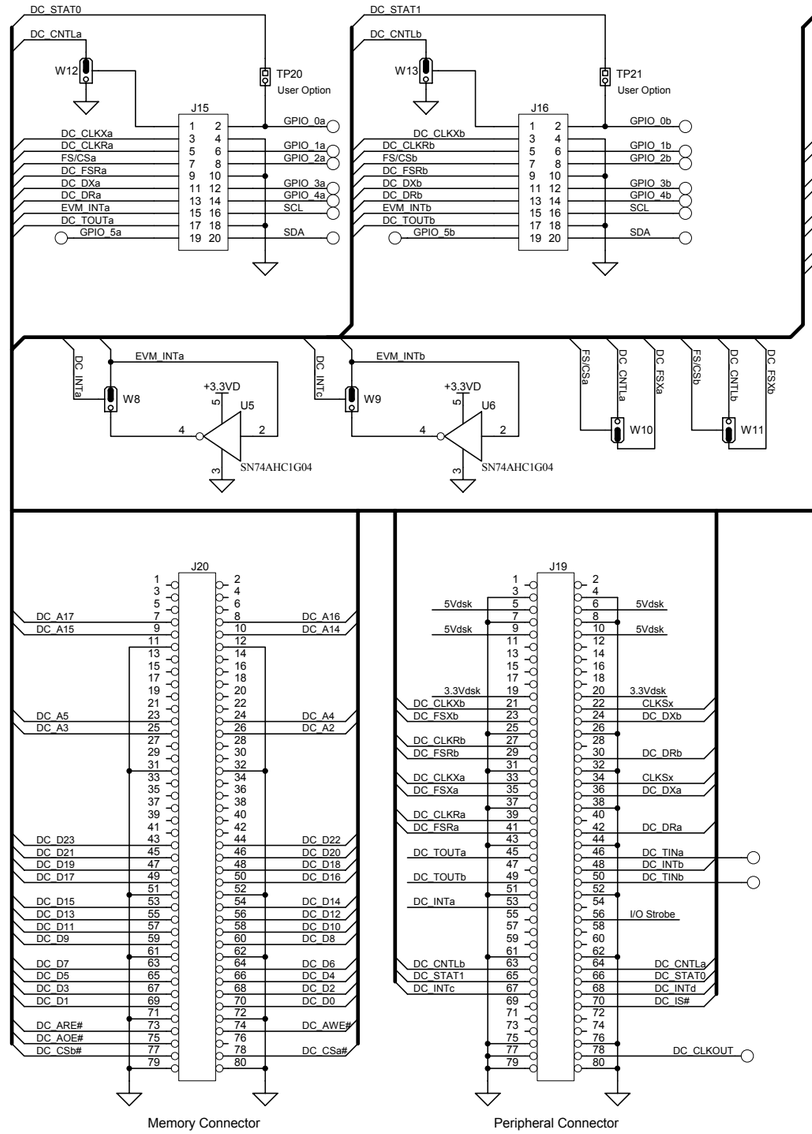


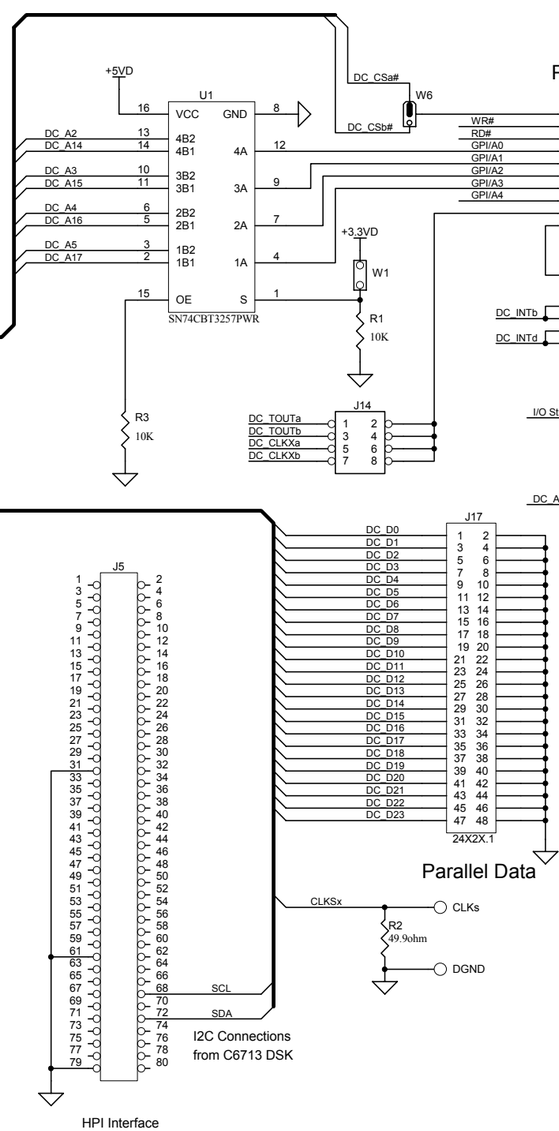


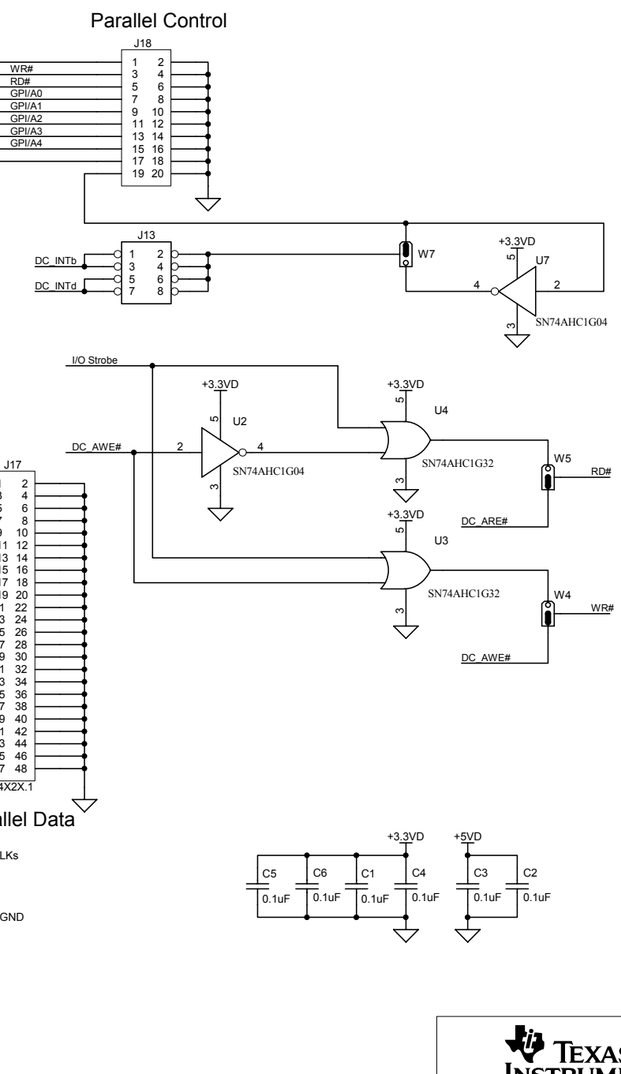
Serial EVM Digital Interface

Note: GPIO Test Points to Switch - See Page 2

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH
B	Design Enhancements	04/02/04







SPRA711 Daughtercard Interface

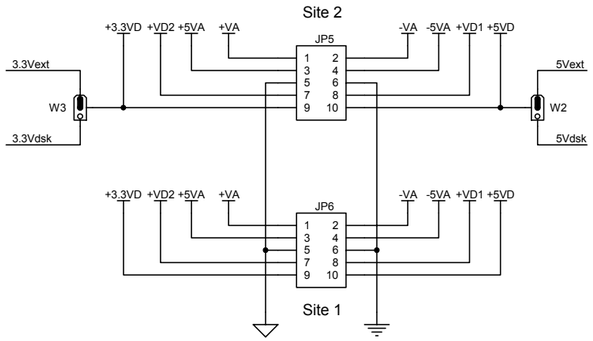
TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

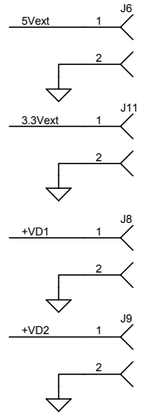
Title: 5-6K Interface Board Schematic

Engineer: Tom Hendrick			
Drawn By: Tom Hendrick	SIZE: B	DATE: 12-May-2004	REV: B
FILE: EDGE #6441282			SHEET: 1 OF: 2

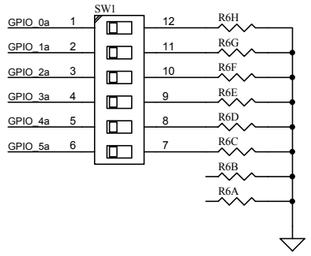
DAP EVM Power Connections



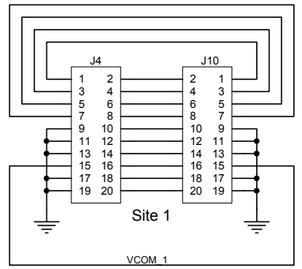
Interface Card Digital Power Connections



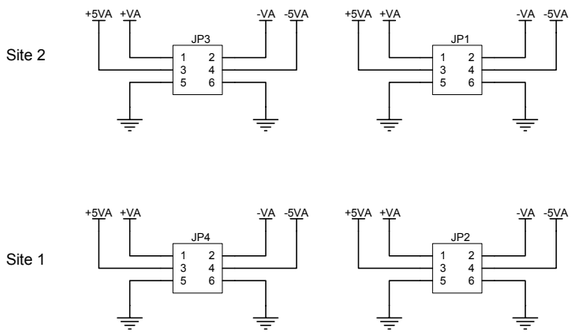
GPIO Switches



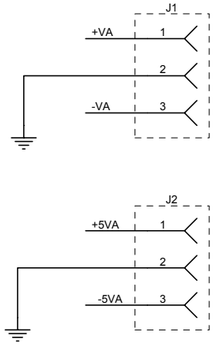
Signal Conditioning In/Out to EVM Analog In/Out

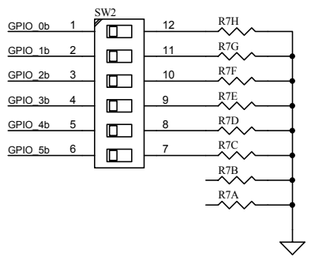


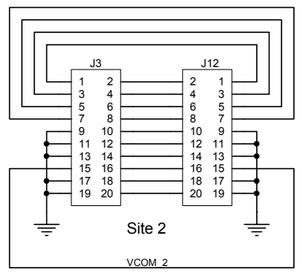
Amplifier Card Power Connections



Interface Card Analog Power Connections







TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: DAP 54xx / 67xx DSK Interface

Engineer: Tom Hendrick					
Drawn By: Tom Hendrick	SIZE: B	DATE: 12-May-2004	REV: B		
FILE: EDGE #6441282			SHEET: 2	OF: 2	