

# **TPS65120EVM-076/ TPS65124EVM-076**

# User's Guide

August 2004

**PMP Portable Power** 

#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address:

Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated

#### **EVM IMPORTANT NOTICE**

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated

#### **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the input voltage range described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated

#### Preface

### **Read This First**

#### About This Manual

This user's guide describes the characteristics, operation, and use of the TPS65120EVM–076 and TPS65124EVM–076 evaluation modules (EVM). Included are EVM specifications, test results, schematic diagram, bill of materials (BOM), and recommended test setup.

#### How to Use This Manual

This document contains the following chapters:

- □ Chapter 1 Introduction
- Chapter 2 EVM Operation
- □ Chapter 3 Board Layout
- □ Chapter 4 Bill of Materials and Schematic

#### **Related Documentation From Texas Instruments**

SLVS531 – TPS6512x data sheet

#### FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

#### If You Need Assistance

Contact your local TI representative.

# Contents

1	1.1 1.2	luction Background Performance Specification Summary Modifications	1-2 1-2
2	EVM	Operation	2-1
	2.1	Input/Output Connections Test Setup	2-2
	2.2	Test Setup	2-3
	2.3	Test Results	2-3
3	Board	l Layout	3-1
	3.1	Board Layout	3-2
4		f Materials and Schematic	
		Bill of Materials	
	4.2	Schematic	4-3

# Figures

2–1	Main Output Efficiency vs Load Current	2-3
2–2	Main Output Ripple Voltage	2-4
2–3	VGH and VGL Output Ripple	2-4
	Top Assembly Layer	
3–2	Top Layer Routing	3-3
	Bottom Layer Routing	
4–1	HPA076 Schematic	4-4

# **Tables**

1–1	Typical Performance Specification Summary for V <sub>IN</sub> = 3.6 V and $T_A = 25^{\circ}C$	1-2
4–1	HPA076 Bill of Materials	4-2

# Introduction

This chapter contains introductory information about the TPS65120EVM–076 and TPS65124EVM–076 evaluation modules.

Горі	c F	age
1.1	Background	1-2
1.2	Performance Specifiction Summary	1-2
1.3	Modifications	1-2

#### 1.1 Background

The TPS65120EVM uses a TPS65120 single inductor, multichannel output IC to provide the three output voltages necessary to power amorphous silicon (a–Si) and low-temperature polysilicon (LTPS) TFT-LCD displays. The TPS65120 has integrated power–up/down sequencing and an auxiliary linear regulator providing an additional 3.3-V rail. The TPS65124EVM uses a TPS65124 IC that provides the same output rails as the TPS65120EVM, except that it has user-programmable power-up/down sequencing and replaces the linear regulator with enable signals for VGH and VGL.

#### 1.2 Performance Specification Summary

0	Output Voltage (V)			Output Current (mA)		
Specification	Min	Тур	Мах	Min	Тур	Max
VMAIN	4.95	5.00	5.05			25
VGH	11.64	12.00	12.36			4
VGL	-12.36	-12.00	-11.64			4
LDOOUT (65120)	3.20	3.30	3.40			20

Table 1–1. Typical Performance Specification Summary for  $V_{IN}$  = 3.6 V and  $T_A$  = 25°C

#### 1.3 Modifications

The HPA076 PCB was designed to allow for several user-defined modifications. In addition to being able to accommodate the other members of the TPS6512x family, the board has unpopulated footprints of passive and active elements which provide the following:

- □ VLOGIC Rail P-channel FET Q1 (e.g., Si1031x) and supporting passives C4, C9, C11, R11, R12, and J6 allow the input voltage to be gated and provide a rail to power peripheral logic circuits . In addition, VLOGIC enables VMAIN, VGH, and VGL after the RC time constant delay formed by R11 and C9 (if R1 is removed).
- VMAIN Power–Down Sequencing The TPS65120/1/2 actively power down VMAIN only after FBL reaches 1.2 V typical. Using N-channel FET Q2 (e.g., Si1032X) and supporting passives R10, R14, and R15 to alter FBL, VMAIN's power-down sequencing trip point can be moved. See the TPS6521x data sheet (SLVS531) for guidance on sizing the passive components.
- Independent VMAIN Sequencing After RUN is pulled high, the TPS6512x devices power up VMAIN. Using dual transistor Q3 (e.g., Si1016X), supporting passives JP4, R16, and R20, and removing R18, a switch can be constructed to switch in VMAIN as the application requires. R18 shorts out Q3.

- More Current From VMAIN An external linear regulator U3 (e.g., TPS79201) powered from BOOT and supporting passives, C14, C15, R17, and R19 can be added to provide more output current for VMAIN. The linear regulator data sheet provides guidance on sizing the supporting passives. Size feedback resistors R17 and R19 so that the regulator output is about 1% below VMAIN. See theTPS6521x data sheet (SLVS531) for guidance on sizing the output capacitor on BOOT relative to C14.
- A Second Negative Rail, VGL2 An external linear regulator U2 (e.g., TPS72301) powered from VGL and supporting passives C5, R5, R6, JP3, and J5 can be added to provide a second negative voltage rail. The linear regulator data sheet provides guidance on sizing the supporting passives. The middle pin of JP3 connects to the EN pin on the TPS72301 IC. Tying this pin to VIN enables the IC. Tying this pin to GND disables the IC. J5 is the output terminal for the second negative rail, VGL2. See the TPS6521x data sheet (SLVS531) for guidance on sizing the output capacitor on VGL relative to C5.
- □ Lower Output Ripple on VGH and VGL C3 and C7 accommodate 10-pF feedforward capacitors that reduce the output ripple on VGH and VGL, respectively.

# **EVM Operation**

This chapter describes how to properly test the TPS65120 and TPS65124 using the TPS65120EVM and TPS65124EVM.

Торі	c Page
2.1	Input/Output Connections 2-2
2.2	Test Setup 2-3
2.3	Test Results

#### 2.1 Input/Output Connections

The EVM's input and output connections are described in the following paragraphs.

- J1-VIN This header connects to the positive terminal of the input power supply.
- □ J2-GND This header connects to the negative terminal of the input power supply.
- □ J3-VGH This header is the output terminal for the boosted gate voltage, VGH.
- **J4-GND** This header is a GND terminal.
- **J7-GND** This header is a GND terminal.
- □ **J8-VGL** This header is the output terminal for the inverted gate voltage, VGL.
- J9-VMAIN This header is the output terminal for the main voltage, VMAIN.
- **J10-GND** This header is a GND terminal.
- □ **J11-BOOT** This header is measurement/sense point for the bootstrap voltage, BOOT.
- ❑ JP1-EN The middle pin of this jumper connects to the EN pin on the IC. Tying this pin to VIN enables VMAIN on the IC. Tying this pin to GND disables VMAIN on the IC.
- □ JP2-RUN The middle pin of this jumper connects to the RUN pin on the IC. Tying this pin to VIN begins the power–up procedure of the IC. Tying this pin to GND disables the IC.
- □ JP5-LDOIN on TPS65120EVM or VGL on TPS65123EVM For the TPS65120EVM, the middle pin of this jumper is a measurement/ sense point for the input to the auxiliary LDO and pin 3 is GND. LDOIN is connected to BOOT through  $0-\Omega$  resistor R7. Pin 1 is floating.

For the TPS65124EVM, the middle pin of this jumper connects to VGL pin on the IC. Tying this pin to ON enables VGL; tying it to OFF disables VGL.

□ JP6-LDOOUT on TPS65120EVM or VGH on TPS65124EVM For the TPS65120EVM, the middle pin of this jumper is the output for the auxiliary linear regulator, and pin 3 is GND. Pin 1 is floating.

For the TPS65124EVM, the middle pin of this jumper connects to VGH pin on the IC. Tying this pin to ON enables VGH. Tying this pin to OFF disables VGH.

The headers and jumpers that were omitted in the previous discussion are not populated on the EVM and are discussed in section 1.3.

#### 2.2 Test Setup

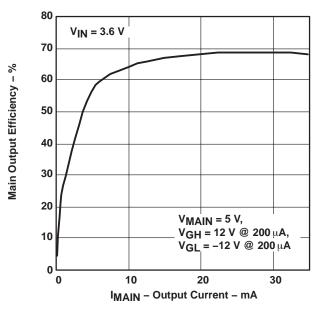
Although the absolute maximum voltage for V<sub>IN</sub> is 6 V, the TPS6512x family is designed to operate with input voltages of 5.5 V or less. For best results with the EVM as packaged, connect a power supply with a 3.3-V output voltage and current limit set to at least 500 mA.

To enable the TPS65120EVM, first short pins 1-2 of jumper JP2 (tie RUN to ON); then short pins 1-2 of jumper JP1 (tie EN to ON).

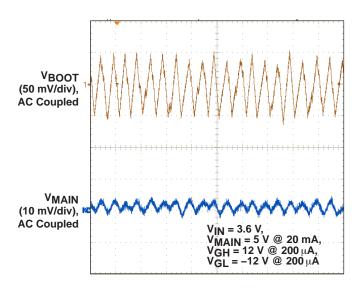
To enable the TPS65124EVM, first short pins 1–2 of jumper JP2 (tie RUN to ON); then short pins 1–2 of jumper JP1 (tie EN to ON) then short pins 1–2 of jumper JP5 and JP6 in any order to enable VGL and VGH, respectively. Connect output loads on each rail not to exceed the maximum current ratings in Table 1–1.

#### 2.3 Test Results



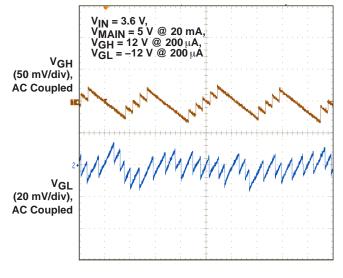






t – Time – 20 μs/div

Figure 2–3. VGH and VGL Output Ripple



t – Time – 20 μs/div

# **Board Layout**

The chapter describes the HPA076 PCB board layout and illustrations.

Topi	c	Page
3.1	Board Layout	3-1

#### 3.1 Board Layout

Board layout is critical for all switch mode power supplies. Figure 3–1, Figure 3–2, and Figure 3–3 show the board layout for the HPA076 PCB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry and special attention has been given to the routing of high-frequency current loops as well as ground.

Figure 3–1. Top Assembly Layer

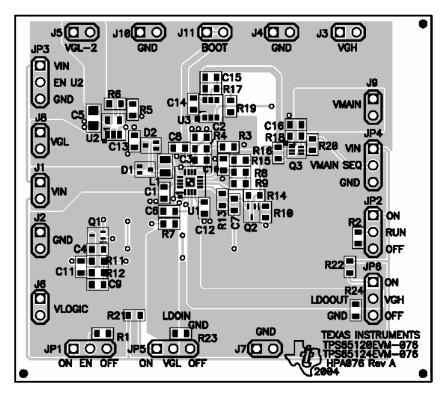


Figure 3–2. Top Layer Routing

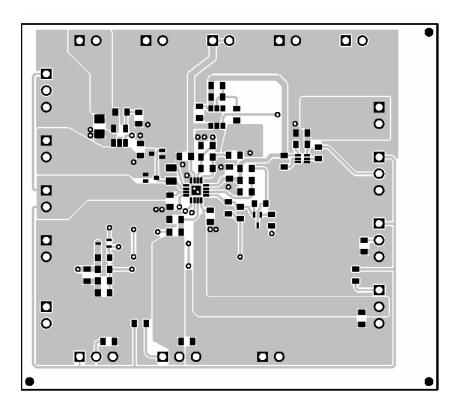
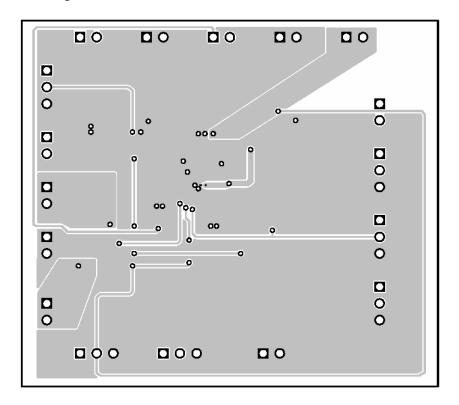


Figure 3–3. Bottom Layer Routing



# **Bill of Materials and Schematic**

This chapter provides the TPS65120EVM and TPS65124EVM bill of materials and schematic.

Topi	с Р	age
4.1	Bill of Materials	4-2
4.2	Schematics	4-3

#### 4.1 Bill of Materials

Table 4–1. HP	A076 Bill of	f Materials
---------------	--------------	-------------

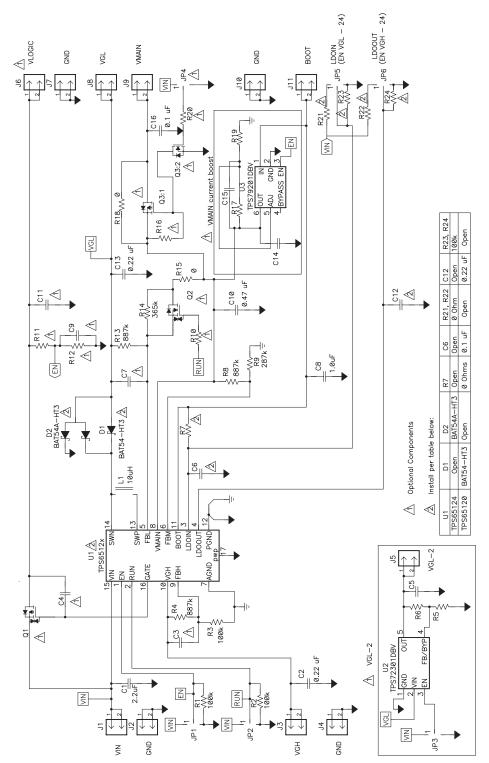
Count -001 -002						Part Number	
		RefDes	Description	Size	MFR		
1	1	C1	Capacitor, ceramic, 2.2–µF, 6.3–V, X5R, 10%	603	TDK	C1608X5R0J225KT	
1	1	C10	Capacitor, ceramic, 0.47–μF, 16–V, X5R, 10%	603	TDK	C1608X5R1C474KT	
1	1	C16	Capacitor, ceramic, 0.1–µF, 25–V, X7R, 10%	603	TDK	C1608X7R1E104KT	
1	0	C12	Capacitor, ceramic, 0.22–µF, 16–V, X5R, 10%	603	AVX	0603YD224KAT2A	
2	2	C2, C13	Capacitor, ceramic, 0.22–µF, 16–V, X5R, 10%	603	AVX	0603YD224KAT2A	
1	0	C6	Capacitor, ceramic, 0.1–µF, 25–V, X7R, 10%	603	TDK	C1608X7R1E104KT	
0	0	C3, C4, C7, C9, C11, C14, C15	Capacitor, ceramic, xxx–µF, vv–V	603			
0	0	C5	Capacitor, ceramic, xxx-µF, vv-V	805			
1	1	C8	Capacitor, ceramic, 1.0–µF, 16–V, X5R, 10%	603	TDK	C1608X5R1C105KT	
1	0	D1	Diode, Schottky, 200-mA, 30-V	LLP75–3B	Vishay	BAT54-HT3-GS08	
0	1	D2	Diode, Dual Schottky, 200-mA, 30-V	LLP75–3B	Vishay	BAT54A-HT3-GS08	
0	0	J5, J6	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 x 2			
9	9	J1–J4, J7–J11	Header, 2–pin, 100 mil spacing, (36–pin strip)	0.100 x 2	Sullins	PTC36SAAN	
0	0	JP3, JP4	Header, 3–pin, 100 mil spacing, (36–pin strip)	0.100 x 3			
4	4	JP1, JP2, JP5, JP6	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN	
1	1	L1	Inductor, 10–μH, 500–mΩ, 200–mA	805	Taiyo Yuden	CB2012T100M	
0	0	Q1	MOSFET, P-ch, -20V, -150 mA, 8 $\Omega$	SC89-3	Siliconix	Si1031X	
0	0	Q2	MOSFET, N–ch, 20V, 200 mA, 5 $\Omega$	SC89-3	Siliconix	Si1032X	
0	0	Q3	MOSFET, Dual Nch, 20V, 0.6A, 0.7 $\Omega,$ Pch, –20V, –0.4 A, 1.2 $\Omega$	SOT-563	Siliconix	Si1016X	
3	3	R1, R2, R3	Resistor, chip, 100 kΩ, 1/16–W, 1%	603	Std	Std	
0	2	R23, R24	Resistor, chip, 100 kΩ 1/16–W, 1%	603	Std	Std	
1	1	R14	Resistor, chip, 365 kΩ, 1/16–W, 1%	603	Std	Std	
3	3	R4, R8, R13	Resistor, chip, 887 kΩ, 1/16–W, 1%	603	Std	Std	
0	0	R5, R6, R10, R11, R12, R16, R17, R19, R20	Resistor, Chip, xx–Ω, 1/16–W	603			
1	0	R7	Resistor, Chip, 0–Ω, 1/16–W, 1%	603	Std	Std	
0	2	R21, R22	Resistor, Chip, 0–Ω, 1/16–W, 1%	603	Std	Std	
2	2	R15, R18	Resistor, Chip, 0–Ω, 1/16–W, 1%	603	Std	Std	
1	1	R9	Resistor, Chip, 287 kΩ, 1/16–W, 1%	603	Std	Std	

Count						
-001	-002	RefDes	Description	Size	MFR	Part Number
1		U1	IC, Single Inductor Quadruple–Output TFT LCD Power Supply	QFN16	TI	TPS65120QFN
	1		IC, Single Inductor Quadruple–Output TFT LCD Power Supply	QFN16	TI	TPS65124QFN
0	0	U2	IC, 100 mA Negative Output LDO Linear Regulators	SOT23-5	TI	TPS72301DBV
0	0	U3	IC, High PSRR, Low Noise LDO, Adj Output, 100–mA	SOT23-6	TI	TPS79201DBV
1	1		PCB, 2.5 ln x 2.2 ln x .062 ln		Any	HPA076
2	4		Shunt, 100–mil, Black	0.100	3M	929950-00

#### 4.2 Schematic

The HPA076 schematic (Figure 4–1) appears on the following page.

Figure 4–1. HPA076 Schematic



4-4