

# TPS23750 Flyback-Converter Evaluation Board – HPA108

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This user's guide describes the function and operation of the HPA108 evaluation module (EVM). A complete description, schematic, bill of materials, assembly drawing, and printed-circuit board artwork are included.

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## 1 Introduction

The HPA108 evaluation module implements an IEEE 802.3af-compliant class-3 power interface and a DC/DC switching converter using the Texas Instruments TPS23750 powered device (PD) controller in a typical power-over-Ethernet (PoE) configuration. The DC/DC converter provided on this EVM is a 3.3-V isolated design using a synchronous flyback topology; however, the BOM shows how to build 3.3-V or 5-V isolated and non-isolated variants. In addition, the EVM provides footprints for a simple diode and an associated snubber to implement a nonsynchronous flyback converter. A small prototype area is included on the printed-circuit board. The EVM accepts a TPS23770 in place of the TPS23750 to support a PD with a legacy undervoltage lockout (UVLO) threshold.

The EVM has separate LEDs that show when the DC/DC converter and the PoE interface are active. Test points are provided at all critical nodes. Power to the EVM is provided over the spare or data lines in an Ethernet cable or by an auxiliary source like a wall adapter.

## 2 Specification, Schematic, and Bill of Materials

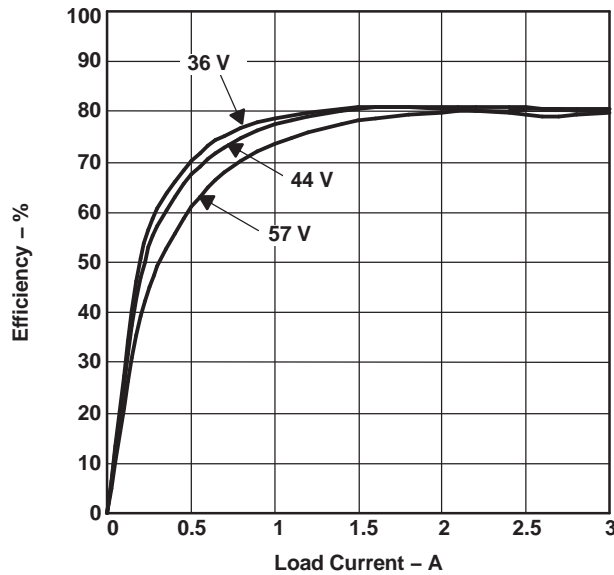
### 2.1 Electrical Specification

Table 1 shows the electrical specification over a  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  operating temperature range. Input voltages are measured at the RJ-45 connector unless otherwise noted.

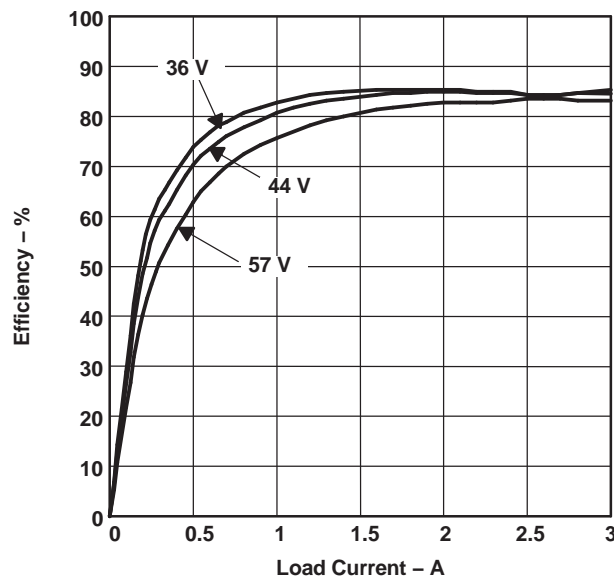
**Table 1. HPA108 Electrical Specification**

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT	
<b>POWER INTERFACE</b>						
Input voltage, $V_{IN}$	Applied to the power pins of connectors J2 or J4	0	–	57	V	
Operating voltage	After startup. Measured at RJ-45 connector J2	36	–	57	V	
	Measured at AUX PWR connector J4	36	–	57		
Input UVLO	Rising input voltage	–	–	42	V	
	Falling input voltage	30	–	–		
Detection voltage range		2.7	–	10.1	V	
Classification voltage range		14.5	–	20.5	V	
Classification current		26	–	30	mA	
Inrush current limit		100	–	180	mA	
Operating current limit		405	–	495	mA	
<b>DC/DC CONVERTER</b>						
Output voltage	$36\text{ V} \leq V_{IN} \leq 57\text{ V}$ , $I_{LOAD} \leq I_{LOAD}(\text{max})$	3.3-V output	3.13	3.3	3.47	V
		5-V output	4.75	5.0	5.25	
Output current, $I_{LOAD}$	$36\text{ V} \leq V_{IN} \leq 57\text{ V}$	3.3-V output	–	–	3	A
		5-V output	–	–	2	
Output ripple voltage, peak-to-peak	$V_{IN} = 44\text{ V}$ , $I_{LOAD} = 3\text{ A}$	3.3-V output	–	15	–	mV
	$V_{IN} = 44\text{ V}$ , $I_{LOAD} = 2\text{ A}$	5-V output	–	15	–	
Efficiency, end-to-end	$V_{IN} = 44\text{ V}$ , $I_{LOAD} = 3\text{ A}$	3.3-V output	–	80%	–	
	$V_{IN} = 44\text{ V}$ , $I_{LOAD} = 2\text{ A}$	5-V output	–	82%	–	
Switching frequency		82	–	118	kHz	

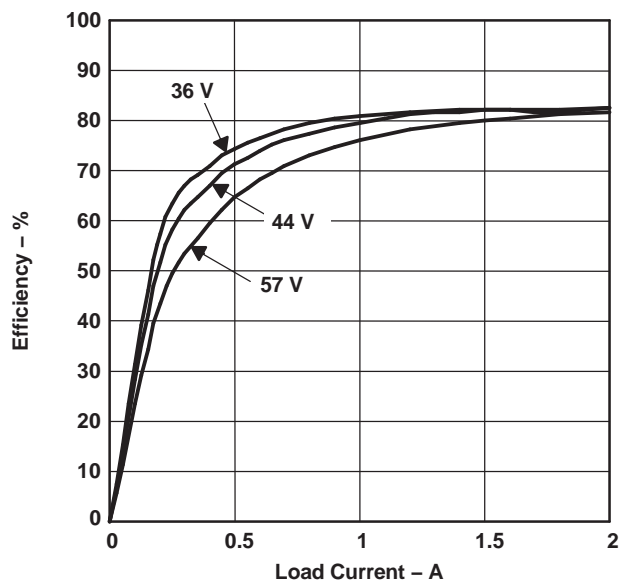
The end-to-end efficiency curves in [Figure 1](#) and [Figure 3](#) include the losses at the PD switch, bridge diode, and data transformer. The DC/DC converter efficiency curves in [Figure 2](#) and [Figure 4](#) exclude these losses. The curves are plotted for the RJ-45 connector voltages shown.



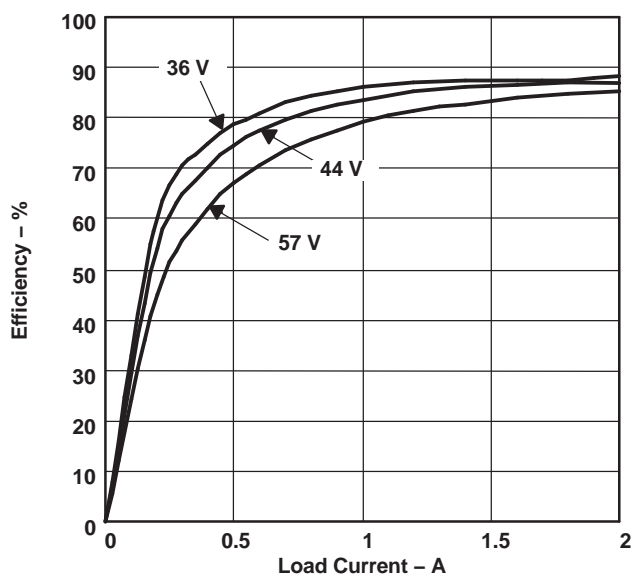
**Figure 1. Typical 3.3-V PD End-to-End Efficiency**



**Figure 2. Typical 3.3-V DC/DC Converter Efficiency**

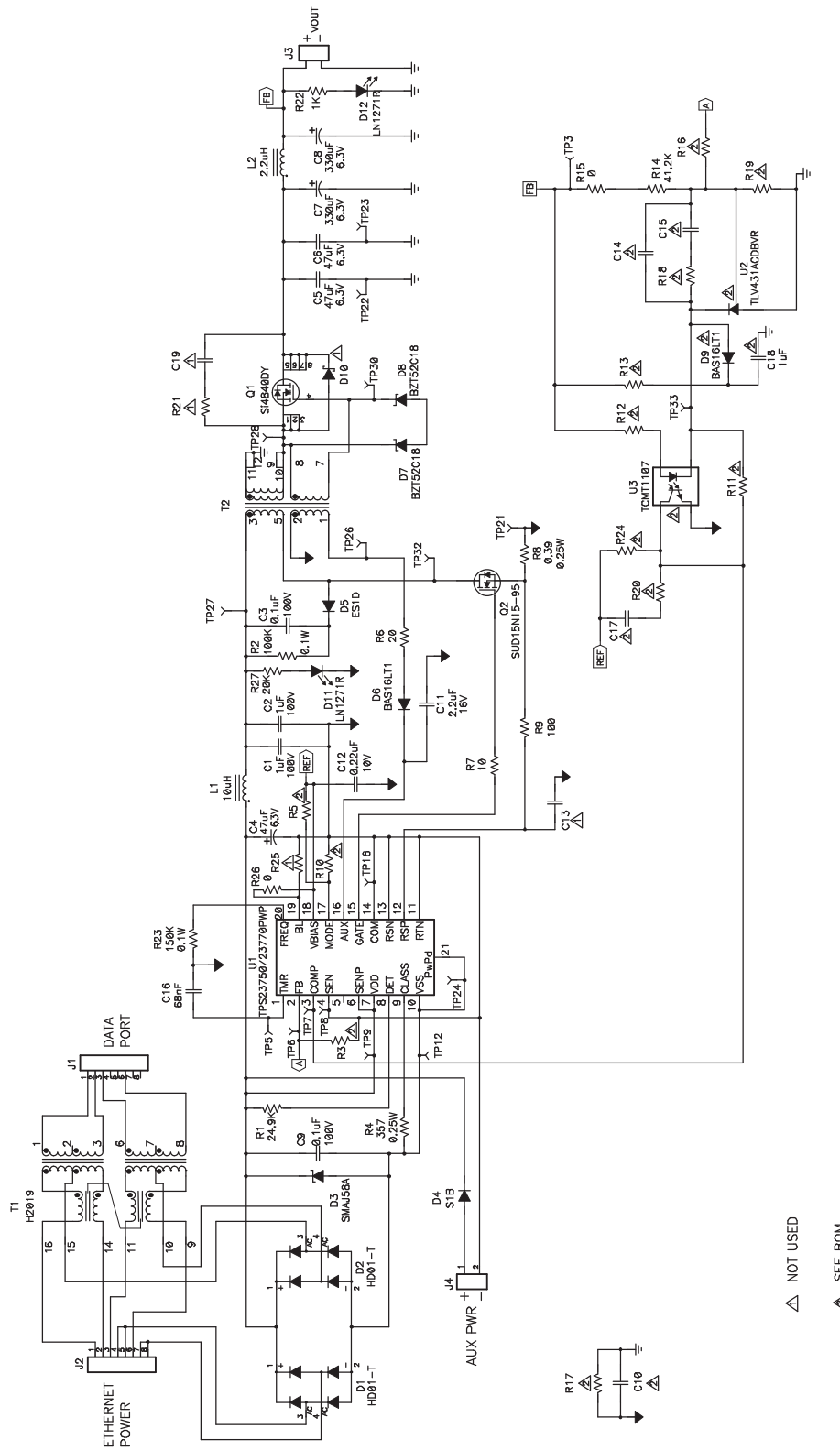


**Figure 3. Typical 5-V PD End-to-End Efficiency**



**Figure 4. Typical 5-V DC/DC Converter Efficiency**

## 2.2 Schematic



**2.3 Bill of Material**
**Table 2. HPA108 Bill of Material (Rev. A)**

Isolated		Non-Isolated		Ref Des	Description	Size	MFR	Part No.
3.3 V	5 V	3.3 V	5 V					
-001	-002	-003	-004					
Count	Count	Count	Count					
2	2	2	2	C1, C2	Capacitor, ceramic, 1 $\mu$ F, 100V, X7R, 10%	1210	Murata	GRM32ER72A105K A01L
1	1	0	0	C10	Capacitor, ceramic, 2200 pF, 2KV, X7R, 20%	1812	TDK	C4532X7R3D222KT
1	1	1	1	C11	Capacitor, ceramic, X7R, 2.2 $\mu$ F, 16-V, 10%	1206	Panasonic	ECJ-3YB1C225K
1	1	1	1	C12	Capacitor, ceramic, 0.22 $\mu$ F, 10-V, X7R	805	Std	Std
0	0	0	0	C13	Not Used	603		
1	1	0	0	C14	Capacitor, ceramic, 33 pF, 50V, C0G, 5%	603	Std	Std
0	0	1	1	C14	Capacitor, ceramic, 15 pF, 50V, C0G, 5%	603	Std	Std
1	1	0	0	C15	Capacitor, ceramic, 1000 pF, 50V, X7R, 10%	603	Std	Std
0	0	1	1	C15	Capacitor, ceramic, 680 pF, 50V, X7R, 10%	603	Std	Std
1	1	1	1	C16	Capacitor, ceramic, 68 nF, 16-V, X7R, 10%	603	Std	Std
1	1	0	0	C17	Capacitor, ceramic, 0.01 $\mu$ F, 25V, X7R, 10%	603	Std	Std
1	1	0	0	C18	Capacitor, ceramic, 1 $\mu$ F, 16V, X7R, 10%	805	Std	Std
0	0	0	0	C19	Not Used	805		
2	2	2	2	C3, C9	Capacitor, ceramic, 0.1 $\mu$ F, 100V, X7R, 10%	805	TDK	C2012X7R2A104K
1	1	1	1	C4	Capacitor, aluminum, 47 $\mu$ F, 63V, 20%	8x10mm	Panasonic	EEVFK1J470P
2	2	2	2	C5, C6	Capacitor, ceramic, 47 $\mu$ F, 6.3V, X5R, 20%	1210	TDK	C3225X5R0J476M
2	2	2	2	C7, C8	Capacitor, aluminum, SM, 330 $\mu$ F, 6.3V, 20%	8x6,2 mm	Panasonic	EEVFK0J331P
2	2	2	2	D1, D2	Bridge rectifier, 100 V, 0.8A, glass passivated, SMD	MINI DIP4	Diodes, Inc.	HD01-T
0	0	0	0	D10	Diode Schottky, 5-A, 40 V	SMC	On Semi	MBRS540T3
2	2	2	2	D11, D12	Diode, LED, red	0.114 x 0.049	Panasonic	LN1271R
1	1	1	1	D3	Diode, TVS, 58V, 1W	SMA	Diodes Inc., STMicro	SMAJ58A
1	1	1	1	D4	Diode, rectifier, 1A, 100 V	SMA	Diodes, Inc.	S1B
1	1	1	1	D5	Diode, rectifier, 1A, 200 V	SMA	On Semi	ES1D
1	1	1	1	D6	Diode, switching, 200-mA, 75V, 225 mW	SOT-23	On Semi	BAS16LT1
1	1	0	0	D9	Diode, switching, 200-mA, 75 V, 225 mW	SOT-23	On Semi	BAS16LT1
2	2	2	2	D7, D8	Diode, Zener, 200 mW, 18V	SOD-323	General Semiconductor	BZT52C18
2	2	2	2	J1, J2	Connector, Jack, Modular, 8 POS	0.705 x 0.820	AMP	520252
2	2	2	2	J3, J4	Terminal block, 2-pin, 6-A, 3,5 mm	0.27 x 0.25 in	OST	ED1514
1	1	1	1	L1	Inductor, SMT, 10 $\mu$ H, 1.1A, 160 m $\Omega$	4.45x6.6mm	Coilcraft	DO1608C-103
1	1	1	1	L2	Inductor, SMT, 2.2 $\mu$ H, 6.1A, 15 m $\Omega$	9.4x12.95 mm	Coilcraft	DO3316P-222HCB
1	1	1	1	Q1	MOSFET, N-ch, 40V, 14A, 9 m $\Omega$ , T <sub>J</sub> = 25°C	SO-8	Vishay	Si4840DY
1	1	1	1	Q2	MOSFET, N-ch, 150V, 15A, 95 m $\Omega$ , T <sub>J</sub> = 25°C	DPAK	Vishay or International Rectifier	SUD15N15-95 or iRF24N15D or iRF13N15D
1	1	1	1	R1	Resistor, chip, 24.9 k $\Omega$ , 1/16W, 1%	603	Std	Std
1	0	0	0	R12	Resistor, chip, 549 $\Omega$ , 1/16W, 1%	603	Std	Std
0	1	0	0	R12	Resistor, chip, 1.00 k $\Omega$ 1/16W, 1%	603	Std	Std
1	0	0	0	R13	Resistor, chip, 3.01 k $\Omega$ , 1/16W, 1%	603	Std	Std
0	1	0	0	R13	Resistor, chip, 1.5 k $\Omega$ , 1/16W, 1%	603	Std	Std
1	1	1	1	R14	Resistor, chip, 41.2 k $\Omega$ , 1/16W, 1%	603	Std	Std
1	0	0	0	R18	Resistor, chip, 41.2 k $\Omega$ s, 1/16W, 1%	603	Std	Std

**Table 2. HPA108 Bill of Material (Rev. A) (continued)**

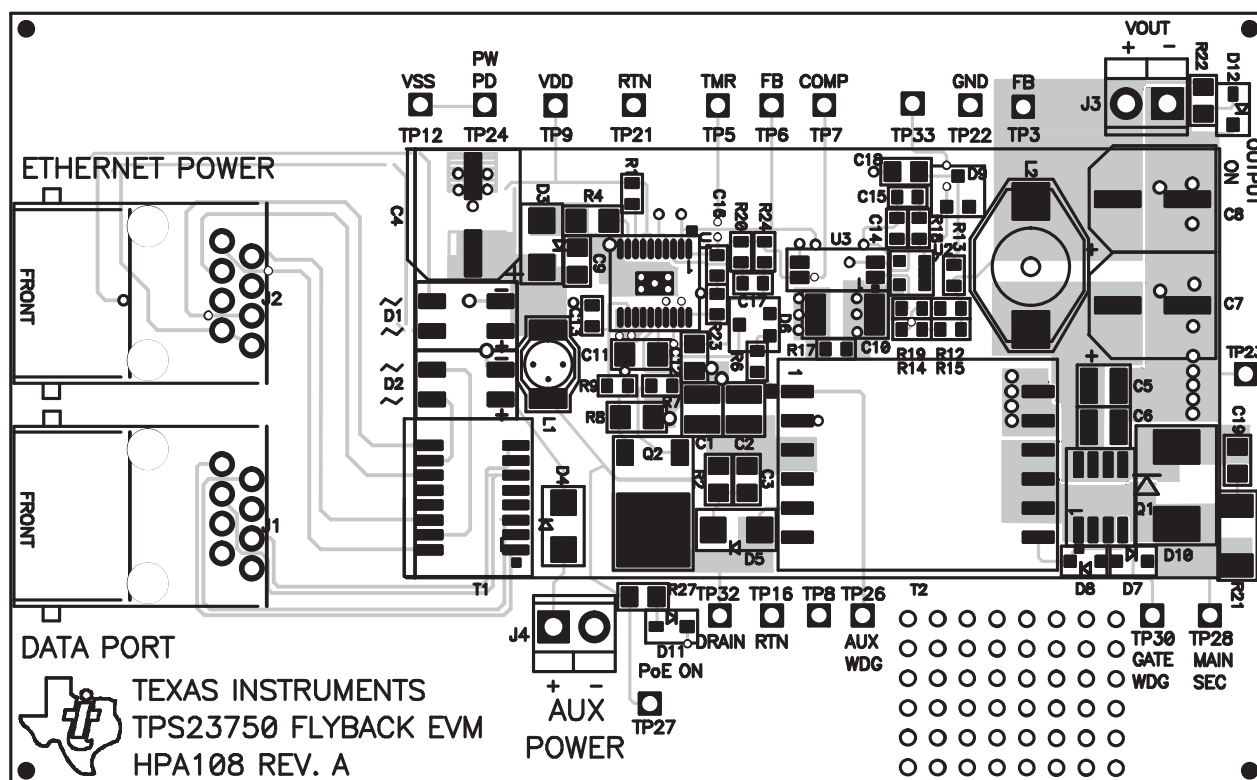
Isolated		Non-Isolated		Ref Des	Description	Size	MFR	Part No.
3.3 V	5 V	3.3 V	5 V					
-001	-002	-003	-004					
Count	Count	Count	Count					
0	1	0	0	R18	Resistor, chip, 86.6K k $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	1	1	R18	Resistor, chip, 200 k $\Omega$ , 1/16W, 1%	603	Std	Std
1	0	0	0	R19	Resistor, chip, 24.3 k $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	1	0	R19	Resistor, chip, 34.8 k $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	0	1	R19	Resistor, chip, 17.4 k $\Omega$ , 1/16W, 1%	603	Std	Std
0	1	0	0	R19	Resistor, chip, 13.3 k $\Omega$ , 1/16W, 1%	603	Std	Std
1	1	1	1	R2	Resistor, chip, 100 k $\Omega$ , 1/10W, 1%	805	Std	Std
1	0	0	0	R20	Resistor, chip, 249 $\Omega$ , 1/16W, 1%	603	Std	Std
0	1	0	0	R20	Resistor, chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	0	0	R25	Not Used	603		
0	0	0	0	R21	Not Used			
1	1	1	1	R23	Resistor, chip, 150 k $\Omega$ , 0.1-W, 1%	603	Std	Std
1	1	0	0	R24	Resistor, chip, 2 k $\Omega$ , 1/16W, 1%	603	Std	Std
1	1	1	1	R27	Resistor, chip, 20 k $\Omega$ , 1/10-W, 5%	805	Std	Std
1	1	1	1	R22	Resistor, Chip, 1 k $\Omega$ , 1/10-W, 5%	805	Std	Std
1	1	0	0	R3	Resistor, chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
1	1	1	1	R4	Resistor, chip, 357 $\Omega$ , 1/4W, 1%	1206	Std	Std
1	1	0	0	R5	Resistor, chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
1	1	1	1	R6	Resistor, chip, 20 $\Omega$ , 1/16W, 5%	603	Std	Std
1	1	1	1	R7	Resistor, chip, 10 $\Omega$ , 1/16W, 5%	603	Std	Std
1	1	1	1	R8	Resistor, Chip, 0.39 $\Omega$ , .25W, 1%	1206	Panasonic	ERJ8RQFR39V
1	1	1	1	R9	Resistor, Chip, 100 $\Omega$ , 1/16W, 1%	603	Std	Std
2	2	2	2	R15, R26	Resistor, Chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	1	1	R17	Resistor, Chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	1	1	R10	Resistor, Chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	1	1	R11	Resistor, Chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
0	0	1	1	R16	Resistor, Chip, 0 $\Omega$ , 1/16W, 1%	603	Std	Std
1	1	1	1	T1	Xfmr, center-tapped, Voice Over IP	0.500 x 0.370	Pulse	H2019
0	1	0	1	T2	XFMR, flyback 2 Pri, 2 Sec, Custom	0.875 x 0.675	Coilcraft Pulse (ALT)	C1174-AL PA1039
1	0	1	0	T2	XFMR, flyback 2 Pri, 2 Sec, Custom	0.875 x 0.675	Coilcraft Pulse (ALT)	C1173-AL PA0691
6	6	6	6	TP12, TP16, TP21, TP22, TP23, TP24	Test Point, Black	0.038	Keystone	5001
12	12	12	12	TP3, TP5, TP6, TP7, TP8, TP9, TP26, TP27, TP28, TP30, TP32, TP33	Test Point, Red	0.038	Keystone	5000

Table 2. HPA108 Bill of Material (Rev. A) (continued)

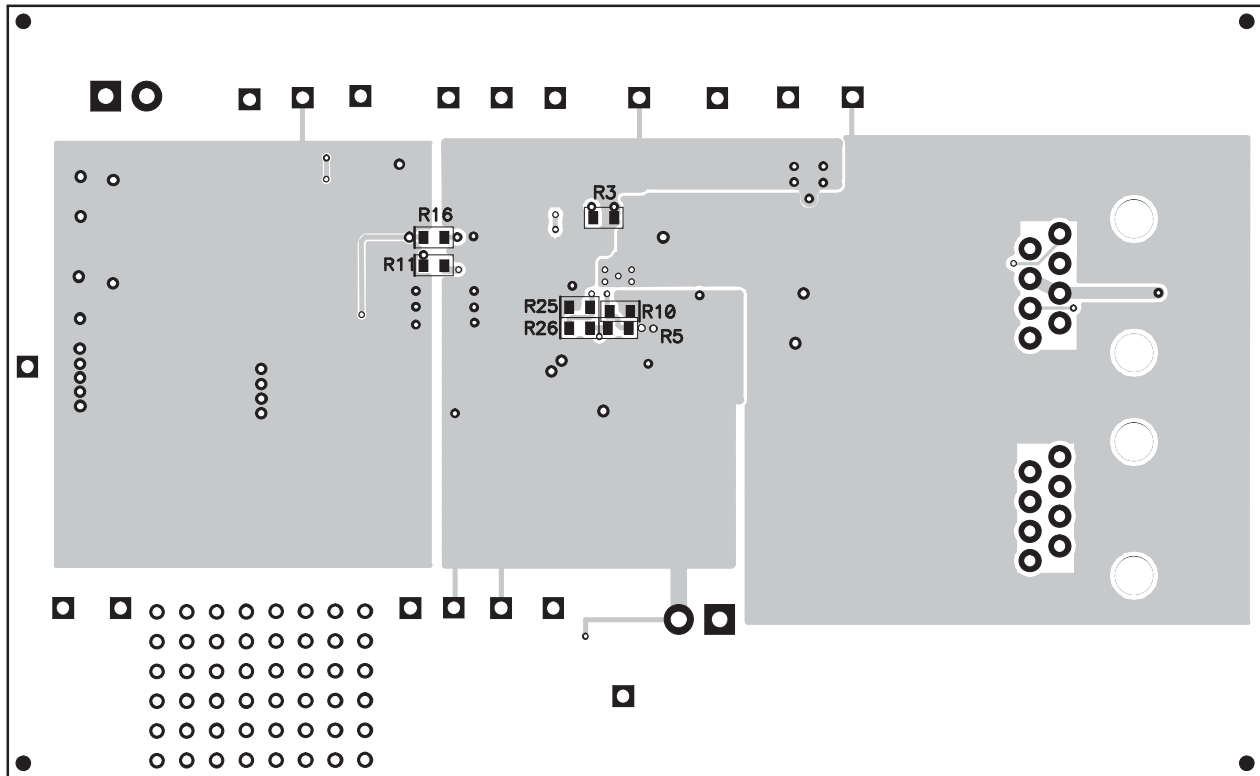
Isolated		Non-Isolated		Ref Des	Description	Size	MFR	Part No.
3.3 V	5 V	3.3 V	5 V					
-001	-002	-003	-004					
Count	Count	Count	Count					
1	1	1	1	U1	IC, IEEE 802.3af Integrated Primary Side Controller	PWP20	TI	TPS23750PWP
1	1	0	0	U2	IC, Shunt Regulator, 1.24 V Ref, 6V, 10 mA, 1%	SOT23-5	TI	TLV431ACDBVR
1	1	0	0	U3	IC, Photocoupler, 3750VRMS, 80–160% CTR	MF4	Vishay	TCMT1107
4	4	4	4	–	Rubber bumper	–	Spec Tech	2566
1	1	1	1	–	PCB, 0 In x 0 In x 0.062 In	–	Any	HPA108

### 3 Board Layout

#### 3.1 Top-Side Layout



### 3.2 Bottom-Side Layout



### 3.3 Layout Considerations

The layout of the PoE front end must use good practice for power and EMI/ESD. A basic set of recommendations include:

- The parts placement must be driven by the power flow in a point-to-point manner such as RJ-45 → Ethernet transformer → diode bridges → TVS and 0.1- $\mu$ F capacitor → TPS23750 → bulk capacitor → converter input.
- All leads should be as short as possible with wide power traces and paired signal and return.
- There should not be any crossovers of signals from one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS23750 should be located over split, local ground planes referenced to  $V_{SS}$  for the PoE input and to RTN for the converter operation. Whereas the PoE side may operate without a ground plane, the converter side must have one. The PowerPad™ must be tied to the  $V_{SS}$  plane or fill area, especially if power dissipation is a concern. Logic ground and power layers should not be present under the Ethernet input or the converter primary side.

- Large copper fills and *traces* should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.

Converter layout benefits from basic rules such as:

1. Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses which include the power semiconductors and magnetics.
2. Reduce the length of all the traces in step 1.
3. Where possible, use vertical pairing.
4. Use the *ground plane* for the switching currents carefully.
5. Keep the high-current and high-voltage switching away from low-level sensing circuits including those outside the power supply.
6. The current sensing on RSP/RSN is the most critical, noise-sensitive signal. It must be protected as in

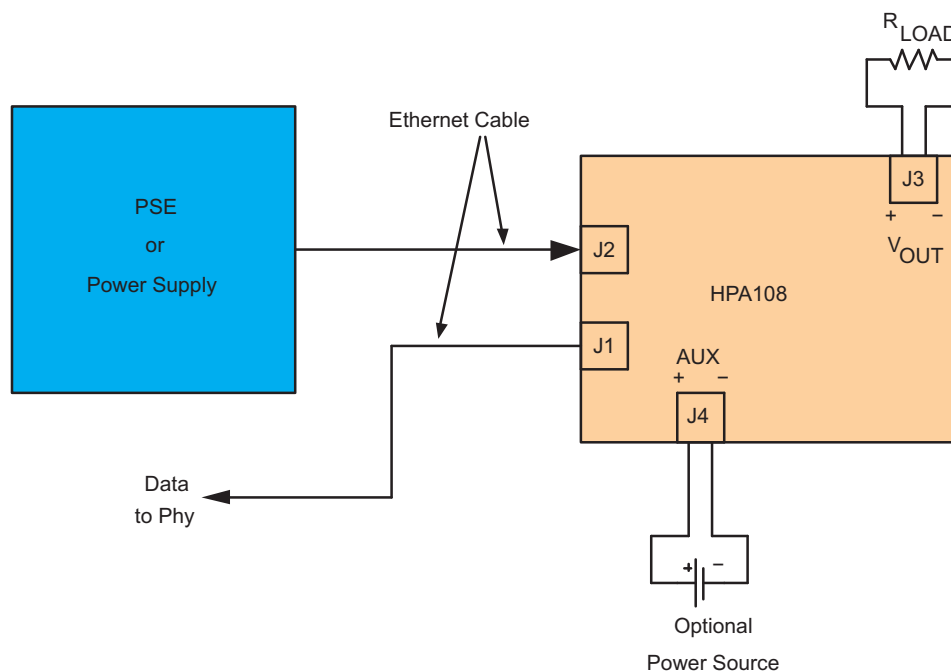
step 5, including exposure to the gate drive sign.

7. Pay special attention to spacing around the high-voltage sections of the converter.

## 4 Using the EVM

### 4.1 Setup

Figure 5 shows a typical EVM setup. The user is encouraged to read the TPS23750 data sheet before using the EVM.



**Figure 5. Typical Setup**

### 4.2 Interface

Table 3 describes the EVM interface.

**Table 3. EVM I/O Interfaces**

Reference Designator	Description
J2	An Ethernet cable connects this port to the power-sourcing equipment (PSE). This port carries both data and power.
J1	This port carries only data. Do not apply power to this port.
J4	This terminal block accepts auxiliary power from a source like a wall adapter.
J3	Output voltage
D12	This LED is lit if the DC/DC converter output is on.
D11	This LED is lit if the PD FET switch is on.

### **4.3 Making Measurements**

Stray magnetic fields from transformer T2 can couple noise into measurements. This noise may be noticeable when measuring a low-level signal like output ripple voltage. Keep the ground lead of the oscilloscope probe short and away from T2 to reduce the amount of noise pick-up.

Ground loops can be created if test equipment is connected to the EVM. Avoid ground loops by floating the test equipment and/or the power supply to the EVM.

### **4.4 EVM Operation**

The TPS23750 data sheet describes the electrical operation and function of the various components in the isolated flyback PD. The circuit provided in the data sheet is similar to the circuit in this EVM.

## **5 Related Documentation**

1. *TPS23750, TPS23770, Integrated 100 V IEEE 802.3af PD and DC/DC Controller* data sheet, [SLVS590](#)
2. *IEEE Std 802.3af*

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### EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 57 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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