

# **TPS2041B/51B EVM Power-Distribution Switch**

This User's Guide describes the characteristics, operation, and use of TPS2041B/51B evaluation modules (EVM) featuring the Texas Instruments TPS2041/51B in the SOT-23 package.

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#### 1 Introduction

These EVMs provide a means for the user to evaluate quickly the functionality and electrical performance of the TPS2041B/51B. All inputs and outputs are brought out to test points for control and monitoring. All passive components are included on the EVM for device operation. The input pin should be connected to an external supply; the output should be connected to a load. The device can be enabled/disabled through the enable pin. Faults can be monitored by observing the OC\_ pin.

## 1.1 Related Documentation From Texas Instruments

TPS204xB/TPS205xB Current-Limited, Power-Distribution Switches data sheet (SLVS514)

# 2 Setup

# 2.1 Input/Output Connector Descriptions

This chapter describes each test point and how to properly connect, set up, and use the TPS2041B/51B EVM.

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#### Setup

#### 2.1.1 TP1 – Output Power

This is the output of the DC/DC power supply. Connect a load between the two terminals of this test point with reference to one of the ground points.

## 2.1.2 TP2, TP7, TP8, TP9 – Ground

Any of these test points can be used as references to the input, output, and oscilloscope probes.

### 2.1.3 TP3 – Overcurrent

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent logic output low.

## 2.1.4 TP4 – Input Power

Apply the input voltage here. Recommended range is 2.7 V to 5.5 V. Note that 6 V is the absolute maximum and -0.3 V is the absolute minimum, so it is extremely important not to exceed these limits.

## 2.1.5 **TP5** – Enable

The enable input is active-low for the TPS2041B and active-high for the TPS2051B. To turn the TPS2041B on, this point must be tied to a low potential. To turn the TPS2051B on, this point must be tied to a high potential. The negative terminal (active-low) and the positive terminal (active-high) of the power supply are recommended points.

## 2.2 Electrical Specifications

	Parameters	Test Conditions	Min	Тур	Max	Unit
Vin	Input voltage		2.7		5.5	V
I <sub>o(out)</sub>	Continuous output current		0		500	mA
	Rdson	$V_{I(IN)}$ = 5 V or 3.3 V, $I_O$ = 0.5 A, -40°C ≤ T <sub>J</sub> ≤ 125°C		95	140	mΩ

## 2.3 Test Results

The figures in this section come from testing the TPS2041B EVM, which has an active-low enable.

## 2.3.1 Apply Power to EVM While Disabled

Figure 1 shows the input (Ch. 1, 5 V/div), output (Ch. 2, 5 V/div), overcurrent (Ch. 3, 5 V/div), and the enable input (Ch. 4, 5 V/div). Because enable is in a logic-high state, 0 volts is observed at the output.

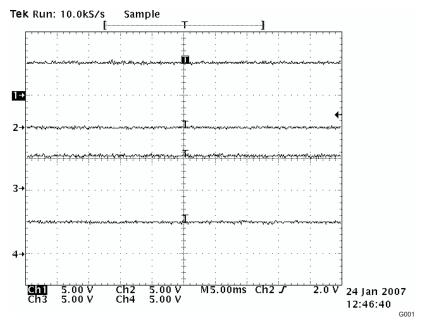


Figure 1. Disabled Device at Power Up

#### 2.3.2 EVM Is Enabled

Figure 2 shows the enable input toggled from a logic-high (Ch. 4) to a logic-low state. When this occurs, the output shoots up to 5 V (Ch. 2).

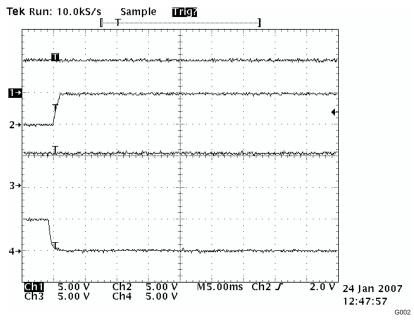


Figure 2. Enabling the Device



Board Layout

Figure 3 shows the overcurrent signal (Ch. 3) pulling low due to a short circuit on the output. The device switches into a constant-current mode and shuts off the switch, so 0 V is seen on the output (Ch 2).

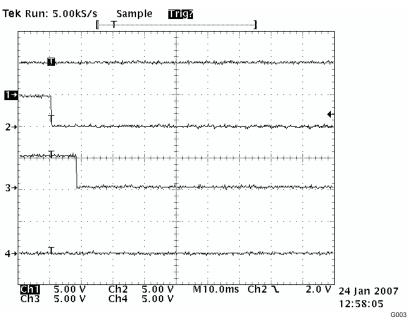


Figure 3. Overcurrent Mode

## 3 Board Layout

This chapter provides the TPS2041B EVM and TPS2051B EVM board layouts and illustrations.

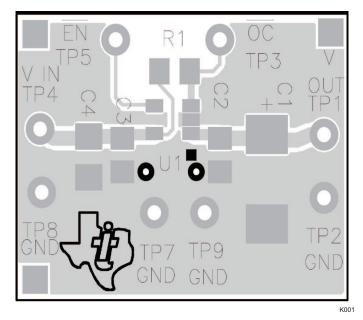


Figure 4. Top-Side Layout of TPS2041B EVM



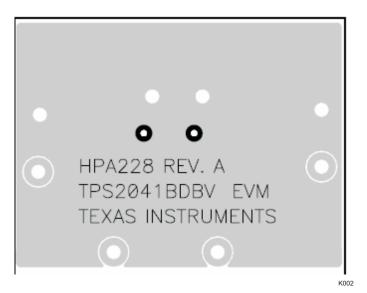
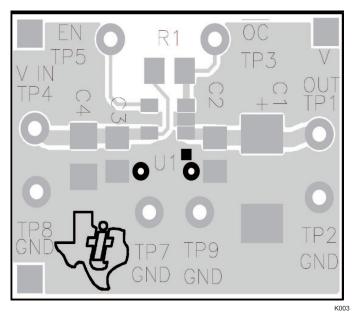
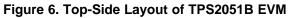


Figure 5. Bottom-Side Layout of TPS2041B EVM







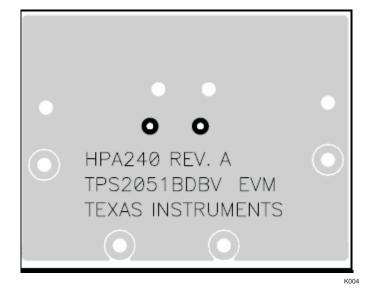


Figure 7. Bottom-Side Layout of TPS2051B EVM

# 3.1 Layout Considerations

- 1. All leads should be as short as possible with wide traces.
- 2. Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses; these include paths to power semiconductors and magnetics.
- 3. Reduce the length of all the traces in described step 2.
- 4. Where possible, use vertical pairing.

## 4 Bill of Materials and Schematics

This chapter provides the Bill of Materials and Schematics for the TPS2041B/51B EVMs.

## 4.1 Bill of Materials

## 4.1.1 TPS2041B EVM BOM

Table 1 is the Bill of Materials for the TPS2041B EVM.

RefDes	Count	Size	Mfr	Part Number	Description	
C1	1	SMD	STD	STD	Capacitor, tantalum, 150-μF, 10-V, 100-mΩ, 20%	
C2, C3	2	0805	STD	STD Capacitor, ceramic, 0.1-µF, 10-V, 20%		
C4	1	1206	STD	STD	Capacitor, ceramic, 10-μF, 10-V, 20%	
R1	1	0805	STD	STD	Resistor, chip, 10-kΩ, 1/10W, 5%	
TP1, TP3, TP4, TP5	4	ТН	Keystone	5000	Test point, red, thru hole, color keyed	
TP2, TP7, TP8, TP9	4	ТН	Keystone	5001	Test point, black, thru hole, color keyed	
U1	1	SOT-23-5	TI	TPS2041BDBV	IC, 80-m $\Omega$ , 500-mA power-distribution single switch	
_	1		Any	HPA228	PCB, 1 in. × 0.8 in. x 0.062 in. (2,54 cm × 2,03 cm × 1,58 mm)	

#### Table 1. TPS2041B EVM BOM

NOTES: 1. These assemblies are ESD sensitive; ESD precautions must be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

## 4.1.2 TPS2051B EVM BOM

Table 2 is the Bill of Materials for the TPS2051B EVM.

RefDes	Count	Size	Mfr	Part Number	Description	
C1	1	SMD	STD	STD	Capacitor, tantalum, 150- $\mu$ F, 10-V, 100-m $\Omega$ , 20%	
C2, C3	2	0805	STD	STD	Capacitor, ceramic, 0.1-µF, 10-V, 20%	
C4	1	1206	STD	STD	Capacitor, ceramic, 10-µF, 10-V, 20%	
R1	1	0805	STD	STD	Resistor, chip, 10-k $\Omega$ , 1/10W, 5%	
TP1, TP3, TP4, TP5	4	TH	Keystone	5000	Test point, red, thru hole, color keyed	
TP2, TP7, TP8, TP9	4	ТН	Keystone	5001	Test point, black, thru hole, color keyed	
U1	1	SOT-23-5	TI	TPS2051BDBV	IC, 80-m $\Omega$ , 500-mA power-distribution single switch	
_	1		Any	HPA240	PCB, 1 in. $\times$ 0.8 in. x 0.062 in. (2,54 cm $\times$ 2,03 cm $\times$ 1,58 mm)	

#### Table 2. TPS2051B EVM BOM

NOTES: 1. These assemblies are ESD sensitive; ESD precautions must be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

# 4.2 Schematics

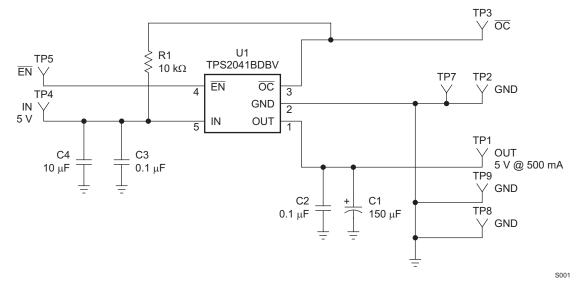
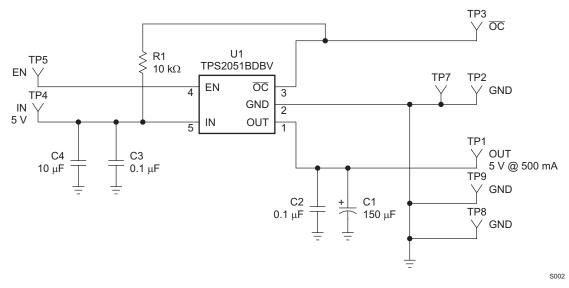


Figure 8. TPS2041B EVM Schematic







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#### **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the input voltage range of -0.3 V to 6.0 V, and the output voltage range of -0.3 V to 6.0 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above -40°C as long as the input and output ranges are maintained. These components include but are not limited to, switching transistors, inductor, and IC. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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