WHITE PAPER

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Enabling small cells
with TI's new multicore SoC

Introduction

The new system-on-chip (SoC) architecture from Texas Instruments (TI) provides a powerful and innovative platform for reducing existing wireless base station product costs and developing new cutting-edge base station technology. Mobile data use is driving the cellular industry to new innovations, which will include a revolutionary change to network topologies. The macro-dominated networks of today will give way to more heterogeneous deployments using layered cells, with small sites residing in and around larger cell sites. This includes both indoor and outdoor networks of different radii and power levels, all working seamlessly together to provide high-speed data and voice services.

TI's recently announced multicore SoC architecture now includes additional functionality both on the higher layer application side as well as the analog radio front end.

The use of smart phones and other mobile data devices are driving an unprecedented increase in the volume and nature of wireless network traffic. The high data rates and bandwidths required to support these applications are a challenge in today's networks. As a result, networks are beginning to change. The most significant change is the addition of small cells and the deployment of a wider variety of base stations.

This paper will explore a number of key features in small cell systems and how TI's new architecture efficiently enables these features.

Small cell overview

Typically referred to as femtocells or picocells, small cell solutions share a number of key distinguishing features that set them apart from traditional macrocell architectures. Although they may be either indoor or outdoor, typically they:

- Support a single sector with a cell radius < 500m.
- Are single-box solutions (digital, analog and RF all co-located).
- Use wireline backhaul (although some outdoor picocells will use wireless backhaul).

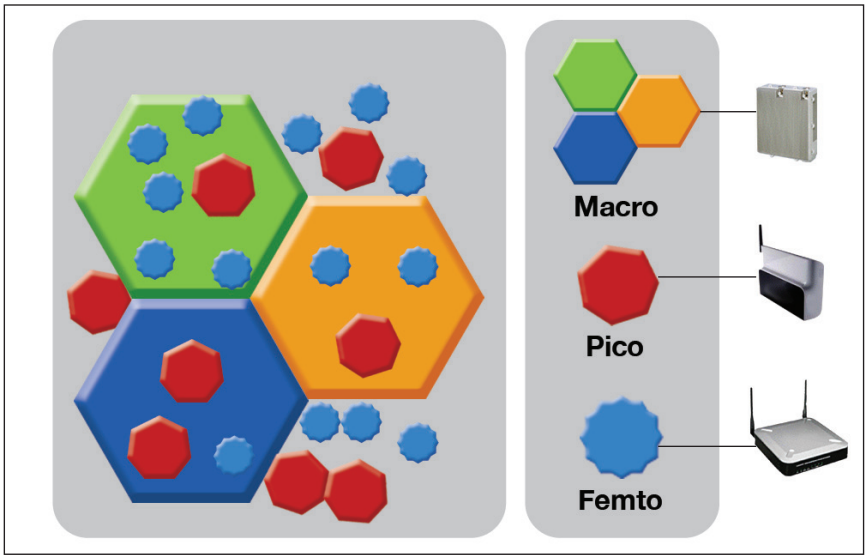
Deploying small cells into a macrocell network introduces challenging interference and handover issues at the edges of the small cell, creating cell-edge conflicts with macrocells.

The dramatic increase of mobile data access is the driving factor behind this change. Although the advent of Long Term Evolution (LTE) will help increase network capacity, there is not enough improvement to keep up with the growth of data usage. The way forward is to reduce the cell radius and increase the number of cells proportionally. This creates an exponential rather than linear growth in network capacity, but reducing the cell radius by two requires an increase of 2^2 cell sites.

Thus, to bring this to fruition, a number of things need to occur:

- Base station cost must decrease.
- Physical size and power consumption must decrease.
- Installation cost must decrease.
- Interference for the overlapping cells must be mitigated.

TI's new SoC architecture addresses all of these critical issues and allows OEMs to develop cost effective and robust small-cell solutions for these new network topologies (Figure 1).



▲ ***Figure 1.*** *Impact of small cells on network architecture*

The first and most obvious impact of the move toward smaller cells is the need for cost reduction. In short, base stations must become less expensive to acquire, maintain and install.

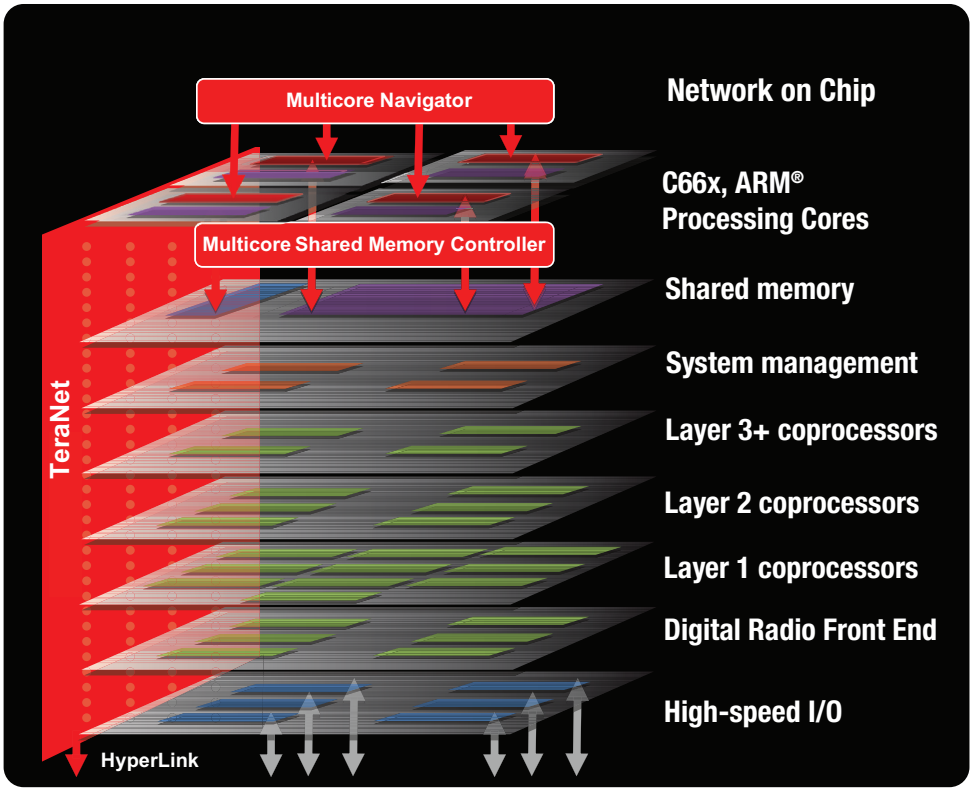
Integration is the key to product cost reduction for the digital processing elements. Typically, a base station processing card will contain three basic elements: a general-purpose processor (GPP), a digital signal processor (DSP), and digital radio front-end logic (typically in a dedicated chip or field programmable gate array) to prepare the signal to be sent to the analog front end. TI's new SoC architecture is built on an architecture that allows the integration of an ARM processing core and digital radio front-end logic with its market-leading DSP.

The ARM core integration portion of the architecture leverages design experience from TI's DaVinci™ processor family. The digital radio front-end's digital radio logic draws from custom IP developed in TI's High Performance Analog (HPA) group. The breadth of TI's experience allows TI SoC designers to bridge the traditional learning curve encountered when building new systems and produce an optimized solution based on field-proven technology quickly and efficiently.

To reduce the installation cost as well as eliminate interference issues, the wireless industry is focused on developing self-optimizing network solutions. Base stations will monitor, detect and communicate with neighboring cells to automatically set up handover conditions and adjust their power and other parameters. The goal is to minimize the impact of interference on adjacent cells. To support this new functionality, programmable and flexible solutions are required. TI's SoC architecture offloads standard, defined processing functions to coprocessors, freeing the programmable ARM and DSP cores for functional enhancements. The result is a fully programmable architecture, enabling solutions that can be easily updated with new algorithms to address emerging requirements as these new networks are deployed.

Wireless operators need to support many standards concurrently as users slowly migrate from one technology to the next. Therefore, it is important that small cell solutions support multiple standards while providing an upgrade path to more advanced technologies. TI's SoC architecture supports all wireless standards for all classes of base station: macrocell, microcell, picocell and femtocell.

Combining these elements into a single SoC stresses many aspects of system design. TI's SoC architecture incorporates the key elements required to cost-effectively meet the needs of all cellular base station types. Figure 2 illustrates the layered design approach TI took in developing its new SoC architecture. Notice that the architecture layering reflects the processing layers present in a small cell.



▲ ***Figure 2.*** *TI's multicore SoC architecture.*

Processing power

TI's new architecture features DSP technology with clock speeds up to 1.2 GHz and total processing capability of up to 256 GMACs – almost a full order of magnitude higher than any currently available or announced DSP from other vendors. In addition, the core supports fixed- and floating-point operations, all with an instruction set that is 100 percent backward-compatible with TI's award-winning C64x+™ DSP instruction set. The unification of fixed- and floating-point operations at processing speeds in excess of 1 GHz represents a significant paradigm shift in the DSP realm. Developers need no longer choose between the raw speed of fixed point and the precision of floating point. For the first time, they will have the best of both worlds, as TI's new architecture supports moving freely and easily between fixed- and floating-point instructions.

The introduction of native floating point running at the industry's highest DSP speeds is a major technological breakthrough. Traditionally, floating-point processors have run much slower than fixed-point processors. As a consequence, they are rarely used in the high-performance arena of cellular base stations – despite the efficiency that floating-point programming would bring to base station development. By combining native floating-point support with the industry-leading fixed-point architecture of the C64x+ DSP, TI has brought the best of both worlds' processing power to bear on cellular systems. Programmers can use optimized 16-bit

code where precision is not a factor and IEEE floating-point precision with algorithms requiring high precision, such as MIMO equalizers. This results in incredibly efficient wireless system architectures with the lowest power consumption, highest performance, and greatest throughput for the base station.

TI's floating-point capability enables the efficient implementation of multiantenna signal processing used in the latest cellular standards such as MIMO and beamforming. The algorithm for these advanced antenna techniques can be compared to a classic N-variables-with-N-unknowns problem, which requires matrix inversion methods to solve. The introduction of matrix inversion to the processing chain has a profound impact on the performance of fixed-point processors. This is because matrix inversions are very susceptible to precision limits, causing 16- and even 32-bit fixed-point operations to either suffer in performance or simply not work well. Programmers are generally forced to use pseudo-floating-point methods to achieve the required precision while trying to retain enough processing horsepower to run the system.

An added benefit of floating-point algorithm design is the ease with which algorithms can be developed, upgraded and ported to real-world systems. A typical design flow for a communications system is to first develop algorithms based on computer models and use these for initial system deployments. These new algorithms are often developed using MATLAB implementations, which are inherently floating point. The challenge then lies in translating these floating-point MATLAB algorithms to fixed-point DSPs while retaining the performance of both the algorithm and of the system, as unwieldy algorithms can use a disproportionate amount of system resources and lower the overall performance of the base station.

It is not uncommon for the process of porting code from MATLAB to a real system to take weeks or months when complicated matrix processing is involved. But with native floating-point support on TI's new architecture, this entire step is removed. Code is easily ported from MATLAB by using floating-point C code and compiling directly onto TI's DSP.

As the deployments grow in scope and usage, engineers gather real-world data and bring it back to the algorithm teams to improve system performance, so the process starts anew. It is difficult to overstate how important this will be to system designers and wireless infrastructure system programmers. Floating point is likely to become even more important in the future, as the trend to multi-antenna signal processing is only going to grow in complexity as LTE evolves into LTE-A and future standards.

Multicore Navigator

One of the biggest issues facing base station OEMs today is developing software for the base station. Software development for macro systems can run into hundreds of developer-years of effort. TI's new architecture leverages experience from previous generations of multicore and base station system development to produce an SoC as simple to use as it is powerful.

A fundamental element of TI's new architecture is the new Multicore Navigator. Multicore Navigator is a system element that enables seamless data movement throughout the SoC.

Once configured, Multicore Navigator handles packet transfers, memory allocation, accelerator triggering and multiple destinations, all without consuming a single cycle of any DSP or ARM core. This

frees the core resources for algorithmic system-level processing without getting bogged down in the details of data movement. Alternate devices typically involve multiple interrupts and context switches, ultimately reducing system performance. As an example, in a TI-based LTE system, mobile data packets arrive on the antenna interface (a dedicated high-speed interface that supports the OBSAI and CPRI standards); get queued and routed to the fast Fourier transform coprocessor (the first step in LTE layer 1 processing) for processing; and then get queued and routed to the appropriate DSP core for the next processing step – all without any core intervention. Similarly, data can arrive from multiple antennas and multiple sectors at the same time and all be routed appropriately and automatically. This means that data can flow between system elements without core intervention and without concern of contention between different cores.

TI's Multicore Navigator evolved from earlier system design elements and draws from a deep understanding of critical base station elements. Multicore Navigator is extremely efficient for packetized data flow and highly optimized for the packet-based processing in both high-speed 3G systems like HSPA+ and 4G systems like LTE and WiMAX. It also provides a hardware mechanism to ensure that queues and data streams are handled atomically, meaning that concurrent transfer operations cannot interfere with each other and that individual cores do not have to wait for other cores to finish processing in order to share resources. This all adds up to full multicore entitlement, which basically means that TI is harnessing the power of multiple cores as if there was one large, powerful core rather than a distributed processing system. This is the holy grail of multicore processing.

TeraNet

SoC architectures will have to support very high external and internal data rates as data moves through the system and out to antennas or transport. Supporting these rates requires a blend of dedicated acceleration and programmable software elements at many different levels. Supporting data movement between these elements is a critical aspect of the design.

TI's TeraNet is part of the SoC's hierarchical network-on-chip, providing multiple terabits per second of non-blocking data transport between cores, peripherals, memory and accelerators. At the system level, this means that all elements can be running simultaneously and independently without waiting for other elements to finish their processing or data transfers first. In a highly optimized and complex system such as a wireless base station, this has a direct impact on performance, allowing system developers to fully unleash the power of the SoC.

Layer 2 processing

The use of MIMO impacts not only the physical layer processing but also the layer 2 scheduling. The emergence of LTE represents a significant shift in scheduling complexity, an area that has not required very complex algorithms with previous standards. Scheduling is the process by which the base station determines how much of the over-the-air bandwidth each mobile user or device will receive in every frame. In LTE, for example, this determination is made every 1 millisecond, based on factors such as user activity (voice, video, gaming, etc.); the user's service plan; and user location (high- or low-signal area).

These factors play a pivotal role in influencing how the scheduler determines the frame allocations. MIMO adds complexity in that it requires the base station to allocate the exact same frequency band to multiple users at once. To accomplish this, the base station must make calculations based on measurements taken from each user to determine which users can be scheduled together. Calculating this requires a matrix inversion every millisecond for every possible combination of users. This can be an onerous task for a real-time, fixed-point processing engine. Poor scheduling performance will result in suboptimal use of expensive spectrum and will likely degrade the user experience. As with MIMO calculations discussed earlier, the new TI architecture with integral floating-point support greatly simplifies and accelerates the necessary processing, since native floating-point support provides tremendous gains for matrix inversion.

Digital radio front end

Small cells can be located either indoors or outdoors and are likely to be completely contained in a single unit. This contrasts with macrocells, where the analog and RF components are typically on top of the tower and the digital baseband processing is in a storage cabinet at the base. To connect efficiently to the co-located analog component, the small cell SoC architecture contains both the digital processing and the interfaces required. This allows a very simple and low-chip count solution that meets the cost, size and power constraints of these designs.

Multicore Shared Memory Controller

Another major improvement on the road to full multicore entitlement is TI's new Multicore Shared Memory Controller. If multiple cores need to process data sequentially, substantial performance can be lost either accessing the data from external memory or when moving the data between the local memory of each core. In TI's new architecture, the Multicore Shared Memory Controller removes this constraint by allowing cores to access shared memory as efficiently as if it were dedicated local memory. This eliminates the need for any data transfers and allows each core to operate immediately and efficiently on data stored in the shared memory. By combining the Multicore Shared Memory Controller with Multicore Navigator and TeraNet, TI enables highly efficient system-level designs, yielding unmatched multicore entitlement for small cell base station developers.

Scalability

As discussed earlier, skyrocketing mobile data consumption heralds a new era in both wireless data speed and cellular network topology. Current cellular networks comprise macrocells primarily, with very limited deployments of picocells and femtocells. At the projected data usage growth rates, even the added spectral efficiencies of LTE will be overwhelmed in a traditional macro-only network topology. The 3GPP standards body recognizes this and is developing methods to simplify the introduction of picocells and femtocells into the network, leading to a heterogeneous network that consists of cells of different sizes rather than a homogenous network of only macrocells. With a view to heterogeneous networks, scalability of solutions and architectures is a critical element for system designers in order to leverage research and development resources across a variety of base station architectures.

Future heterogeneous networks

TI's new SoC architecture brings an unprecedented level of software reuse by sharing the same basic elements regardless of base station type. The new architecture supports varying numbers of processing elements in each device. Processing elements may be cores or coprocessing accelerators targeting all base station functions. This combination of flexible hardware and software design means shorter development time across different projects. The results are optimized hardware costs and lower engineering costs, as equipment manufacturers leverage their designs across all of the elements in a heterogeneous network, offering common, lower cost base stations to operators.

The key feature bringing everything together is TI's Multicore Navigator, which abstracts the notion of multicore and allows each core to act independently under the control of the Multicore Navigator hardware. Because of the abstraction of cores, coprocessors and peripherals, software developed targeting Multicore Navigator requires minimal modification, as the hardware is scaled to the performance needs of the different types of base stations in a heterogeneous network. This common architecture (Figure 3) – across multiple base station products – also affords a new ease of maintenance and installation for wireless operators.

▲ ***Figure 3.*** *New femtocell devices based on TI's multicore SoC architecture integrate fixed and floating point capabilities in the industry's highest performing CPU.*

Conquering the small cell challenges

Now then, how do these architectural features address the challenges of the small cell solution deployments? First, the unprecedented level of functional integration into one device, along with the performance efficiencies afforded by the architecture, provides us with a small cell solution that is physically smaller, lower in power consumption and lower in bill of materials cost over existing technology. Furthermore, the scalable architecture of the base station SoCs allows manufacturers to leverage common software across multiple base station sizes and designs, reducing the development cost and time to market for each platform. This reduces base station product costs while providing commonality of installation and maintenance. Finally, the flexible, programmable, multi-standard SoC affords OEMs the ability to include needed state-of-the-art cell interference cancellation and other advanced cell management techniques. All told, TI's new architecture provides the industry's first truly scalable architecture covering both small cell and macro cell markets.

Conclusion

The changes coming to cellular networks are dramatic and pervasive. The vast amount of data flowing through the system is increasing every day; operators and base station manufacturers are racing to keep up. Innovations at the device level will help provide the tools required to sustain and improve the infrastructure to support the next generation of wireless devices.

TI's new multicore SoC architecture is just one example of the many ways TI is leading this technology forward into the next generation of cellular technology. Such advancements enable wireless service providers to successfully meet the challenges of increasing network data demands by giving equipment manufactures the tools and technology to rapidly and efficiently deploy and maintain cost- and performance-optimized femtocell base stations.

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In his role as the strategic and technical marketing director at Texas Instruments, Arnon Friedmann is driving the company's efforts in cellular base station infrastructure technology. His efforts have enabled TI to maintain leadership positions in this evolving climate. In his 12 years in the industry, he has gained extensive experience in digital communications research and development for magnetic storage, DSL and wireless systems applications. Friedmann earned a Ph.D. in communications theory and systems and a bachelor's degree in engineering physics from the University of California San Diego.

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