IBIS QUALITY REPORT

Part Name: SN65LVDT2
Part Technology Type: LVDS buffer
Marketing part Number: SN65LVDT2DBV; SN65LVDT2D
IBIS Zip File Name: SN65LVDT2_2p1.zip
IBIS File Name: sn65lvdt2.ibs
Available package types: SOT23-5; SOIC-8
Date: 11/11/2008 **IBIS Quality Report Revision: 1.1**
Datasheet Link: http://focus.ti.com/docs/prod/folders/print/sn65lvdt2.html

Contact IBIS modeling Support at elab_ibis@list.ti.com for questions

IBIS MODEL QUALITY CHECKLIST

IBIS Quality Summary:

Included IBIS quality summary information in quality report. For more information on IBIS Quality specification visit http://www.vhdl.org/pub/ibis/quality_wip/

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**********************************************************************
                        IBIS Quality Summary
**********************************************************************
|IQ Over all Quality of IBIS model of component:  Level 2b
|
|IQ Level 0 – 0 errors 0 warnings
|
IQ Level1 – All Level1 checks are done for completeness and correctness; they are either        OK or NA
|
|IQ Level2 – V-T IBIS data compared to TISPICE models. TISPICE used for IBIS model generation
|
IQ Level2b – C_comp Laboratory and TISPICE Correlation
|
|IQ BEGIN IBIS Quality Checklist
|IQ File: sn65lvdt2.ibs   IQ Level: 2b
|IQ COMPONENT: SN65LVDT2DBV   Level:1
|IQ COMPONENT SN65LVDT2D      Level:1
|IQ MODEL: RECEIVER_IN        Level:2
|IQ MODEL: RECEIVER_OUT       Level:2b
|IQ END IBIS Quality Checklist
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IBIS MODEL CORRELATION

Measurement Correlation

1. For Output or I/O model compare IOH and IOL data from measurement to those of IBIS model. Measurement data and simulations in TISPICE are compared across Process, Voltage and Temperature corners. Any special conditions used for simulating or measuring are included.

   Simulation Tool and version used: TISPICE vs. IBIS, simulated using TISPICE
   Measurement conditions used:
   Typical part used with nominal process at room temperature 27C and 3.3V VCC
   Model conditions used:
   Min: 100C, weak process, 3.0V VCC
   Typ: 40C, nominal process, 3.3V VCC
   Max: -40C, strong process, 3.6V VCC

   i. Measured IOH vs. IBIS IOH

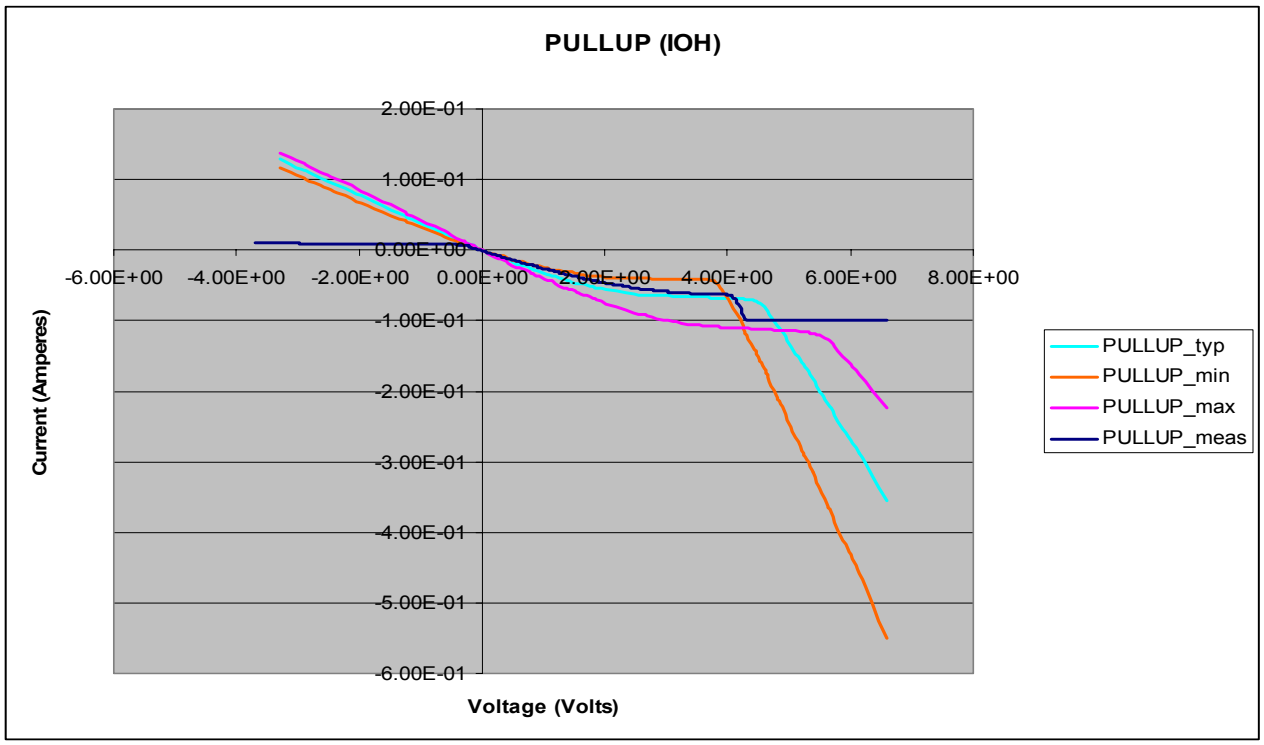

Figure (i)

   ii. Measured IOL vs. IBIS IOL

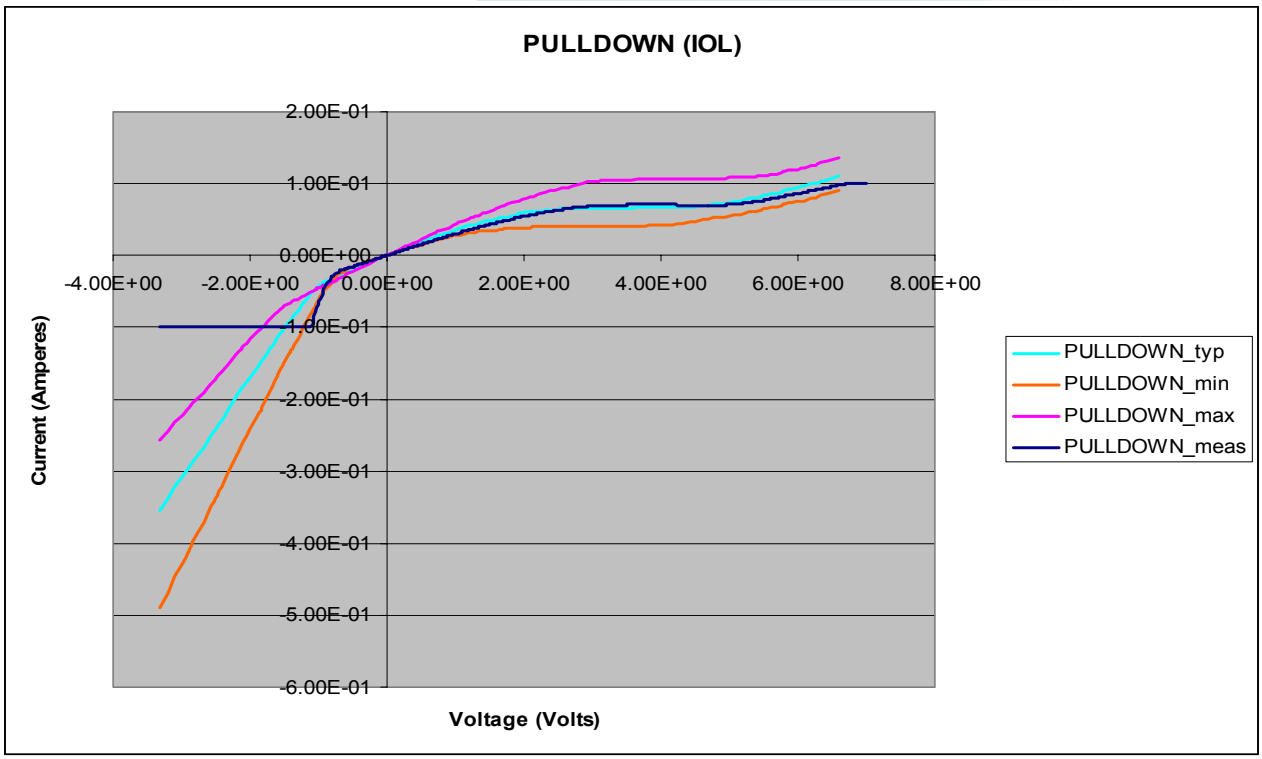

Figure (ii)

Note:

1. Pullup and pulldown curves show current limited to +/- 100mA, that's the clamp current limitation on the parameter analyzer used to do the DC sweeps.
2. RECEIVER_OUT cannot be turned off or tri-stated on SN65LVDT2. Hence power and gnd clamps cannot be separated out from pullup and pulldown curves respectively.
3. ESD devices are not well modeled in TISPICE. The mismatch in IOL is due to mismatch of clamp characteristics and TISPICE simulations. However, notice that in operating range of 0 to VCC, IOL characteristics match very closely.

2. Compare IBIS C_comp with measured C_comp. Table provides comparison for all models and all package types

   Component Name: **SN65LVDT2DBV**

		IBIS			Measurement		
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
	C_comp	3.014pF	3.098pF	3.164pF	NA	NA	NA
R output	**C_package**	0.28366pF	0.28366pF	0.28366pF	NA	NA	NA
	C_total	**3.29766pF**	**3.38166**	**3.44766pF**	**3.35pF**	**3.4pF**	**3.45pF**

	C_comp	5.176pF	5.419pF	5.651pF	NA	NA	NA
A/B Input	**C_package**	0.27573pF	0.281555pF	0.28738pF	NA	NA	NA
	C_total	**5.45755pF**	**5.69473pF**	**5.93838pF**	**5.65pF**	**5.8pF**	**5.95pF**

Table (i)

Component Name: **SN65LVDT2D**

		IBIS			**Measurement**		
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
	C_comp	3.014pF	3.098pF	3.164pF	NA	NA	NA
R output	**C_package**	0.41431pF	0.41431pF	0.41431pF	NA	NA	NA
	C_total	**3.42831pF**	**3.51231pF**	**3.57831pF**	**3.35pF**	**3.4pF**	**3.45pF**
	C_comp	5.176pF	5.419pF	5.651pF	NA	NA	NA
A/B Input	**C_package**	0.42529pF	0.449905pF	0.47452pF	NA	NA	NA
	C_total	**5.60129pF**	**5.86891pF**	**6.12552pF**	**5.65pF**	**5.8pF**	**5.95pF**

Table (ii)

Note: Total IOCAP was measured on pins A, B and R. TI's pkg analyzer is deemed to be very close to silicon and hence separate measurements for each Package are not taken. From total IOCAP measurements and from TI's pkg numbers (from simulations), ccomp was estimated for each of these packages. An over all ccomp was estimated so that ccomp is common between both the packaged part types. This is done to have a common die model for both package types.

Overall ccomp used in TISPICE simulations and IBIS model:

		Min	**Typ**	**Max**
R output	**C_comp IBIS**	3.014pF	3.098pF	3.164pF
	CCOMP avg MEAS SPEC	2.936pF	3.051pF	3.166pF
A/B Input	**C_comp IBIS**	5.176pF	5.419pF	5.651pF
	CCOMP avg MEAS SPEC	5.176pF	5.419pF	5.662pF

Note:
1. In the above table the c_comp value used in IBIS file for RECEIVER_OUT model is slightly higher than the overall spec we obtained from measuring both SN65LVDT2DBV and SN65VDT2D parts. TISPICE Sims showed slightly higher value of c_comp without adding any extra capacitance to match to measurement spec for c_comp adjustment.
2. Datasheet IOCAP spec on Input pins is around 5.8pF. Output pin (R) Output cap is around 3.4pF for typical case. These values should be included in datasheet soon. Typical corner parts only were available for measurements.

3. Clamp data if available, include for all models
   i. GND CLAMP data compared between IBIS and Silicon measurements

Not Available.

ii. POWER CLAMP data compared between IBIS and Silicon measurements

Not Available.

IBIS vs. TISPICE Correlation

1. For all Outputs and Inputs correlate V-T transient simulations using IBIS(B-element) and TISPICE netlist to ensure correlation

   i. Use below setup and node naming conventions for IBIS and TISPICE deck file(*.sp file). Run simulation for all corner case and at maximum allowable speed grade

Case a: RECEIVER_IN A &B vs. TISPICE A &B at 200MHz, with pkg

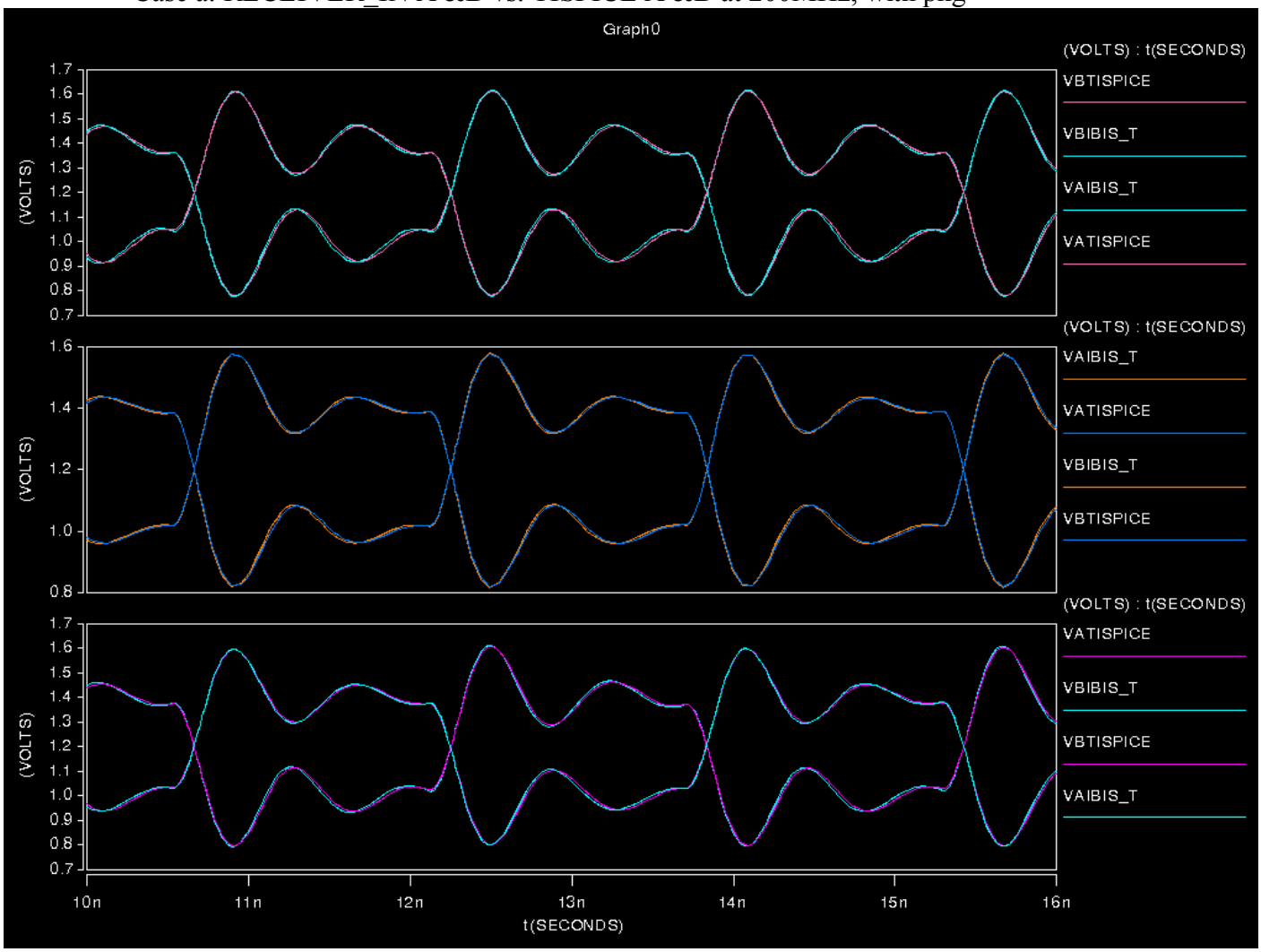

Figure (iii)

Note: Quality report v1.1 is updated with correlation waveforms at better resolution. The discrepancy in the v1.0 report was owing to the use of 0 to VCC swing at diff input pins, instead of realistic range of 1V to 1.4V on A & B signals. The discrepancy is resolved in v1.1 Quality report.

Case b: Output R from IBIS vs. R from TISPICE at 315MHz, with pkg

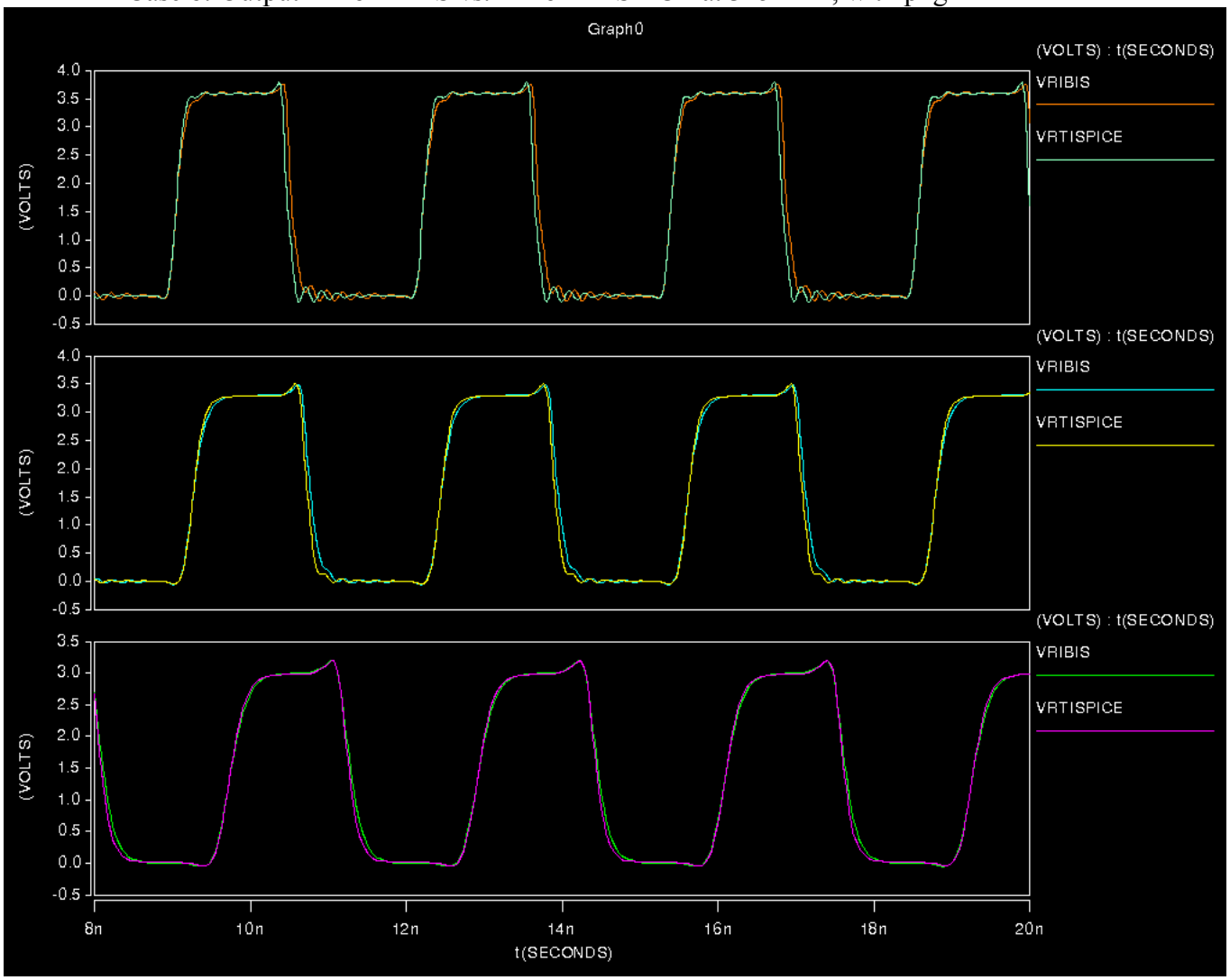

Figure (iv)

Schematic used for Correlation:

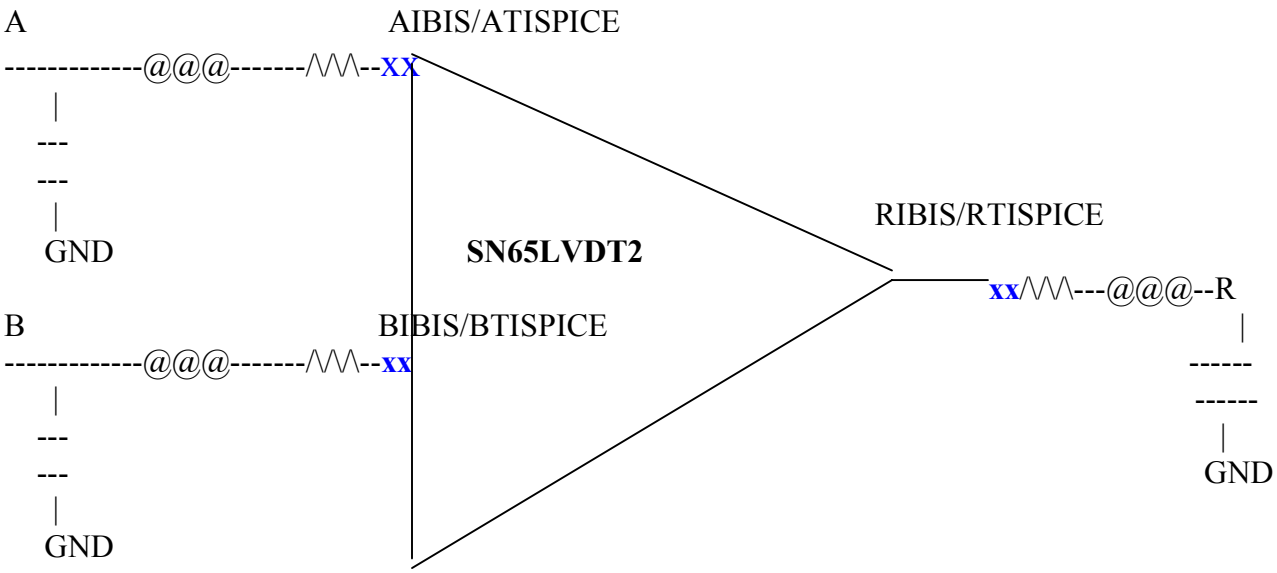

Figure (vii)

Note: **"xx"** indicate nodes at which results are shown in the waveforms.

Revision History:

Rev 1.0: 1/0/31/2008

Initial version of Quality report

Rev 1.1: 11/11/2008

Added Note 3 for Figure (ii)

Updated Note for Figure (iii)

Updated report with high resolution correlation waveforms for A/B and R signals, Figure (iii) and Figure (iv)