Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

Place Block Diagram here (if appropriate) or delete this text box.
If using a block diagram from another tool, save the picture as a .bmp file.
Then, use menu Place|Drawing Tools|Graphic to insert the .png/.svg/.bmp file on the schematic.

Orderable:		Designed for: Public Release	Mod. Date: 5/6/2021
TID #: N/A		Project Title: DRV8328AEVM	
Number: MD053	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 004	Sheet: 1 of 5
Drawn By:		File: MD053A_BlockDiagram.SchDoc	Size: B
Engineer: Aaron Barrera		Contact: http://www.ti.com/support	

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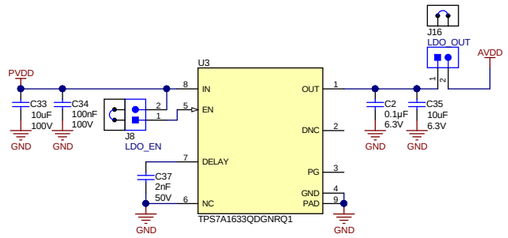
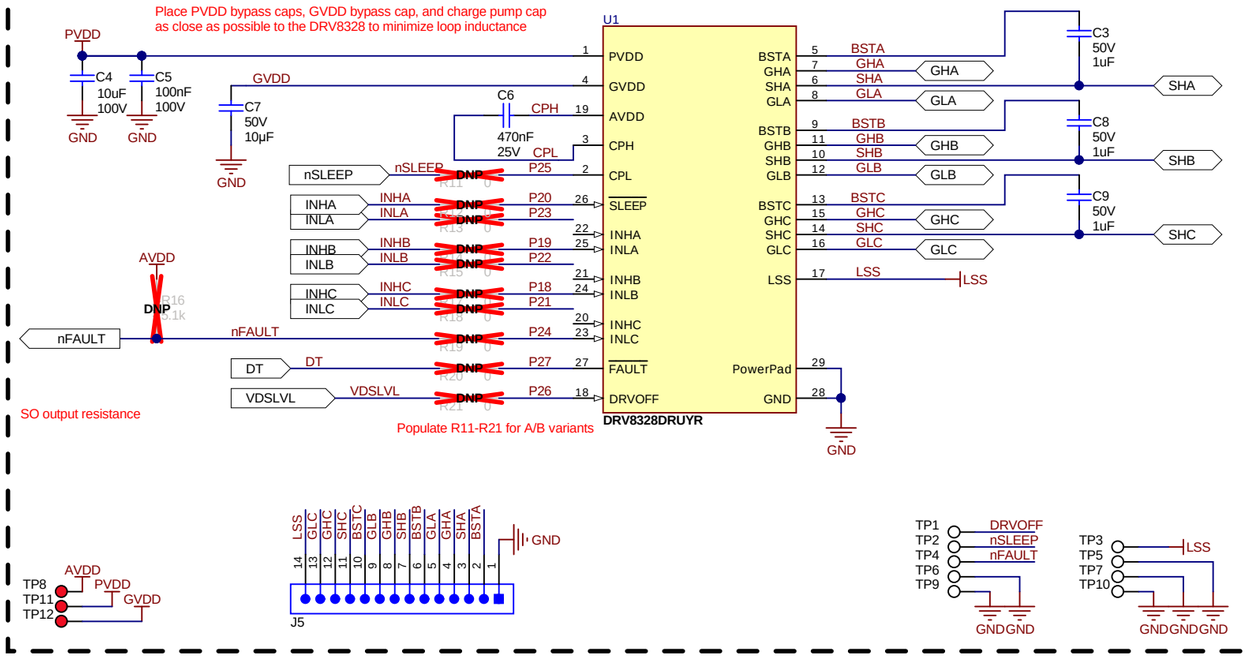
http://www.ti.com

Remove LDO_OUT jumper if DRV8328C/D is used to prevent back-powering LDO

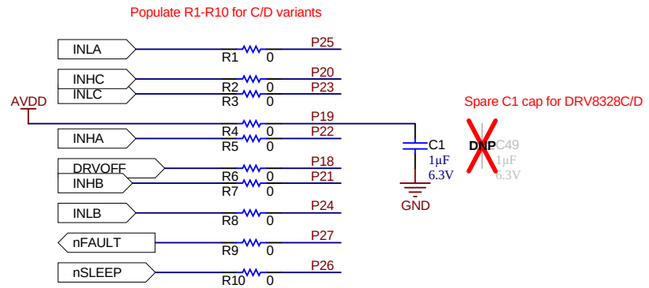


Orderable:	Designed for: Public Release	Mod. Date: 10/27/2021
TID #: N/A	Project Title: DRV8328AEVM	
Number: MD053 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 004	Sheet: 2 of 3
Drawn By:	File: MD053A_LDO.SchDoc	Size: A2
Engineer: Aaron Barrera	Contact: http://www.ti.com/support	http://www.ti.com

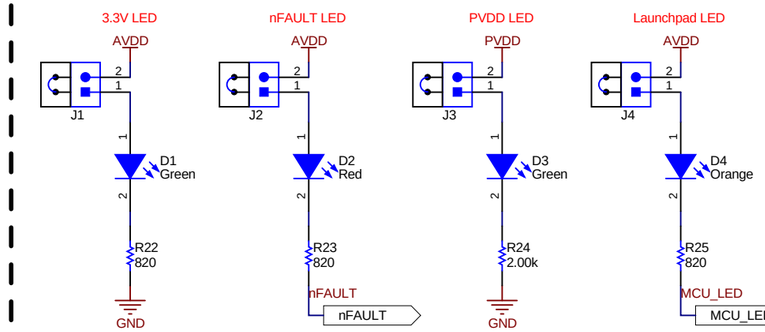
DRV8328A/B/C/D



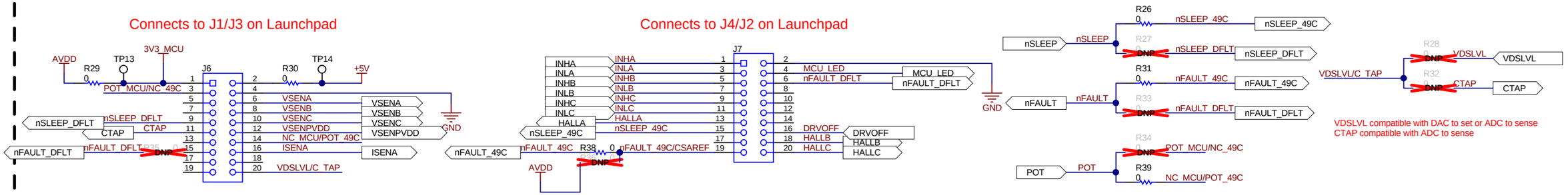
DRV8328C/D VARIANT PIN SELECT



STATUS LEDS



LAUNCHPAD CONNECTORS AND CONNECTIONS



Orderable:		Designed for: Public Release	Mod. Date: 10/27/2021
TID #: N/A		Project Title: DRV8328AEVM	
Number: MD053	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 004	Sheet: 2 of 5
Drawn By:		File: MD053A_DRIVER.SchDoc	Size: B
Engineer: Aaron Barrera		Contact: http://www.ti.com/support	

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POWER STAGE AND FETS

PHASE A

PVDD

RC Snubber, HS Drain to LS Source cap, and GS Cap or Res are all recommended, but optional, protection circuits

GHA — R43 10 — GHA_FET — Q1 (CSD18536KTTT)
TP15
R46 DNP 10 — D5 DNP 1N4448WX-TP — C13 DNP 2nF 50V
R40 DNP 50 — C10 DNP 3900pF 100V

SHA — NT1 Net-Tie — OUTA

GLA — R49 10 — GLA_FET — Q4 (CSD18536KTTT)
TP18
R52 DNP 10 — D8 DNP 1N4448WX-TP — C25 DNP 2nF 50V
C24 DNP 3900pF 100V — R55 DNP 50

OUTA — OUTA
C19 100V 0.01uF
C14 100V 2.2uF
GND

LSS — LSS

PHASE B

GHB — R44 10 — GHB_FET — Q2 (CSD18536KTTT)
TP16
R47 DNP 10 — D6 DNP 1N4448WX-TP — C15 DNP 2nF 50V
R41 DNP 50 — C11 DNP 3900pF 100V

SHB — NT2 Net-Tie — OUTB

GLB — R50 10 — GLB_FET — Q5 (CSD18536KTTT)
TP19
R53 DNP 10 — D9 DNP 1N4448WX-TP — C26 DNP 2nF 50V
C22 DNP 3900pF 100V — R56 DNP 50

OUTB — OUTB
C20 100V 0.01uF
C16 100V 2.2uF
GND

Populate diodes to control sink and source current independently

PHASE C

GHC — R45 10 — GHC_FET — Q3 (CSD18536KTTT)
TP17
R48 DNP 10 — D7 DNP 1N4448WX-TP — C17 DNP 2nF 50V
R42 DNP 50 — C12 DNP 3900pF 100V

SHC — NT3 Net-Tie — OUTC

GLC — R51 10 — GLC_FET — Q6 (CSD18536KTTT)
TP20
R54 DNP 10 — D10 DNP 1N4448WX-TP — C27 DNP 2nF 50V
C23 DNP 3900pF 100V — R57 DNP 50

OUTC — OUTC
C21 100V 0.01uF
C18 100V 2.2uF
GND

External C_GS capacitors can be replaced with k ohm pull down resistors if desired

Low pass filter

Low pass filter
Place near BP header

ISENA — ISENA — R59 56 — SOA
C31 2200pF — GND

Place as close to sense resistor as possible

U2 INA180A1IDBVR
OUT (1) — VS (5) — AVDD
GND (2) — GND
IN+ (3) — SP
IN- (4) — SN
C29 0.1uF — GND

Route as differential pair Kelvin connection to shunt

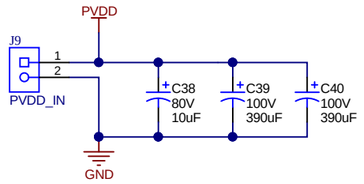
TP32 — SP — R58 0
DNP C28 330pF 100V — GND
DNP C30 50V 0.01uF
R60 0.001
TP33 — SN — R61 0
DNP C32 330pF 100V — GND
GND

KO

Orderable:	Designed for: Public Release	Mod. Date: 10/24/2021
TID #: N/A	Project Title: DRV8328AEVM	
Number: MD053 Rev: A	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 004	Sheet: 3 of 5
Drawn By:	File: MD053A_FETS_AND_POWER_STAGE.SchDoc	Size: B
Engineer: Aaron Barrera	Contact: http://www.ti.com/support	

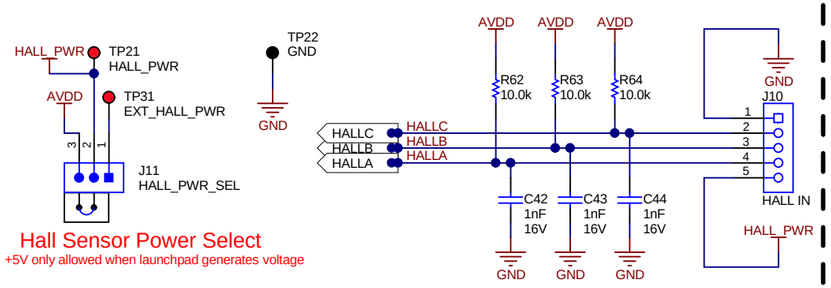
Texas Instruments
http://www.ti.com

MAIN SUPPLY INPUT



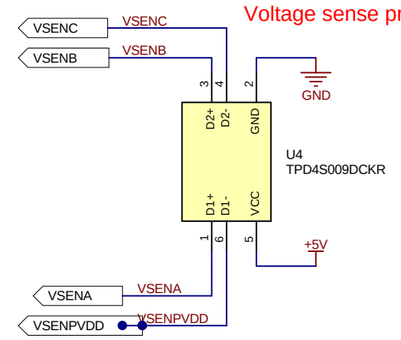
4.5-V to 60-V Operation
65V ABS MAX
35A Rated connector

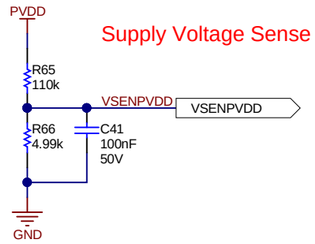
HALL SENSOR INPUT AND POWER

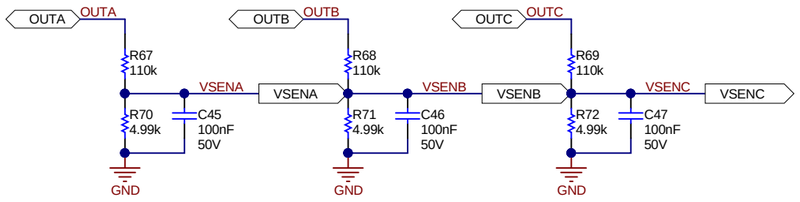


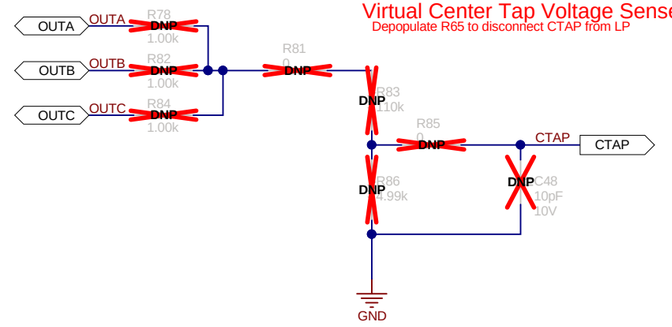
Hall Sensor Power Select
+5V only allowed when launchpad generates voltage

VOLTAGE SENSE & PROTECTION

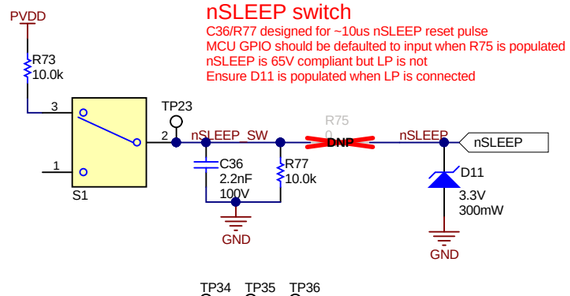


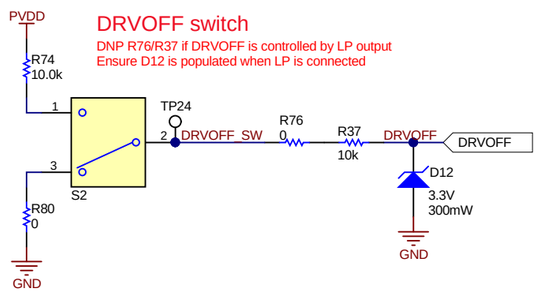


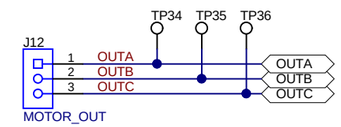




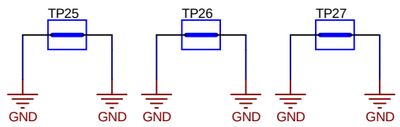
CONNECTORS, SELECTORS, & ANALOG CONTROL INTERFACE

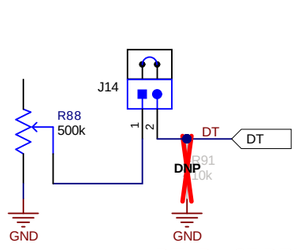




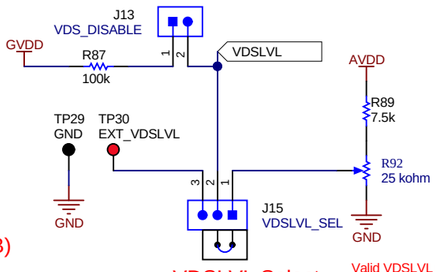


Motor Phase Connector
35A rated



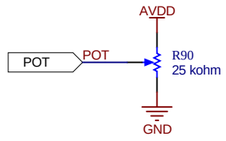


DT (Pin 27 DRV8328A/B)
DT = GND: t_Dead = 55 ns
DT = Floating: t_Dead = 160 ns (DRV8328B) or 55 ns (DRV8328A)
DT = 10 k < R88 < 390 k: t_Dead = linear between 100 ns - 2000 ns
R88 [ohms] = (t_Dead [ns])*200 - 10000
All values typical



VDSLVL Select
POT select by default

Valid VDSLVL range: 0.1V - 2.5V
POT Voltage range: 0V - 2.538V



General purpose pot for MCU

Orderable:		Designed for: Public Release	Mod. Date: 10/28/2021
TID #: N/A		Project Title: DRV8328AEVM	
Number: MD053	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 004	Sheet: 4 of 5
Drawn By:		File: MD053A_POWER_AND_CONNECTORS.SchDoc	Size: B
Engineer: Aaron Barrera		Contact: http://www.ti.com/support	

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H1 1
NY PMS 440 0025 PH

H2 1
NY PMS 440 0025 PH

H3 1
NY PMS 440 0025 PH

H4 1
NY PMS 440 0025 PH

H5
1902C

H6
1902C

H7
1902C

H8
1902C

DNP
FID1

DNP
FID2

DNP
FID3

PCB Number: MD053
PCB Rev: A

PCB
LOGO
Texas Instruments

CE Mark

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo


CAUTION HOT SURFACE


CAUTION HOT SURFACE


CAUTION HOT SURFACE

Variant/Label Table	
Variant	Label Text
001	DRV8328AEVM
002	DRV8328BEVM
003	DRV8328CEVM
004	DRV8328CEVM

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable:		Designed for: Public Release	Mod. Date: 10/28/2021
TID #: N/A		Project Title: DRV8328AEVM	
Number: MD053	Rev: A	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 004	Sheet: 5 of 5
Drawn By:		File: MD053A_Hardware.SchDoc	Size: B
Engineer: Aaron Barrera		Contact: http://www.ti.com/support	

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