AM62x SKEVM WITH FULTON PMIC

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VER	0.09

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TEXAS INSTRUMENTS

MISTRAL

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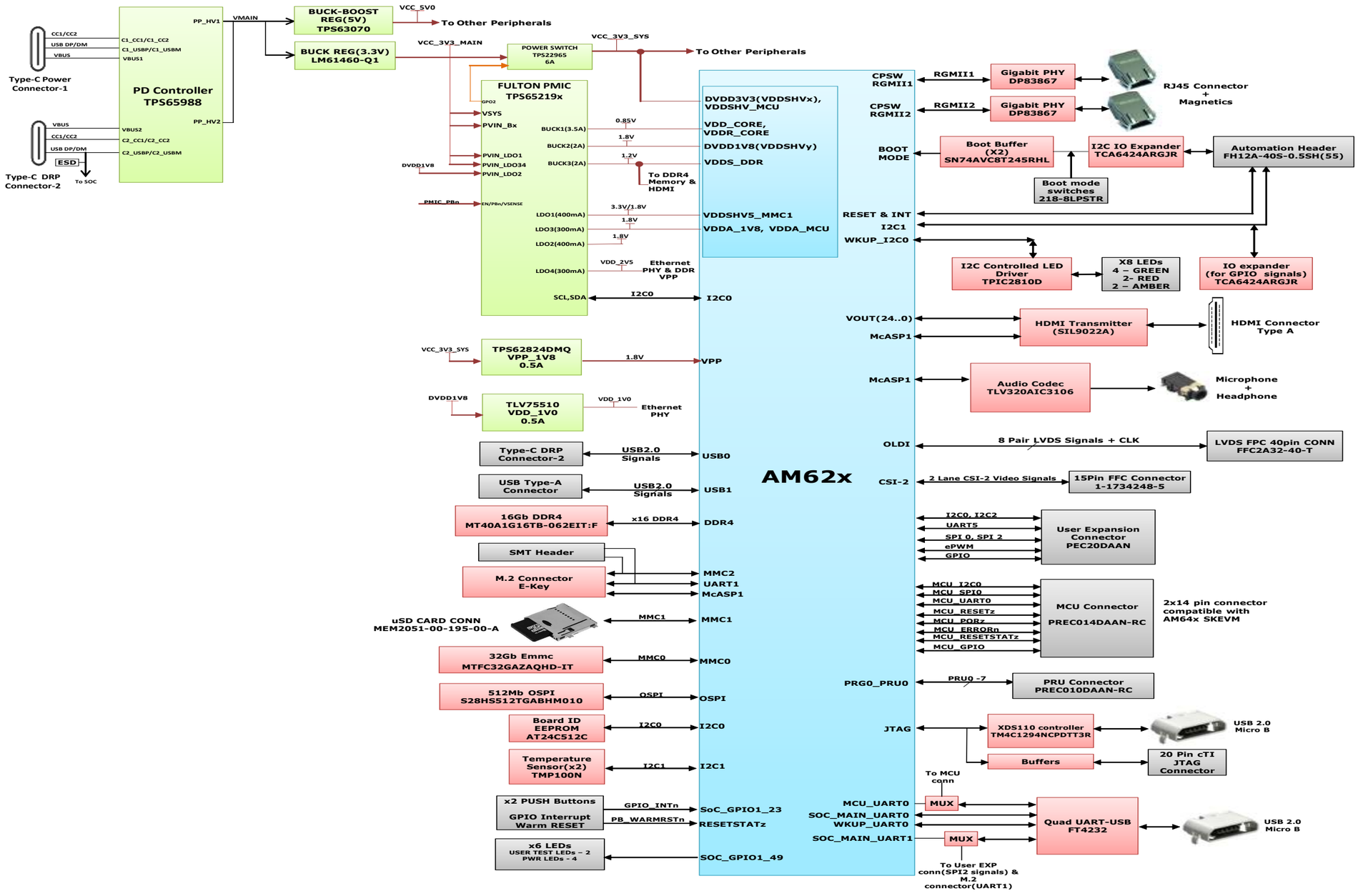
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	29 AUG 2022	Drafted from E1 Schematics. R651 value changed to 1K. DNI'd R618 and R676.Changed the I2C buffer parts to TCA9517DR. Changed the part SN74AVC4T245RSVR to SN74AVC4T245DGVR	Mistral Design Team		
0.02	08 SEP 2022	Added the second GPIO Expander U110 Part# TCA6408ARGTR	Mistral Design Team		
0.03	21 SEP 2022	Changed the Current monitors Res Filter values from 10E to 0E to the Sense pins.	Mistral Design Team		
0.04	19 OCT 2022	Added Testpoint to TEMP_DIODE_P pin of SoC. Changed the GPIO_OLDI_RSTn net name to GPIO_TS_RSTn.	Mistral Design Team		
0.05	24 OCT 2022	Changed the Fulton PMIC part from TPS6521903RHBR to TPS6521904RHBR. Mounted R699 and DNI'd R123. DNI'd the current monitor section of U36	Mistral Design Team		
0.06	3 Nov 2022	Changed the DDR4 part from MT40A1G16KD-062E IT:E to MT40A1G16TB-062E IT:F. Changed the eMMC part from MTFC16GAPALBH-IT to MTFC32GAZAQHD-IT.	Mistral Design Team		
0.07	15 Nov 2022	Removed the PMIC_STBY connection from SOC to PMIC.	Mistral Design Team		
0.08	22 Nov 2022	Added 2x 47uF on VCC_5V0. DNI'd C432, C433(10uF) and changed C415 to 4.7uF. Added 22pF CAP across R108	Mistral Design Team		
0.09	1 Dec 2022	Removed MMC2 connector section (J18) and associated resistors	Mistral Design Team		

BLOCK DIAGRAM



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Title	BLOCK DIAGRAM AM62x SKEVM		
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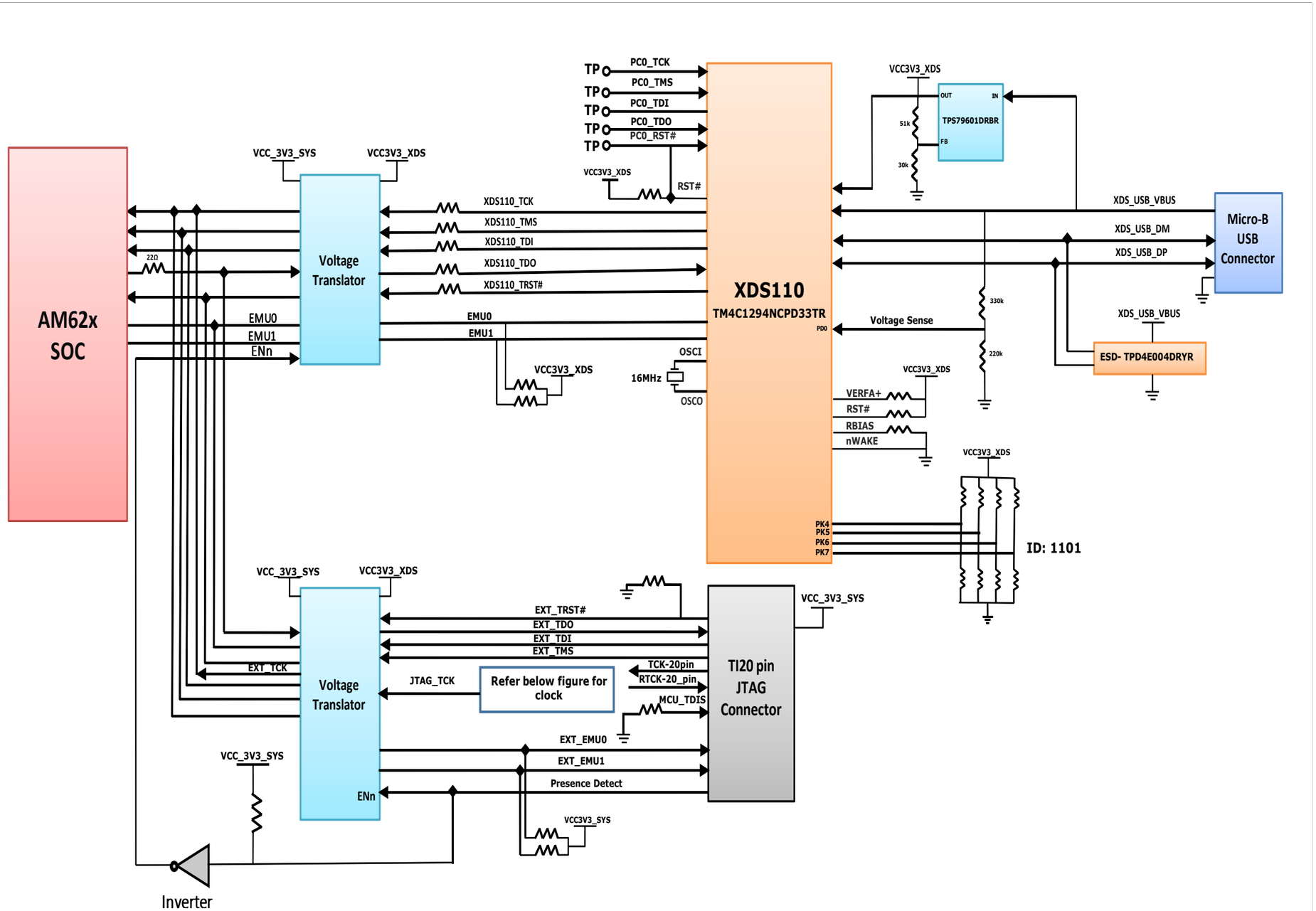
BLOCK DIAGRAM_XDS110



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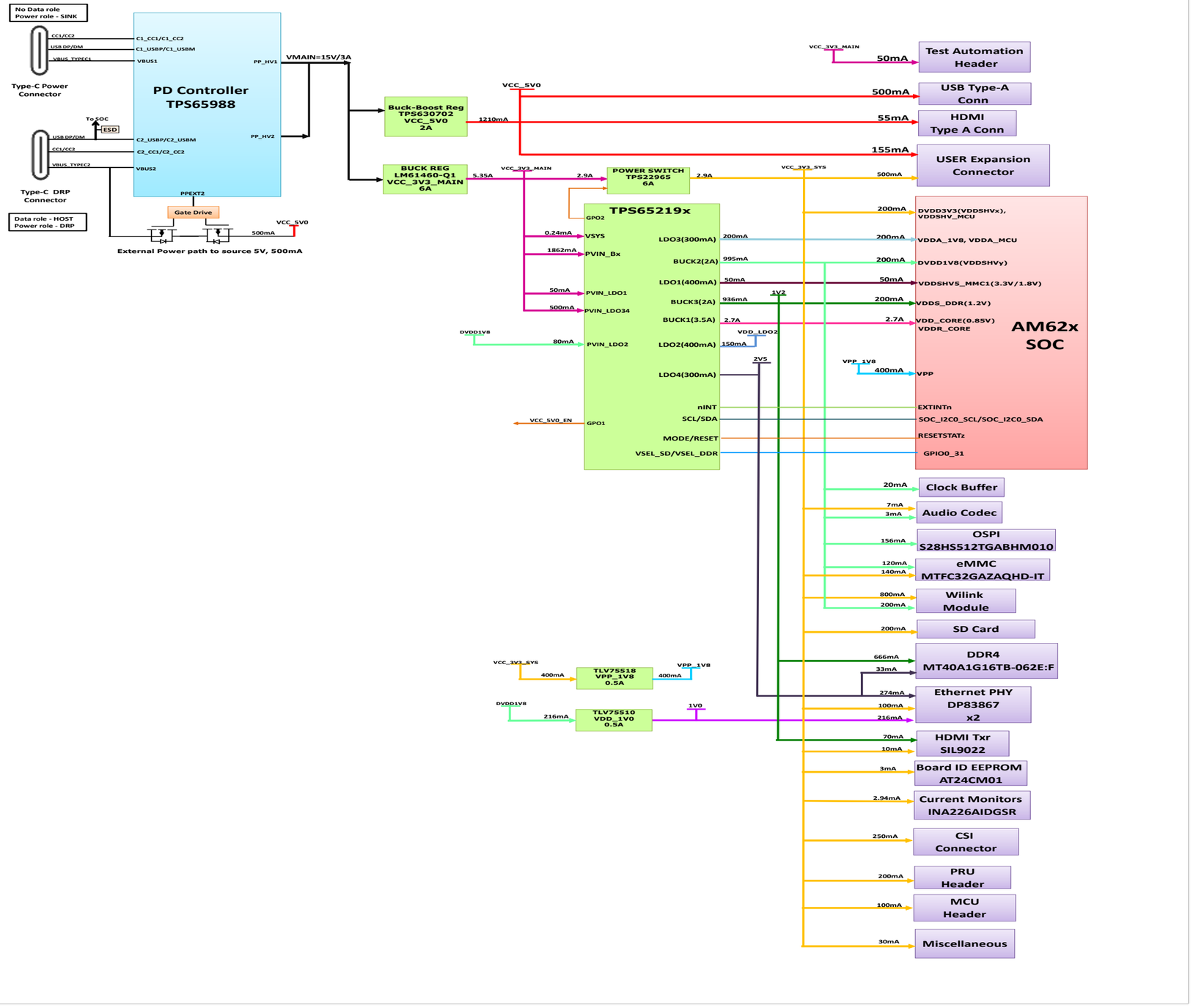
POWER BLOCK DIAGRAM



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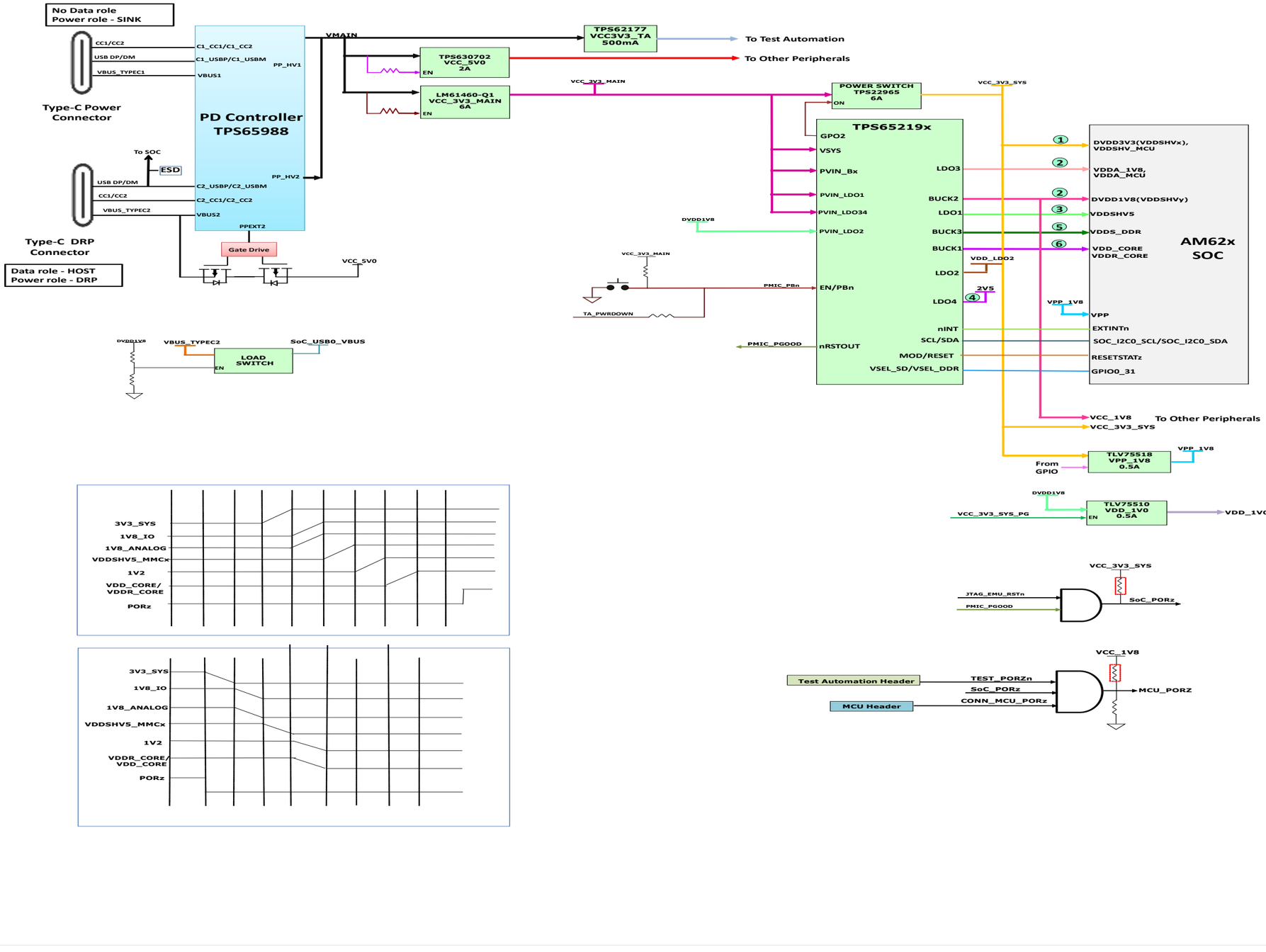
POWER SEQUENCE



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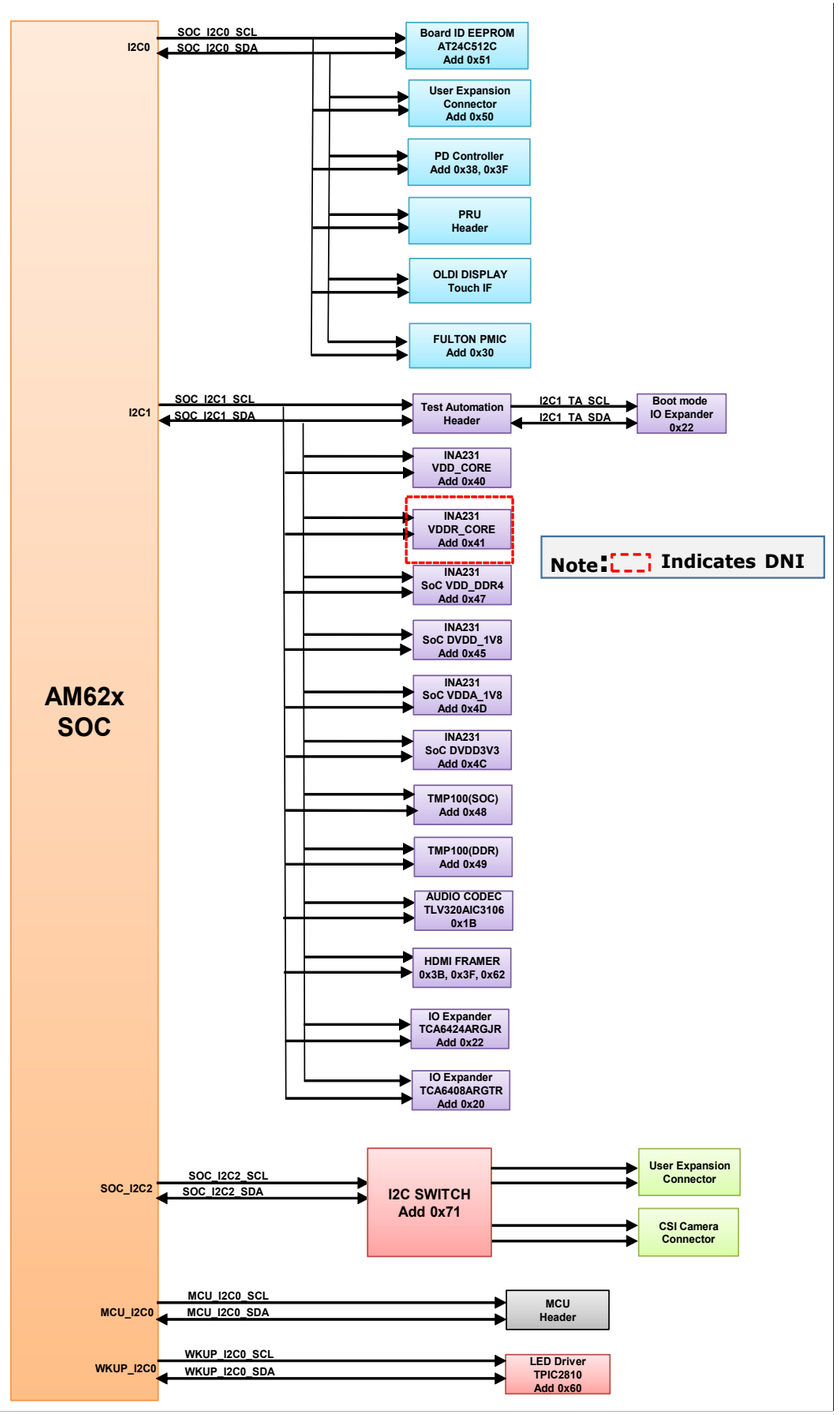
I2C TREE



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Title	I2C TREE	
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt PMIC_INTn	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 01									
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 02									
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

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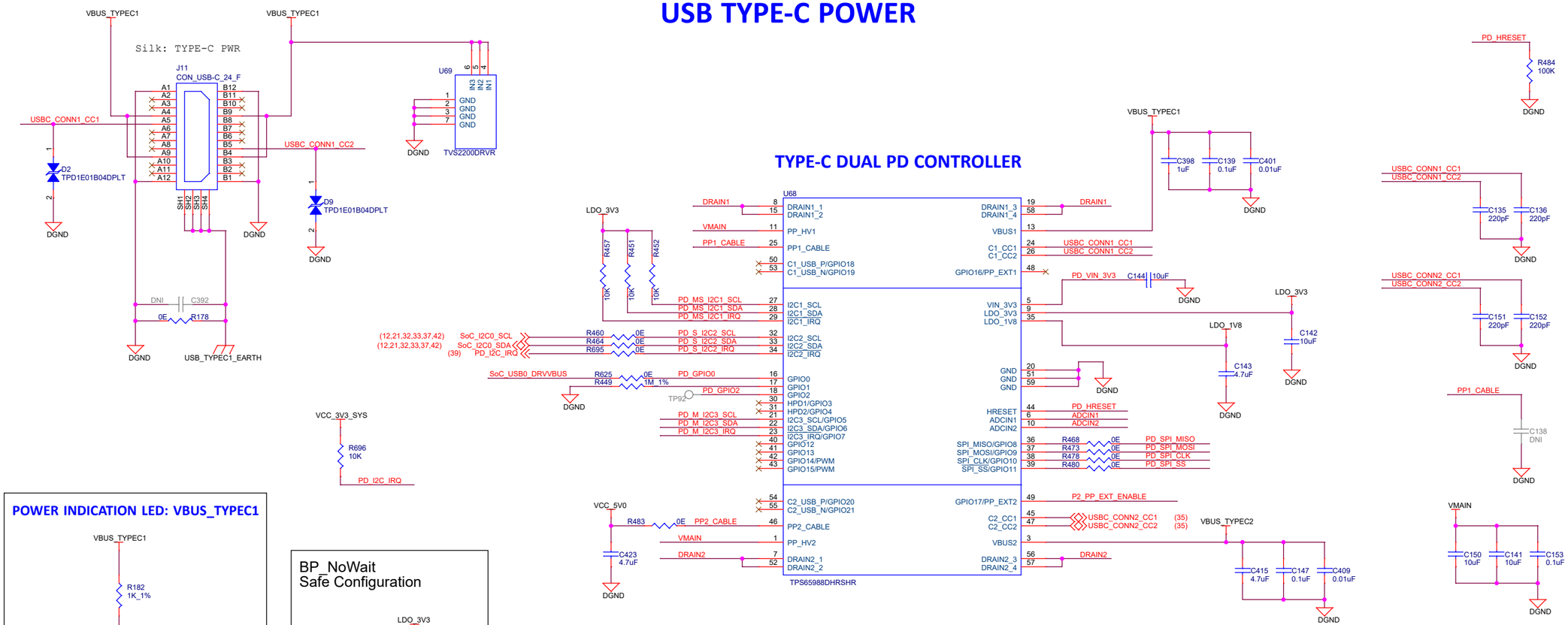
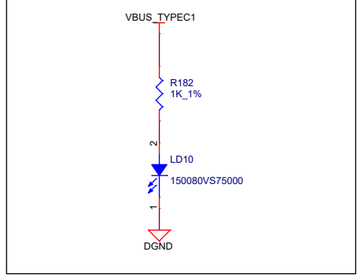
USB TYPE-C POWER

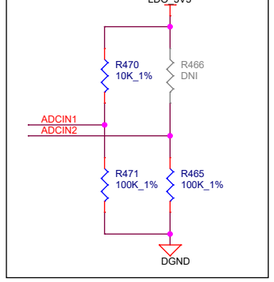
TYPE-C DUAL PD CONTROLLER



POWER INDICATION LED: VBUS_TYPEC1

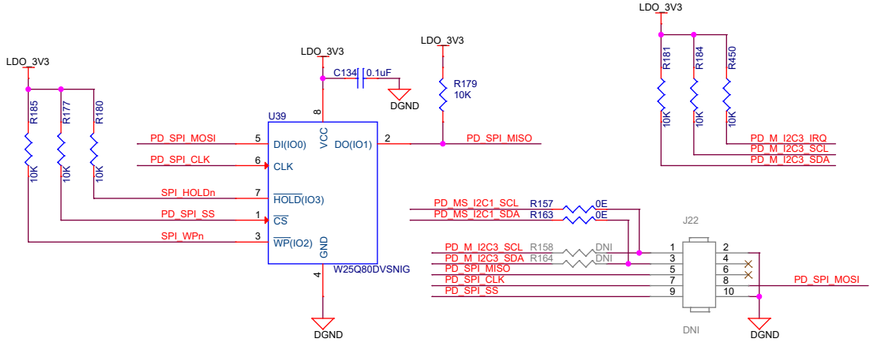


BP_NoWait
Safe Configuration

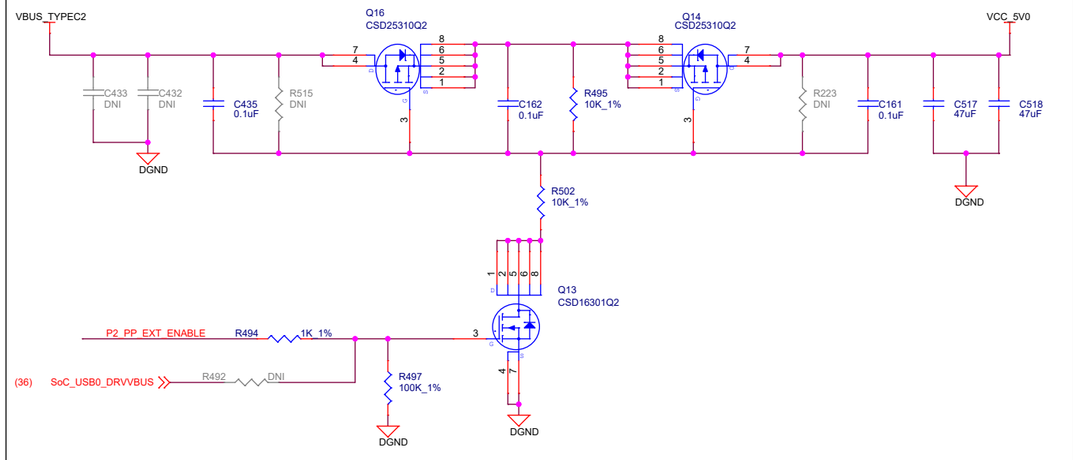


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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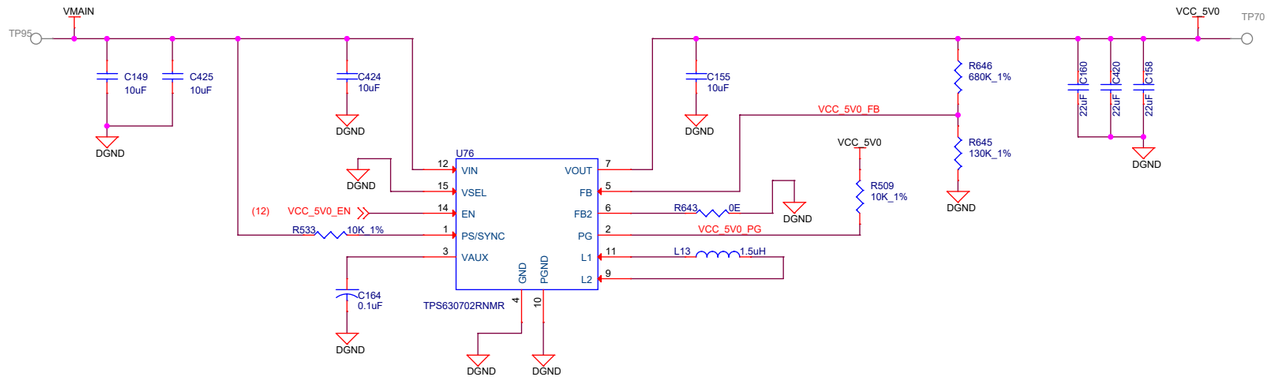
PERIPHERAL POWER SUPPLY-1



GROUND TEST POINTS

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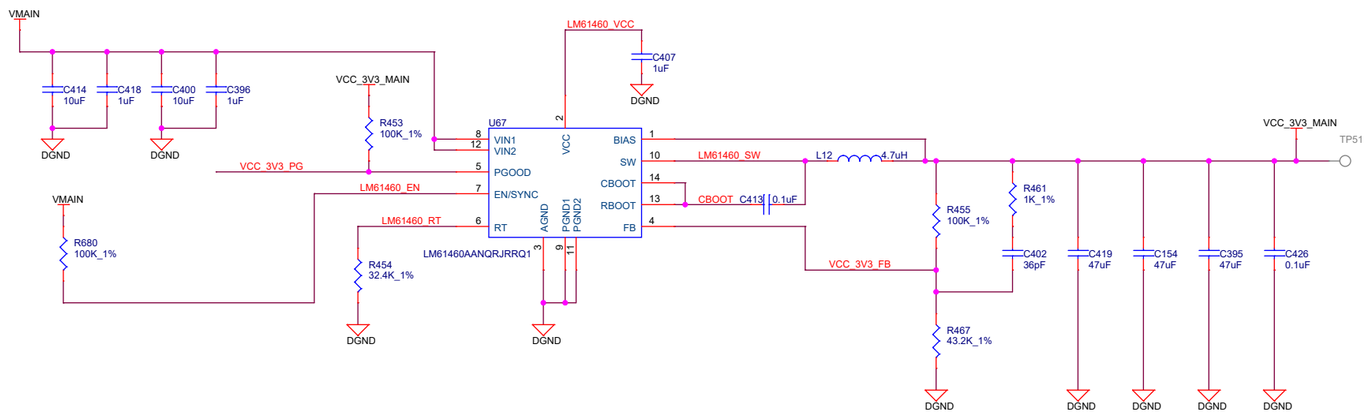
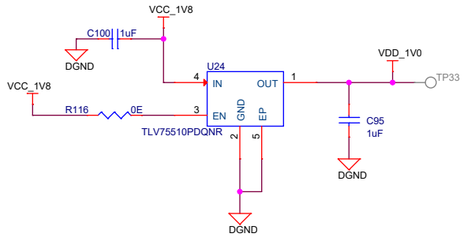
PERIPHERAL POWER SUPPLY-2

3.3V, 6.0AMPS SUPPLY

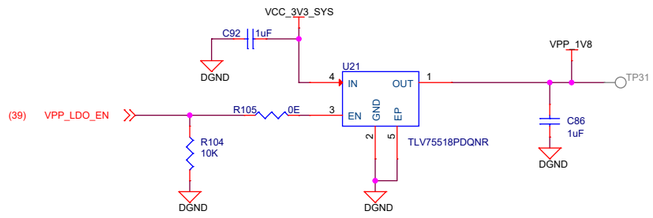
VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A



1.0V, 0.5AMPS SUPPLY (ETHERNET)



1.8V VPP, 0.5AMPS SUPPLY



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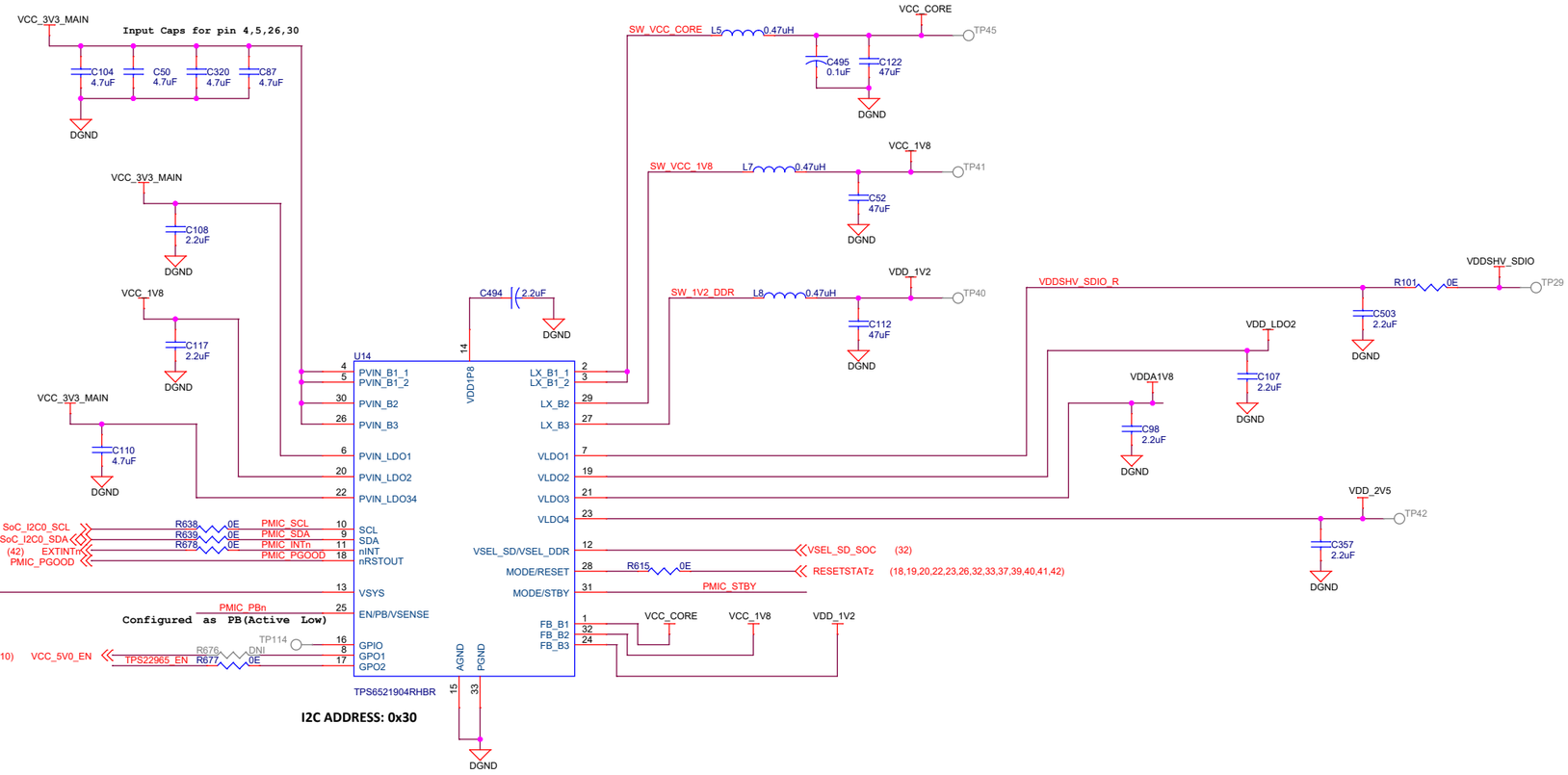
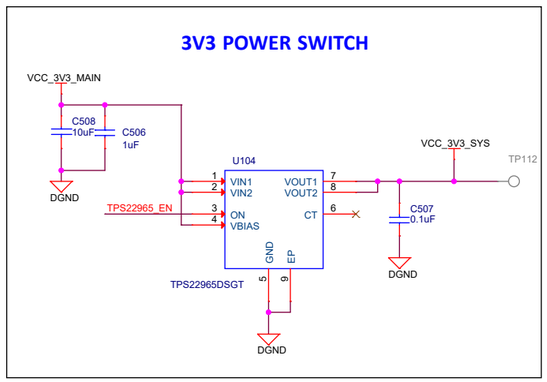
FULTON PMIC

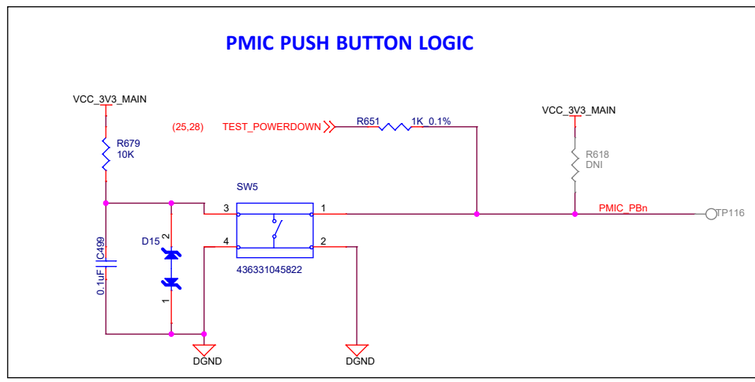
PMIC REGULATORS	VOLTAGE RAIL	CURRENT(mA)
BUCK 1	VCC_CORE(0.85V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDD_LDO2	150
LDO 3	VDDA1V8	200
LDO 4	VDD_2V5	300



3V3 POWER SWITCH



PMIC PUSH BUTTON LOGIC



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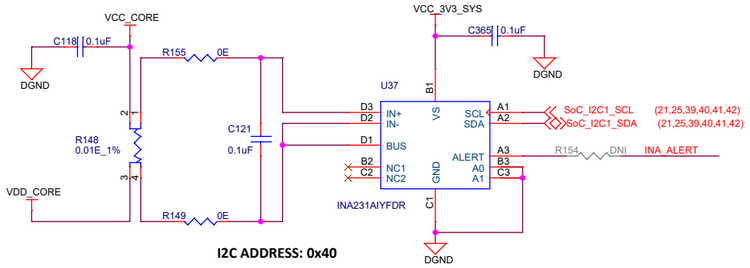
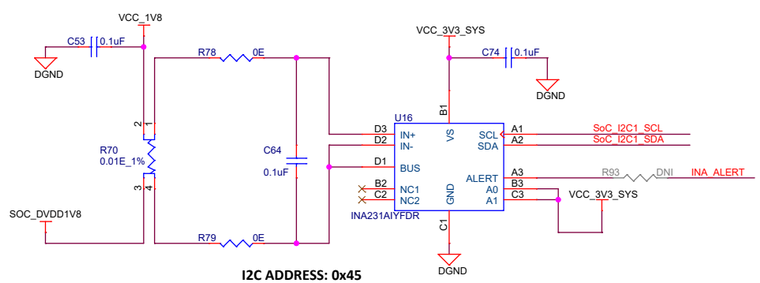
CURRENT MONITORING DEVICES

VDD_CORE



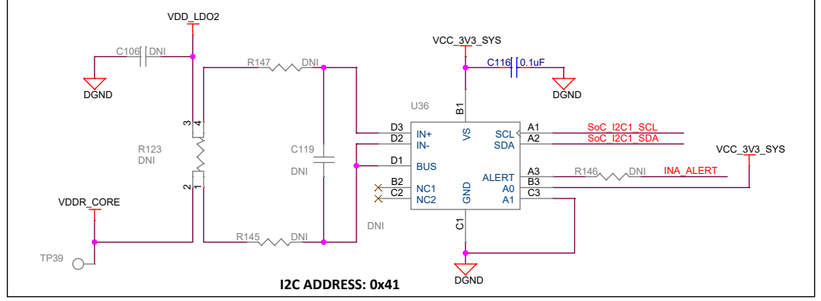
I2C ADDRESS: 0x40

SoC_DVDD1V8



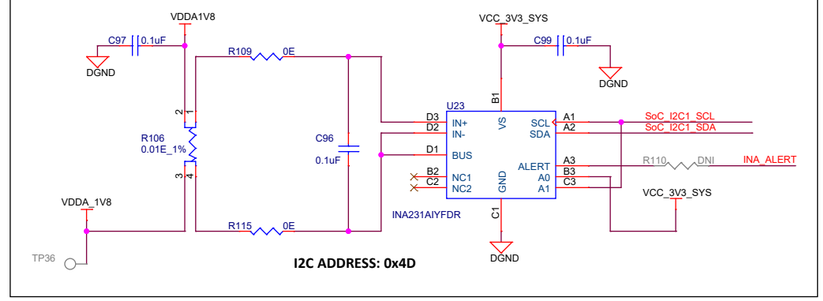
I2C ADDRESS: 0x45

VDDR_CORE



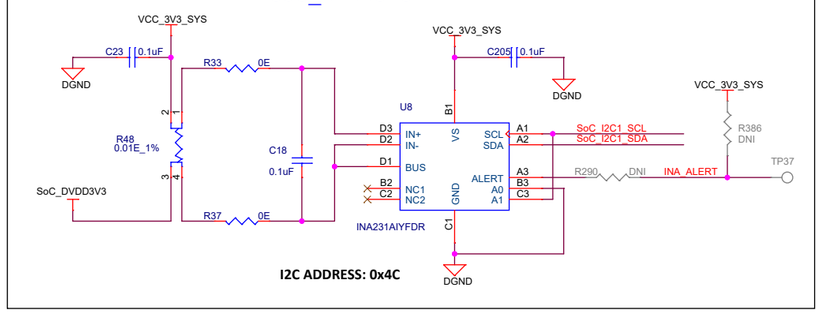
I2C ADDRESS: 0x41

VDDA_1V8



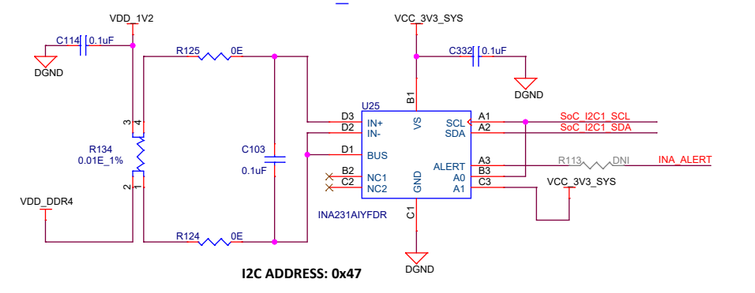
I2C ADDRESS: 0x4D

SoC_DVDD3V3



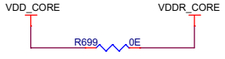
I2C ADDRESS: 0x4C

VDD_DDR4



I2C ADDRESS: 0x47

RES Option to short VDD_CORE and VDDR_CORE rails when both are 0.85V(Both should be generated from the same source)



CORE SUPPLY	ARRAY CORE SUPPLY	Assembly
0.75 VDD_CORE	0.85 VDDR_CORE	DNI R699 and Mount R123
0.85 VDD_CORE	0.85 VDDR_CORE	DNI R123 and Mount R699

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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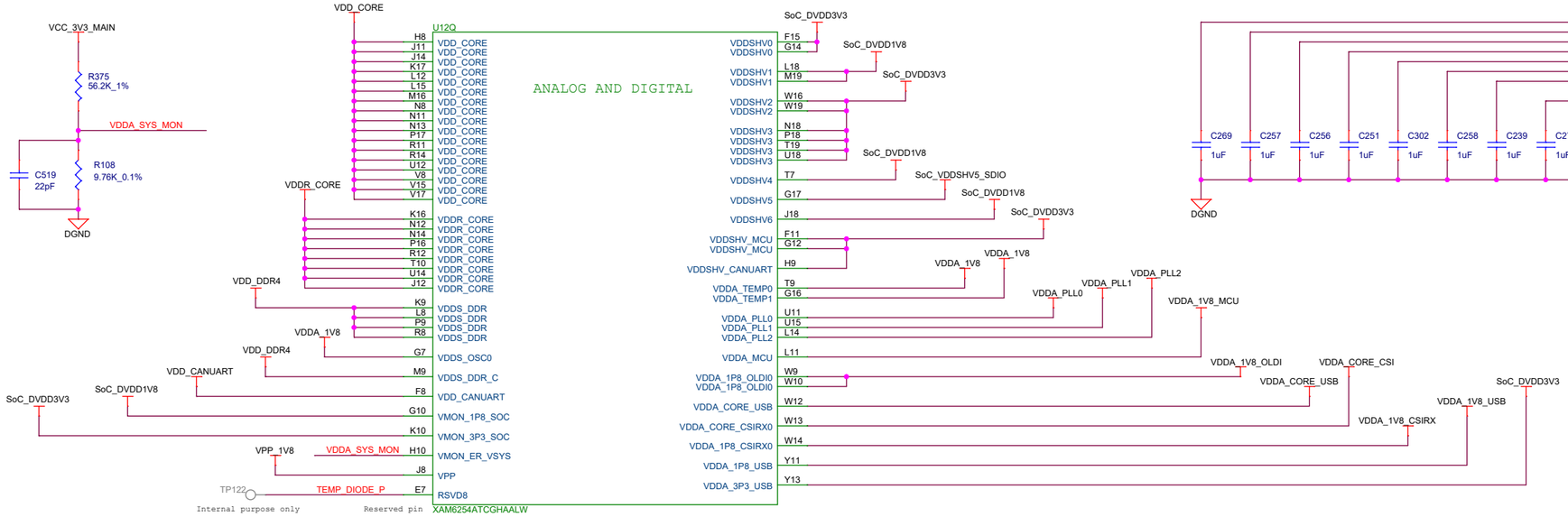
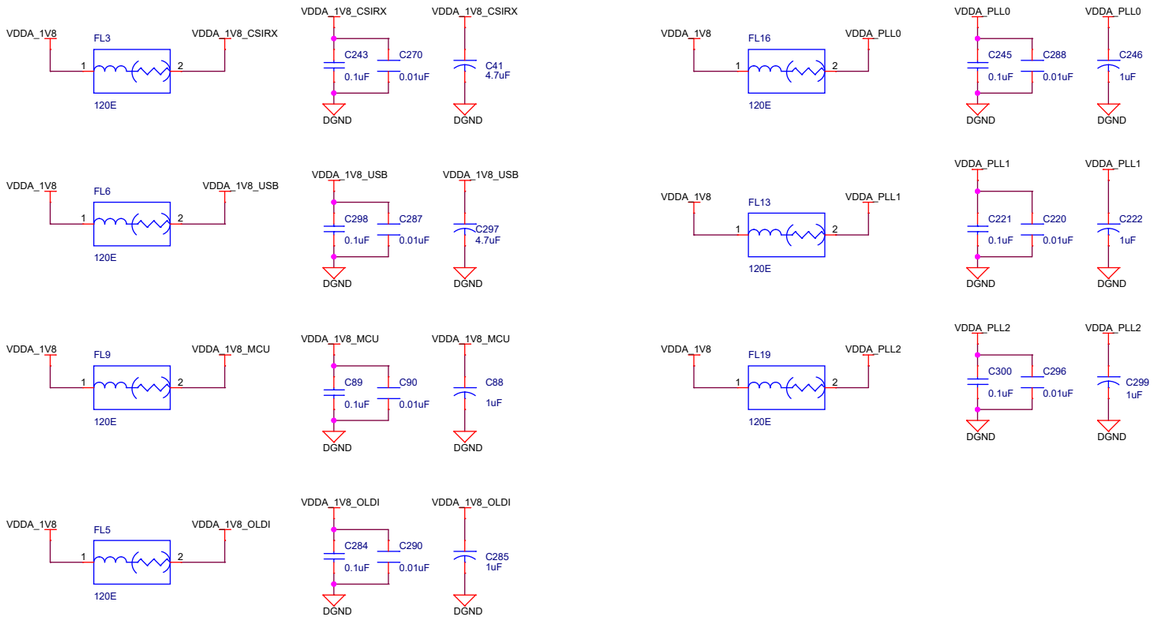
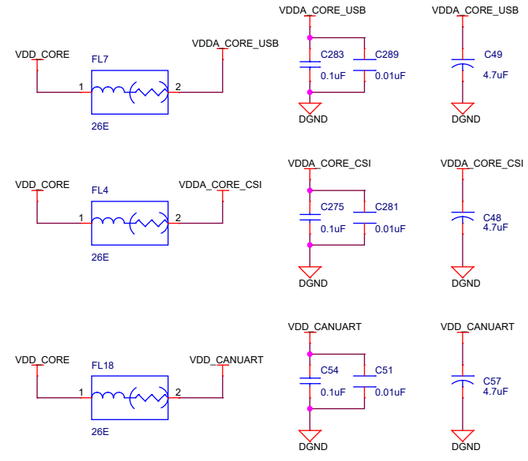
SOC POWER



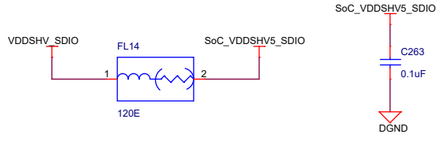
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY



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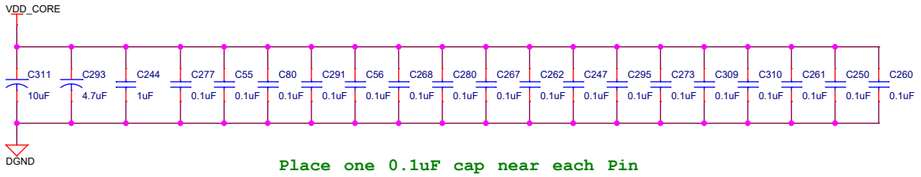
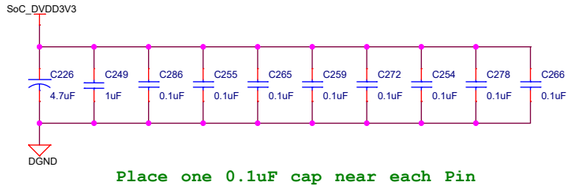
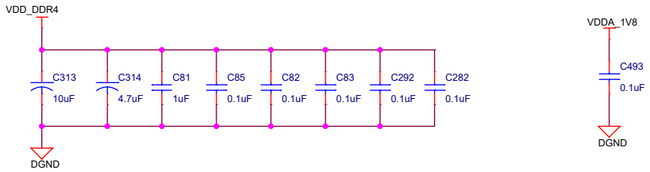
SOC POWER DECAPS



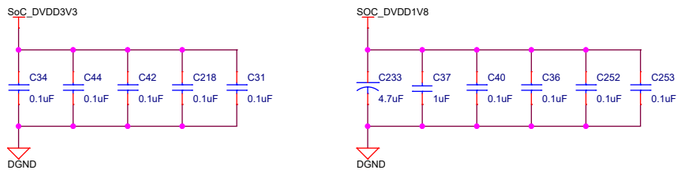
Place one 0.1uF cap near each Pin



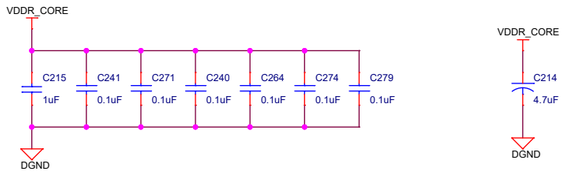
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

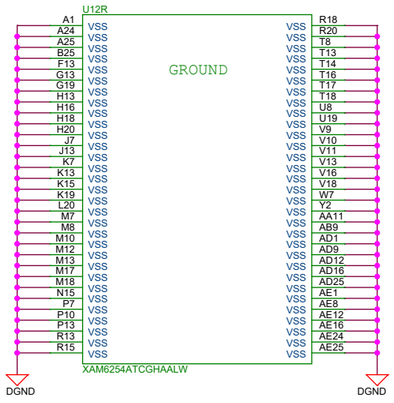


Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

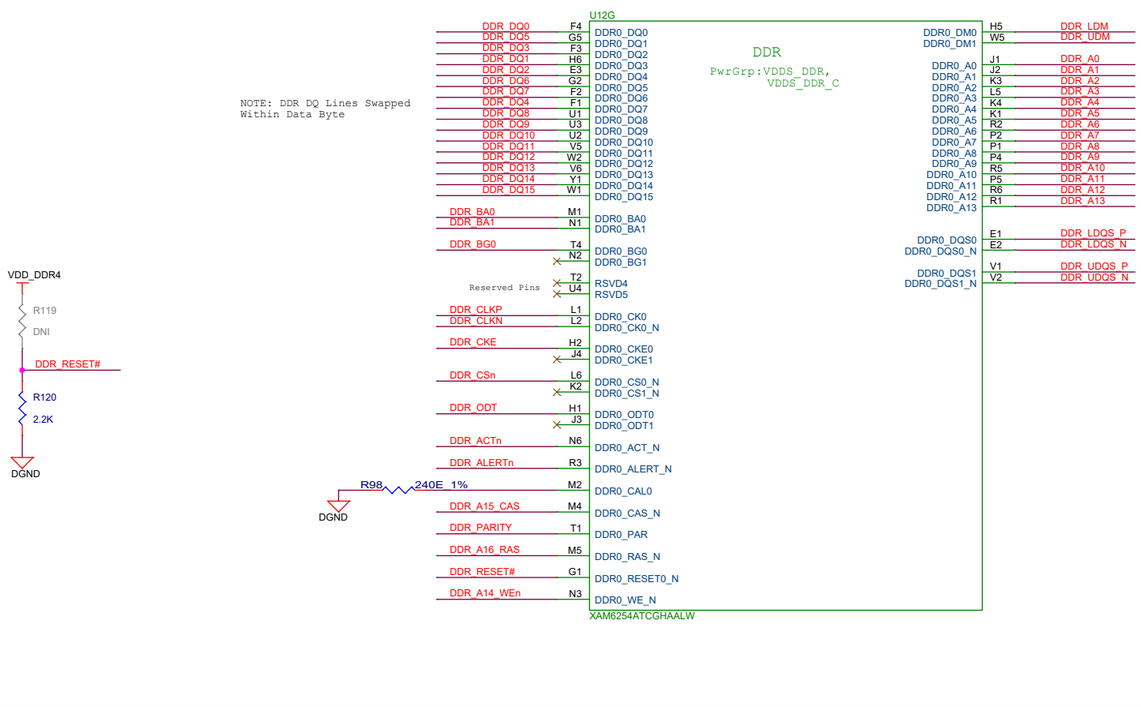
SOC VSS



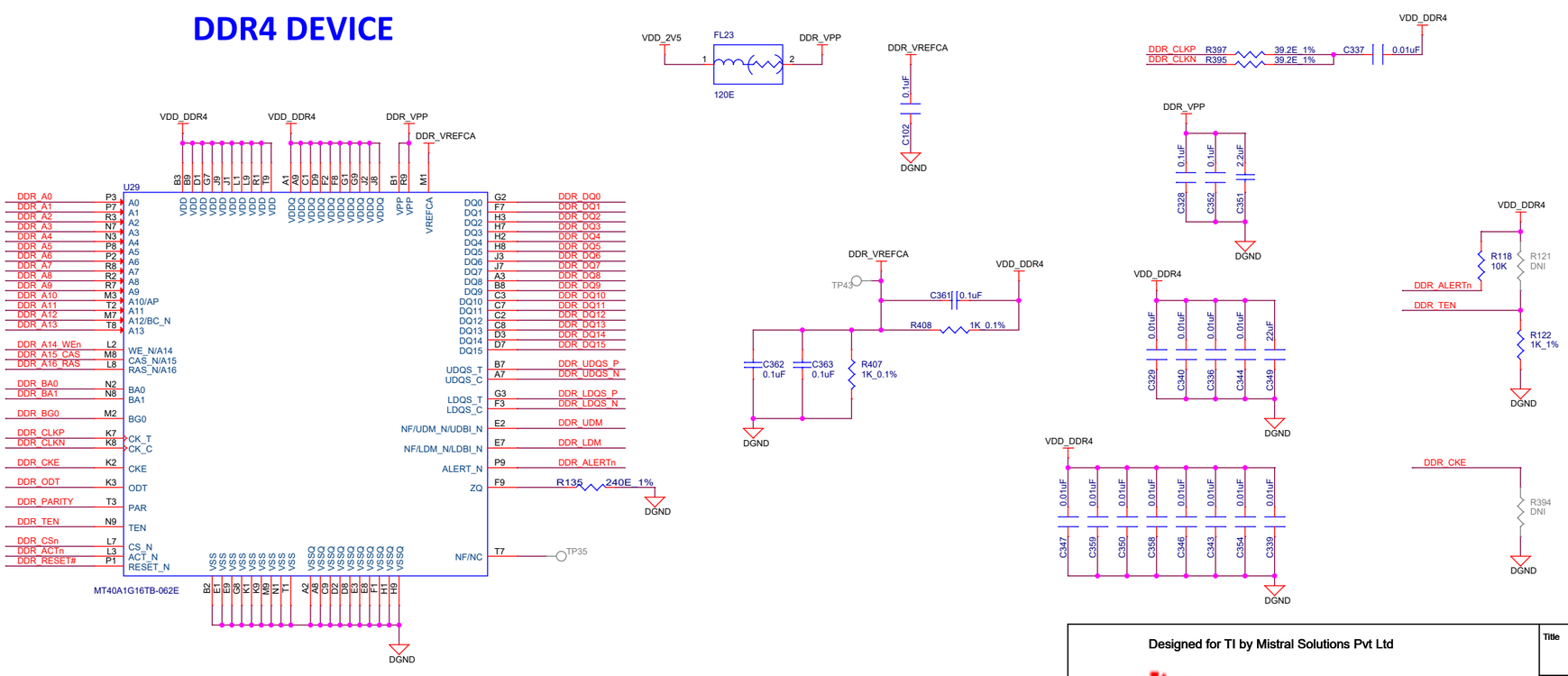
Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC POWER CAPS & SOC VSS	
Size: C	Variant Name = PROC142A(002)	Rev
Date: Tuesday, November 22, 2022	Sheet 15 of 44	

SOC DDR INTERFACE



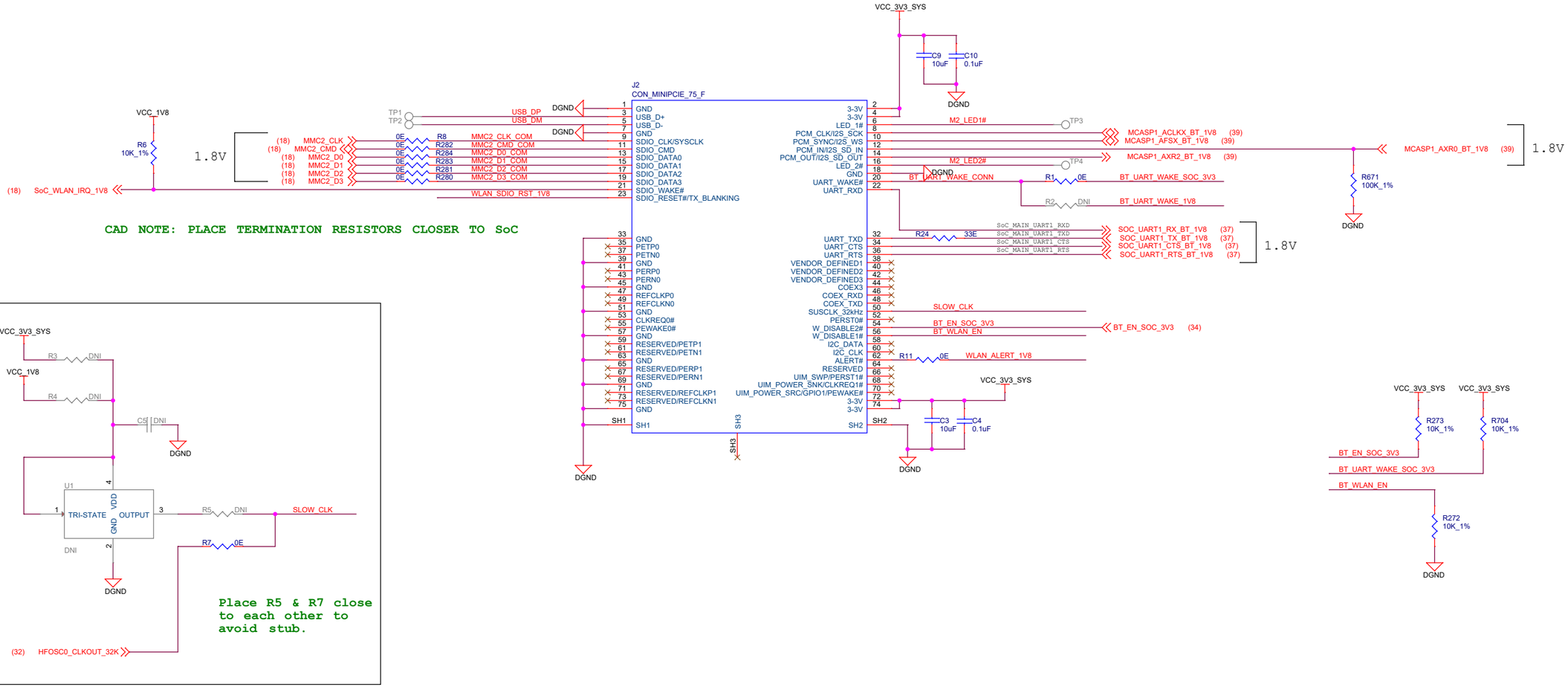
DDR4 DEVICE



Designed for TI by Mistral Solutions Pvt Ltd

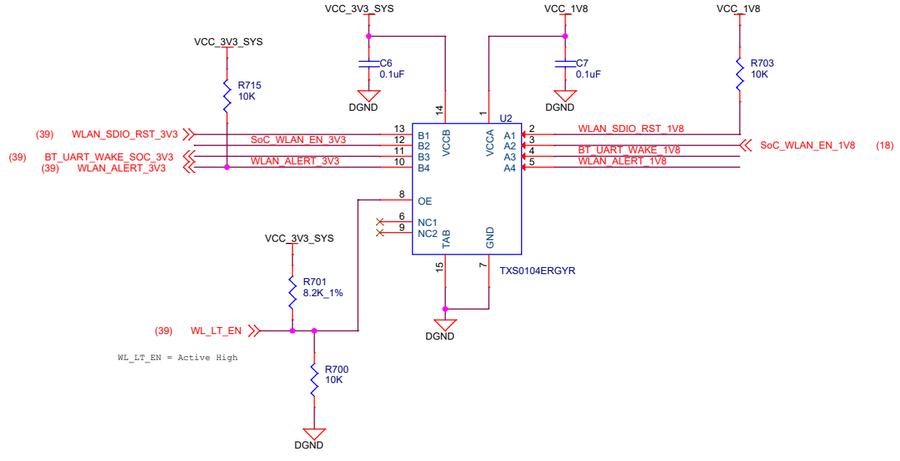
Title	DDR4 Interface	
Size	Variant Name = PROC142A(002)	Rev
C		A
Date:	Tuesday, November 22, 2022	Sheet 16 of 44

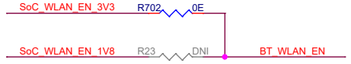
M.2 INTERFACE

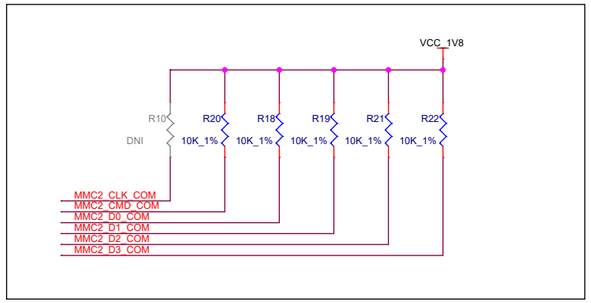


CAD NOTE: PLACE TERMINATION RESISTORS CLOSER TO SoC

Place R5 & R7 close to each other to avoid stub.



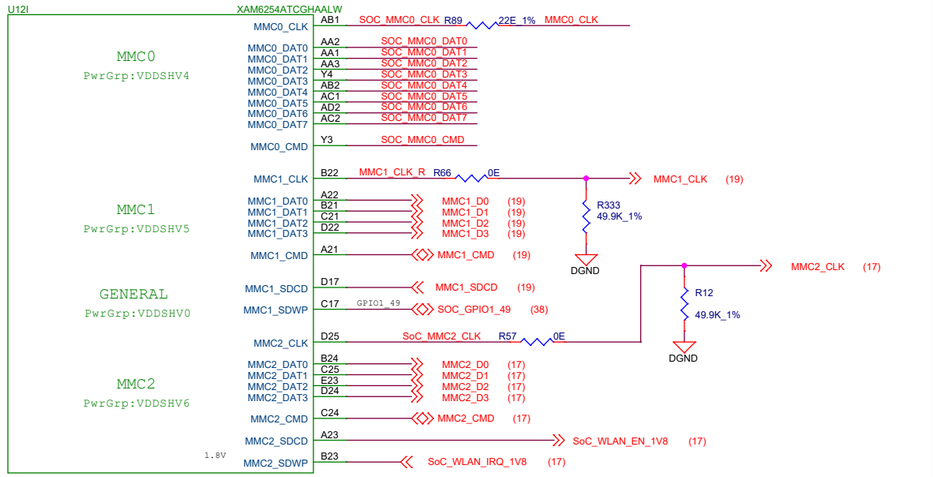




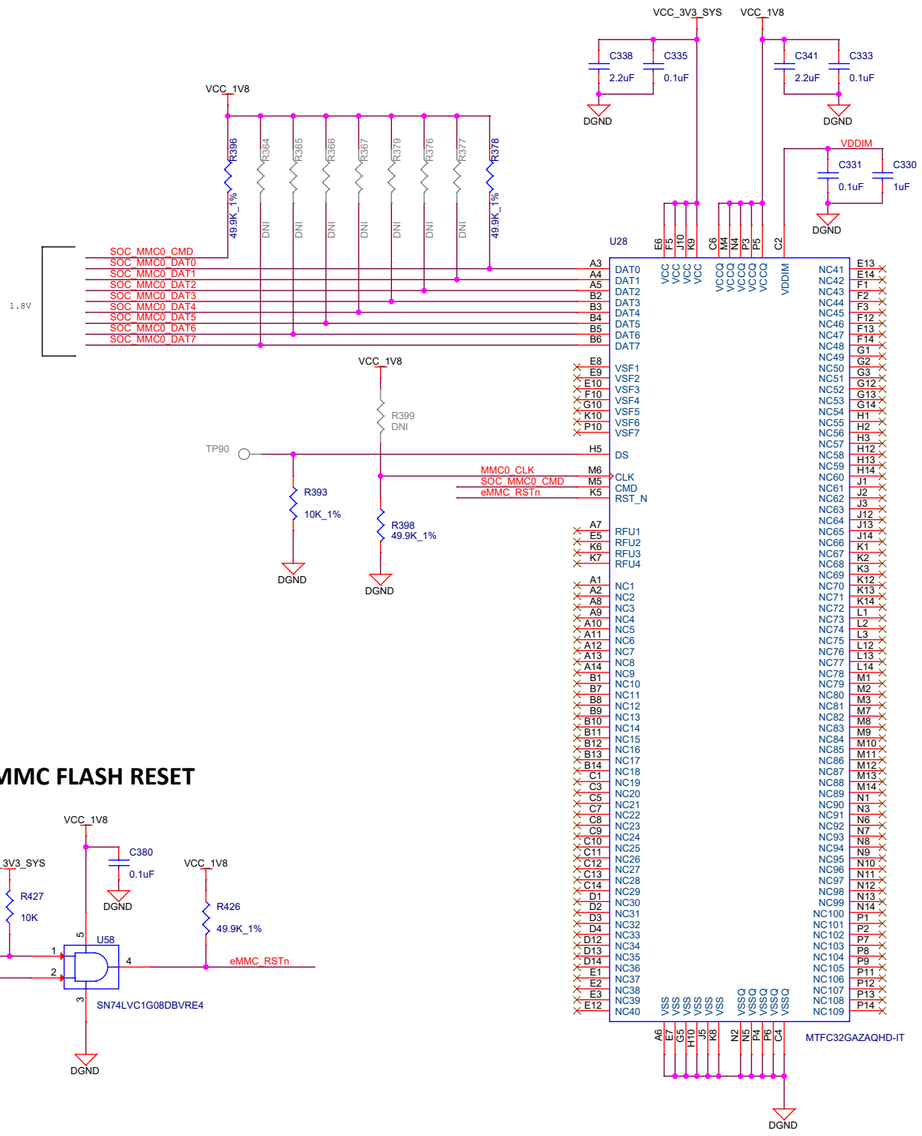
Designed for TI by Mistral Solutions Pvt Ltd

Title	M.2 CONNECTOR	
Size	PROC142A(002)	Rev
C		A
Date:	Tuesday, December 06, 2022	Sheet 17 of 44

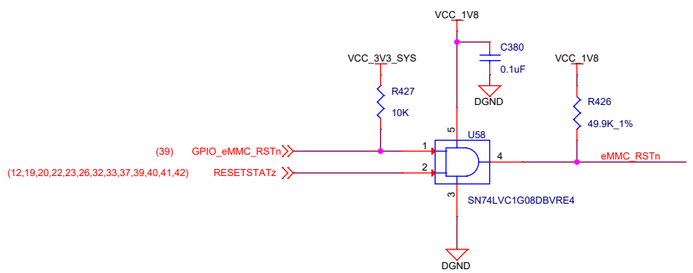
SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET

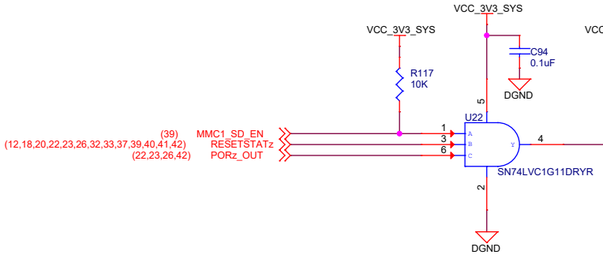


Designed for TI by Mistral Solutions Pvt Ltd

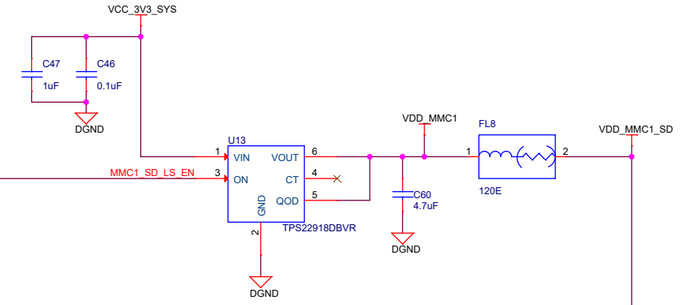
Title	eMMC FLASH INTERFACE	
Size C	PROC142A(002)	Rev A
Date: Tuesday, November 22, 2022	Sheet 18 of 44	

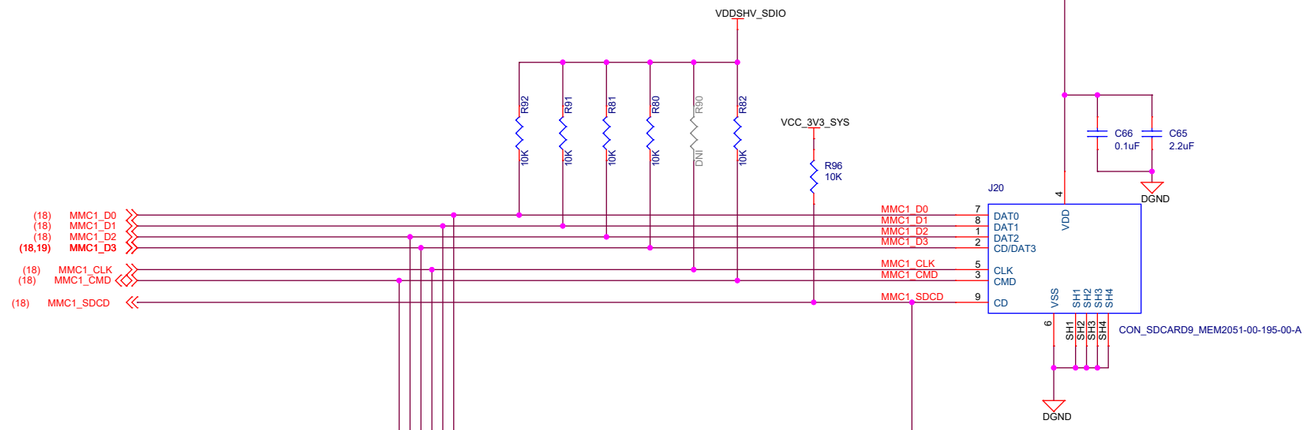
SD CARD INTERFACE

SD CARD RESET



LOAD SWITCH

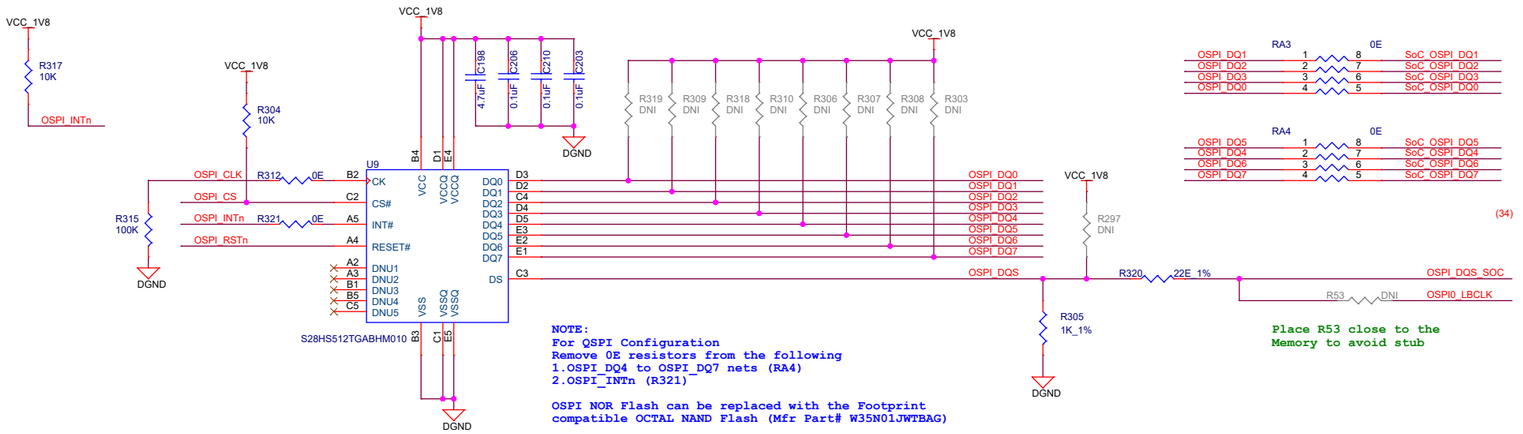




Designed for TI by Mistral Solutions Pvt Ltd

Title	SD CARD INTERFACE	
Size C	PROC142A(002)	Rev A
Date: Tuesday, November 22, 2022	Sheet 19 of 44	

OSPI FLASH

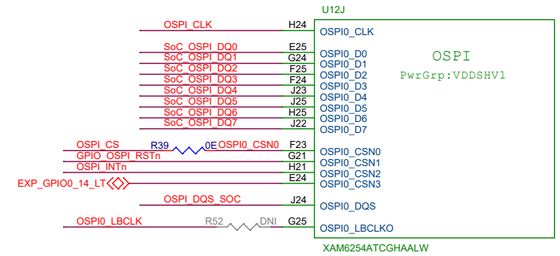


NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA4)
2.OSPI_INTn (R321)

OSPI NOR Flash can be replaced with the Footprint
compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

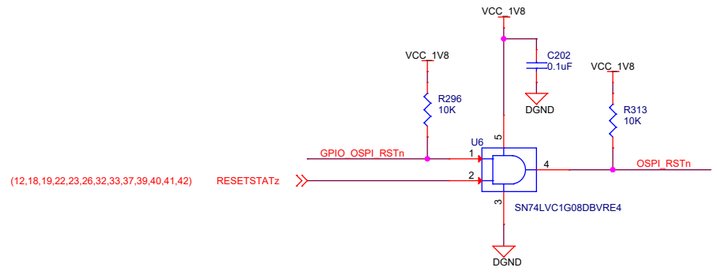
Place R53 close to the
Memory to avoid stub

SOC OSPI INTERFACE



Place R52 close to the SOC Ball
with as little trace as possible

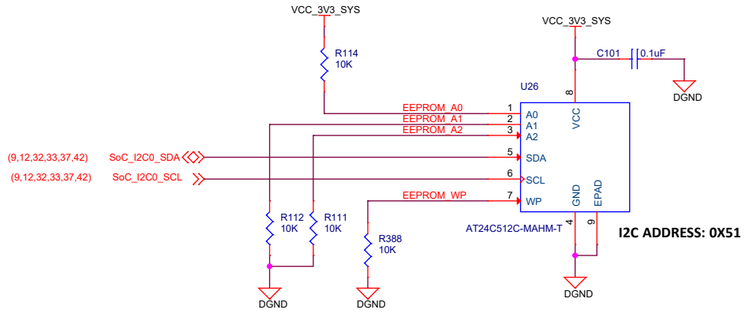
OSPI FLASH RESET



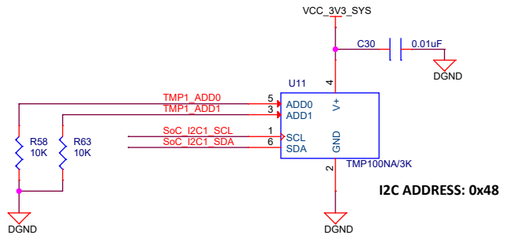
Designed for TI by Mistral Solutions Pvt Ltd

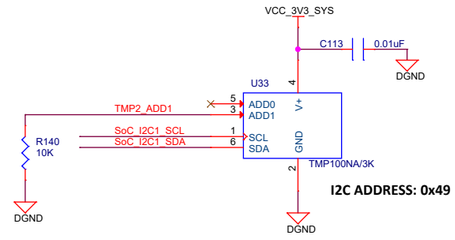
Title	OSPI INTERFACE	
Size: C	PROC142A(002)	Rev: A
Date: Tuesday, November 22, 2022	Sheet 20 of 44	

BOARD ID EEPROM



TEMPERATURE SENSORS





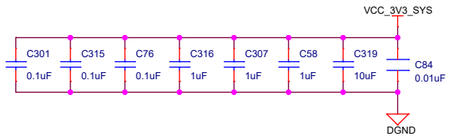
CAD NOTE: PLACE TEMP SENSOR U11 CLOSE TO SoC

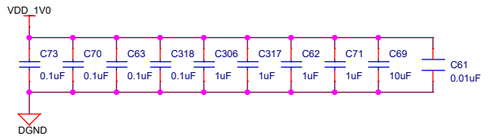
CAD NOTE: PLACE TEMP SENSOR U33 CLOSE TO DDR4

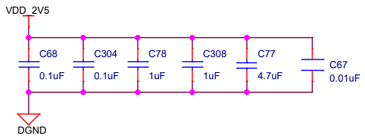
Designed for TI by Mistral Solutions Pvt Ltd

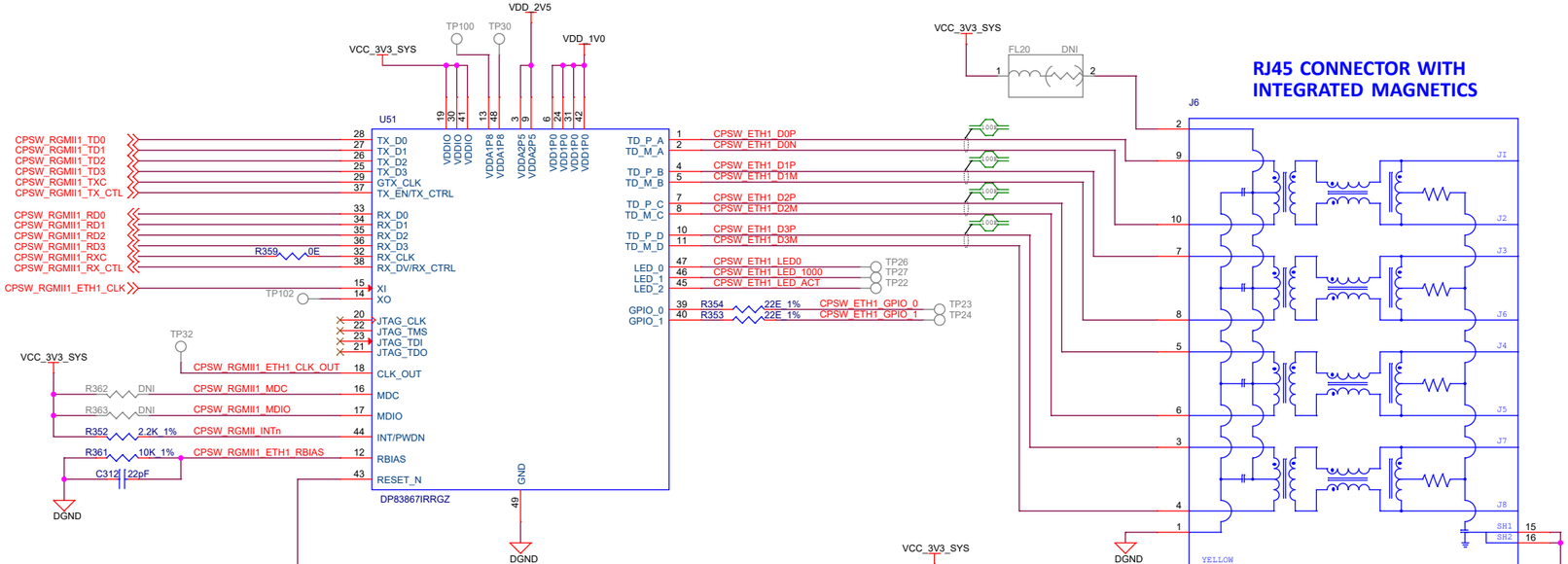
Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size C	PROC142A(002)	Rev A
Date: Tuesday, November 22, 2022	Sheet 21 of 44	

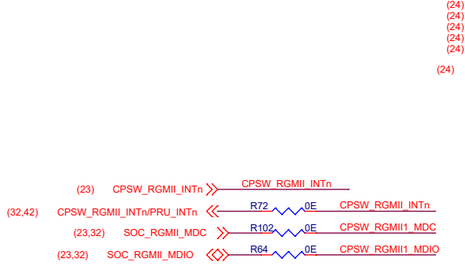
CPSW RGMII 1 - PHY











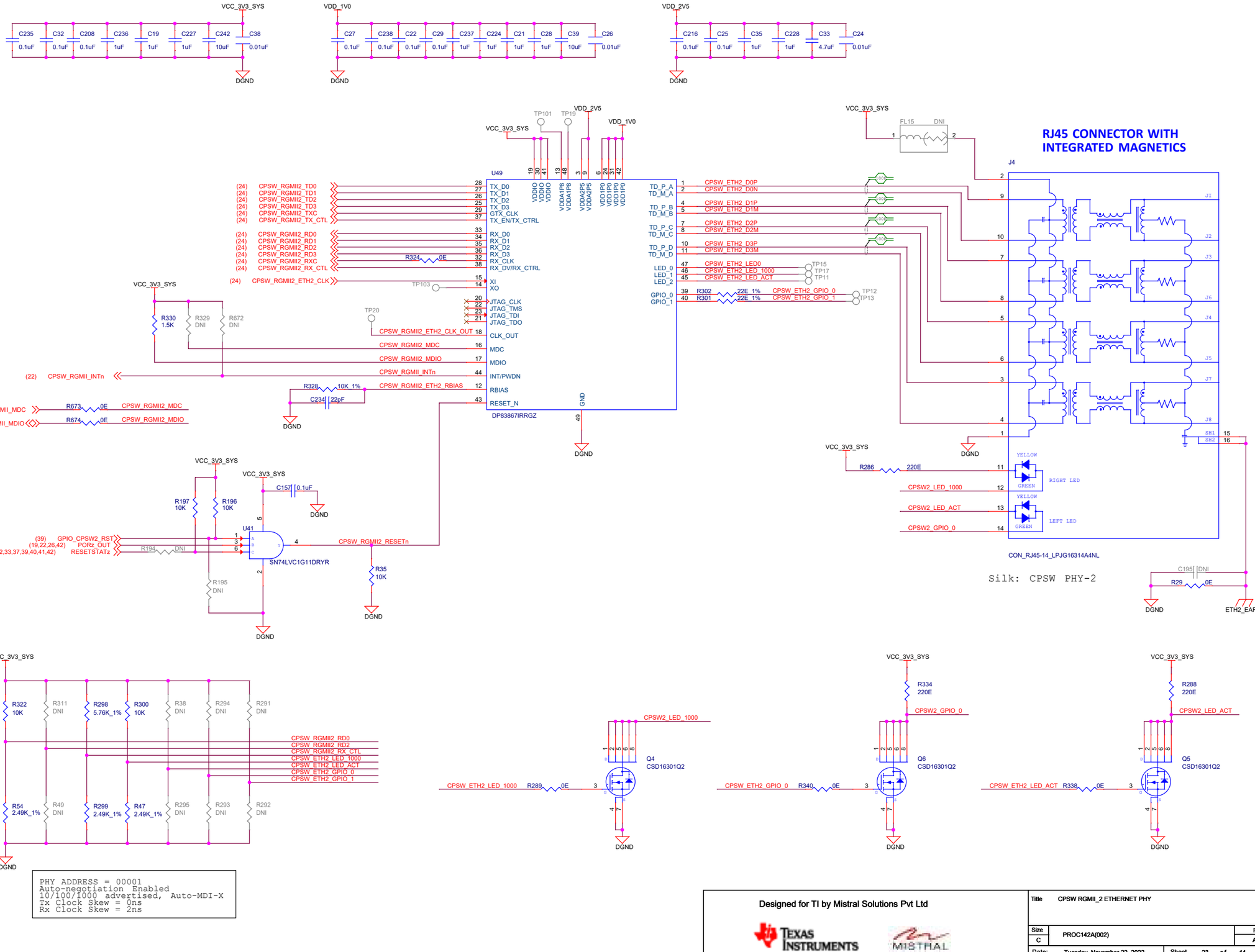
Silk: CPSW PHY-1

```
PHY ADDRESS = 00000
Auto-negotiation  Enabled
10/100/1000  advertised,  Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size: C	PROC142A(002)	Rev: A
Date: Tuesday, November 22, 2022	Sheet 22 of 44	

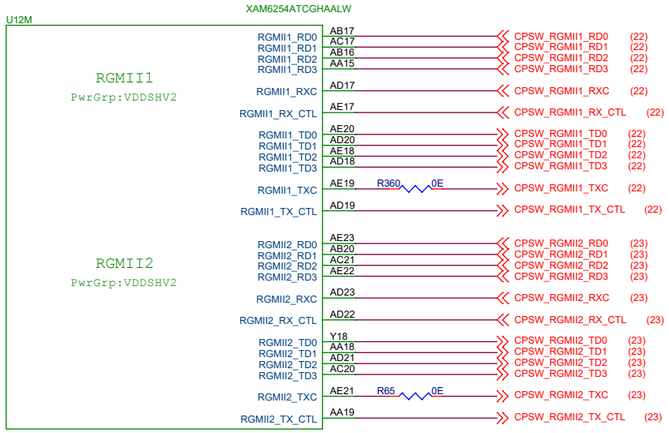
CPSW RGMII 2 - PHY

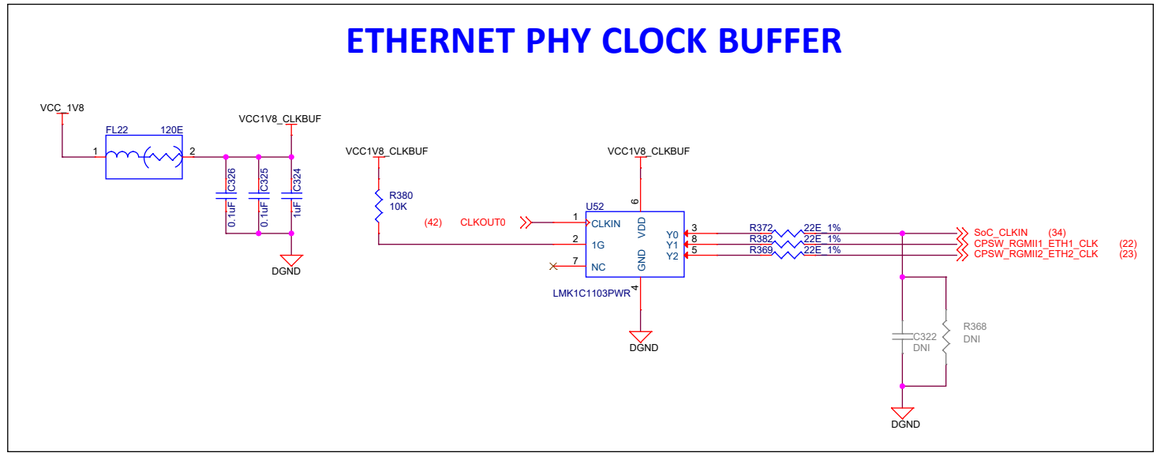


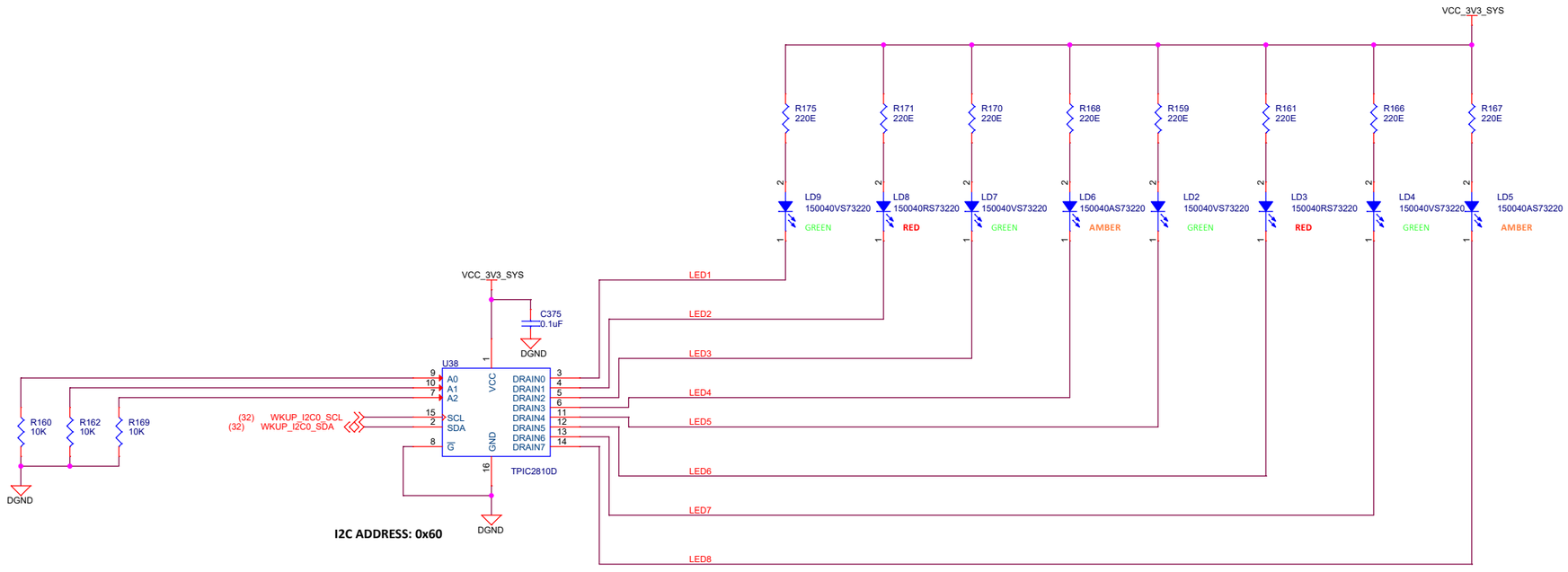
PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_2 ETHERNET PHY	
Size C	PROC142A(002)	Rev A
Date: Tuesday, November 22, 2022	Sheet 23 of 44	



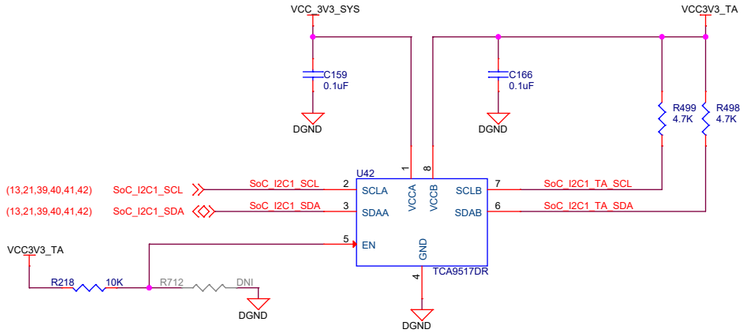




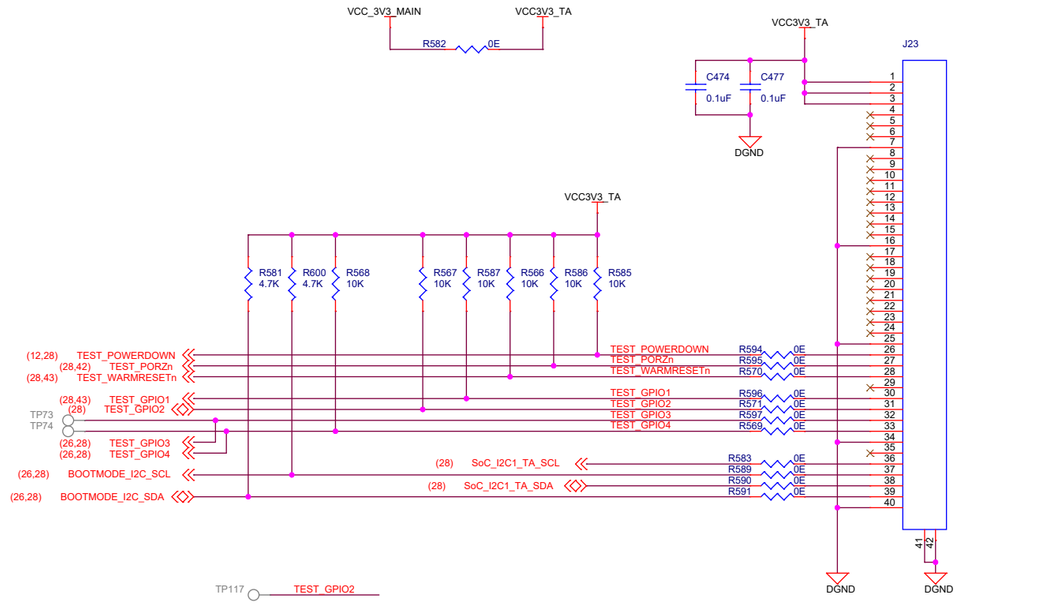
Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC142A(002)	Rev A
Date: Tuesday, November 22, 2022	Sheet 24 of 44	

I2C BUS BUFFER



40-PIN TEST AUTOMATION HEADER



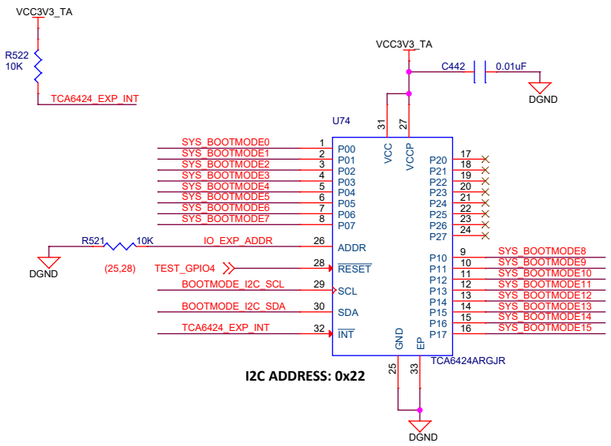
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to a Testpoint	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

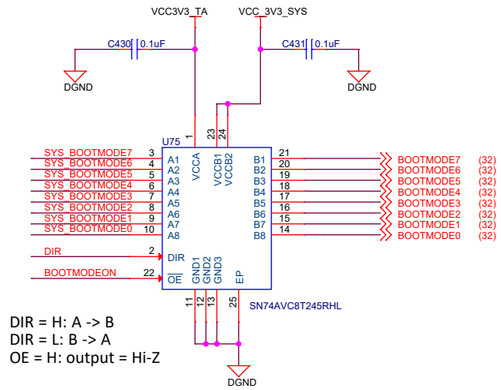
Designed for TI by Mistral Solutions Pvt Ltd

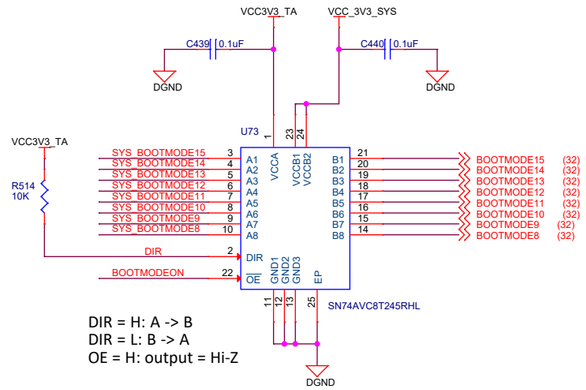
Title	TEST AUTOMATION		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 25 of 44	

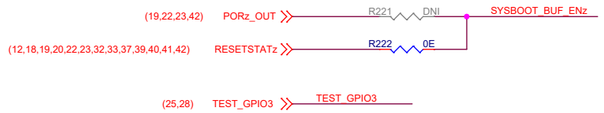
BOOTMODE IO EXPANDER

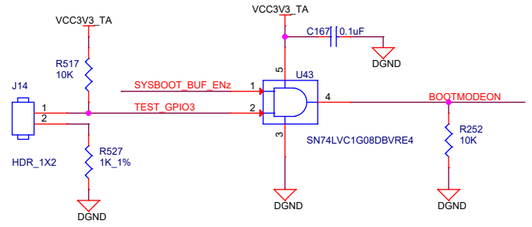


BOOT MODE BUFFERS

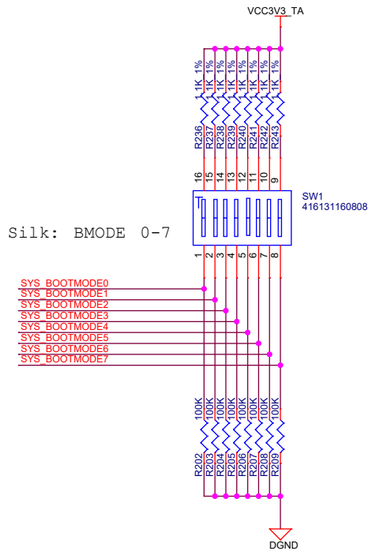




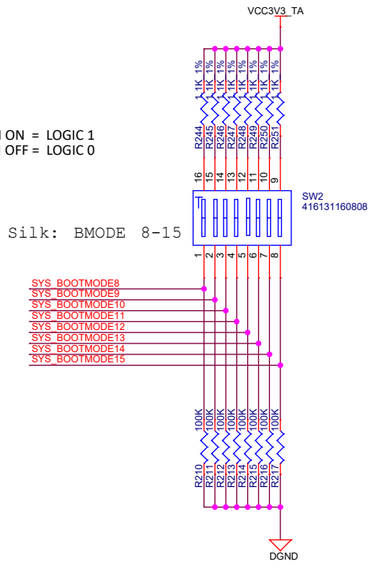




BOOT MODE SWITCHES



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 26 of 44	

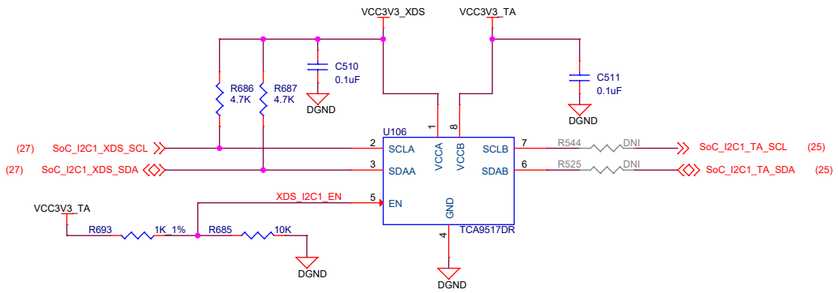
XDS110 DEBUGGER

Silk: JTAG

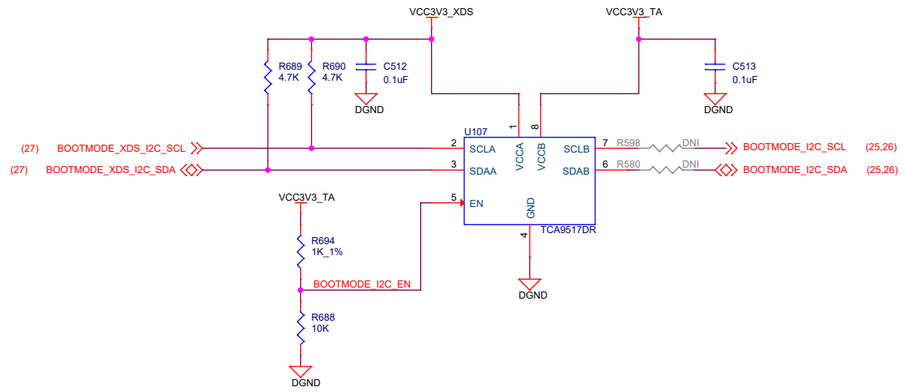
Sets the unique ID of the Debugger

Designed for TI by Mistral Solutions Pvt Ltd	Title: XDS110 DEBUGGER	
	Size: C	PROC142A(002) — Rev: A
	Date: Tuesday, November 22, 2022	Sheet 27 of 44

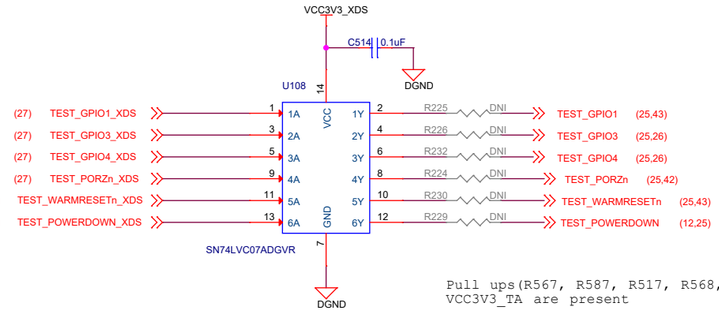
I2C_TA BUS BUFFER



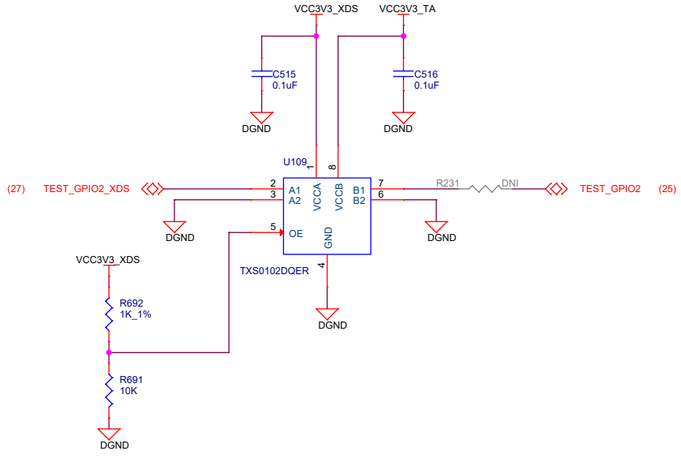
BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



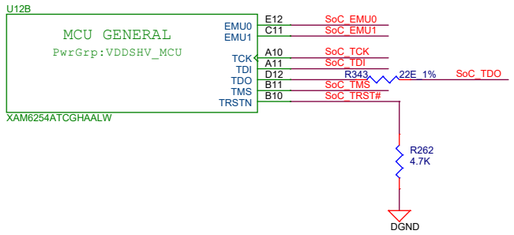
Pull ups(R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present

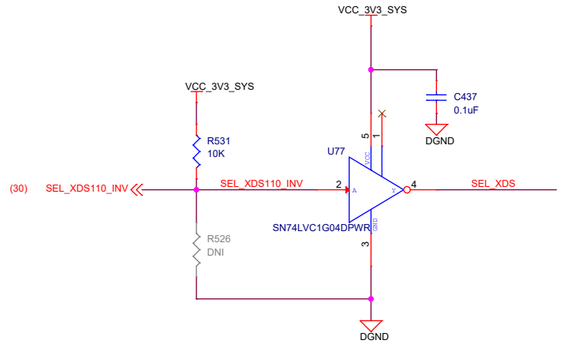


Designed for TI by Mistral Solutions Pvt Ltd

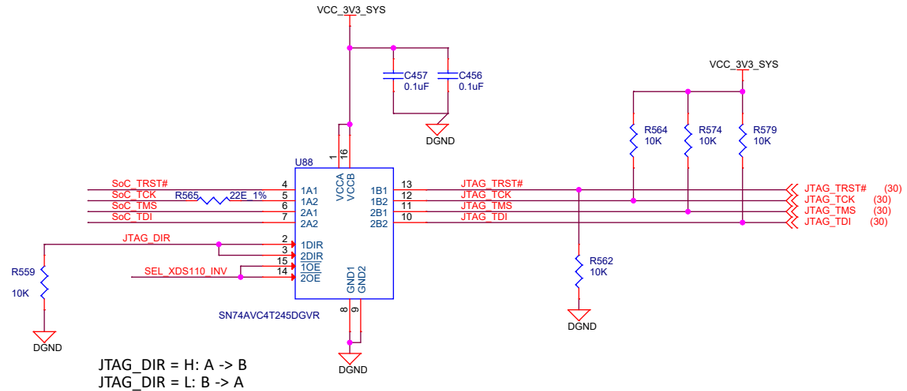
Title	AUTOMATION SIGNALS BUFFER		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 28 of 44	

JTAG SOC SECTION

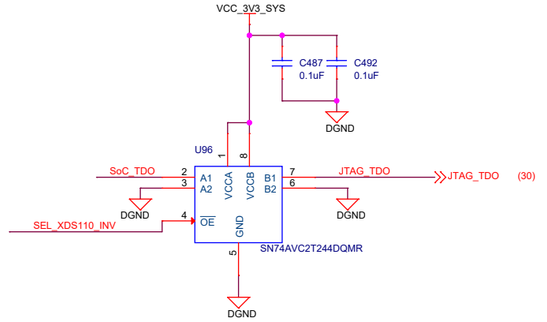




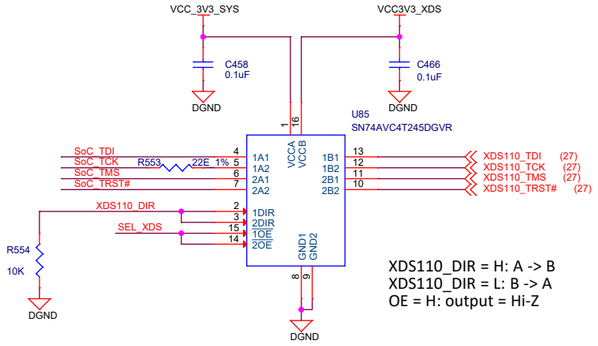
cTI20 JTAG BUFFERS



JTAG_DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

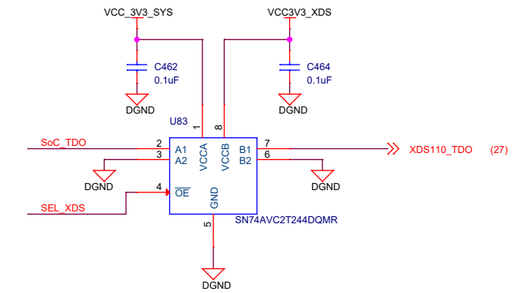


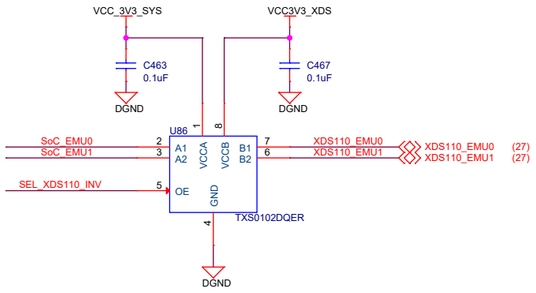
BUFFER XDS110

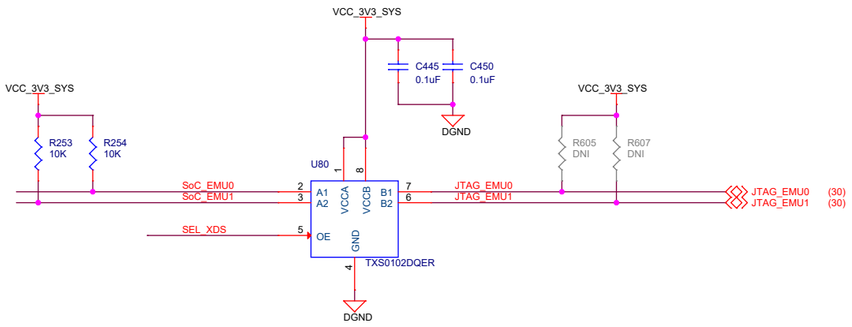


XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

CAD NOTE: Buffers U88 and U96 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.



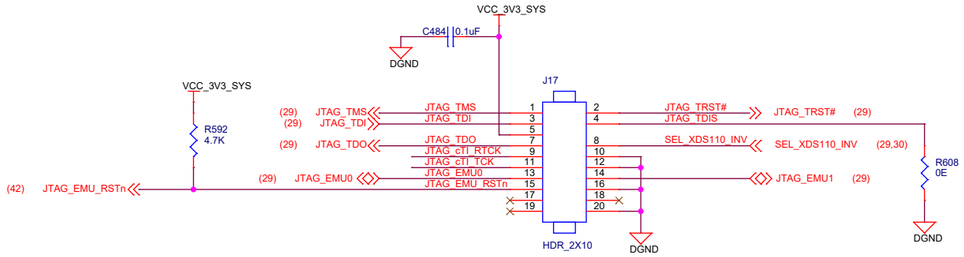




Designed for TI by Mistral Solutions Pvt Ltd

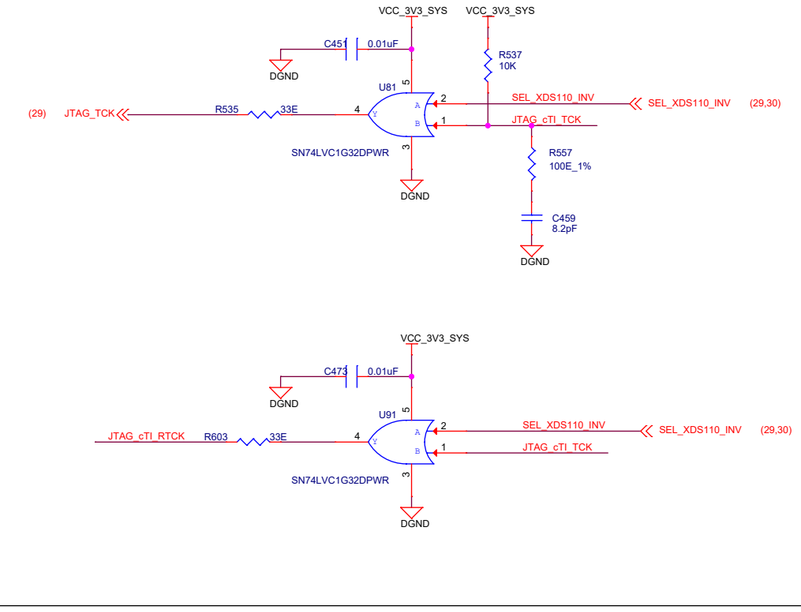
Title	JTAG BUFFER		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 29 of 44	

JTAG 20 PIN cTI CONNECTOR



Silk: cTI

JTAG CLOCK BUFFER

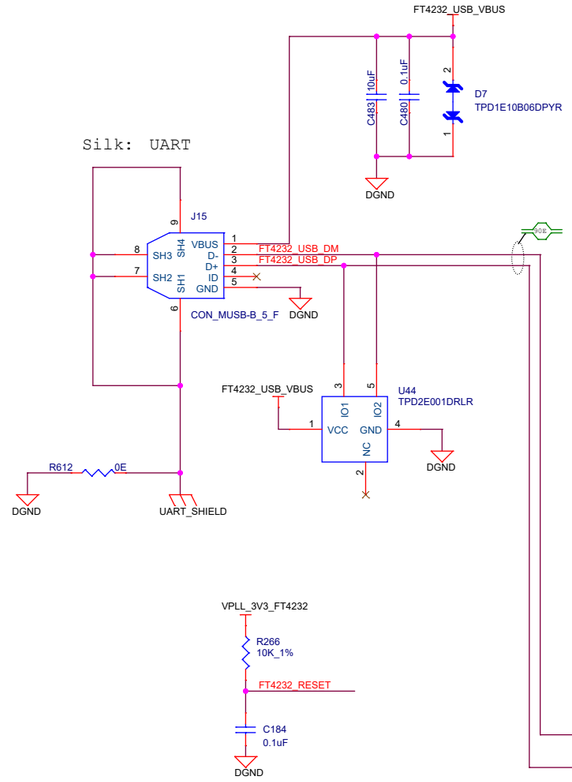


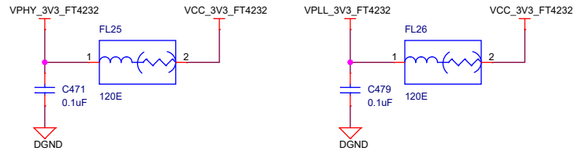
Designed for TI by Mistral Solutions Pvt Ltd

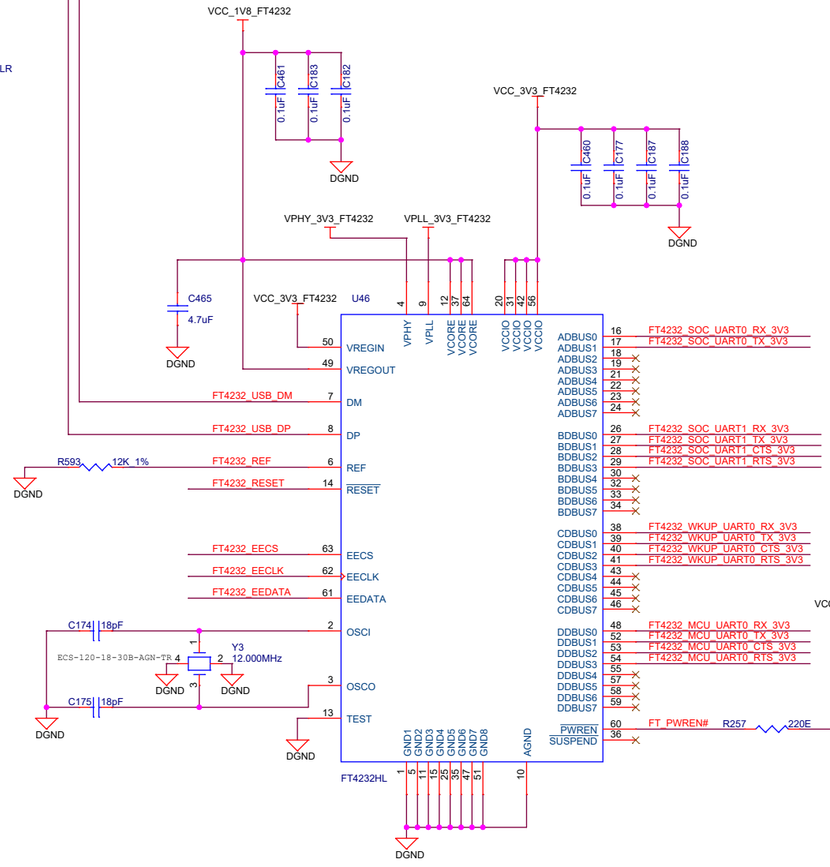
Title	JTAG 20 PIN cTI CONNECTOR	
Size: C	PROC142A(002)	Rev: A
Date: Tuesday, November 22, 2022	Sheet 30 of 44	

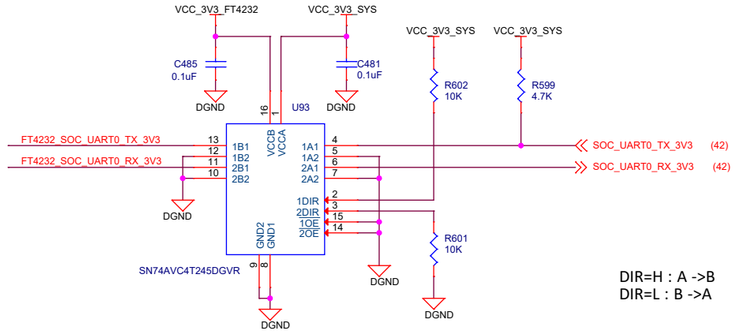
FT4232 UART

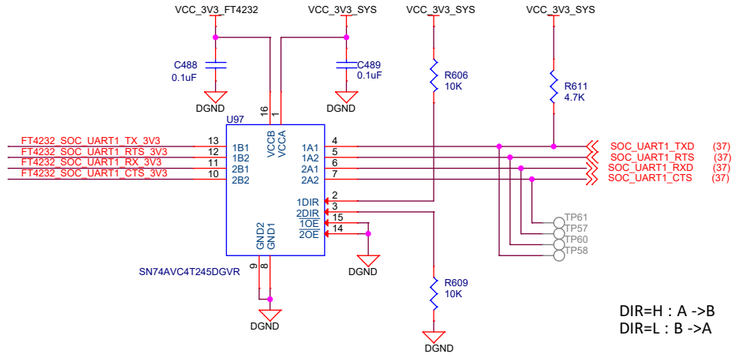
Silk: UART

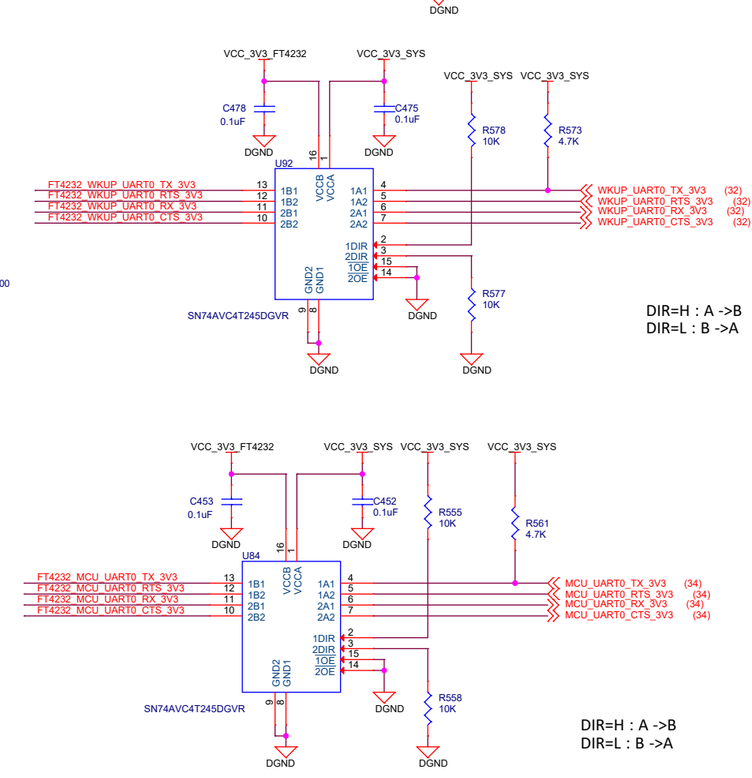




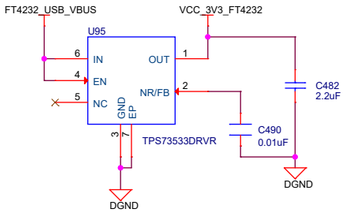




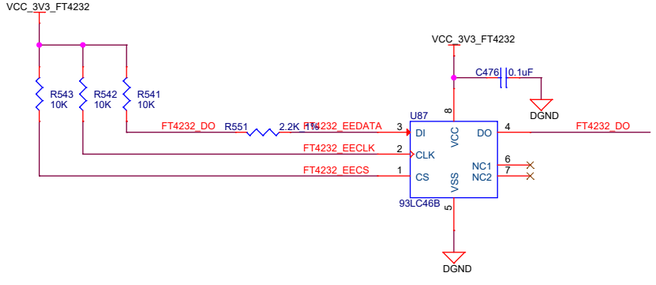




FT4232: 5V to 3.3V@500mA LDO



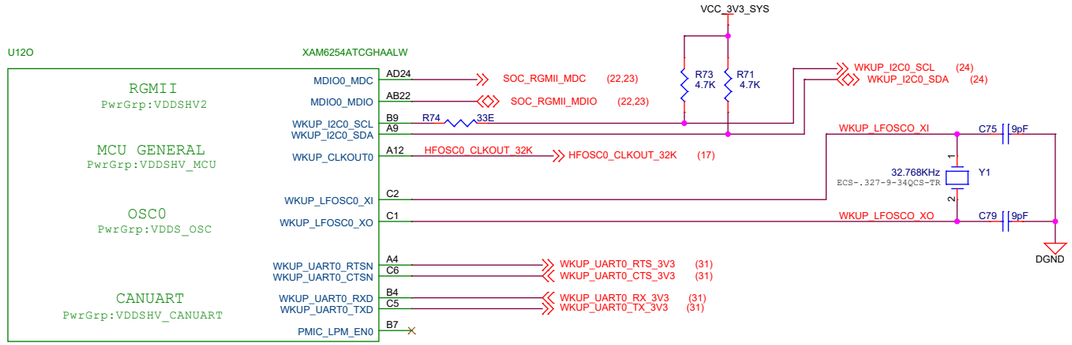
EEPROM



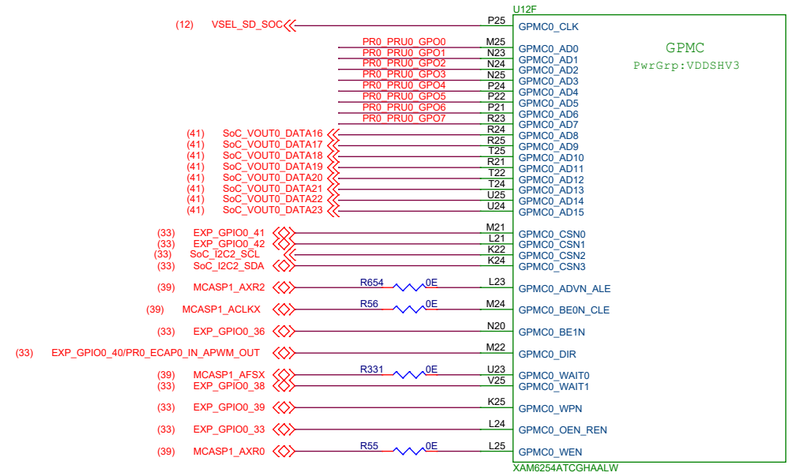
Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 31 of 44	

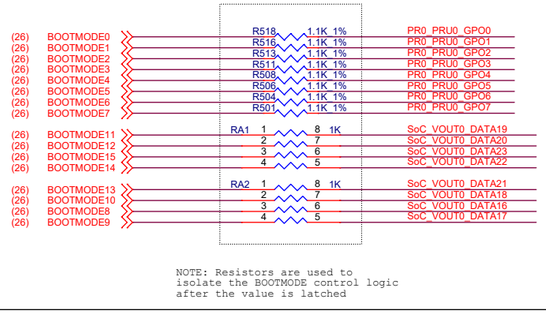
SOC WKUP DOMAIN



SOC GPMC

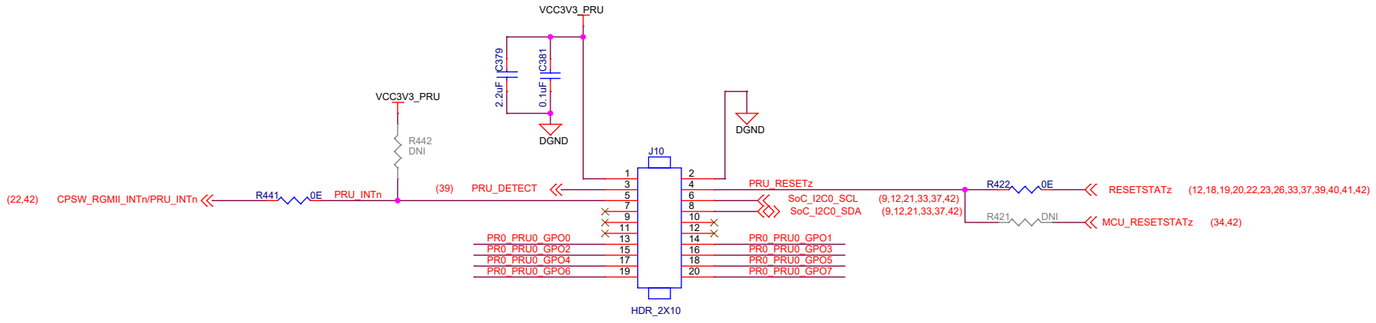


BOOTMODE PINS



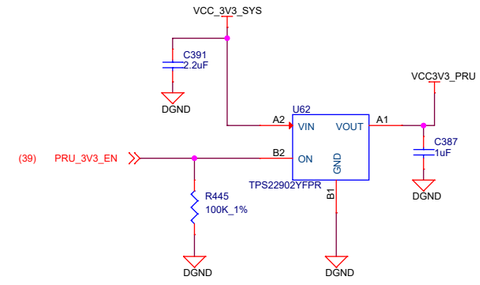
NOTE: Resistors are used to isolate the BOOTMODE control logic after the value is latched

PRU HEADER



Silk: PRU HDR

POWER SWITCH FOR PRU HEADER



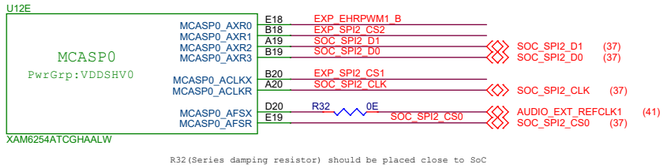
3V3 supply of PRU Header is limited to sourcing 500mA max.

NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

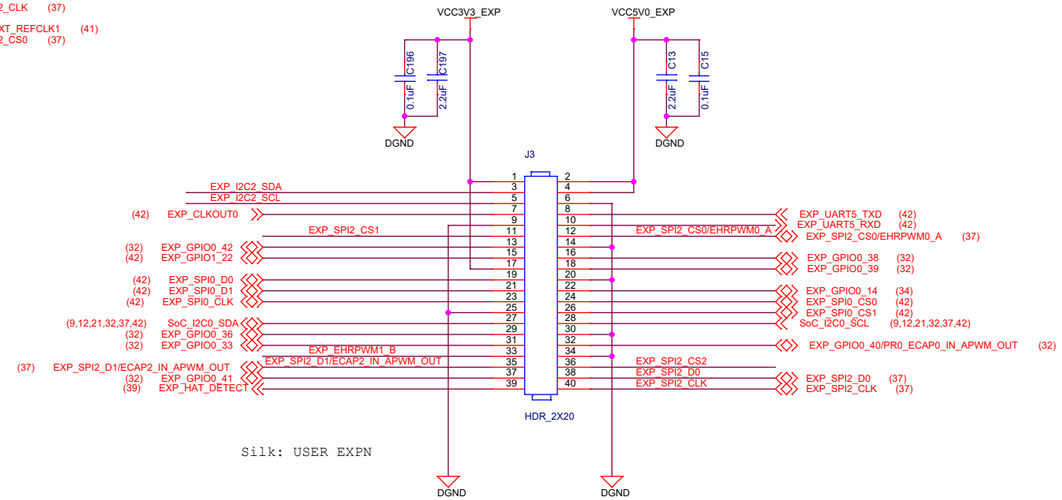
Designed for TI by Mistral Solutions Pvt Ltd

Title	PRU HEADER	
Size	PROC142A(002)	Rev A
Date:	Tuesday, November 22, 2022	Sheet 32 of 44

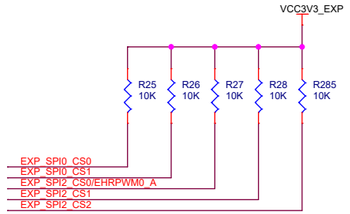
USER EXPANSION CONNECTOR



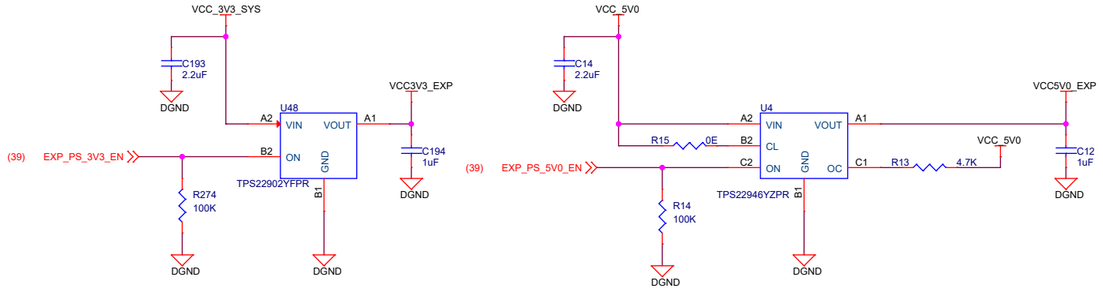
R32(Series damping resistor) should be placed close to SoC



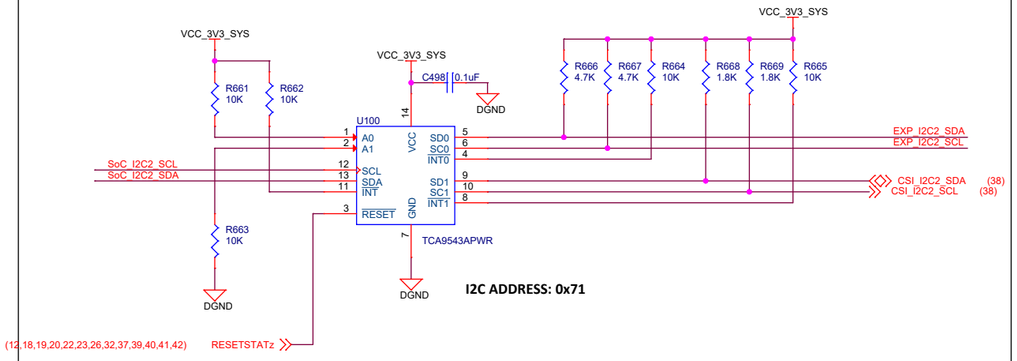
Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2



NOTE:

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

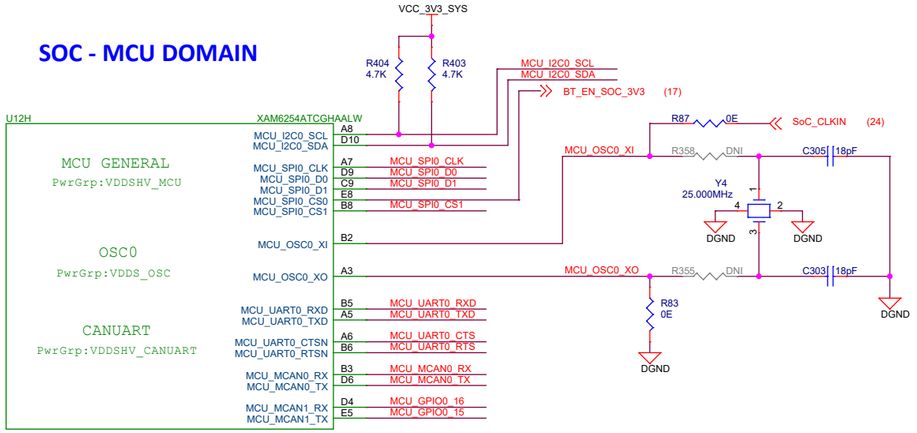
5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

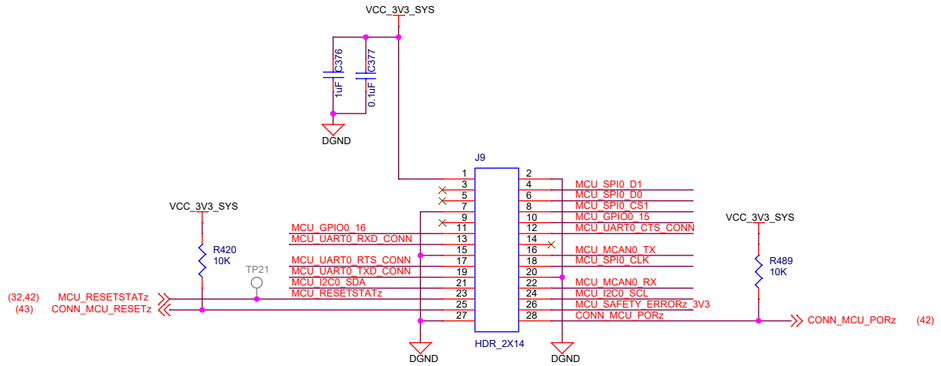
Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, December 06, 2022	Sheet 33 of 44	

SOC - MCU DOMAIN

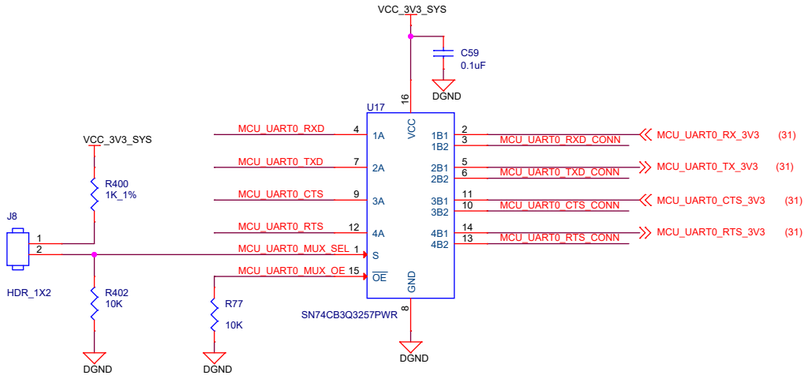


MCU HEADER

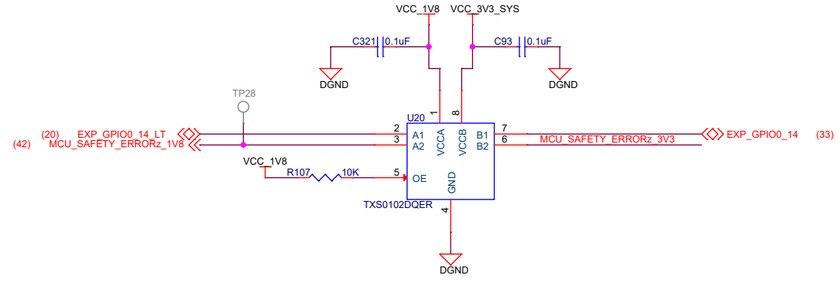


Silk: MCU HDR

MCU_UART0 MUX



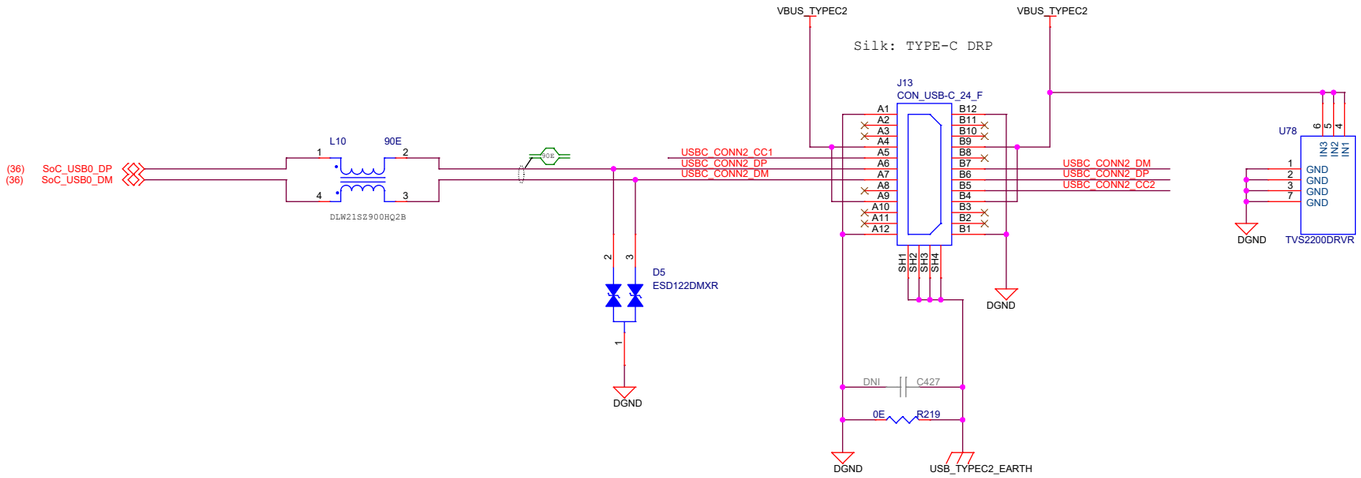
OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

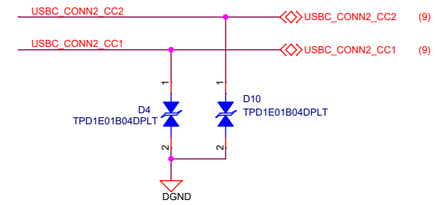


Designed for TI by Mistral Solutions Pvt Ltd

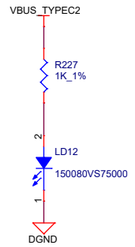
Title	MCU HEADER		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 34 of 44	

USB0 TYPE-C DRP

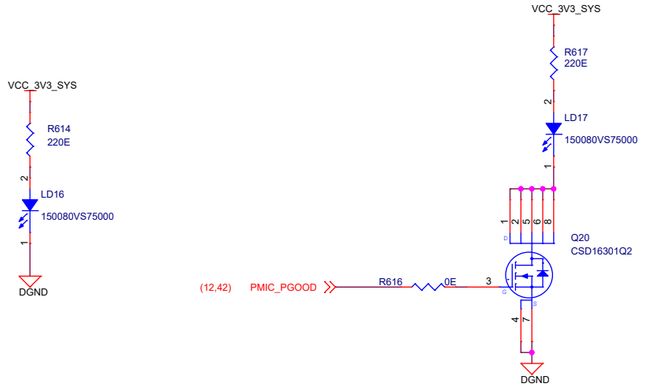




POWER INDICATION LED: VBUS_TYPEC2



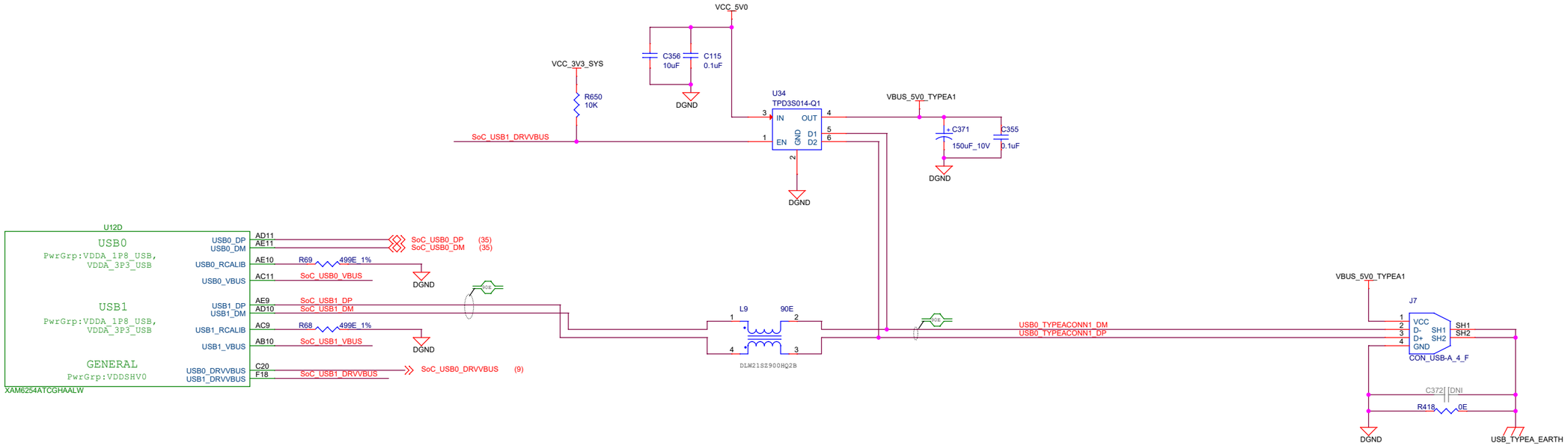
POWER RAIL LEDS



Designed for TI by Mistral Solutions Pvt Ltd

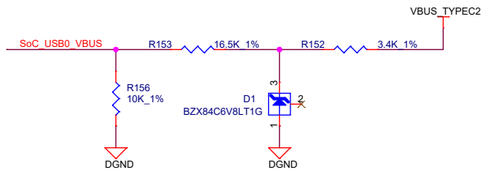
Title	USB0 TYPE-C DRP	
Size	PROC142A(002)	Rev
C		A
Date:	Tuesday, November 22, 2022	Sheet 35 of 44

USB1 TYPE-A

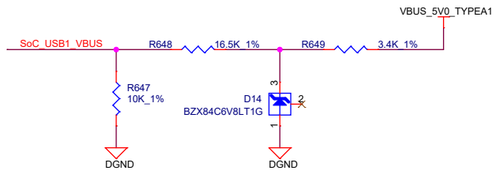


Silk: TYPE-A

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



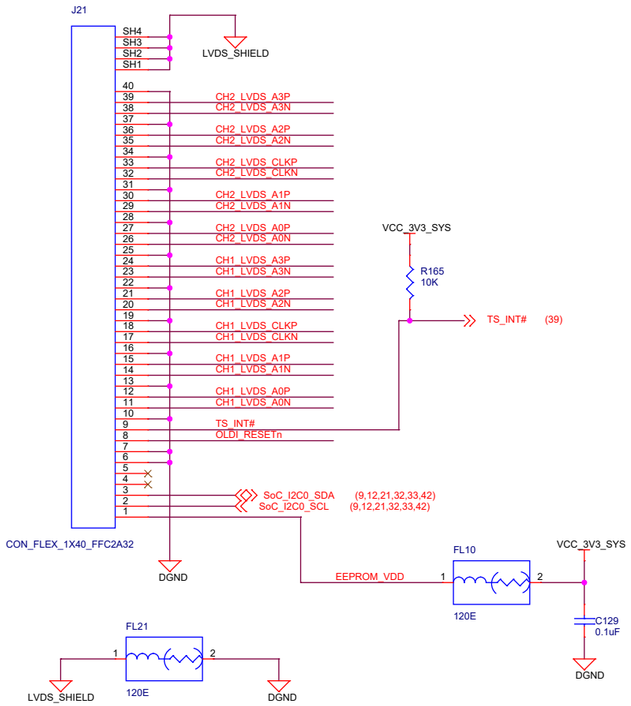
Note: Recommended VBUS circuit for SoC_USB1_VBUS

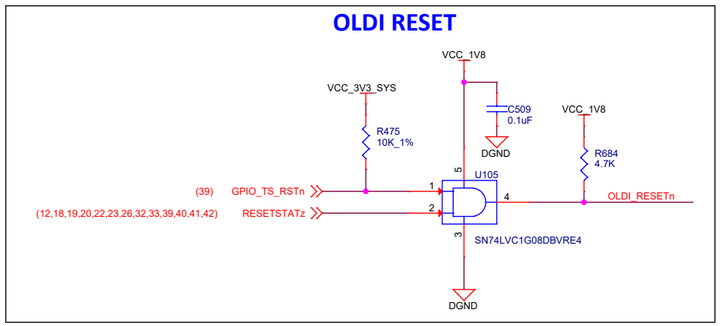


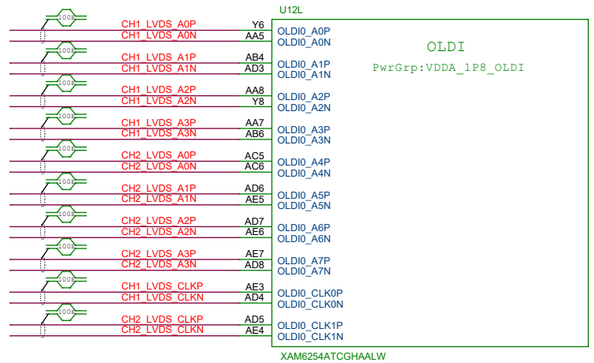
Designed for TI by Mistral Solutions Pvt Ltd

Title	USB1 TYPE-A		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 36 of 44	

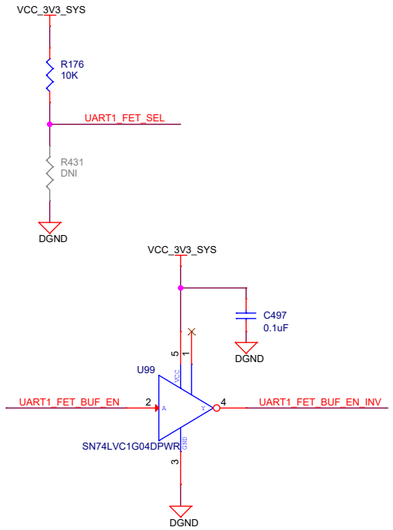
OLDI DISPLAY INTERFACE

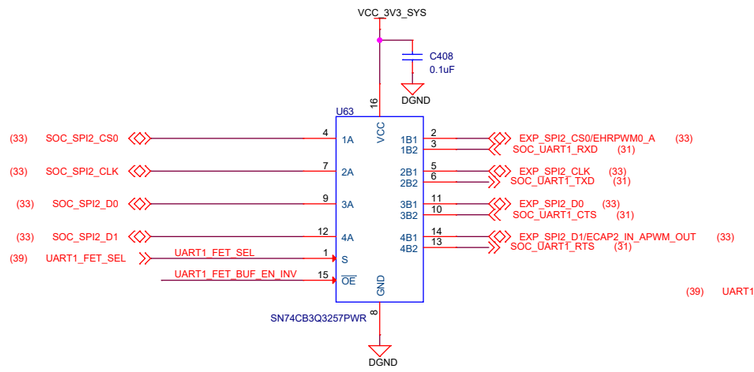


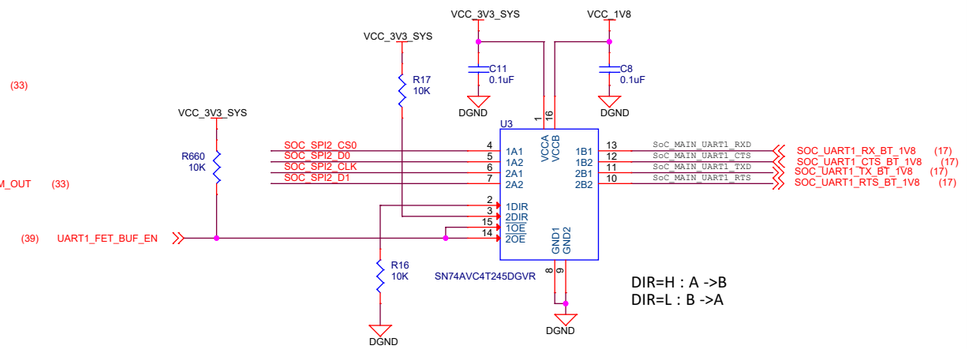




SoC UART1 FET SWITCH & BUFFER







OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	FT4232
L	L	An=nB1	EXP CONN

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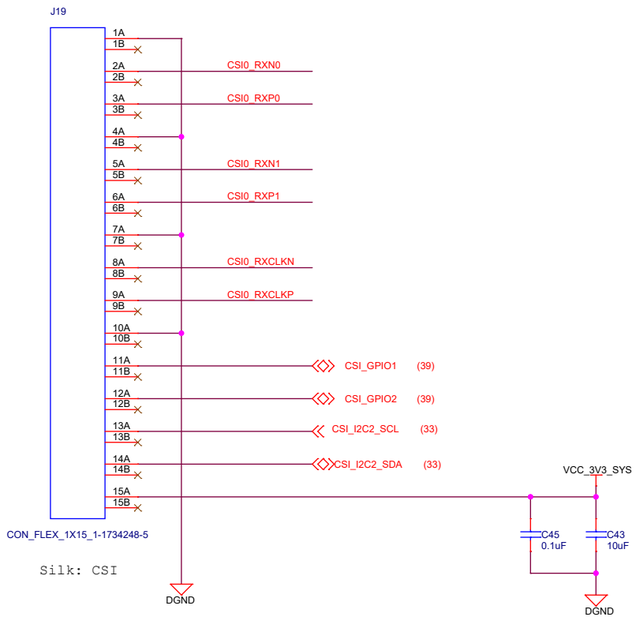
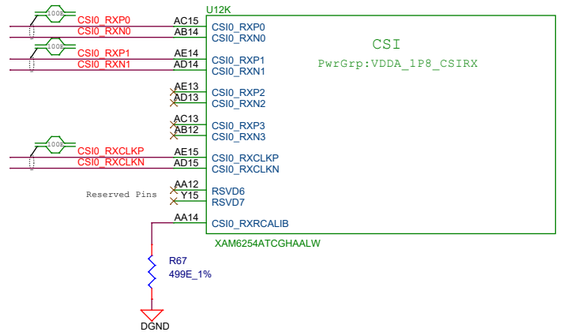
Title	OLDI DISPLAY INTERFACE		
Size	PROC142A(002)		Rev
C			A
Date:	Tuesday, November 22, 2022	Sheet 37 of 44	

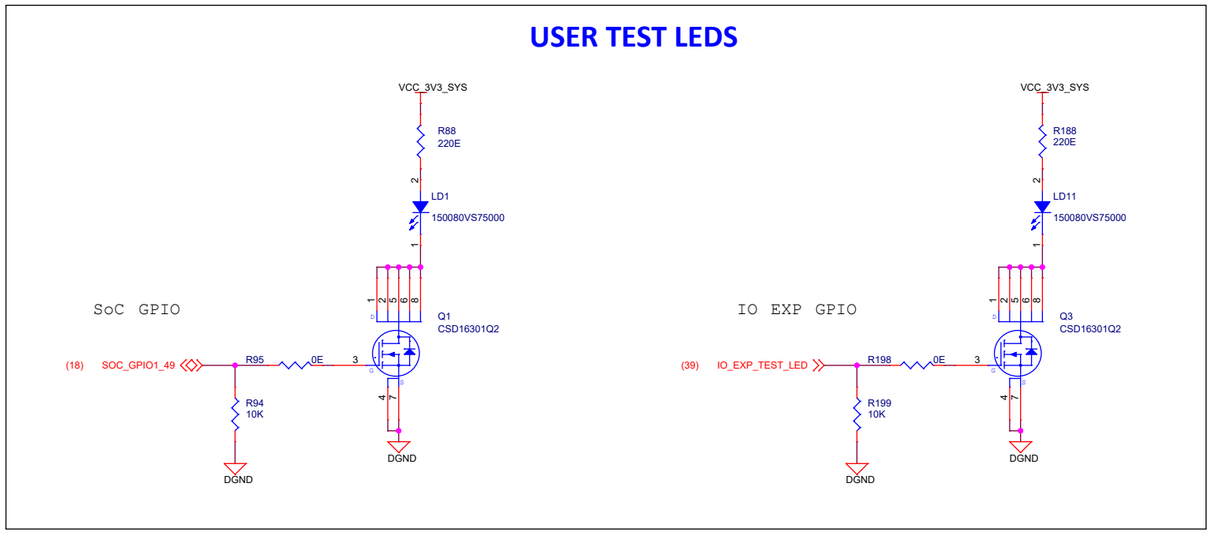
CSI INTERFACE

CSI CAMERA HEADER





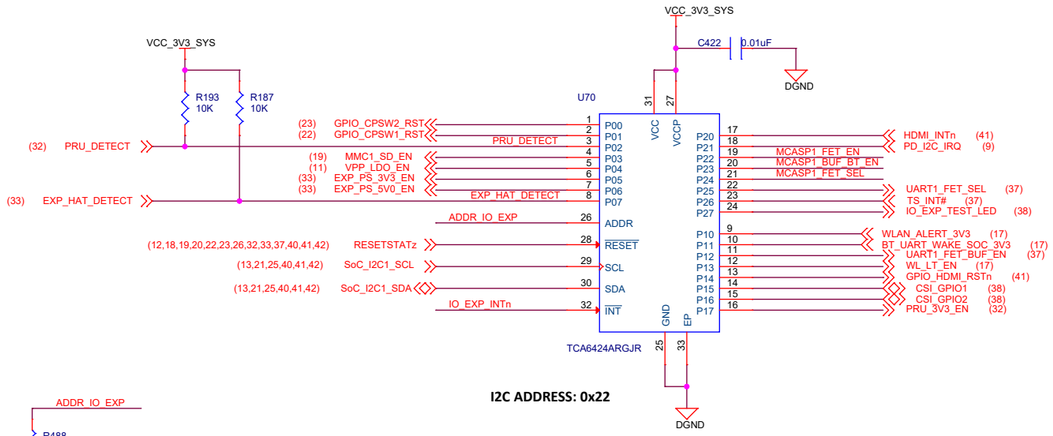
USER TEST LEDS

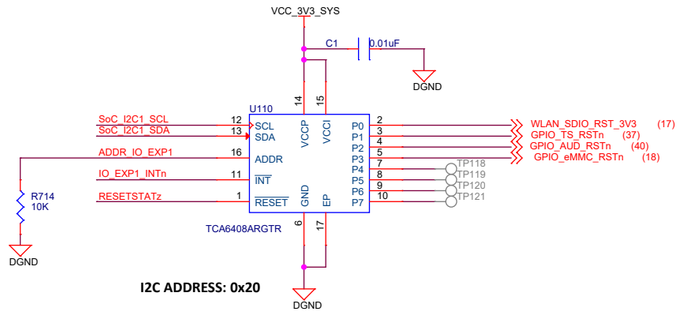


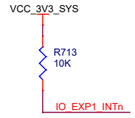
Designed for TI by Mistral Solutions Pvt Ltd

Title	CSI INTERFACE & USER TEST LEDS	
Size C	PROC142A(002)	Rev A
Date: Tuesday, November 22, 2022	Sheet 38 of 44	

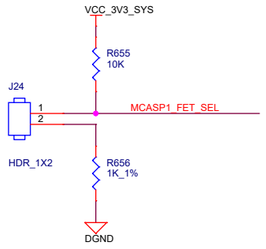
IO EXPANDERS

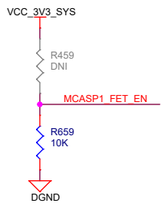


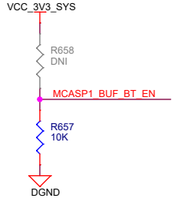


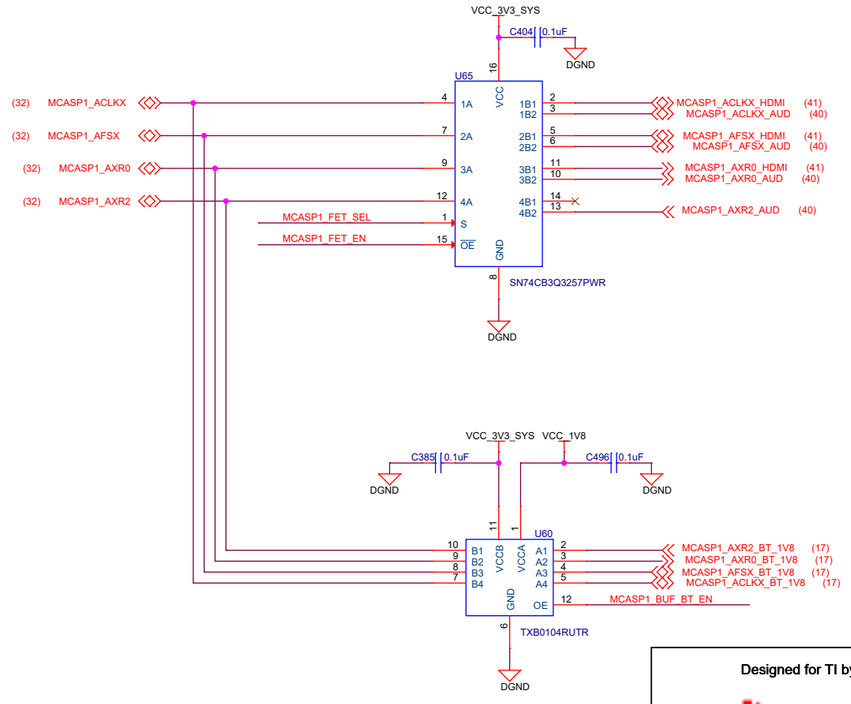


MCASP1 FET SWITCH & BUFFER









OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title	IO EXPANDER	
Size C	PROC142A(002)	Rev A
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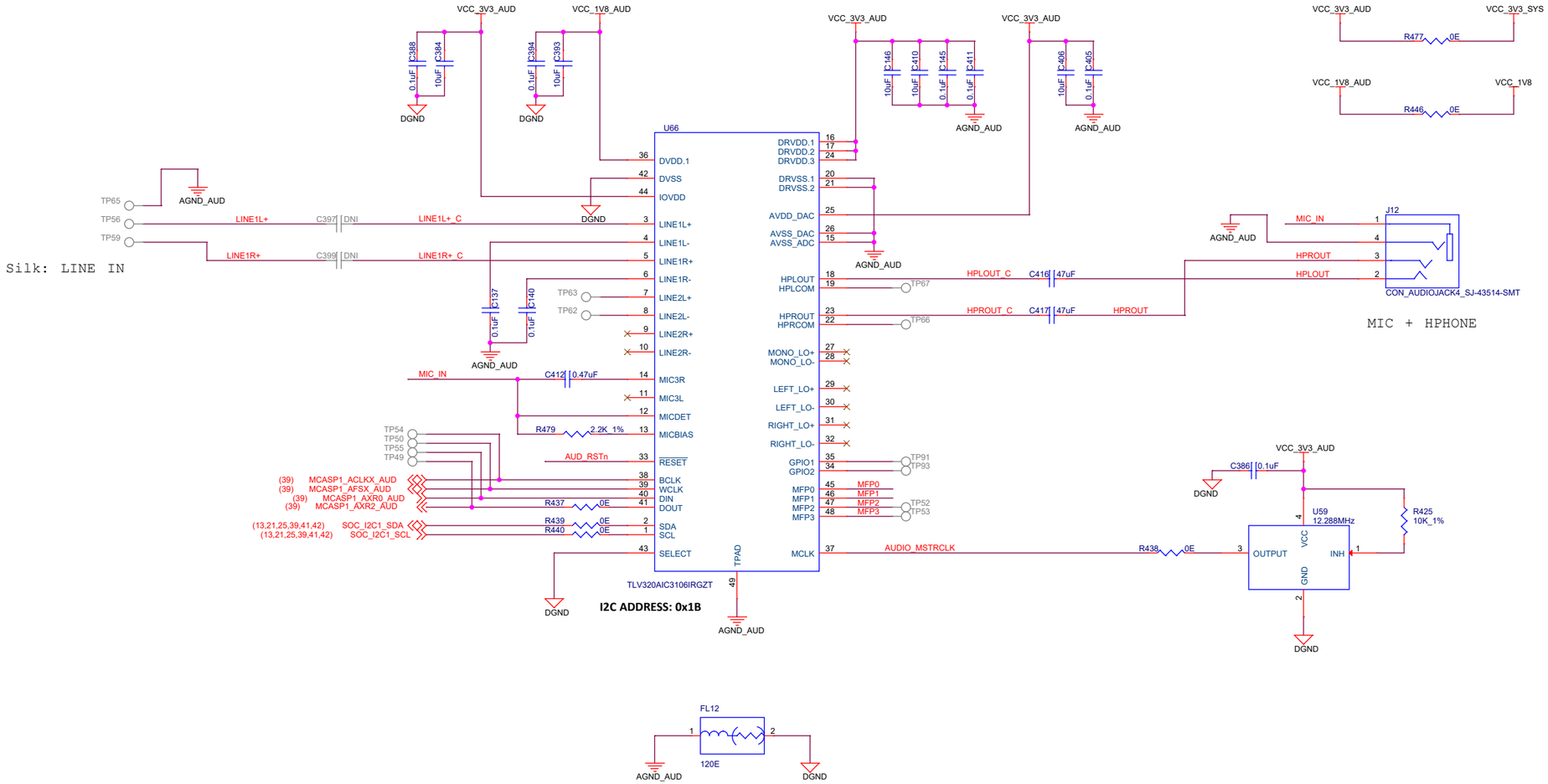
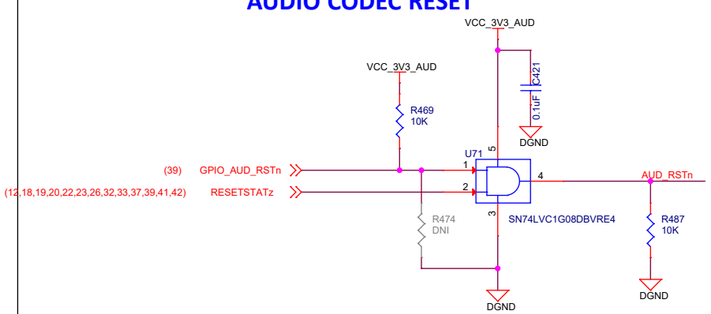
AUDIO CODEC

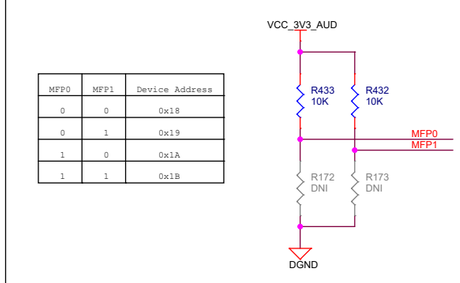


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO CODEC		
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HDMI INTERFACE

U12N — XAM6254ATCGHAALW — VOUT0 (PwrGrp:VDDSHV3)

VOUT0_DATA0	U22	SoC_VOUT0_DATA0
VOUT0_DATA1	V24	SoC_VOUT0_DATA1
VOUT0_DATA2	W25	SoC_VOUT0_DATA2
VOUT0_DATA3	W24	SoC_VOUT0_DATA3
VOUT0_DATA4	Y25	SoC_VOUT0_DATA4
VOUT0_DATA5	Y24	SoC_VOUT0_DATA5
VOUT0_DATA6	Y23	SoC_VOUT0_DATA6
VOUT0_DATA7	AA25	SoC_VOUT0_DATA7
VOUT0_DATA8	V21	SoC_VOUT0_DATA8
VOUT0_DATA9	W21	SoC_VOUT0_DATA9
VOUT0_DATA10	V20	SoC_VOUT0_DATA10
VOUT0_DATA11	AA23	SoC_VOUT0_DATA11
VOUT0_DATA12	AB25	SoC_VOUT0_DATA12
VOUT0_DATA13	AA24	SoC_VOUT0_DATA13
VOUT0_DATA14	Y22	SoC_VOUT0_DATA14
VOUT0_DATA15	AA21	SoC_VOUT0_DATA15
VOUT0_PCLK	AC24	SoC_VOUT0_PCLK — R60 0E — HDMI_PCLK
VOUT0_DE	Y20	SoC_VOUT0_DE
VOUT0_VSYNC	AC25	SoC_VOUT0_VSYNC
VOUT0_HSYNC	AB24	SoC_VOUT0_HSYNC

VDD_1V2 — FB3 (300E) — VHDMI_AVCC_1V2: C232 22uF, C230 10uF, C231 0.1uF, C229 0.1uF

VHDMI_CVCC_1V2: C213, C209, C200, C207, C225, C217 0.1uF; FB2 (300E); C201 10uF

VHDMI_IOVCC_3V3: C223, C212 0.1uF, C199 10uF; FB1 (300E) from VCC_3V3_SYS; C204 10uF

VHDMI_IOVCC_3V3: R61 4.7K; R316 DNI, R323 DNI, R325 10K

U10

1	CSCL	(13,21,25,39,40,42) SoC_I2C1_SCL
2	CSDA	(13,21,25,39,40,42) SoC_I2C1_SDA
72	CI2CA	
51	RESET#	HDMI_RSTn
22	IDCK	HDMI_PCLK
32	D0	SoC_VOUT0_DATA0
31	D1	SoC_VOUT0_DATA1
30	D2	SoC_VOUT0_DATA2
29	D3	SoC_VOUT0_DATA3
28	D4	SoC_VOUT0_DATA4
27	D5	SoC_VOUT0_DATA5
25	D6	SoC_VOUT0_DATA6
24	D7	SoC_VOUT0_DATA7
23	D8	SoC_VOUT0_DATA8
20	D9	SoC_VOUT0_DATA9
19	D10	SoC_VOUT0_DATA10
18	D11	SoC_VOUT0_DATA11
17	D12	SoC_VOUT0_DATA12
16	D13	SoC_VOUT0_DATA13
15	D14	SoC_VOUT0_DATA14
14	D15	SoC_VOUT0_DATA15
13	D16	(32) SoC_VOUT0_DATA16
11	D17	(32) SoC_VOUT0_DATA17
10	D18	(32) SoC_VOUT0_DATA18
9	D19	(32) SoC_VOUT0_DATA19
8	D20	(32) SoC_VOUT0_DATA20
7	D21	(32) SoC_VOUT0_DATA21
6	D22	(32) SoC_VOUT0_DATA22
4	D23	(32) SoC_VOUT0_DATA23
34	HSYNC	SoC_VOUT0_HSYNC
35	VSYNC	SoC_VOUT0_VSYNC
33	DE	SoC_VOUT0_DE
36	SPDIF	
38	MCLK	HDMI_MSTRCLK
45	SCK	(39) MCASP1_ACLKX_HDMI
44	WS	(39) MCASP1_AFSX_HDMI
48	DSDA	HDMI_I2C_SDA
49	DSCL	HDMI_I2C_SCL
52	INT	HDMI_INTn (39)
54	HPD	HDMI_HPD
56	EXT_SWING	HDMI_EXTSWING
59	TXC+	HDMI_CLK+
58	TXC-	HDMI_CLK-
62	TX0+	HDMI_TX0+
61	TX0-	HDMI_TX0-
65	TX1+	HDMI_TX1+
64	TX1-	HDMI_TX1-
68	TX2+	HDMI_TX2+
67	TX2-	HDMI_TX2-
71	CEC_A	HDMI_CEC
50	CEC_D	HDMI_CEC_D — TP18
55	RSVDL	
69	IO_SEL	R62 0E — DGND
70	VDDQ	
41	SD0	
40	SD1	HDMI_AUDD1 — TP16
39	SD2	HDMI_AUDD2 — TP14
37	SD3	HDMI_AUDD3 — TP88
60, 66	AVCC12_1, AVCC12_2	VHDMI_AVCC_1V2
5, 12, 26, 42, 47, 53	CVCC12_1, CVCC12_2, CVCC12_3, CVCC12_4, CVCC12_5, CVCC12_6	VHDMI_CVCC_1V2
3, 21, 46	IOVCC1, IOVCC2, IOVCC3	VHDMI_IOVCC_3V3
57, 43, 63, 73	IOGND, CGND, AGND, PAD	DGND

R327 4.3K_1% — DGND; R326 DNI — DGND

R287 0E — Sil9022ACNU — DGND

I2C ADDRESS: 0x3B, 0x3F, 0x62

VCC_3V3_SYS — C20 0.1uF — DGND; R41 10K_1%

U7: 12.288MHz, VCC, INH, OUTPUT, GND; R34 DNI; (33) AUDIO_EXT_REFCLK1

HDMI ESD DEVICE

VCC_3V3_SYS — C248 10uF — DGND; VCC_5V0 — C219 10uF — DGND; VCC_3V3_SYS — R314 0E

VCC_5V0_HDMICONN — C211 10uF — DGND

U50 — TPD12S016PWR

18	D0+	HDMI_TX0+
17	D0-	HDMI_TX0-
21	D1+	HDMI_TX1+
20	D1-	HDMI_TX1-
23	D2+	HDMI_TX2+
22	D2-	HDMI_TX2-
16	CLK+	HDMI_CLK+
15	CLK-	HDMI_CLK-
8	SCL_B	HDMI_CONN_I2CSCL
9	SDA_B	HDMI_CONN_I2CSDA
10	HPD_B	HDMIConn_HPD
7	CEC_B	HDMI_CONNCEC
12	CT_HPD	
5	LS_OE	
2	SCL_A	HDMI_I2C_SCL
3	SDA_A	HDMI_I2C_SDA
4	HPD_A	HDMI_HPD
1	CEC_A	HDMI_CEC
24	VCCA	
11	VCC5V	
13	5V_OUT	
6, 14, 19	GND1, GND2, GND3	DGND

NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR

J5 — CON_HDMI_1X19_F

1	HDMI_TX2+
2	
3	HDMI_TX2-
4	HDMI_TX1+
5	
6	HDMI_TX1-
7	HDMI_TX0+
8	
9	HDMI_TX0-
10	HDMI_CLK+
11	
12	HDMI_CLK-
13	HDMI_CONNCEC
14	
15	HDMI_CONN_I2CSCL
16	HDMI_CONN_I2CSDA
17	
18	VCC_5V0_HDMICONN
19	HDMIConn_HPD
20, 21, 22, 23	DGND

FL17: 120E — DGND; HDMI_EARTH

Silk: HDMI

HDMI RESET

VCC_3V3_SYS — R389 10K; C323 0.1uF — DGND

U54: SN74LVC1G08DBVRE4

(39) GPIO_HDMI_RST	1
(12,18,19,20,22,23,26,32,33,37,39,40,42) RESETSTATz	2
	3 — R390 DNI — DGND
4	HDMI_RSTn — R373 10K — DGND
5	VCC_3V3_SYS

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Size C	PROC142A(002)	Rev A
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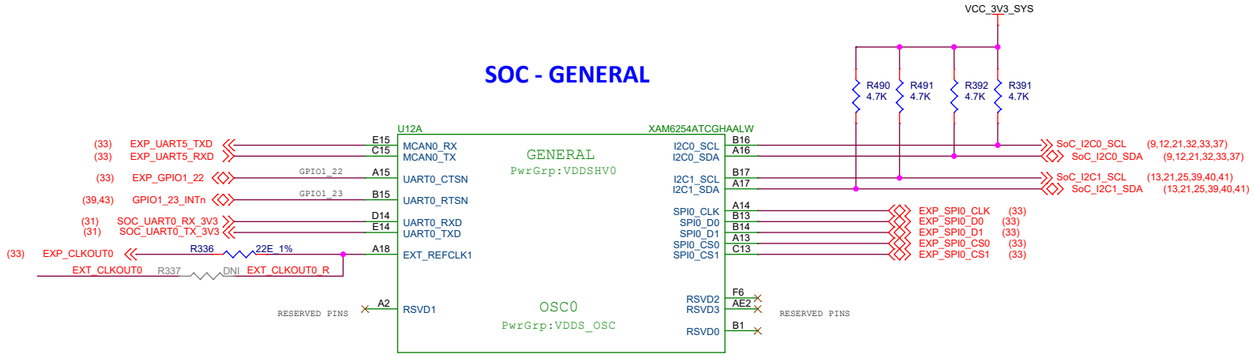
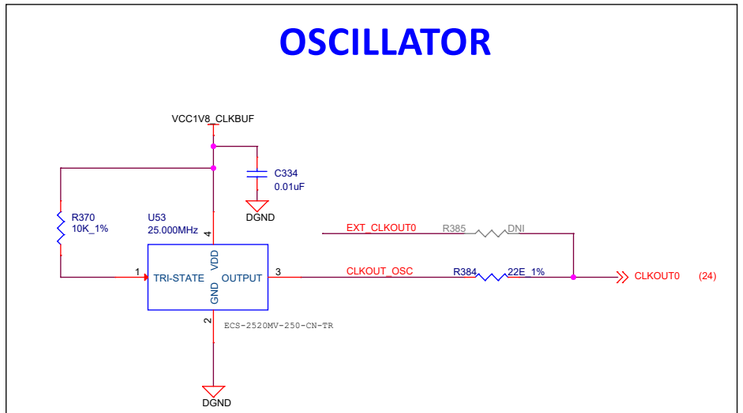
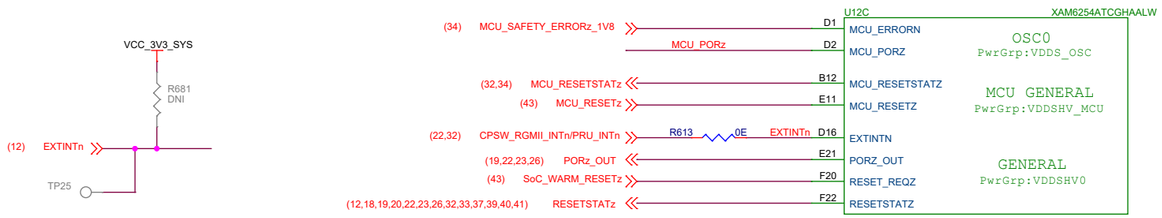
SOC - GENERAL

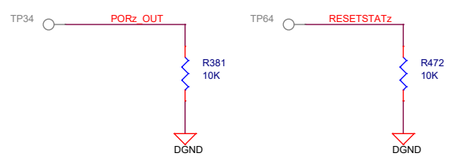


OSCILLATOR

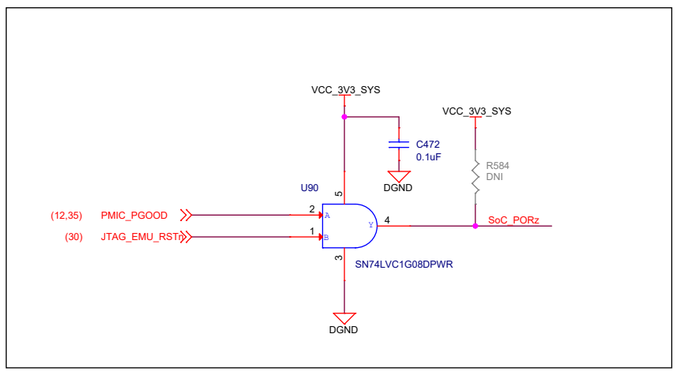


SOC - RESET

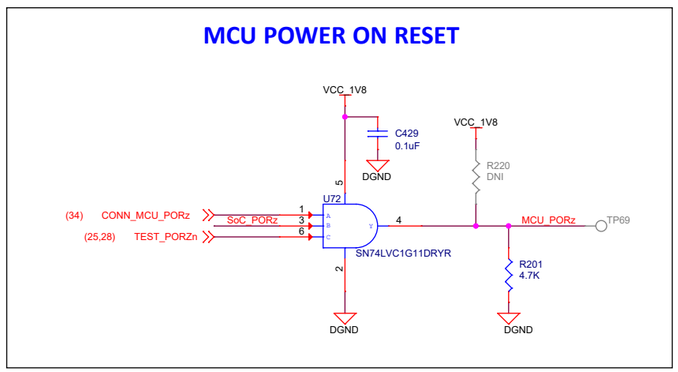




Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence



MCU POWER ON RESET



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Title	OSCILLATOR		
Size	PROC142A(002)		Rev
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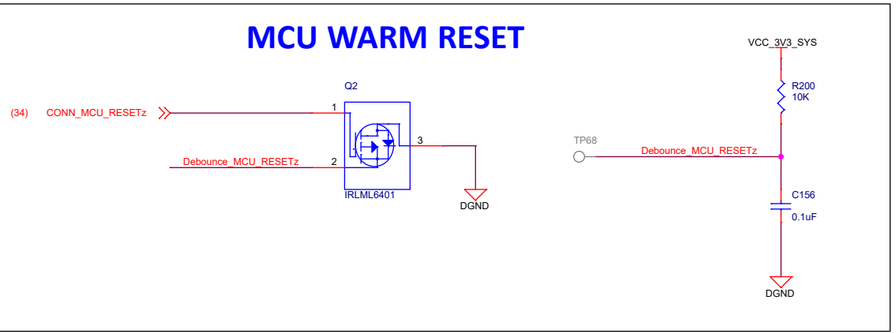
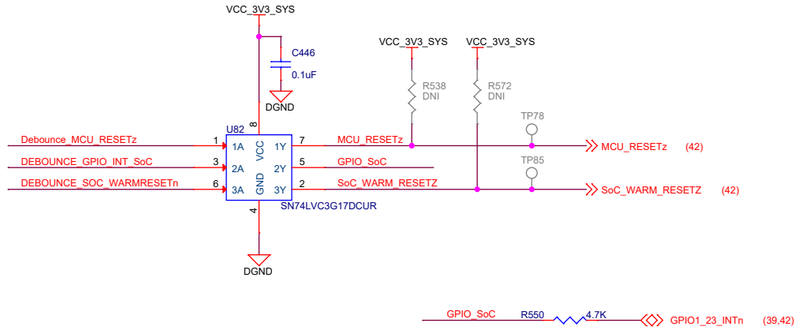
RESET

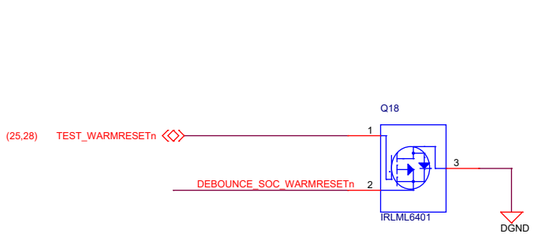
MCU WARM RESET

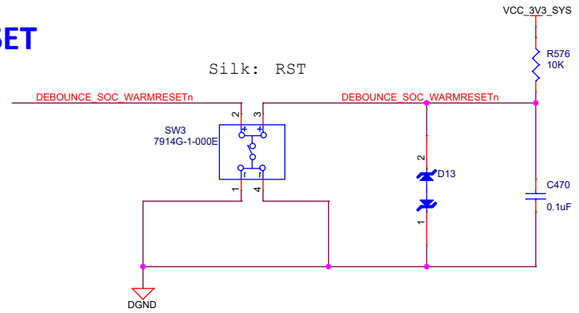


DEBOUNCE CIRCUIT

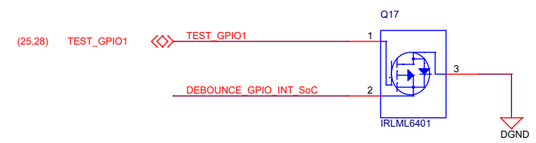


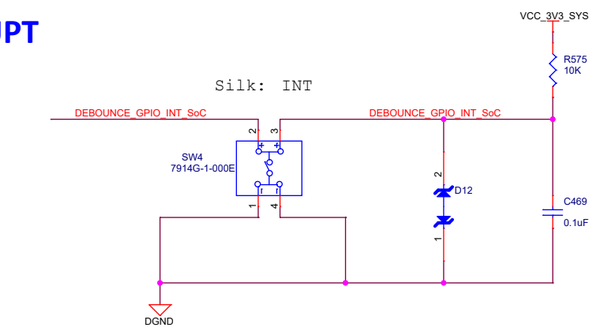
SOC WARM RESET





USER INTERRUPT





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Title	RESET	
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HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PROC142E1

PROC142E1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

LABELS

Board Serial No.

LBL1

PCB LABEL

DNI

Assembly Revision

LBL2

PCB LABEL

DNI

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

ORDERABLE PART NO

LBL3

PCB LABEL

THT-103-423-10

Oderable Part Number	
Variant	**Label Text**
001	SK-AM62-P1
002	SK-AM62B-P1

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Title	HARDWARE SCHEMATICS		
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