NOTES

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.

2. REFERENCE DESIGNATORS USED:

   A. INTEGRATED CIRCUTS: U1-U13
   B. CERAMIC CAPS: C1 - C63, C65 - C110
   C. LOW ESL TANTALUM CAPS: CT1-CT15
   D. RESISTORS: R1-R81
   E. RESISTOR PACKS: RP1-R21
   F. CONNECTORS/HEADERS: JP1 - JP2, JH1, J1, P1 - P3
   G. CRYSTALS: Y1-Y3
   H. EMI FILTERS: E1 - E3
   I. FERRITE BEADS: L1-L3
   J. FUSES: F1-F2
   K. TEST POINTS: TP1-TP2

3. OBSERVE THE FOLLOWING LAYOUT NOTES:
   FORMAT: PAGENUMBER.NOTENUMBER
   2.1, 2.2, 2.3, 3.1, 3.2, 3.3, 3.4, 4.1, 4.2, 4.3, 5.1, 5.2,
   5.3, 6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 7.1, 7.2, 7.3, 7.4, 7.5, 8.1,
   8.2, 9.1, 9.2, 9.3, 10.1, 10.2, 10.3 11.1, 11.2, 12.1,
   12.2, 12.3, 12.4, 12.5, 12.6, 12.7

4. ALL 0100nf AND 220nf CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THE ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

5. BOARD PROPERTIES

   A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE - DEVIATIONS PERMITTED TO MEET AC TIMINGS GOALS
   B. 50 OHM MATCHED IMPEDANCE
   C. OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
   D. INNER LAYERS 1.0 OZ CU
   E. FR4 BOARD MATERIAL
   F. MINIMUM TRACE WIDTH/SPACING 4 MILS
   G. MINIMUM VIA SIZE 10/19 MIL
   H. BOARD SHALL MEET PCI 3.3V 32BIT SHORT-FORM EXPANSION CARD SPECIFICATION
   J. THERMAL RELIEFS SHALL NOT BE USED EXCEPT ON THROUGH-HOLE PARTS
   K. STACKUP: (4 LAYER)
      1. TOP - SIGNAL ROUTING
      2. GROUND PLANE
      3. SPLIT POWER (3V3 & CVDD)
      4. BOTTOM - SIGNAL ROUTING
   L. ALL PARTS AND IC PIN 1 DESIGNATORS SHALL BE MARKED ON THE SILK SCREEN

Rev	Description	Owner
1.0	Preliminary Design	TCH
1.1	Fixed CVDD feedback open Added notes for power supply design improvements Altered default Rs for CLK freq select	TCH
1.2	Fixed USB OE Problem	TCH
1.3	Changes for EMI	TCH
1.4	Added R80 & R81 Pullups on USB bridge	TCH

SCHEMATIC CONTENTS

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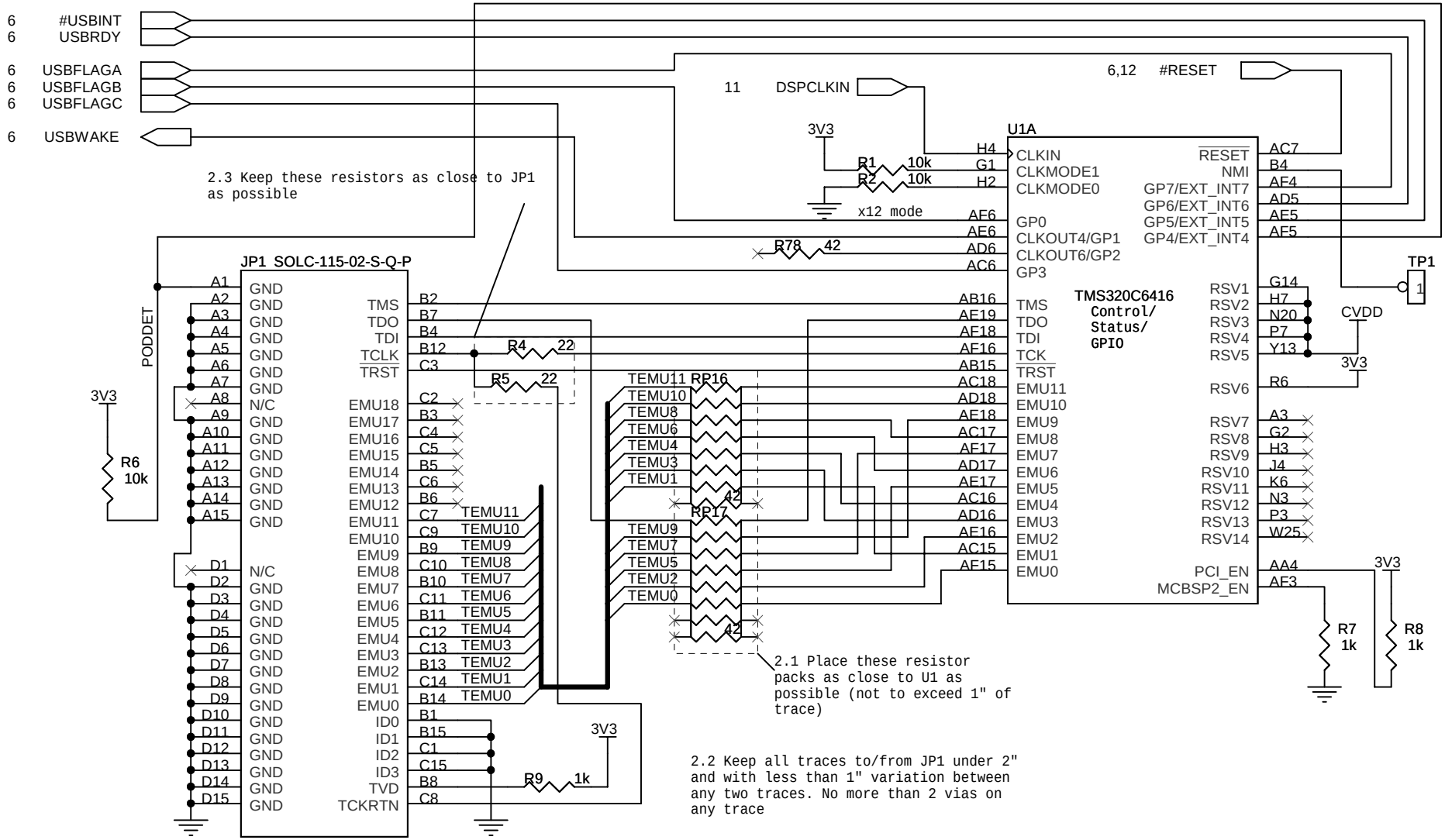

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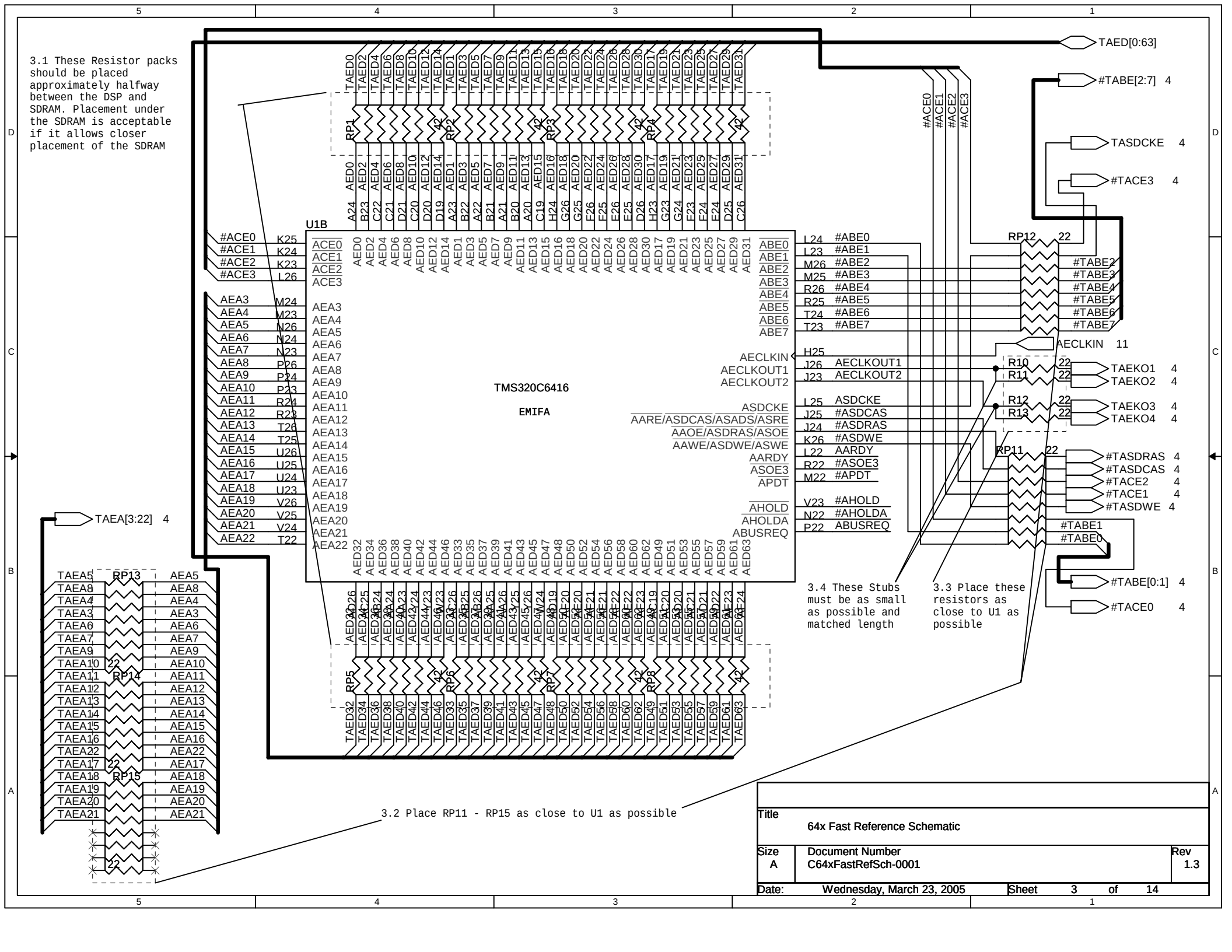
3.1 These Resistor packs should be placed approximately halfway between the DSP and SDRAM. Placement under the SDRAM is acceptable if it allows closer placement of the SDRAM
TAED[0:63]
#TABE[2:7] 4
TASDCKE 4
#TACE3 4
#ACE0
#ACE1
#ACE2
#ACE3
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
42
U1B
TMS320C6416
EMIFA
#ACE0 K25
#ACE1 K24
#ACE2 K23
#ACE3 L26
AEA3 M24
AEA4 M23
AEA5 N26
AEA6 N24
AEA7 N23
AEA8 P26
AEA9 P24
AEA10 P23
AEA11 R24
AEA12 R23
AEA13 T26
AEA14 T25
AEA15 U26
AEA16 U25
AEA17 U24
AEA18 U23
AEA19 V26
AEA20 V25
AEA21 V24
AEA22 T22
L24 #ABE0
L23 #ABE1
M26 #ABE2
M25 #ABE3
R26 #ABE4
R25 #ABE5
T24 #ABE6
T23 #ABE7
H25 AECLKIN
J26 AECLKOUT1
J23 AECLKOUT2
L25 ASDCKE
J25 #ASDCAS
J24 #ASDRAS
K26 #ASDWE
L22 AARDY
R22 #ASOE3
M22 #APDT
V23 #AHOLD
N22 #AHOLDA
P22 ABUSREQ
RP12 22
#TABE2
#TABE3
#TABE4
#TABE5
#TABE6
#TABE7
AECLKIN 11
R10 22
R11 22
R12 22
R13 22
TAEKO1 4
TAEKO2 4
TAEKO3 4
TAEKO4 4
RP11 22
#TASDRAS 4
#TASDCAS 4
#TACE2 4
#TACE1 4
#TASDWE 4
#TABE1
#TABE0
#TABE[0:1] 4
#TACE0 4
TAEA[3:22] 4
RP13
RP14
RP15
22
3.4 These Stubs must be as small as possible and matched length
3.3 Place these resistors as close to U1 as possible
3.2 Place RP11 - RP15 as close to U1 as possible
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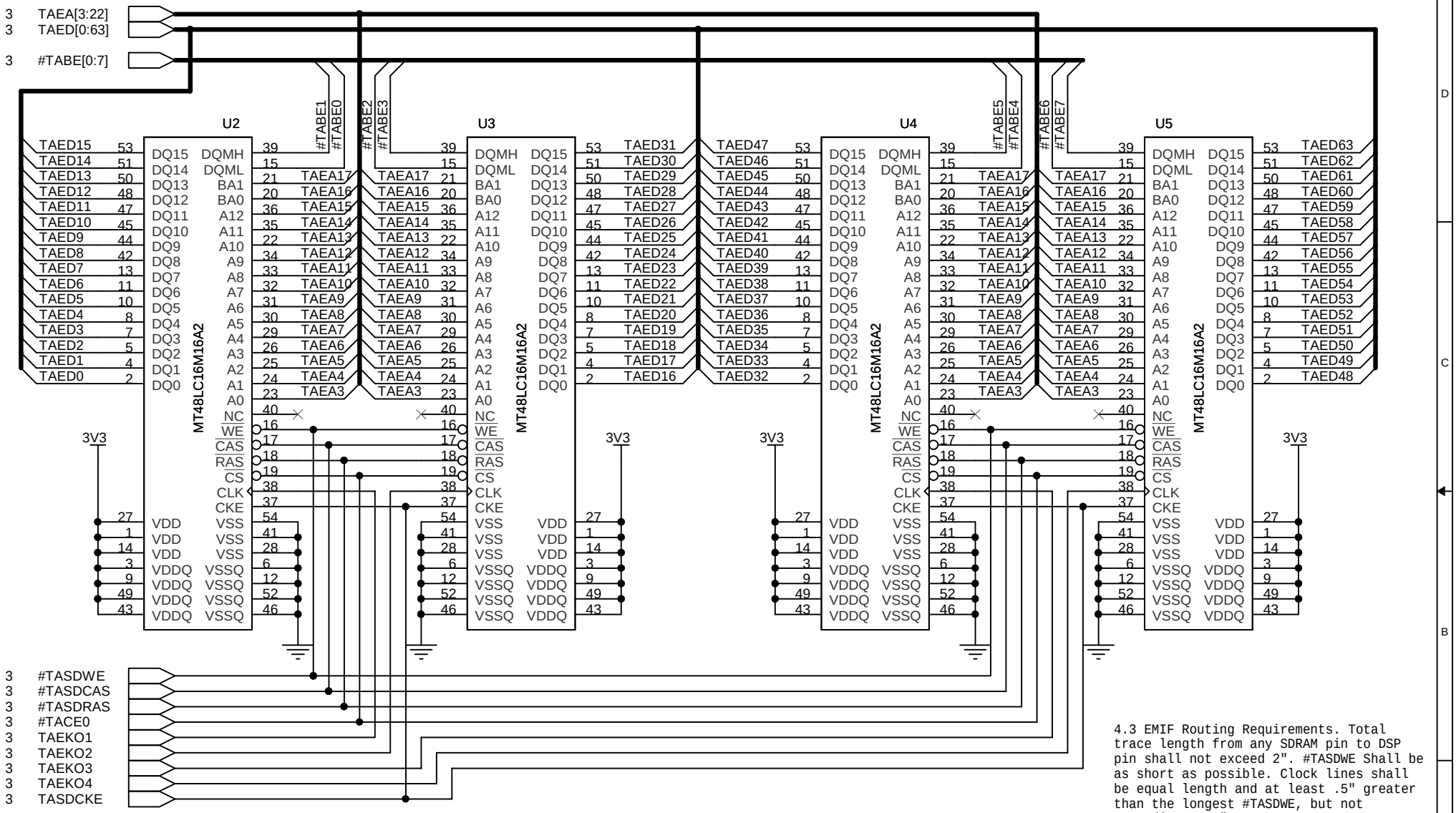

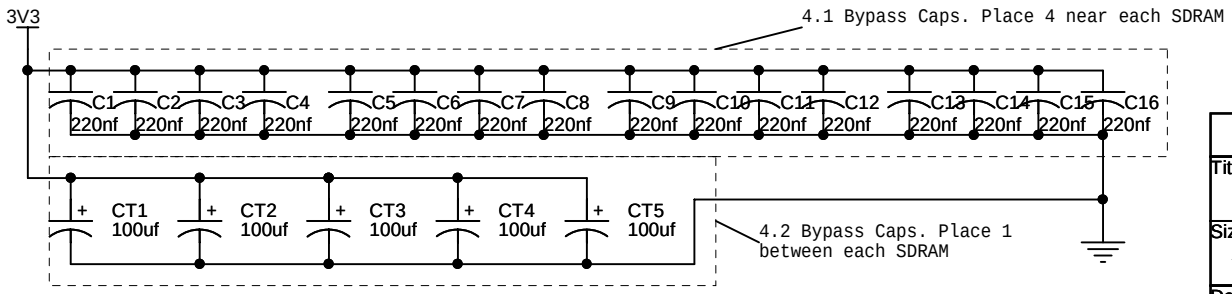

4.3 EMIF Routing Requirements. Total trace length from any SDRAM pin to DSP pin shall not exceed 2". #TASDWE Shall be as short as possible. Clock lines shall be equal length and at least .5" greater than the longest #TASDWE, but not exceeding 2.75". EMIF A traces must pass IBIS timng check

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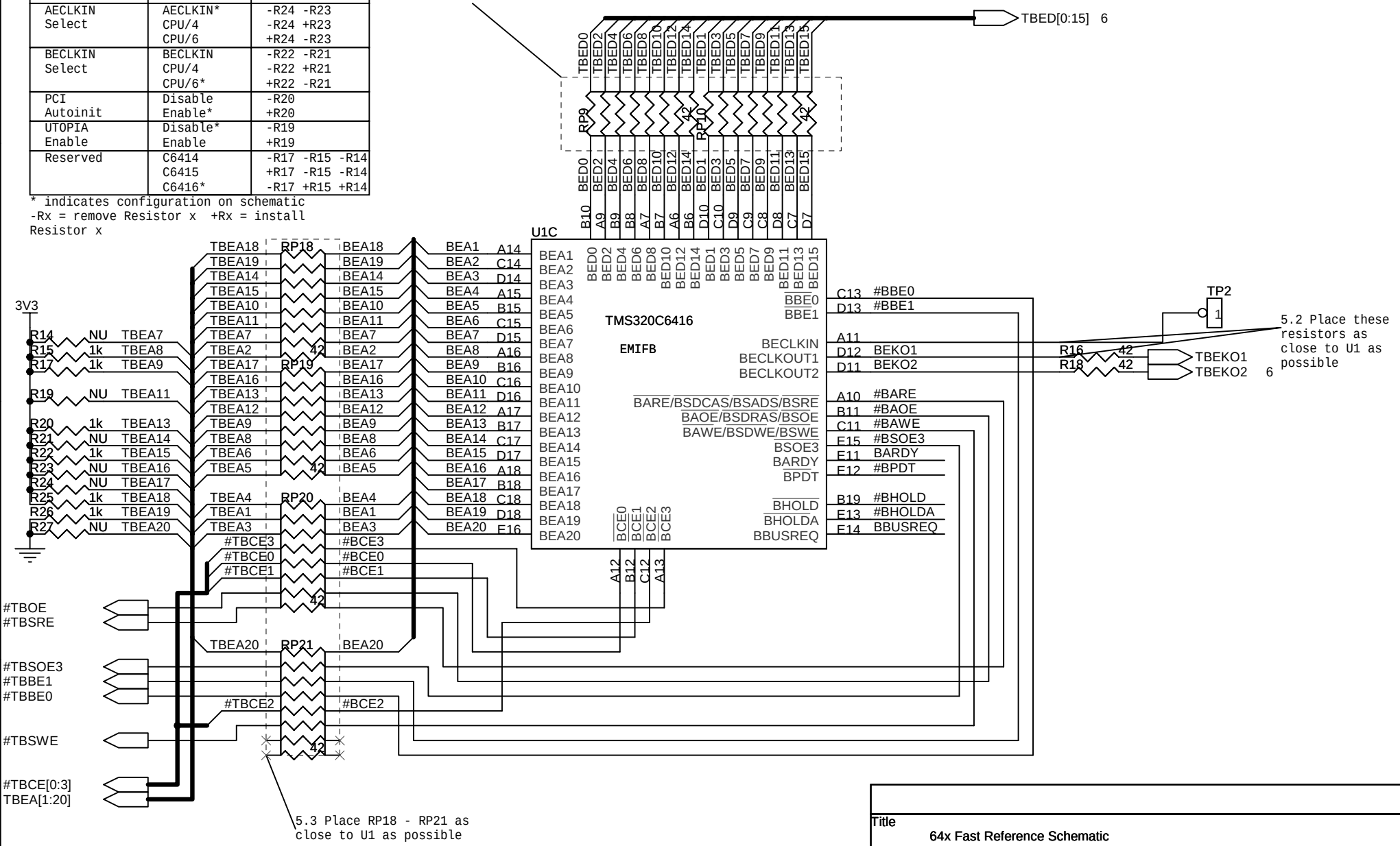
Boot Configuration

Endianness	Big	+R27
	Little*	-R27
Bootmode	None	+R26 -R25
	PCI*	+R26 +R25
	ROM	-R26 -R25
AECLKIN Select	AECLKIN*	-R24 -R23
	CPU/4	-R24 +R23
	CPU/6	+R24 -R23
BECLKIN Select	BECLKIN	-R22 -R21
	CPU/4	-R22 +R21
	CPU/6*	+R22 -R21
PCI Autoinit	Disable	-R20
	Enable*	+R20
UTOPIA Enable	Disable*	-R19
	Enable	+R19
Reserved	C6414	-R17 -R15 -R14
	C6415	+R17 -R15 -R14
	C6416*	-R17 +R15 +R14

* indicates configuration on schematic
-Rx = remove Resistor x +Rx = install Resistor x

5.1 These Resistor packs should be placed approximately halfway between the DSP and U6



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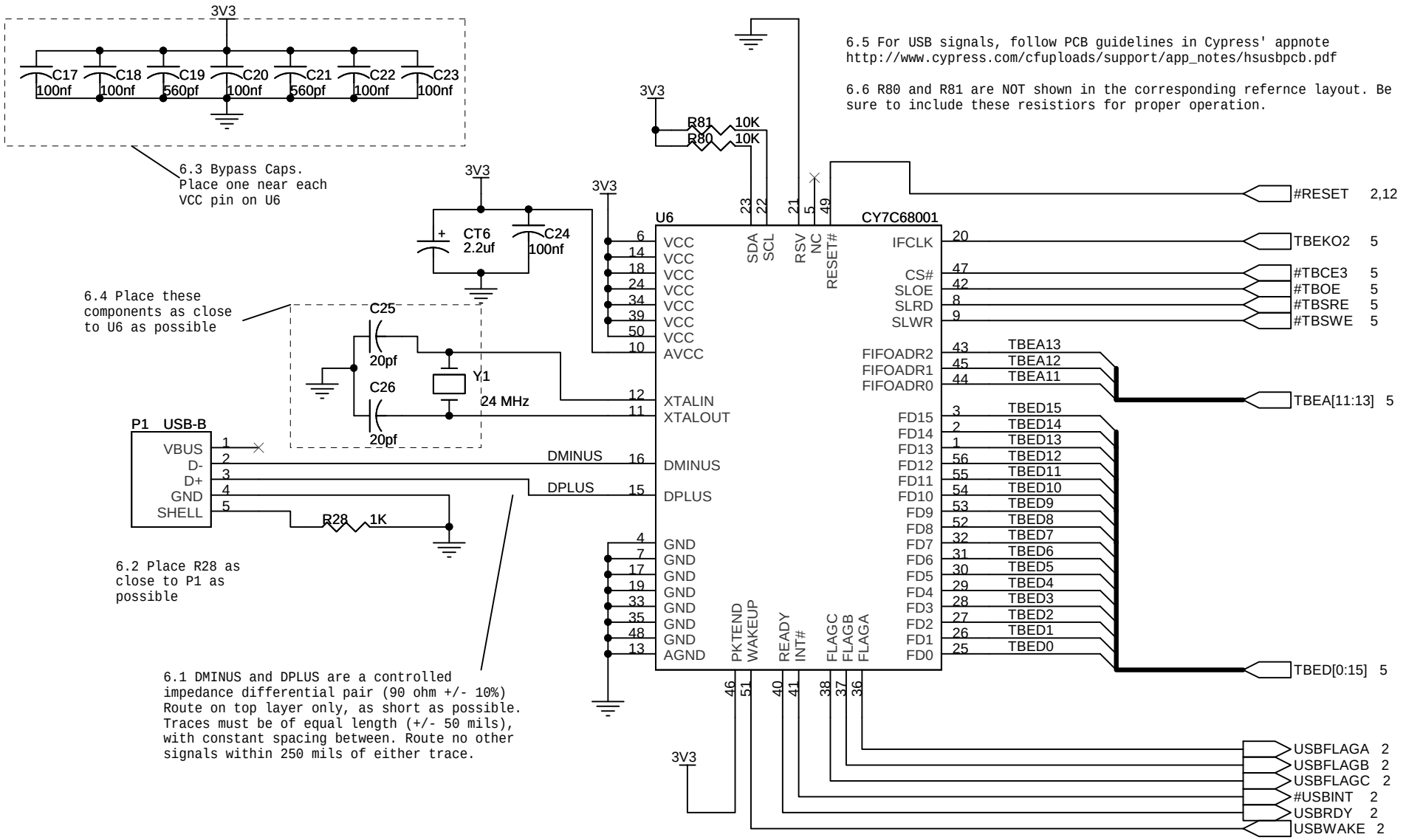

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7.5 Min 25 mils width

F1

5A

5V

C27 100nf

C28 100nf

7.3 Place these componets as close to P2 as possible. Cap pad to pin pad must be <0.25" and at least 0.02" wide

C29 100nf

C30 100nf

C31 100nf

C32 100nf

P2

B1	-12V	TRST#	A1		
B2	TCK	+12v	A2		
B3	GND	TMS	A3		
B4	TD0	TDI	A4		
B5	+5v	+5v	A5		
B6	+5v	INTA#	A6	PINTA#	
B7	INTB#	INTC#	A7		
B8	INTD#	+5v	A8		
B9	PRSNT1#	RSV	A9		
B10	RSV	+3.3v	A10		
B11	PRSNT2#	RSV	A11		
B12	KEY	KEY	A12		
B13	KEY	KEY	A13		
B14	RSV	3.3vAUX	A14		
B15	GND	RST#	A15	PRST#	
PCLK B16	CLK	+3.3v	A16		
B17	GND	GNT#	A17	PGNT#	
PREQ# B18	REQ#	GND	A18		
B19	+3.3v	PME#	A19		
PAD31 B20	AD31	AD30	A20	PAD30	
PAD29 B21	AD29	+3.3v	A21		
B22	GND	AD28	A22	PAD28	
PAD27 B23	AD27	AD26	A23	PAD26	
PAD25 B24	AD25	GND	A24		
B25	+3.3v	AD24	A25	PAD24	
PCBE#3 B26	C/BE#3	IDSEL	A26	PIDSEL	
PAD23 B27	AD23	+3.3v	A27		
B28	GND	AD22	A28	PAD22	
PAD21 B29	AD21	AD20	A29	PAD20	
PAD19 B30	AD19	GND	A30		
B31	+3.3v	AD18	A31	PAD18	
PAD17 B32	AD17	AD16	A32	PAD16	
PCBE#2 B33	C/BE#2	+3.3v	A33		
B34	GND	FRAME#	A34	PFRAME#	
PIRDY# B35	IRDY#	GND	A35		
B36	+3.3v	TRDY#	A36	PTRDY#	
PDEVSEL# B37	DEVSEL#	GND	A37		
B38	GND	STOP#	A38	PSTOP#	
B39	LOCK#	+3.3v	A39		
PPERR# B40	PERR#	RSV	A40		
B41	+3.3v	RSV	A41		
PSERR# B42	SERR#	GND	A42		
B43	+3.3v	PAR	A43	PPAR	
PCBE#1 B44	C/BE#1	AD15	A44	PAD15	
PAD14 B45	AD14	+3.3v	A45		
B46	GND	AD13	A46	PAD13	
PAD12 B47	AD12	AD11	A47	PAD11	
PAD10 B48	AD10	GND	A48		
B49	M66EN	AD9	A49	PAD9	
B50	GND	GND	A50		
B51	GND	GND	A51		
PAD8 B52	AD8	C/BE#0	A52	PCBE#0	
PAD7 B53	AD7	+3.3v	A53		
B54	+3.3v	AD6	A54	PAD6	
PAD5 B55	AD5	AD4	A55	PAD4	
PAD3 B56	AD3	GND	A56		
B57	GND	AD2	A57	PAD2	
PAD1 B58	AD1	AD0	A58	PAD0	
B59	+3.3v	+3.3v	A59		
B60	ACK64#	REQ64#	A60		
B61	+5v	+5v	A61		
B62	+5v	+5v	A62		

3.3v PCI Connector

7.1 PCLK trace shall be 2.5" +/- 0.1"

7.2 All other PCI traces shall be < 1.5"

U1D

TMS320C6416

HPI/PCI/ McBSP2/GPIO

PFRAME#	R4	HINT/PFRAME	
PSTOP#	T4	HCNITL0/PSTOP	
PDEVSEL#	R1	HCNTL1/PDEVSEL	
PTRDY#	R3	HHWIL/PTRDY	
PCBE#0	W3	PCBE0	
PCBE#1	T2	HDS2/PCBE1	
PCBE#2	P1	HR/W/PCBE2	
PCBE#3	L2	GP10/PCBE3	
PPAR	T3	HAS/PPAR	
PPERR#	R2	HCS/PPERR	
PSERR#	T1	HDS1/PSERR	
PIRDY#	P4	HRDY/PIRDY	
PIDSEL	M3	GP9/PIDSEL	
PREQ#	F1	GP11/PREQ	
PGNT#	J3	GP12/PGNT	
PINTA#	G4	GP13/PINTA	
PCLK	F2	GP14/PCLK	
PRST#	G3	GP15/PRST	

HD0/AD0	AA3	PAD0	
HD1/AD1	AA1	PAD1	
HD2/AD2	Y4	PAD2	
HD3/AD3	Y2	PAD3	
HD4/AD4	Y3	PAD4	
HD5/AD5	Y1	PAD5	
HD6/AD6	W4	PAD6	
HD7/AD7	W2	PAD7	
HD8/AD8	V2	PAD8	
HD9/AD9	V3	PAD9	
HD10/AD10	V1	PAD10	
HD11/AD11	V4	PAD11	
HD12/AD12	U2	PAD12	
HD13/AD13	U3	PAD13	
HD14/AD14	U1	PAD14	
HD15/AD15	U4	PAD15	
HD16/AD16	P5	PAD16	
HD17/AD17	N1	PAD17	
HD18/AD18	N5	PAD18	
HD19/AD19	M1	PAD19	
HD20/AD20	N4	PAD20	
HD21/AD21	M2	PAD21	
HD22/AD22	M4	PAD22	
HD23/AD23	L1	PAD23	
HD24/AD24	L4	PAD24	
HD25/AD25	K1	PAD25	
HD26/AD26	L3	PAD26	
HD27/AD27	K2	PAD27	
HD28/AD28	K4	PAD28	
HD29/AD29	J1	PAD29	
HD30/AD30	K3	PAD30	
HD31/AD31	J2	PAD31	

CLKS2/GP8	AE4		
CLKR2	AB1		
FSR2	AC1		
DR2/XSP_DI	AB3		
CLKX2/XSP_CLK	AC2		
FSX2	AB2		
DX2/XSP_DO	AA2		
XSP_CS	AD1		

R79 42

7.4 Place C33 as close to U7 as possible

U7

93LC66B

1	CS	Vcc	8
2	CLK	NC	7
3	DI	NC	6
4	DO	Vss	5

3V3

C33 100nf

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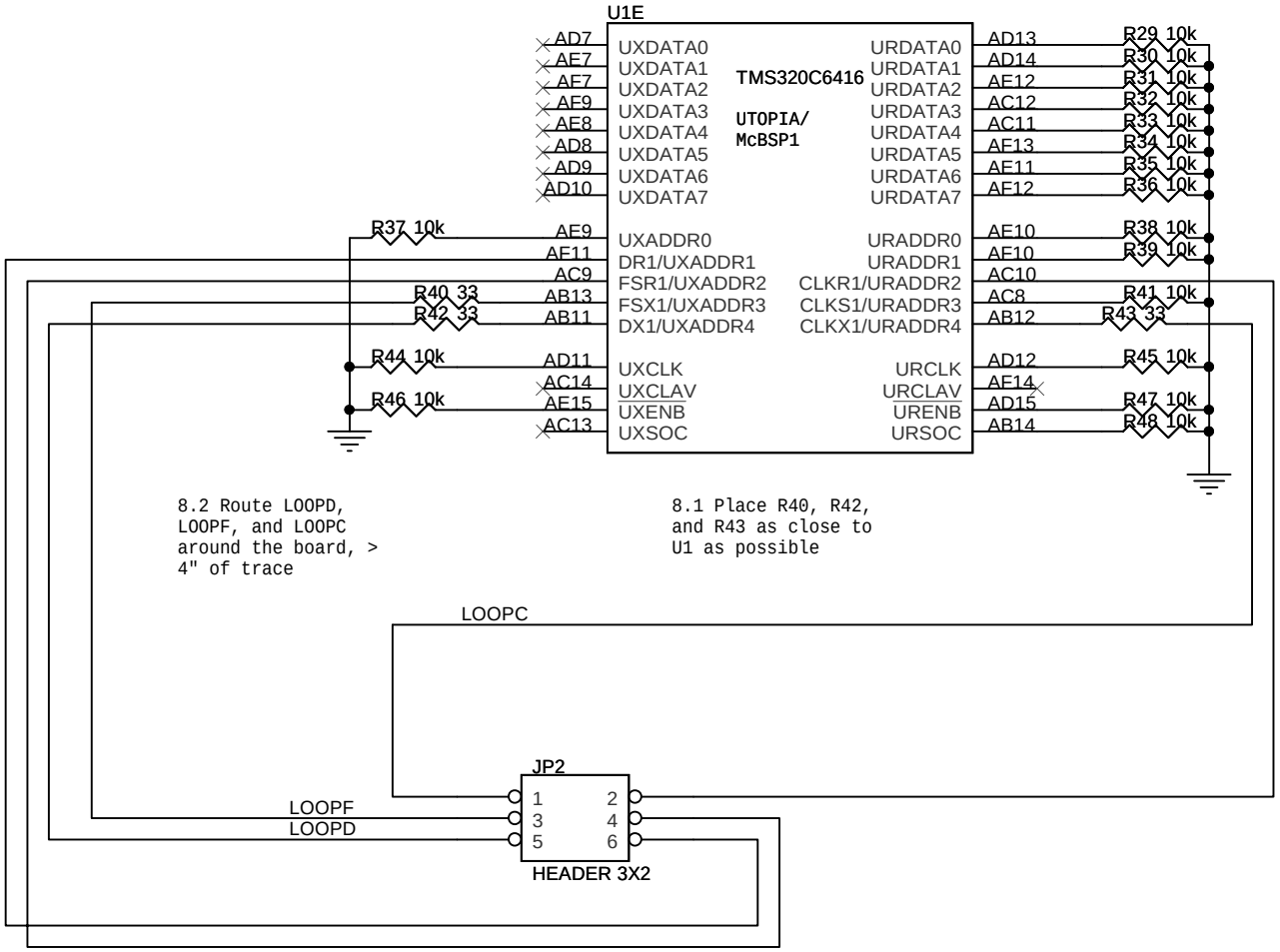

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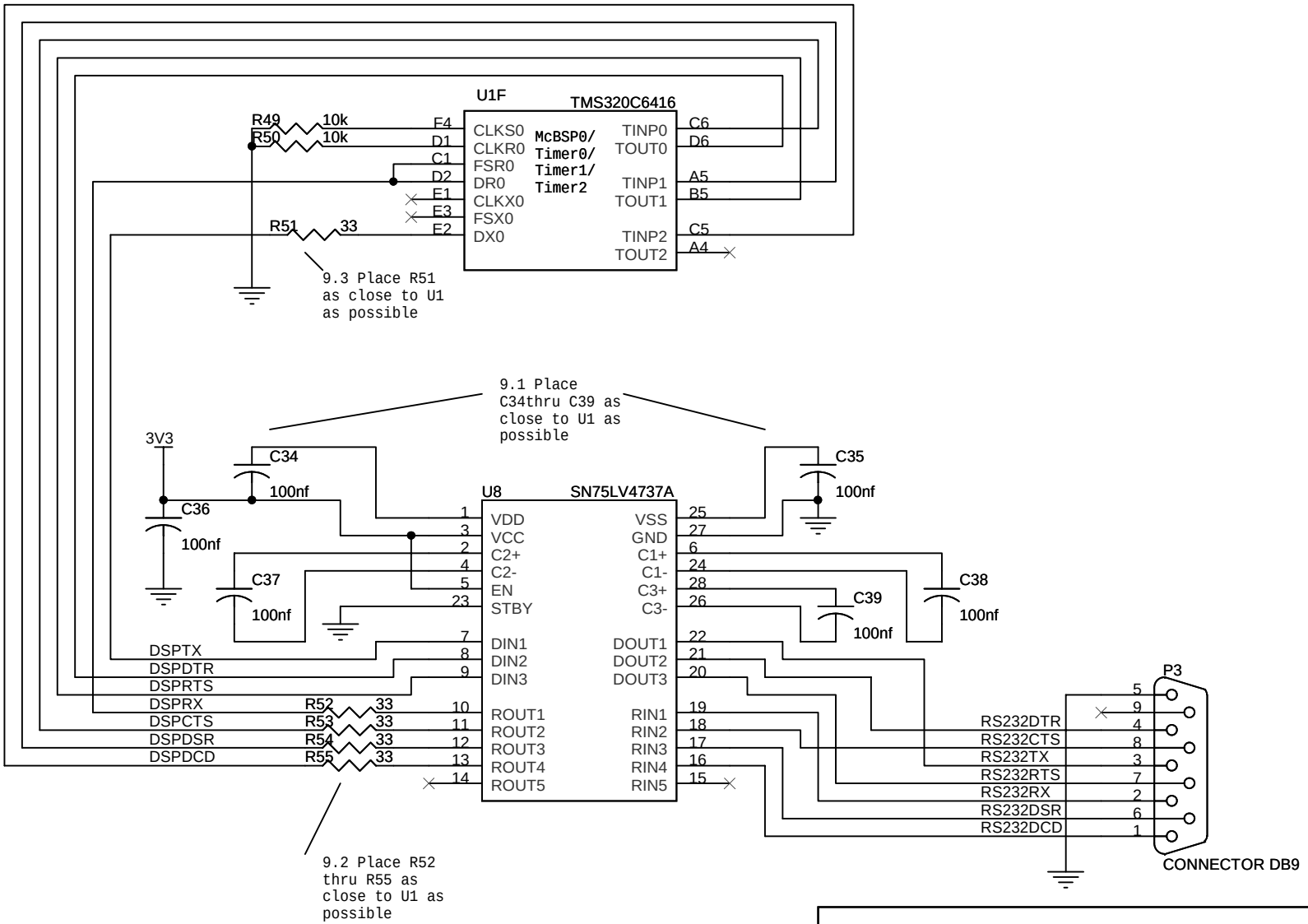

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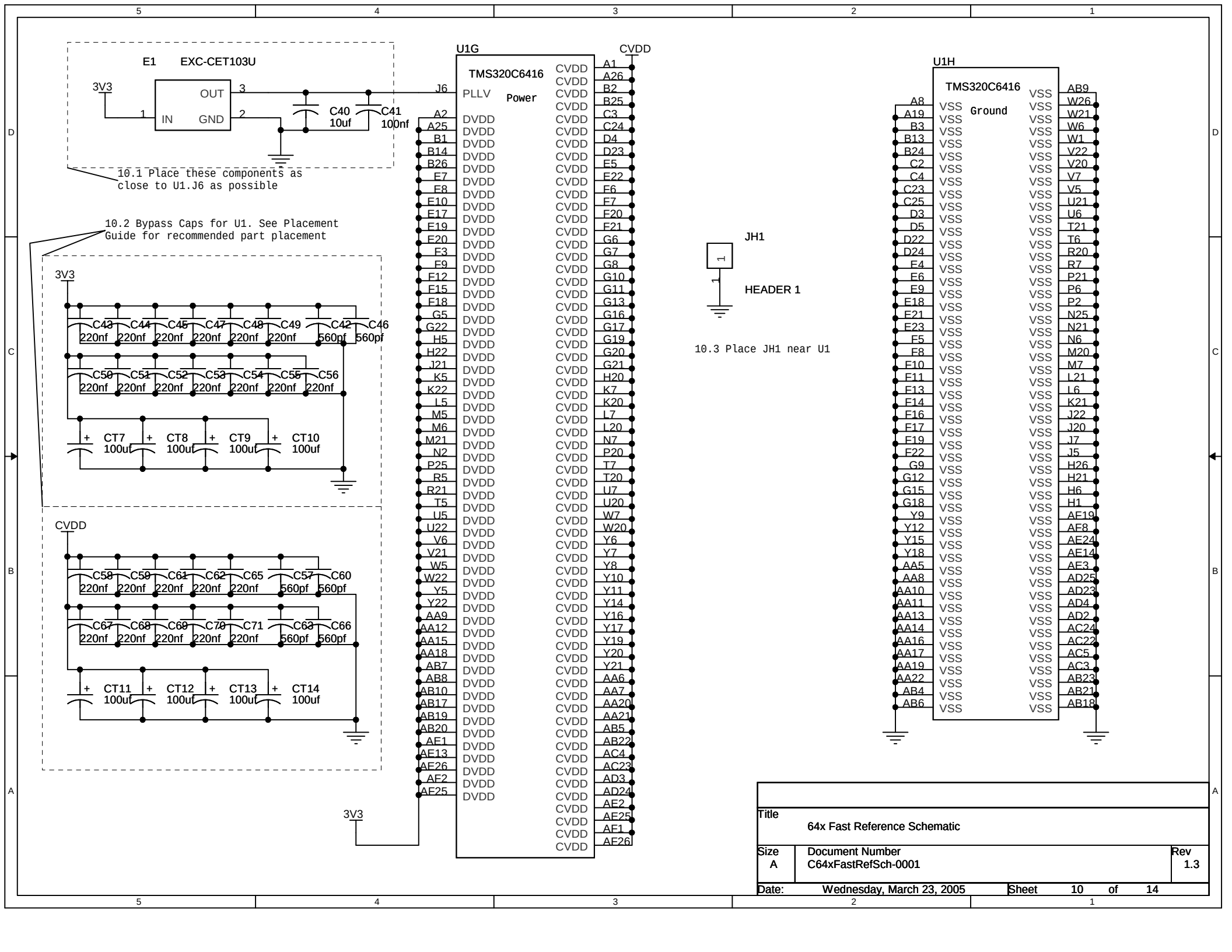
E1 EXC-CET103U
3V3
OUT
IN
GND
C40 10uf
C41 100nf
10.1 Place these components as close to U1.J6 as possible
10.2 Bypass Caps for U1. See Placement Guide for recommended part placement
C43 C44 C45 C47 C48 C49 C42 C46
220nf 560pf
C50 C51 C52 C53 C54 C55 C56
220nf
CT7 CT8 CT9 CT10
100uf
CVDD
C58 C59 C61 C62 C65 C57 C60
C67 C68 C69 C70 C71 C63 C66
CT11 CT12 CT13 CT14
U1G
TMS320C6416
PLLV
Power
DVDD
CVDD
J6
JH1
HEADER 1
10.3 Place JH1 near U1
U1H
TMS320C6416
Ground
VSS
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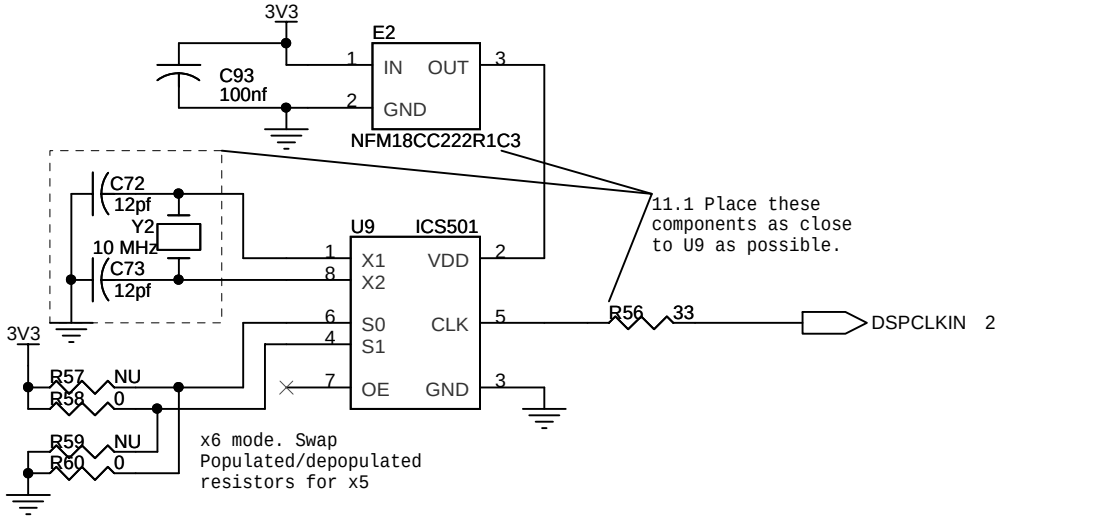

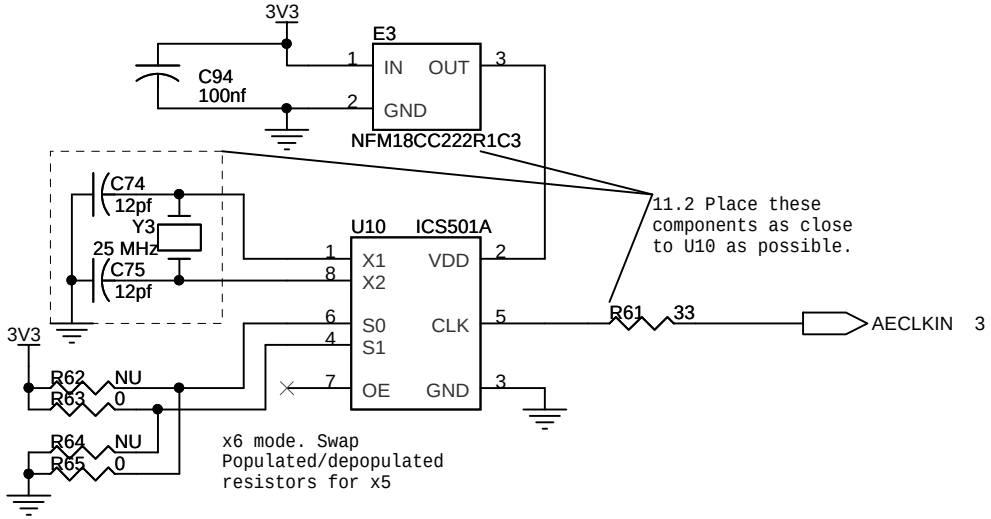

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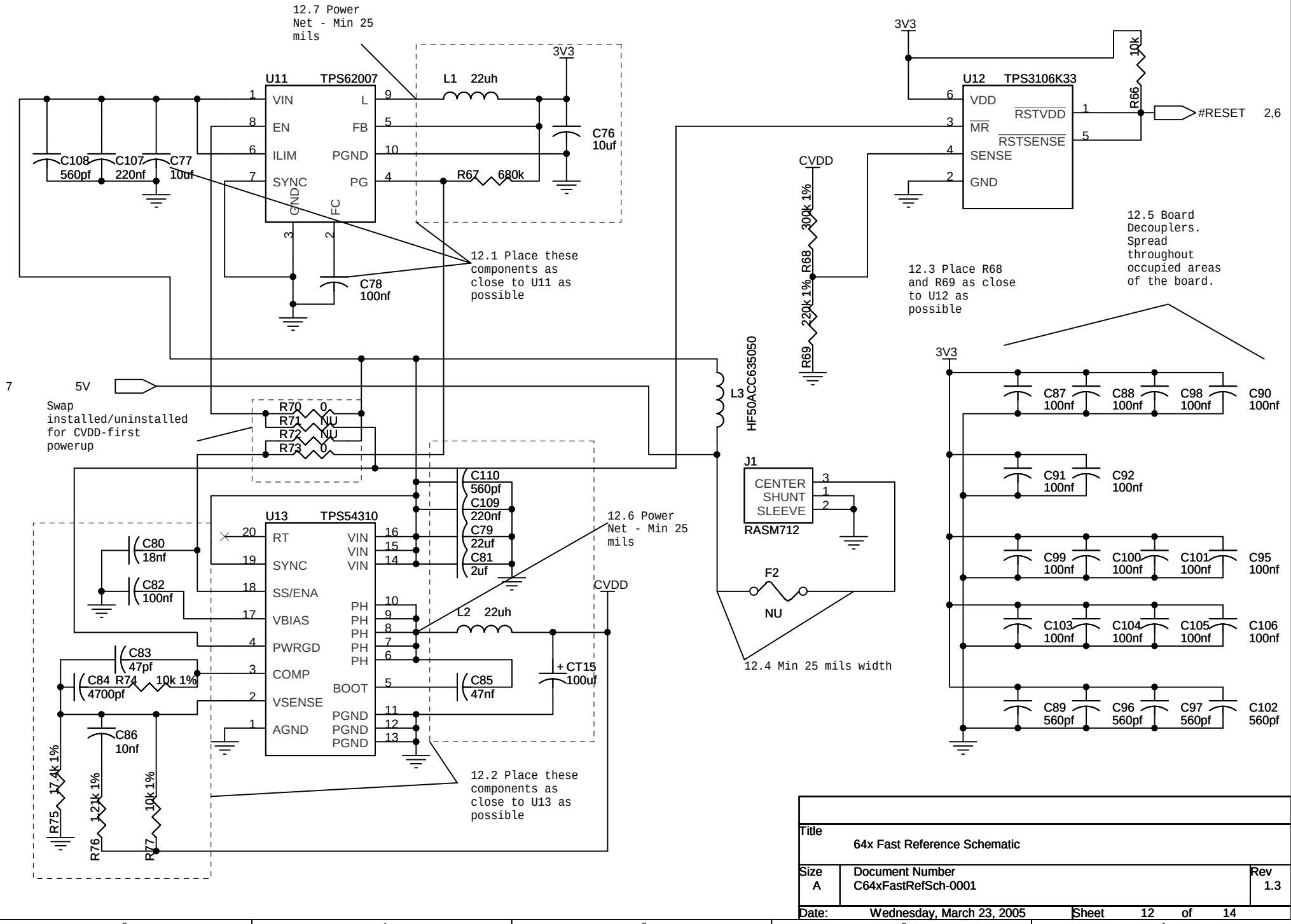

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