

Product Clip

Standard Linear and Logic

Little Logic Portfolio and Roadmap

Texas Instruments (TI) offers one of the most comprehensive portfolios of single-, dual- and triple-gate logic functions in the industry. With ultra small footprints and technologies ranging from the lowest power logic technology in the market, AUP, to the fastest 1.8-V logic technology, AUC, TI can meet any design needs.

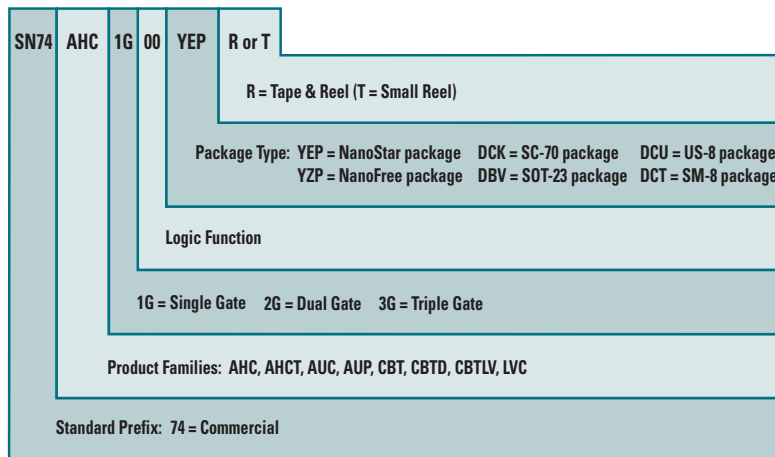
NEW FUNCTIONS

- SN74AUC1G74** – Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset
- SN74AUC2G34** – Dual Buffer Gate
- SN74AUC2G79** – Dual Positive-Edge-Triggered D-Type Flip-Flop
- SN74AUC2G80** – Dual Positive-Edge-Triggered D-Type Flip-Flop
- SN74AUP1G08** – Low-Power Single 2-Input Positive-AND Gate
- SN74AUP1G57** – Low-Power Configurable Multiple-Function Gate
- SN74AUP1G58** – Low-Power Configurable Multiple-Function Gate
- SN74AUP1G97** – Low-Power Configurable Multiple-Function Gate
- SN74AUP1G98** – Low-Power Configurable Multiple-Function Gate
- SN74LVC1G34** – Single Buffer Gate
- SN74LVC1G38** – Single 2-Input NAND Gate With Open Drain Output
- SN74LVC1G373** – Single D-Type Latch With 3-State Output
- SN74LVC1G374** – Single D-Type Flop-Flop With 3-State Output
- SN74LVC2G79** – Dual Positive-Edge-Triggered D-Type Flip-Flop
- SN74LVC2G80** – Dual Positive-Edge-Triggered D-Type Flip-Flop
- SN74LVC3GU04** – Triple Inverter Gate

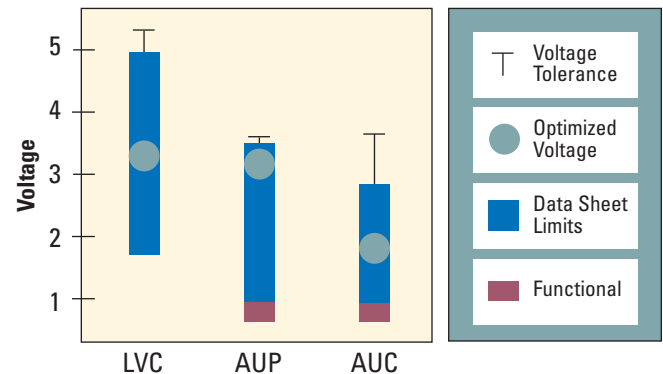
Little Logic Family Characteristics	Fastest Speed 1.8V	Broadest Portfolio	Lowest Power
	AUC	LVC	AUP
V_{CC}	0.8V to 2.7V	1.65V to 5.5V	0.8V to 3.6V
I_{CC}	10 μ A	10 μ A	0.9 μ A
I_I	5 μ A	5 μ A	0.5 μ A
I_{OFF}	10 μ A	10 μ A	0.6 μ A
I_{OZ}	10 μ A	5 μ A	0.6 μ A
C_{PD}	19 pF	26 pF	4.3 pF
C_{IN}	3 pF	4 pF	1.5 pF
C_{OUT}	NS	NS	3 pF
$T_{PD(max)}$	2 ns (30 pF)	3.6 ns (15 pF)	4.3 ns (5 pF), 5.9 ns (15 pF)
I_{OH}/I_{OL}	9 mA	24 mA	4 mA

Note: The C_{PD} , I_{OH} , I_{OL} and T_{PD} data represent the 3.3-V V_{CC} node except for AUC. AUC data represents the 2.5-V V_{CC} node.

Part Number Definition



Little Logic Voltage Positioning



Single-Gate Functions

Function	Part #	Pins	SN74AUC1G			SN74LVC1G			SN74AUP1G		
			Package Suffix			Package Suffix			Package Suffix		
			DBV/DCK	DCU/DCT	YEP/YZP	DBV/DCK	DCU/DCT	YEP/YZP	DBV/DCK	DCU/DCT	YEP/YZP
2-Input NAND	00	5						May '04		June '04	
2-Input NOR	02	5						May '04		June '04	
Inverter	04	5						June '04			
Inverter (Unbuffered)	U04	5									
Inverter w/Open -Drain	06	5						June '04			
Buffer/Driven w/Open	07	5						June '04			
2-Input AND	08	3,3								June '04	
3-Input NAND	10	6									
3-Input AND	11	6									
Schmitt-Trigger Inverter	14	5						May '04		June '04	
Schmitt-Trigger Buffer/Driver	17	5						May '04			
1 of 2 Non-inverting Mux	18	6									
1 of 2 Decoder	19	6									
3-Input NOR	27	6									
2-Input OR	32	5						May '04			
Buffer Gate	34	5						May '04	May '04		
2-Input NAND w/Open Drain	38	5				March '04		May '04	May '04		
Configurable	57	6									
Configurable	58	6									
Analog Switch	66	5									
D-F/F (CLR & PRE)	74	8									
D-F/F (Q output)	79	5						June '04			
D-F/F (/Q output)	80	5						June '04			
2-Input XOR	86	5									
Configurable	97	6									
Configurable	98	6									
3-state Buffer (/OE)	125	5									
3-state Buffer (/OE)	126	5									
2-Input NAND w/Schmitt-Trigger	132	5				March '04		May '04			
D-Type FF w/Async Cir	175	6				March '04		May '04			
3-state Buffer (invert)	240	5									
3-Input OR	332	6									
D-Type Latch w/3-State	373	6						May '04			
D-Type FF w/3-State	374	6						May '04			
3-Input XOR	386	6									
Analog Switch	3157	6									

Dual-Gate Functions

Function	Part #	Pins	SN74AUC2G			SN74LVC2G			SN74AUP2G		
			Package Suffix			Package Suffix			Package Suffix		
			DBV/DCK	DCU/DCT	YEP/YZP	DBV/DCK	DCU/DCT	YEP/YZP	DBV/DCK	DCU/DCT	YEP/YZP
2-Input NAND	00	8									
2-Input NOR	02	8									
Inverter	04	6									
Inverter (Unbuffered)	U04	6									
Inverter w/Open-Drain	06	6									
Buffer/Driven w/Open-Drain	07	6									
2-Input AND	08	8									
Schmitt-Trigger Inverter	14	6									
Schmitt-Trigger Buffer/Driver	17	6									
2-Input OR	32	8									
Buffer	34	6									
2-Input NAND w/Open Drain	38	8									
Analog Mux/Demux	53	8				April '04					
Analog Switch	66	8									
D-F/F (CLR & PRE)	74	8									
D-F/F (Q output)	79	8									
D-F/F (/Q output)	80	8									
2-Input XOR	86	8									
3-state Buffer (/OE)	125	8									
3-state Buffer (/OE)	126	8									
2-Input NAND w/Schmitt-Trigger	132	8					Mar '04				
Mux/Demux	157	8									
3-state Buffer (invert)	240	8									
3-state Buffer (Non-invert)	241	8									

Triple-Gate Functions

Function	Part #	Pins	SN74AUC3G			SN74LVC3G			SN74AUP3G		
			Package Suffix			Package Suffix			Package Suffix		
			DBV/DCK	DCU/DCT	YEP/YZP	DBV/DCK	DCU/DCT	YEP/YZP	DBV/DCK	DCU/DCT	YEP/YZP
Inverter	04	8									
Inverter (Unbuffered)	U04	8					March '04				
Inverter w/Open-Drain	06	8									
Buffer/Driver w/Open-Drain	07	8									
Schmitt-Trigger Inverter	14	8									
Schmitt-Trigger Buffer/Driver	17	8									
Buffer	34	6									

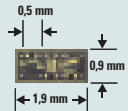
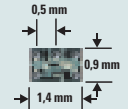
Key

- Released and in full production
- In queue, estimated release date

Packaging

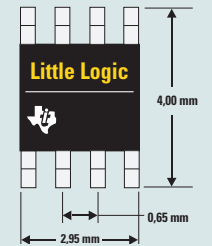
Wafer Chip-Scale

NanoStar/NanoFree

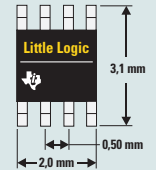


Lead Frame

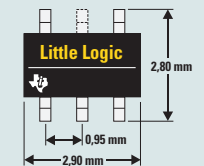
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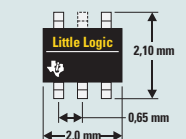
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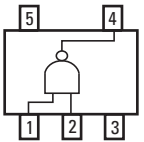
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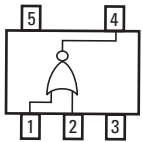
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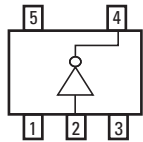
Single-Gate Diagrams



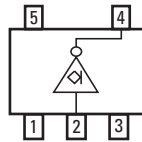
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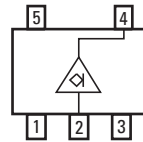
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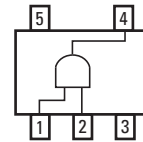
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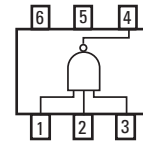
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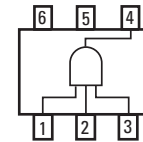
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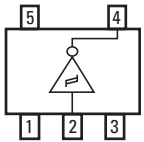
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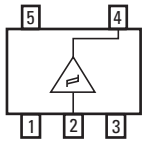
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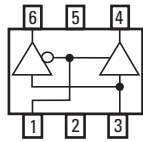
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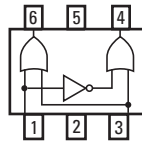
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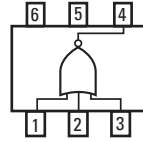
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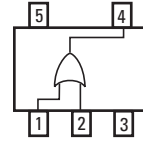
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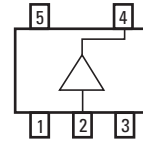
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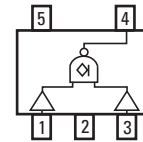
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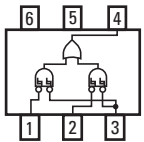
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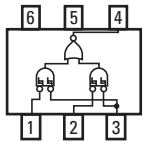
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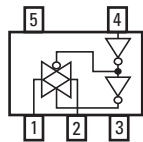
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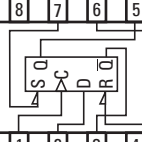
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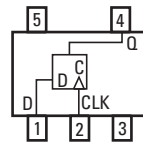
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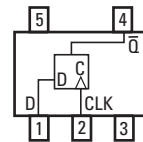
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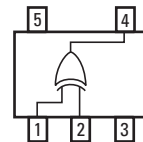
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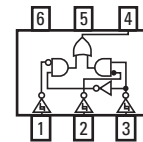
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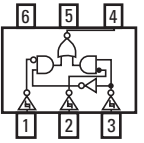
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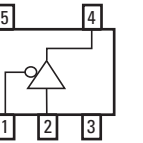
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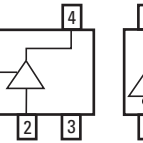
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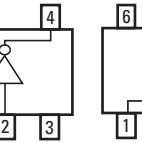
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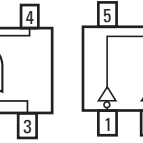
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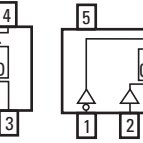
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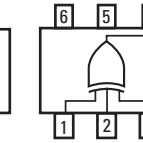
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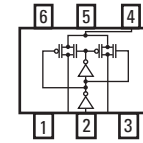
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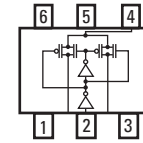
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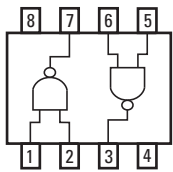


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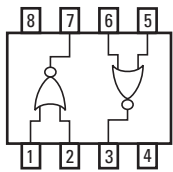


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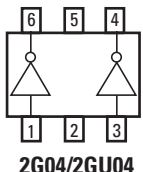
Dual-Gate Diagrams



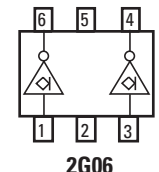
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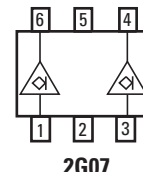
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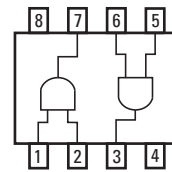
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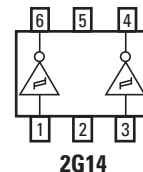
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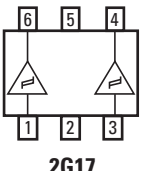
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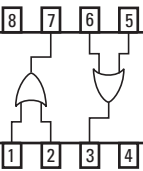
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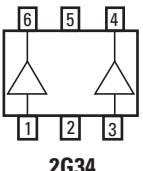
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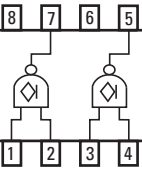
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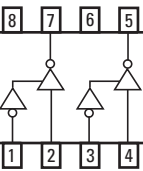
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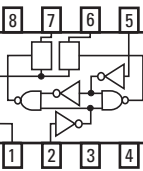
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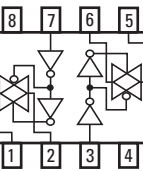
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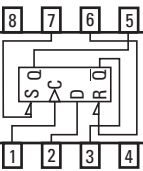
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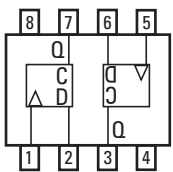
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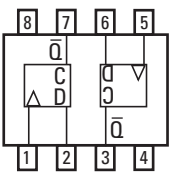
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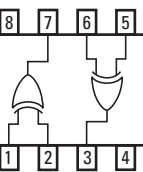
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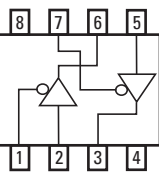
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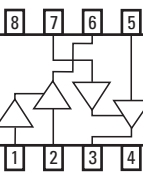
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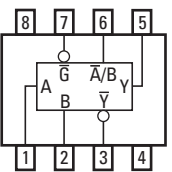
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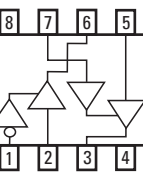
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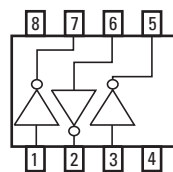


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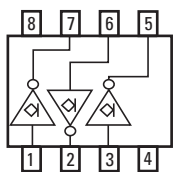


2G241

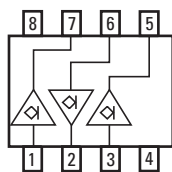
Triple-Gate Diagrams



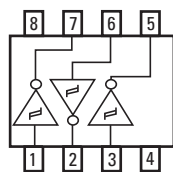
3G04/3GU04



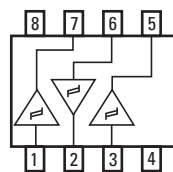
3G06



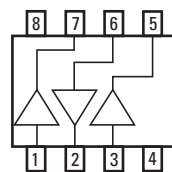
3G07



3G14



3G17



3G34

Competitor Part Prefixes

TI	Toshiba	Fairchild	ON	STMicro	Philips	IDT	Pericom
Little Logic							
SN74AHC1G	TC7S	NC7S	MC74VHC1G	74V1G			
SN74AHCT1G	TC7SHET	NC7ST	MC74VHC1GT	74V1T			
SN74LVC1G	TC7SZ	NC7SZ	NL17SZ	74LX1G	74LVC1G	IDT74LVC1G	P174STX1G
SN74LVC2G	TC7WZ	NC7WZ	NL27WZ				
SN74LVC3G	TC7WZ	NC7NZ	NL37WZ				
SN74AUC1G		NC7SV	NL17SV				
SN74AUC2G		NC7WV					
SN74AUP1G		NC7SP					
Little Logic Signal Switch							
SN74CBT1G	TC7SB	NC7SB					
SN74CBTLV1G	TC7SBL						
SN74LVC1G66		NC7SZ66					
SN74LVC2G66		NC7WB66					

NOTE: Philips and IDT are alternate source.

Competitor Package Cross Reference

	TI	Fairchild	ON	Toshiba	Philips	IDT	Pericom	STMicro	TI Package Suffix Decoder
NanoStar	YEP	L6*							YEP is NanoStar
NanoFree	YZP								YZP is NanoFree, Pb-FREE
SOT-23 (5-pin)	DBV	M5	DT	F	GV		TX	ST	DBV is 5 and 6-pin leadframe
SC-70 (5-pin)	DCK	P5	DF	FU	GW	DY	CX	CT	DCK is 5 and 6-pin leadframe, slightly smaller than DBV
SOT-23 (6-pin)	DBV	DT			GV				DBV is 5 and 6-pin leadframe
SC-70 (6-pin)		DCK	P6	DF		DW			DCK is 5 and 6-pin leadframe, slightly smaller than DBV
SM-8 (8-pin)	DCT			FU					DCT is 8-pin leadframe
US-8 (8-pin)	DCU	K8	US	FK	DC				DCU is 8-pin leadframe, slightly smaller than DCT

*Nanostar measures smaller than L6 package.

Note: Pb-FREE, NanoFree classified per J-STD-020B MSL-1 rated.

www.ti.com/nanostar

For more information including samples and data sheets:

Logic Home: logic.ti.com

Little Logic Home: www.ti.com/littlelogic

Little Logic Selection Guide: <http://focus.ti.com/pdfs/logic/littlelogicsg.pdf>

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